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National
Semiconductor
Corporation

Hamilton Avnet
ELECTRONICS
AN AVNET COMPANY
4940 Research Dr., N.W., Huntsville, AL 35805
(205) 837-7210

# Linear Databook 1

- *Voltage Regulators*
- *Operational Amplifiers*
- *Buffers*
- *Voltage Comparators*
- *Instrumentation Amplifiers*
- *Surface Mount*

**HAMILTON/AVNET ELECTRONICS**
4940 Research Drive N.W.
Huntsville, AL 35805
(205) 837-7210
MS WATS 1-800-633-2992
AL WATS 1-800-572-2907

Hamilton Avnet
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Field Sales Representative

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Charlie Sporck

Charles E. Sporck
President, Chief Executive Officer
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Charles Sporck

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

# Linear Databook 1

## 1988 Edition

## General Information

- Alphanumeric
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- Package Cross Reference
- Linear Databook 2 Selection Guides
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  - Analog Switches/Multiplexers
  - Analog-to-Digital Converters
  - Digital-to-Analog Converters
  - Sample and Hold
  - Temperature Sensors
  - Voltage References
- Linear Databook 3 Selection Guides
  - Audio Circuits
  - Radio Circuits
  - Video Circuits
  - Motion Control
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## Buffers

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You can rely on National LINEAR to develop the most comprehensive product offering for use in the commercial, computer, automotive, telecommunication, industrial or military business segments. More than 1,000 basic LINEAR products (5400 options) allow design engineers to find the optimum Linear IC solution from National Semiconductor.

The Linear product line is presented in 3 Databooks. All sections are referenced and cross-indexed to provide quick and easy access. The technical information and basic product specifications are presented in data sheet format, including maximum ratings, electrical characteristics, performance curves and package information.

Additional application information is available as specific application notes or completely compiled in the LINEAR APPLICATIONS HANDBOOK. A product cross reference to the specific application note has been provided. This handbook and the 3-volume set of Linear Data Books represent a complete base of information to the National LINEAR product line.

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# Product Status Definitions

## Definition of Terms

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| MM54HC4053 Triple 2-Channel Analog Multiplexer | Linear 2 |
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| MM74HC4051 8-Channel Analog Multiplexer | Linear 2 |
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**National Semiconductor Corporation**

# CROSS REFERENCE BY PART NUMBER

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers are listed in this section and reference the nearest National Semiconductor Corp. direct replacement or recommended replacement with either an improved or functional replacement. The following notations are appended to assist you in finding the best option.

| | |
|---|---|
| No reference note ..... | "DIRECT REPLACEMENT" |
| Note (1) ................ | "IMPROVED REPLACEMENT" Pin-for-Pin replacement with "SUPERIOR" Electrical Specifications. |
| Note (2) ................ | "FUNCTIONAL REPLACEMENT" Similar device. Consult datasheet to determine the suitability for specific application. |
| Note (3) ................ | "SIMILAR DEVICE" with superior performance. Consult datasheet to determine suitability of the replacement for specific application. |

| **ANALOG DEVICES** | **NATIONAL** | |
|---|---|---|
| AD0P07 | LM607 | (1) |
| ADDAC-08 | DAC0800 | |
| ADDAC-08 | DAC0801 | |
| ADDAC-08 | DAC0802 | |
| ADDAC80 | DAC1280+ | (1) |
| ADDAC85 | DAC1280+ | (1) |
| AD101A | LM101A | (1) |
| AD201A | LM201A | (1) |
| AD301A | LM301A | (1) |
| AD506 | LH0022 | (2) |
| AD509 | LH0003 | (2) |
| AD521 | LM363 | (2) |
| AD521 | LH0036 | (2) |
| AD524 | LH0038 | (2) |
| AD537 | LM331 | (2) |
| AD562 | DAC1266 | (3) |
| AD563 | DAC1265 | (3) |
| AD565A | DAC1265 | |
| AD566A | DAC1266 | |
| AD567 | DAC1230 | (2) |
| AD573 | ADC1005 | (2) |
| AD573 | ADC1025 | (2) |
| AD581 | LM581 | |
| AD581 | LH0070 | (1) |
| AD582 | LF398 | (2) |
| AD583 | LF198 | (3) |
| AD588 | LM369 | (2) |
| AD589M | LM385 | (1) |
| AD589U | LM185 | (1) |
| AD590 | LM135 | (2) |
| AD590 | LM34 | (3) |
| AD590 | LM134 | (2) |
| AD590 | LM35 | (3) |
| AD611K | LF411AC | (1) |
| AD611J | LF411C | (1) |
| AD614 | LH0086 | (2) |
| AD624 | LH0038 | (2) |
| AD650 | LM331 | (2) |
| AD651 | LM331 | (2) |
| AD654 | LM331 | (2) |
| AD673 | ADC0841 | (2) |
| AD741 | LM741 | |
| ADLH0032 | LH0032 | (2) |
| ADLH0033 | LH0033 | (2) |
| AD0042 | LH0042 | (2) |
| AD3542 | LH0042 | (2) |
| AD5035 | LH0042 | (2) |
| AD7502 | LF13509 | (2) |
| AD7516 | CO4066B | (2) |
| AD7523 | DAC0832 | (2) |
| AD7523 | DAC0831 | (2) |
| AD7523 | DAC0830 | (2) |
| AD7524 | DAC0830 | (3) |
| AD7524 | DAC0831 | (3) |
| AD7524 | DAC0832 | (3) |
| AD7533 | DAC1020 | |
| AD7533 | DAC1022 | |
| AD7533 | DAC1021 | |
| AD7541A | DAC1218 | (2) |
| AD7541A | DAC1219 | (2) |
| AD7541 | DAC1219 | (1) |
| AD7541 | DAC1218 | (1) |
| AD7542 | DAC1210 | (2) |
| AD7542 | DAC1209 | (2) |
| AD7542 | DAC1208 | (2) |
| AD7545 | DAC1209 | (2) |
| AD7545 | DAC1210 | (2) |
| AD7545 | DAC1208 | (2) |
| AD7548 | DAC1230 | (2) |
| AD7548 | DAC1232 | (2) |
| AD7548 | DAC1231 | (2) |
| AD7552 | ADC1225 | (2) |
| AD7552 | ADC1205 | (2) |
| AD7571 | ADC1005 | (2) |
| AD7571 | ADC1025 | (2) |
| AD7575 | ADC0820 | (2) |
| AD7576 | ADC0820 | (2) |
| AD7578 | ADC1225 | (2) |
| AD7578 | ADC1205 | (2) |
| AD7820 | ADC0820 | |

| **APEX** | **NATIONAL** | |
|---|---|---|
| PA01 | LM12 | (2) |
| PA01 | LH0101 | (2) |
| PA07 | LM12 | (2) |
| PA10 | LM12 | (2) |
| PA10 | LH0101 | (2) |
| PA11 | LM12 | (2) |
| PA51 | LM12 | (2) |
| PA73 | LM12 | (2) |

| **BURR-BROWN** | **NATIONAL** | |
|---|---|---|
| SHC80 | LF398 | (2) |
| SHC85 | LF398 | (2) |
| HOS-100 | LH0033 | (2) |
| INA102 | LH0038 | (2) |
| SHC298A | LF398A | (1) |
| 3507 | LM6361 | (2) |
| 3533 | LH0033 | (2) |
| 3542 | LH0042 | (2) |
| 3550 | LM6361 | (2) |
| 3551 | LM6361 | (2) |
| 3553 | LH0063 | (2) |
| 3554 | LH0032 | (2) |
| 3571 | LM675 | (2) |
| 3572 | LH0021 | (2) |
| 3573 | LM675 | (2) |
| 3606A6 | LH0084 | (2) |
| 3606A6 | LH0086 | (2) |
| 3626 | LH0036 | (2) |
| 3629 | LH0038 | (2) |

| CTS | NATIONAL | |
|---|---|---|
| CTS0002 | LH0002 | (1) |
| CTS0004 | LH0004 | (1) |
| CTS0021 | LH0021 | (1) |
| CTS0024 | LH0024 | (1) |
| CTS0032 | LH0032 | (1) |
| CTS0033 | LH0033 | (1) |
| CTS0041 | LH0041 | (1) |
| CTS0042 | LH0042 | (1) |
| CTS2101A | LH2101A | (1) |
| CTS2111 | LH2111 | (1) |

| ELANTEC | NATIONAL | |
|---|---|---|
| ELH0002 | LH0002 | (1) |
| ELH0021 | LH0021 | (1) |
| ELH0032 | LH0032 | (1) |
| ELH0033 | LH0033 | (1) |
| ELH0041 | LH0041 | (1) |
| ELH0101 | LH0101 | (1) |
| EL2006C | LM6261 | (2) |
| EL2006 | LM6161 | (2) |
| EHA2500 | LM6161 | (2) |
| EHA2502 | LM6161 | (2) |
| EHA2505 | LM6361 | (2) |
| EHA2510 | LM6161 | (2) |
| EHA2512 | LM6161 | (2) |
| EHA2515 | LM6361 | (2) |
| EHA2520 | LM6164 | (2) |
| EHA2522 | LM6164 | (2) |
| EHA2525 | LM6364 | (2) |
| EHA2600 | LM6161 | (2) |
| EHA2602 | LM6161 | (2) |
| EHA2605 | LM6361 | (2) |
| EHA2620 | LM6164 | (2) |
| EHA2622 | LM6164 | (2) |
| EHA2625 | LM6364 | (2) |

| EXAR | NATIONAL | |
|---|---|---|
| XR084M | LF147 | (1) |
| XR084 | LF347 | (1) |
| XR146 | LM146 | (1) |
| XR246 | LM246 | (1) |
| XR346 | LM346 | (1) |
| XR-1001 | MF4C-100 | (1) |
| XR-1002 | MF4C-50 | (1) |
| XR1458 | LM1458 | (1) |

| FAIRCHILD | NATIONAL | |
|---|---|---|
| µA78XXKM | LM140K-XX | (1) |
| µ78LXXACH | LM78LXXACH | (1) |
| µ78XXUC | LM340T-XX | (1) |
| µ78XXUC | LM78XXCT | (1) |
| µA78LXXACLP | LM78LXXACZ | (1) |
| µA78LXXAWC | LM78LXXACZ | (1) |
| µ78MXXCKC | LM78XXCK | (1) |
| µ78MXXCKC | LM78MXXCT | (1) |
| µA78MXXUC | LM341P-XX | (1) |
| µA78MXXCKC | LM78XXCT | (1) |
| µA78XXKC | LM340K-XX | (1) |
| µA79XXUC | LM79LXXACZ | (1) |
| µA79XXUC | LM79MXXCP | (1) |
| µA79XXCKC | LM79XXCT | (1) |
| µA79XXCKC | LM79MXXCP | (1) |
| µA79XXUC | LM79MXXCH | (1) |
| µA79XXUC | LM320T-XX | (1) |
| µA79XXCKC | LM79MXXCH | (1) |
| µA79XXCKC | LM79LXXACZ | (1) |
| µA79MXXAUC | LM320MP-XX | (1) |
| µA79XXKM | LM120K-XX | (1) |
| µA79XXKC | LM320K-XX | (1) |
| µA79XXUC | LM79XXCT | (1) |
| µA101A | LM101A | (1) |
| µA102 | LM102 | (1) |
| µA105HM | LM105H | (1) |
| µA107 | LM107 | (1) |
| µA108A | LM108A | (1) |
| µA108 | LM108 | (1) |
| µA109KM | LM109K STEEL | (1) |
| µA110 | LM110 | (1) |
| µA111 | LM111 | (1) |
| µA124 | LM124 | (1) |
| µA139 | LM139 | (1) |
| µA139A | LM139A | (1) |
| µA201A | LM201A | (1) |
| µA207 | LM207 | (1) |
| µA208 | LM208 | (1) |
| µA208A | LM208A | (1) |
| µA211 | LM211 | (1) |
| µA224 | LM224 | (1) |
| µA239 | LM239 | (1) |
| µA239A | LM239A | (1) |
| µA248 | LM248 | (1) |
| µA249 | LM249 | (1) |
| µA301A | LM301A | (1) |
| µA302 | LM302 | (1) |
| µA304HC | LM304H | (1) |
| µA305HC | LM305H | (1) |
| µA305AHC | LM305AH | (1) |
| µA307 | LM307 | (1) |
| µA308A | LM308A | (1) |
| µA308 | LM308 | (1) |
| µA309KC | LM309K STEEL | (1) |
| µA310 | LM310 | (1) |
| µA311 | LM311 | (1) |
| µA317KC | LM317K STEEL | (1) |
| µA317UC | LM317T | (1) |
| µA318 | LM318 | (1) |
| µA324 | LM324 | (1) |
| µA339 | LM339 | (1) |
| µA339A | LM339A | (1) |
| µA348 | LM348 | (1) |
| µA349 | LM349 | (1) |
| µA376TC | LM376N | (1) |
| µA555TC | LM555CN | (1) |
| µA556PC | LM556CN | (1) |
| µA709 | LM709 | (1) |
| µA709 | LM709 | (1) |
| µA710 | LM710 | (1) |
| µA710 | LM710 | (1) |
| µA711 | LM711 | (1) |
| µA714 | LM607 | (1) |
| µA723HM | LM723H | (1) |
| µA723HC | LM723CH | (1) |
| µA723DC | LM723CJ | (1) |
| µA723MJ | LM723J | (1) |
| µA723CJ | LM723CJ | (1) |
| µA723DM | LM723J | (1) |
| µA723PC | LM723CN | (1) |
| µA723CN | LM723CN | (1) |
| µA725 | LM725 | (1) |
| µA725 | LM725 | (1) |
| µA733CN | LM733CN | (1) |
| µA733 | LM733 | (1) |
| µA741 | LM741 | (1) |
| µA741 | LM741 | (1) |
| µA747 | LM747 | (1) |
| µA747 | LM747 | (1) |
| µA748 | LM748 | (1) |
| µA748 | LM748 | (1) |
| µA760 | LM760 | (1) |
| µA771B | LF411 | (1) |
| µA771 | LF351 | (1) |
| µA771A | LF411 | (1) |
| µA772B | LF412A | (1) |
| µA772 | LF353 | (1) |
| µA772A | LF412A | (1) |
| µA774 | LF347 | (1) |
| µA774B | LF347B | (1) |
| µA776 | LM4250 | (1) |
| µA1458 | LM1458 | (1) |
| µC1496P | LM1496N | (1) |
| µC1496G | LM1496H | (1) |
| µA1558 | LM1558 | (1) |
| µC1596G | LM1596H | (1) |
| TDA2310 | LM381 | (1) |
| µA2901 | LM2901 | (1) |
| µA2902 | LM2902 | (1) |
| TCA3089 | LM3089N | (1) |
| µA3301 | LM3301 | (1) |
| µA3302 | LM3302 | (1) |
| µC4558CD | LM833CN | (1) |
| µA7392 | LM1014 | (1) |

| HARRIS | NATIONAL | |
|---|---|---|
| HA-OP07 | LM607 | (1) |
| HF-10 | MF10 | |
| HI-201 | LF13201 | |
| HI-300 | AH5020 | (2) |
| LM741 | LM741 | (1) |
| HA2400 | LM604AM | (2) |
| HA2404 | LM604AM | (2) |
| HA2405 | LM604C | (2) |
| HA2406 | LM604C | (2) |
| HA2500 | LM6161 | (2) |
| HA2502 | LM6161 | (2) |
| HA2505 | LM6361 | (2) |
| HA2510 | LM6161 | (2) |
| HA2512 | LM6161 | (2) |
| HA2515 | LM6361 | (2) |
| HA2520 | LM6164 | (2) |
| HA2520 | LH0003 | (1) |
| HA2522 | LH0003 | (1) |
| HA2522 | LM6164 | (2) |
| HA2525 | LH0003 | (1) |
| HA2525 | LM6364 | (2) |
| HA2530 | LH0024 | (2) |
| HA2535 | LH0024 | (2) |
| HA2540 | LH0032 | (2) |
| HA2541-5 | LM6361 | (2) |
| HA2541-2 | LM6161 | (2) |
| HA2542 | LH0032 | (2) |
| HA2542-2 | LM6164 | (2) |
| HA2542-5 | LM6164 | (2) |
| HA2600 | LM6161 | (2) |
| HA2602 | LM6161 | (2) |
| HA2605 | LM6361 | (2) |
| HA2620 | LM6164 | (2) |
| HA2622 | LM6164 | (2) |
| HA2625 | LM6364 | (2) |
| HA2640 | LH0004 | (1) |
| HA5033 | LH0033 | (1) |
| HA5162 | LH0062 | (2) |
| A5180 | LH0052 | (1) |

| HEWLETT PACKARD | NATIONAL | |
|---|---|---|
| HCTL-100 | LM628 | (3) |

| HITACHI | NATIONAL | |
|---|---|---|
| HA13421A | LM18293 | (3) |
| HA17082 | LF353 | (1) |
| HA17082A | LF412 | (1) |
| HA17084 | LF347 | (1) |
| HA17084A | LF347B | (1) |
| HA17094 | LM2904 | (1) |
| HA17301 | LM3301 | (1) |
| HA17324 | LM324 | (1) |
| HA17339 | LM339 | (1) |
| HA17358 | LM358 | (1) |
| HA17393 | LM393 | (1) |
| HA17458 | LM1458 | (1) |
| HA17741 | LM741 | (1) |
| HA17747 | LM747 | (1) |
| HA17901 | LM2901 | (1) |
| HA17902 | LM2902 | (1) |
| HA17903 | LM2903 | (1) |

| LINEAR TECHNOLOGY | NATIONAL | |
|---|---|---|
| REF-01 | LM168 | (1) |
| REF-01 | LM368 | (1) |
| LM129 | LM129 | |
| LM134 | LM134 | |
| LM185 | LM185 | |
| LM199 | LM199 | |
| LM234 | LM234 | |
| LM329 | LM329 | |
| LM334 | LM334 | |
| LM385 | LM385 | |
| LM399 | LM399 | |
| AD581 | LM581 | |
| AD581 | LH0070 | |
| LT1001 | LM607A | (1) |
| LT1004C | LM385 | |
| LT1004M | LM185 | |
| LT1009M | LM136-2.5 | |
| LT1009C | LM336-2.5 | |
| LT1019C | LM368 | (2) |
| LT1019M | LM168 | (2) |
| LT1020 | LP2951 | (3) |
| LT1021M | LM169 | (1) |
| LT1021C | LM369 | (1) |
| LT1029M | LM136-5.0 | |
| LT1029C | LM336-5.0 | |
| LT1031 | LH0070 | |

| LSI COMPUTER | NATIONAL | |
|---|---|---|
| LS7261 | LM621 | (3) |
| LS7263 | LM621 | (3) |

| MICRA | NATIONAL | |
|---|---|---|
| MC0002 | LH0002 | (1) |
| MC0003 | LH0003 | (1) |
| MC0004 | LH0004 | (1) |
| MC0032 | LH0032 | (1) |
| MC0033 | LH0033 | (1) |
| MC0041 | LH0041 | (1) |
| MC0063 | LH0063 | (1) |

| MICRO POWER SYSTEMS | NATIONAL | |
|---|---|---|
| MPOP07 | LM607 | (1) |
| MP108 | LM108 | (1) |
| MP108A | LM108A | (1) |
| MP155A | LF155A | (1) |
| MP155 | LF155 | (1) |
| MP156 | LF156 | (1) |
| MP156A | LF156A | (1) |
| MP157 | LF157 | (1) |
| MP157A | LF157A | (1) |
| MP208A | LM208A | (1) |
| MP208 | LM208 | (1) |
| MP308 | LM308 | (1) |
| MP308A | LM308A | (1) |
| MP355A | LF355A | (1) |
| MP356A | LF356A | (1) |
| MP357A | LF357A | (1) |
| MP2108A | LH2108A | (1) |
| MP5010H | LM385 | |
| MP5010L | LM385 | |
| MP5010G | LM185 | |
| MP5010H | LM185 | |
| MP5010L | LM185 | |
| MP5010G | LM385 | |

| MOTOROLA | NATIONAL | |
|---|---|---|
| DAC-08 | DAC0800 | |
| DAC-08 | DAC0802 | |
| DAC-08 | DAC0801 | |
| MC78XXACT | LM340AT-XX | (1) |
| MC78XXCK | LM78XXCK | (1) |
| MC78LXXACP | LM78LXXACZ | (1) |
| MC78MXXCT | LM78XXCK | (1) |
| MC78MXXCT | LM341P-XX | (1) |
| MC78LXXACG | LM78LXXCH | (1) |
| LM78XXCT | LM78LXXCH | (1) |
| MC78MXXCT | LM78MXXCT | (1) |
| MC78XXCT | LM78XXCT | (1) |
| MC78LXXCP | LM78LXXACZ | (1) |
| MX78MXXCT | LM342P-XX | (1) |
| MC78LXXCG | LM78LXXACH | (1) |
| MC79XXCK | LM320K-XX | (1) |
| MC79MXXCKC | LM320MP-XX | (1) |
| MC79XXCK | LM79XXCK | (1) |
| MC79XXCKC | LM320T-XX | (1) |
| LM79XXCP | LM79XXCT | (1) |
| MC79XXCT | LM79MXXCH | (1) |
| MC79LXXCP | LM320LZ-XX | (1) |
| MC79LXXACG | LM320H-XX | (1) |
| MC79LXXCLP | LM320LZ-XX | (1) |
| MC79XXCT | LM79MXXCP | (1) |
| MC79LXXACP | LM79LXXACZ | (1) |
| MC79LXXCP | LM79LXXCZ | (1) |
| MC79XXCT | LM320T-XX | (1) |
| MC79XXCT | LM79XXCT | (1) |
| MC79XXCT | LM79LXXACZ | (1) |
| LM79XXCP | LM79LXXACZ | (1) |
| LM79XXCP | LM79MXXCH | (1) |
| LM79XXCP | LM79MXXCP | (1) |
| LM109K | LM109K STEEL | (1) |
| LM109H | LM109H | (1) |
| LM117H | LM117K STEEL | (1) |
| LM123K | LM123K STEEL | (1) |
| LM137H | LM137H | (1) |
| LM137K | LM137K STEEL | (1) |
| LM140K | LM140K-XX | (1) |
| LM150K | LM150K STEEL | (1) |
| LM285 | LM285 | |
| LM309H | LM309H | (1) |
| LM309H | LM309K | (1) |
| LM309K | LM309K STEEL | (1) |
| LM317H | LM317H | (1) |
| LM317LZ | LM317LZ | (1) |
| LM317T | LM317T | (1) |
| LM317KC | LM317T | (1) |
| LM317K | LM317K STEEL | (1) |
| LM323K | LM323K STEEL | (1) |
| LM330-XKC | LM330T-XX | (1) |
| LM337H | LM337H | (1) |
| LM337K | LM337K STEEL | (1) |
| LM337KC | LM337T | (1) |
| LM337T | LM337T | (1) |
| LM340T-XX | LM340T-XX | (1) |
| LM340T-XX | LM340K-XX | (1) |
| LM340-XXKC | LM340T-XX | (1) |
| LM350T | LM350T | (1) |
| LM350K | LM350K STEEL | (1) |
| LM350KC | LM350T | (1) |
| LM350KA | LM350K STEEL | (1) |
| LM385 | LM385 | |
| AD562A | DAC1266 | (2) |
| AD563A | DAC1265 | (2) |
| μPC741 | LM741 | |
| MC1408 | DAC0806 | |
| MC1408 | DAC0808 | |
| MC1408 | DAC0807 | |
| MC1414 | LM1414 | (1) |
| MC1436 | LM343 | (1) |
| MC1458 | LM1458 | (1) |
| MC1496 | LM1446 | |
| MC1508 | DAC0808 | |
| MC1514 | LM1514 | (1) |
| MC1536 | LM143 | (1) |
| MC1558 | LM1558 | (1) |
| MC1596G | LM1596CH | (1) |
| MC1709 | LM709 | (1) |
| MC1709 | LM709 | |
| MC1710 | LM710 | |
| MC1723CL | LM723CJ | (1) |
| MC1723CG | LM723CH | (1) |
| MC1723CP | LM723CN | (1) |
| MC1723CL | LM723CM | (1) |
| MC1723L | LM723J | (1) |
| MC1723G | LM723H | (1) |
| MC1733CG | LM723CH | (1) |
| MC1741 | LM741 | (1) |
| MC1741 | LM741 | |
| MC1747 | LM747 | (1) |
| MC1747 | LM747 | |
| MC1748 | LM748 | |
| LM2930-XKC | LM2930T-XX | (1) |
| MC3301 | LM3301 | (1) |
| MC3302 | LM3302 | (1) |
| MC3361 | LM3361AN | (1) |
| MC3401 | LM3401 | (1) |
| MC3410 | DAC1020 | (2) |
| MC3412 | DAC1265 | (1) |
| MC3510 | DAC1020 | (2) |
| MC4741 | LM348 | (1) |
| MC14442 | ADC0829 | (2) |
| MC14444 | ADC0830 | (2) |
| MC34001A | LF411C | (1) |
| MC34001B | LF411C | (1) |
| MC34001 | LF351 | (1) |
| MC34002B | LF412C | (1) |
| MC34002 | LF353 | (1) |
| MC34002A | LF412A | (1) |
| MC34004B | LF347B | (1) |
| MC34004 | LF347 | (1) |
| MC34004B | LF147 | (1) |
| MC34004 | LF147 | (1) |
| MC35001 | LF411M | (1) |
| MC35001A | LF411M | (1) |
| MC35001B | LF411M | (1) |
| MC35002B | LF412M | (1) |
| MC35002 | LF412M | (1) |
| MC35002A | LF412AM | (1) |

| | | |
|---|---|---|
| MC145040 | ADC0811 | (2) |
| MC145041 | ADC0811 | |

| **PRECISION-MONOLITHIC INC.** | **NATIONAL** | |
|---|---|---|
| REF-01J | LM368-10 | (1) |
| REF-01 | LM369 | (1) |
| AMP-01 | LH0038 | (2) |
| DAC-02 | DAC1022 | (2) |
| DAC-02 | DAC1020 | (2) |
| REF-02 | LM368-5.0 | (3) |
| DAC-02 | DAC1021 | (2) |
| DAC-03 | DAC1020 | (2) |
| DAC-03 | DAC1022 | (2) |
| BUF03 | LH0033 | (1) |
| DAC-03 | DAC1021 | (2) |
| OP05 | LM607 | (2) |
| DAC-05 | DAC1020 | (2) |
| DAC-05 | DAC1021 | (2) |
| DAC-05 | DAC1022 | (2) |
| SW06B | LF11333 | |
| SW06G | LF13333 | |
| SW06F | LF13333 | |
| OP07 | LM607 | (1) |
| DAC-08 | DAC0801 | |
| DAC-08 | DAC0800 | |
| MUX-08E | LF13508 | |
| DAC-08 | DAC0802 | |
| OP15 | LF411 | (1) |
| MUX-24E | LF13509 | |
| REF-43 | LM368-2.5 | (1) |
| OP77 | LM607 | (1) |
| OP100 | LH0052 | (2) |
| DAC100 | DAC1021 | (2) |
| DAC100 | DAC1020 | (2) |
| DAC100 | DAC1022 | (2) |
| OP105/111 | LH0052 | (2) |
| PM108A | LM108A | (1) |
| PM108 | LM108 | (1) |
| PM139A | LM139A | (1) |
| PM139 | LM139 | (1) |
| PM155 | LF155 | (1) |
| PM155A | LF155A | (1) |
| PM156 | LF156 | (1) |
| PM156A | LF156A | (1) |
| PM157 | LF157 | (1) |
| PM157A | LF157A | (1) |
| SW201G | LF13201 | |
| SW201B | LF11201 | |
| SW201F | LF13201 | |
| SW202B | LF11202 | |
| SW202F | LF13202 | |
| SW202G | LF13202 | |
| PM208A | LM208A | (1) |
| PM208 | LM208 | (1) |
| OP215 | LF412 | (1) |
| PM308A | LM308A | (1) |
| PM308 | LM308 | (1) |
| DAC312 | DAC1266 | (2) |
| PM339A | LM339A | (1) |
| PM355 | LF355 | (1) |
| PM355A | LF355A | (1) |
| PM356A | LF356A | (1) |
| PM356 | LF356 | (1) |
| PM357A | LF357A | (1) |
| PM357 | LF357 | (1) |
| PM420 | LF124 | (1) |
| OPA501/3573 | LH0101 | (2) |
| PM725 | LM725 | (1) |
| PM-725 | LM725 | |
| PM741 | LM741 | (1) |
| PM-741 | LM741 | |
| PM-747 | LM747 | |
| PM747 | LM747 | (1) |
| DAC888 | DAC0831 | (2) |
| DAC888 | DAC0832 | (2) |
| DAC888 | DAC0830 | (2) |
| ADC910 | ADC1005 | (2) |
| ADC910 | ADC1025 | (2) |
| DAC0812 | DAC1208 | (2) |
| DAC0812 | DAC1209 | |
| DAC0812 | DAC1210 | |
| DAC1408 | DAC0806 | (2) |
| DAC1408 | DAC0808 | (2) |
| DAC1408 | DAC0807 | (2) |
| PM2108A | LH2108A | (1) |
| PM7533 | DAC1021 | |
| PM7533 | DAC1020 | |
| PM7533 | DAC1022 | |
| PM7541 | DAC1219 | |
| PM7541 | DAC1218 | |

| **RAYTHEON** | **NATIONAL** | |
|---|---|---|
| REF-01 | LM369 | (1) |
| REF-01T | LM368 | (1) |
| REF-02 | LM368-5.0 | (3) |
| REF-03 | LM368-2.5 | (1) |
| LP365 | LP365 | |
| RC714 | LM607 | (1) |
| RC741 | LM741 | (1) |
| RC741 | LM741 | |
| RC747 | LM747 | |
| RC747 | LM747 | (1) |
| RC1458 | LM1458 | (1) |
| RC1558 | LM1558 | (1) |

| **RCA/ INTERSIL/G.E.** | **NATIONAL** | |
|---|---|---|
| CA081C | TL081C | (2) |
| CA081A | LF411C | (2) |
| CA081 | LF411M | (2) |
| CA081B | LF411C | (2) |
| CA082C | TL082C | (2) |
| CA082B | LF412C | (2) |
| CA082 | LF412M | (2) |
| CA082A | LF412C | (2) |
| CA084B | LF347B | (2) |
| CA084 | LF147 | (2) |
| CA084C | LF347 | (2) |
| CA124 | LM124 | (1) |
| CA139 | LM139 | (1) |
| CA139A | LM139A | (1) |
| CA158 | LM158 | (1) |
| CA158A | LM158A | (1) |
| DG201 | LF11201 | |
| DG211 | LF13201 | |
| DG212 | LF13202 | |
| CA224 | LM224 | (1) |
| CA239 | LM239 | (1) |
| CA239A | LM239A | (1) |
| CA258 | LM258 | (1) |
| CA258A | LM258A | (1) |
| CA301A | LM301A | (1) |
| CA307 | LM307 | (1) |
| CA311 | LM311 | (1) |
| CA324 | LM324 | (1) |
| CA339A | LM339A | (1) |
| CA339 | LM339 | (1) |
| CA358A | LM358A | (1) |
| CA358 | LM358 | (1) |
| CA741 | LM741 | |
| CA741 | LM741 | (1) |
| CA747 | LM747 | (1) |
| CA747 | LM747 | |
| CA748 | LM748 | (1) |
| μA748 | LM748 | |
| CA748 | LM748 | |
| ADC0801 | ADC0801 | |
| ADC0802 | ADC0802 | |
| ADC0803 | ADC0803 | |
| ADC0804 | ADC0804 | |
| CA1458 | LM1458 | (1) |
| CA1558 | LM1558 | (1) |
| CA3105 | LM675 | (2) |
| CA3290 | LF393 | (2) |
| CA3401 | LM3401 | (1) |
| IH5009 | AH5009 | |
| IH5010 | AH5010 | |
| IH5011 | AH5011 | |
| IH5012 | AH5012 | |
| IH6108 | LF13508 | |
| IH6208 | LF13509 | |
| ICL7114 | ADC1205 | (2) |
| ICL7114 | ADC1225 | (2) |
| AD7520 | DAC1021 | |
| AD7520 | DAC1020 | |
| AD7520 | DAC1022 | |
| AD7521 | DAC1221 | |
| AD7521 | DAC1220 | |
| AD7521 | DAC1222 | |
| AD7530 | DAC1020 | (3) |
| AD7530 | DAC1021 | (3) |
| AD7530 | DAC1022 | (3) |
| AD7531 | DAC1220 | |
| AD7531 | DAC1221 | |
| AD7531 | DAC1222 | |
| AD7533 | DAC1020 | |
| AD7533 | DAC1021 | |
| AD7533 | DAC1022 | |
| AD7541 | DAC1219 | |
| AD7541 | DAC1218 | |
| ICL7650 | LMC668 | (1) |
| ICL8069 | LM385-1.2 | |
| ICL8069 | LM313 | |
| ICH8530 | LH0101 | (2) |

| **SAMSUNG** | **NATIONAL** |
|---|---|
| LM741 | LM741 |

| **SGS** | **NATIONAL** | |
|---|---|---|
| L78M12CV | LM341P-12 | (1) |
| L78M15CV | LM341P-15 | (1) |
| L78S12CV | LM340T-12 | (1) |
| L78S05CV | LM340T-5.0 | (1) |
| L78S15CV | LM340T-15 | (1) |
| L78M05CV | LM341P-5.0 | (1) |
| LM117K | LM117K | (1) |
| L123CB | LM723CN | (1) |
| L272 | LM18272 | |
| L293 | LM18293 | |
| L298 | LM18298 | |
| LM317T | LM317T | (1) |
| LM317K | LM317K | (1) |
| LM748 | LM748 | |
| TDA2310 | LM381 | |
| LM2930A | LM2930T-5.0 | (1) |
| LM2931A | LM2931AT-5.0 | (1) |
| TCA3089 | LM3089 | |
| L7805CT | LM7805CK | (1) |

| | | |
|---|---|---|
| L7815CV | LM7815CT | (1) |
| L7905ACV | LM320T-5.0 | (1) |
| L7905CT | LM7905CK | (1) |
| L7905CV | LM7905CT | (1) |
| L7912CT | LM7912CK | (1) |
| L7912ACV | LM320T-12 | (1) |
| L7915CT | LM7915CK | (1) |
| L7915ACV | LM320T-15 | (1) |

| **SIEMENS** | **NATIONAL** | |
|---|---|---|
| TCA365 | LH0101 | (1) |

| **SIGNETICS** | **NATIONAL** | |
|---|---|---|
| DAC-08 | DAC0802 | |
| DAC-08 | DAC0801 | |
| DAC-08 | DAC0800 | |
| 78LXXACS | LM78XXACZ | (1) |
| 78LXXADB | LM78XXACH | (1) |
| 78LXXCDB | LM78LXXCH | (1) |
| 78LXXCS | LM78LXXCZ | (1) |
| 78XXCU | LM78XXCT | (1) |
| 78XXDA | LM78XXCK | (1) |
| 79XXDA | LM79XXCK | (1) |
| 79XXCU | LM79XXCT | (1) |
| LM109DB | LM109H | (1) |
| TBA120S-4 | TBA120SIV | |
| TBA120S-3 | TBA120SIII | |
| TBA120S-2 | TBA120SII | |
| LF198 | LF198 | |
| LF298 | LF298 | |
| LM309DA | LM309K | (1) |
| LM309DB | LM309H | (1) |
| LM340XXLL | LM340TXX | (1) |
| LM340XXDA | LM340KXX | (1) |
| LF398 | LF398 | |
| NE529 | LM361 | (1) |
| SE529 | LM161 | (1) |
| SE532 | LM158 | (1) |
| SA532 | LM2904 | (1) |
| NE532 | LM358 | (1) |
| SA534 | LM2902 | (1) |
| NE555N | LM555CN | |
| SE567 | LM567 | (2) |
| μA723CN | LM723CN | (1) |
| μA723CL | LM723CH | (1) |
| μA723L | LM723H | (1) |
| μA723CF | LM723CJ | (1) |
| μA723F | LM723J | (1) |
| μA741 | LM741 | |
| μA747 | LM747 | |
| ADC0801 | ADC0801 | |
| ADC0802 | ADC0802 | |
| ADC0803 | ADC0803 | |
| ADC0804 | ADC0804 | |
| ADC0805 | ADC0805 | |
| MC1408 | DAC0808 | |
| MC1408 | DAC0807 | |
| MC1408 | DAC0806 | |
| MC1496N | LM1496N | |
| MC1508 | DAC0808 | |
| MC1596K | LM1596H | |
| NE4558D | LM833CM | (2) |
| NE4558N | LM833CN | (2) |
| NE4558 | LM833 | (2) |
| NE5034 | ADC0841 | (2) |
| SE5118 | DAC0830 | (2) |
| NE5118 | DAC0830 | (2) |
| NE5410 | DAC1020 | (2) |
| SE5410 | DAC1020 | (2) |
| NE5532P | LM833CN | (2) |
| NE5532 | LM833 | |
| NE5532N | LM833CN | (2) |

| **SILICON GENERAL** | **NATIONAL** | |
|---|---|---|
| SG101 | LM101A | (1) |
| SG101A | LM101A | (1) |
| SG107 | LM107 | (1) |
| SG124 | LM124 | (1) |
| SG201 | LM201A | (1) |
| SG201A | LM201A | (1) |
| SG207 | LM207 | (1) |
| SG224 | LM224 | (1) |
| SG301A | LM301A | (1) |
| SG307 | LM307 | (1) |
| SG324 | LM324 | (1) |
| SG741 | LM741 | (1) |
| SG741 | LM741 | (1) |
| SG1173 | LM675 | (2) |
| SG1436 | LM343 | (1) |
| SG1536 | LM143 | (1) |
| SG3173 | LM675 | (2) |

| **SILICONIX** | **NATIONAL** | |
|---|---|---|
| DG201 | LF13201 | |
| DG202 | LF13202 | |
| DG211 | LF13201 | |
| DG212 | LF13202 | |
| DG508 | LF13508 | |
| DG509 | LF13509 | |

| **SPRAGUE** | **NATIONAL** | |
|---|---|---|
| UDN22933 | LM18293 | |

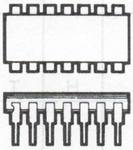
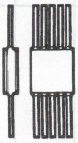
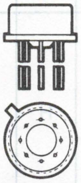
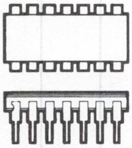
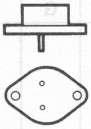
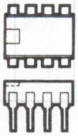
| **TELEDYNE** | **NATIONAL** | |
|---|---|---|
| TP0032 | LH0032 | (1) |
| TP0033 | LH0033 | (1) |

| **TEXAS INSTRUMENTS** | **NATIONAL** | |
|---|---|---|
| μA78XXCKC | LM78XXCT | (1) |
| μA78LXXACL | LM78LXXACZ | (1) |
| μA78MXXCKD | LM78MXXCP | (1) |
| μA79MXXCKD | LM79MXXCP | (1) |
| μA79XXCKC | LM79XXCT | (1) |
| TL061A | LF441 | (1) |
| TL061B | LF441A | (1) |
| TL061 | LF441 | (1) |
| TL062A | LF442 | (1) |
| TL062B | LF442 | (1) |
| TL062 | LF442 | (1) |
| TL064A | LF444 | (1) |
| TL064 | LF444 | (1) |
| TL071B | LF411 | (1) |
| TL071A | LF411 | (1) |
| TL071 | LF351 | (1) |
| TL072 | LF353 | (1) |
| TL072A | LF412 | (1) |
| TL072B | LF412 | (1) |
| TL074 | LF347 | (1) |
| TL074A | LF347B | (1) |
| TL081B | LF411 | (1) |
| TL081 | TL081 | (1) |
| TL081A | LF411 | (1) |
| TL082B | LF412 | (1) |
| TL082A | LF412 | (1) |
| TL082 | TL082 | (1) |
| TL084A | LF347B | (1) |
| TL084 | LF347 | (1) |
| TL087 | LF411A | (1) |
| TL088 | LF411A | (1) |
| TLC274BI | LMC660AI | (2) |
| TLC274BM | LMC660AM | (2) |
| TLC274M | LMC660AM | (2) |
| TLC274AC | LMC660AI | (2) |
| TLC274BC | LMC660AI | (2) |
| TLC274AM | LMC660AM | (2) |
| TLC274I | LMC660AI | (2) |
| TLC274C | LMC660C | (2) |
| TLC274AI | LMC660AI | (2) |
| TL288 | LF412A | (1) |
| LM317KC | LM317T | (1) |
| TL487N | LM3915N | (2) |
| TL489N | LM3914N | (2) |
| TL490N | LM3914N | (2) |
| TL491N | LM3914N | (2) |
| TL520 | ADC0848 | (2) |
| TL521 | ADC0848 | (2) |
| TL522 | ADC0848 | (2) |
| TL530 | ADC0830B | |
| TL531 | ADC0830C | |
| TL532 | ADC0829B | |
| TLC532A | ADC0829B | (2) |
| TLC533A | ADC0829C | (2) |
| TL533 | ADC0829C | |
| TLC540 | ADC0811 | (2) |
| TLC541 | ADC0811 | |
| TLC549 | ADC0831 | (2) |
| μA709 | LM709 | |
| μA723CN | LM723CN | (1) |
| μA723CJ | LM723CJ | (1) |
| μA723MJ | LM723J | (1) |
| μA733CN | LM733CN | |
| μA741 | LM741 | |
| μA747 | LM747 | |
| ADC0801 | ADC0801 | |
| ADC0802 | ADC0802 | |
| ADC0803 | ADC0803 | |
| ADC0804 | ADC0804 | |
| ADC0805 | ADC0805 | |
| ADC0808 | ADC0808 | |
| ADC0809 | ADC0809 | |
| ADC0831 | ADC0831 | |
| ADC0832 | ADC0832 | |
| ADC0834 | ADC0834 | |
| ADC0838 | ADC0838 | |
| RC4558 | LM833 | |
| RV4558D | LM833CM | |
| RC4558D | LM833CM | |

| **THOMSON** | **NATIONAL** | |
|---|---|---|
| LM105H | LM105H | (1) |
| LM109K | LM109K STEEL | (1) |
| LM117K | LM117K STEEL | (1) |
| LM117H | LM117H | (1) |
| LM123K | LM123K STEEL | (1) |
| LM134 | LM134 | |
| LM135 | LM135 | |
| LM137K | LM137K STEEL | (1) |
| LM137H | LM137H | (1) |
| LM138K | LM138K STEEL | (1) |
| LF198 | LF198A | (1) |
| LM234 | LM234 | |
| LM235 | LM235 | |
| LF298 | LF298 | |
| LM305H | LM305H | (1) |
| LM309H | LM309H | (1) |
| LM309K | LM309K STEEL | (1) |

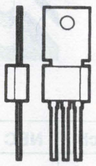
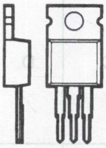
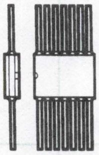
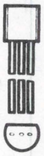
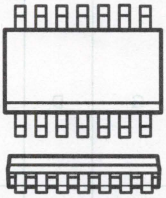
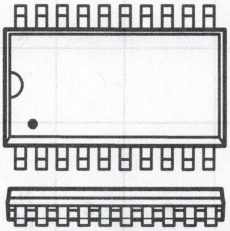
| | | |
|---|---|---|
| LM317K | LM317K STEEL | (1) |
| LM317H | LM317H | (1) |
| LM323K | LM323K STEEL | (1) |
| LM334 | LM334 | (1) |
| LM335A | LM335A | (1) |
| LM335 | LM335 | (1) |
| LM337H | LM337H | (1) |
| LM337K | LM337K STEEL | (1) |
| LM338K | LM338K STEEL | (1) |
| LF398 | LF398A | (1) |
| µA741 | LM741 | (1) |
| µA748 | LM748 | (1) |
| TBC0136 | LM336 | (1) |
| µA7805CK | LM7805KC | (1) |
| µA7805MK | LM140K-5.0 | (1) |
| µA7812MK | LM140K-12 | (1) |
| µA7812CK | LM7812KC | (1) |
| µA7815CK | LM7815KC | (1) |
| µA7815MK | LM140K-15 | (1) |
| µA7905MK | LM120K-5.0 | (1) |
| µA7905CK | LM7905KC | (1) |
| µA7912MK | LM120K-12 | (1) |
| µA7912CK | LM7912KC | (1) |
| µA7915MK | LM120K-15 | (1) |
| µA7915CK | LM7915KC | (1) |
| | | |
| **TOSHIBA** | **NATIONAL** | |
| TA7504 | LM741 | |
| TA75339 | LM2901 | (1) |
| TA75358 | LM2904 | (1) |
| TA75393 | LM2903 | (1) |
| TA75902 | LM2902 | (1) |
| | | |
| **UNITRODE** | **NATIONAL** | |
| L293 | LM18293 | |
| L298 | LM18298 | |

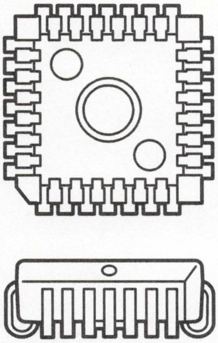
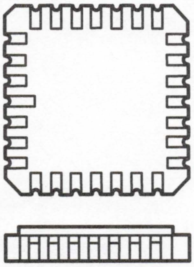
# Industry Package Cross-Reference Guide

| | | NSC | Signetics | Fairchild | Motorola | TI | RCA | Hitachi | NEC | LTC |
|---|---|---|---|---|---|---|---|---|---|---|
|  | 4/16 Lead Glass/Metal DIP | D | I | D | L | | D | C | D | D |
|  | Glass/Metal Flat Pack | F | Q | F | F | F,<br>S | K | F | | Q |
|  | TO-99, TO-100, TO-5 | H | T,<br>K,<br>L,<br>DB | H | G | L | S*,<br>V1** | | A | H |
|  | 8-, 14- and 16-Lead Low Temperature Ceramic DIP | J | F | R,<br>D | U | J | | G | D | J,<br>J8 |
|  | TO-3 (Steel) | K | | | KS | | | | | K |
| | TO-3 (Aluminum) | KC | DA | K | K | K | | | | |
|  | 8-, 14- and 16-Lead Plastic DIP | N | V,<br>A,<br>B | T,<br>P | P | P,<br>N | E | P | C | N,<br>N8 |

*With dual-in-line formed leads

**With radically formed leads

| | | NSC | Signetics | Fairchild | Motorola | TI | RCA | Hitachi | NEC | LTC |
|---|---|---|---|---|---|---|---|---|---|---|
|  | TO-202<br>(D-40, Durawatt) | P | | | | | KD | | | |
|  | TO-220<br>3- & 5-Lead | T | U | U | | KC | | T | H | T |
| | TO-220<br>11-, 15- & 23-Lead | T | | | | | | | | |
|  | Low Temperature Glass Hermetic Flat Pack | W | | F | F | W | | | | |
|  | TO-92<br>(Plastic) | Z | S | W | P | LP | | | H | Z |
|  | | | | | | | | | | |
|  | SO (Narrow Body) | M | D | S | D | D | M | MP | G | S |
| | SO (Wide Body) | WM | | | | DW | | | | |

| | | NSC | Signetics | Fairchild | Motorola | TI | RCA | Hitachi | NEC | LTC |
|---|---|---|---|---|---|---|---|---|---|---|
|  | PCC | V | A | Q | FN | FN | Q | CP | L | |
|  | LCC<br>Leadless Ceramic<br>Chip Carrier | E | G | L1 | U | FK/<br>FG/FH | BJ | CG | K | |

# Linear 2 Databook

## Selection Guides

**Active Filters**

**Analog Switches/Multiplexers**

**Analog-to-Digital Converters**

**Digital-to-Analog Converters**

**Sample and Hold**

**Temperature Sensors**

**Voltage References**

National
Semiconductor
Corporation

# Active Filters
# Definition of Terms

**$f_{CLK}$:** the switched capacitor filter external clock frequency.

**$f_o$:** center of frequency of the second order function complex pole pair. $f_O$ is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence.

**Q:** quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of $f_O$ over the −3 dB bandwidth of the 2nd order bandpass filter. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

**$H_{OBP}$:** the gain in (V/V) of the bandpass output at $f = f_O$.

**$H_{OLP}$:** the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz.

**$H_{OHP}$:** the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$.

**$Q_Z$:** the quality factor of the 2nd order function complex zero pair, if any. ($Q_Z$ is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

**$f_Z$:** the center frequency of the 2nd order function complex zero pair, if any. If $f_Z$ is different from $f_O$, and if the $Q_Z$ is quite high it can be observed as a notch frequency at the allpass output.

**$f_{notch}$:** the notch frequency observed at the notch output(s) of the MF10.

**$H_{ON_1}$:** the notch output gain as $f \rightarrow 0$ Hz.

**$H_{ON_2}$:** the notch output gain as $f \rightarrow f_{CLK}/2$.

National
Semiconductor
Corporation

# Active Filter Selection Guide

| Device # | Type | Function | Max Order | Max Freq Accuracy | Freq Range | Typ. Q Accuracy | Max F x Q |
|---|---|---|---|---|---|---|---|
| MF10 (S, T) | Universal | Universal | 4th | ±0.6% | 0.1–30 kHz | ±2% | 200 kHz |
| MF8 (T) | Bandpass | Chebyshev<br>Butterworth | 4th | ±1.0% | 0.1–20 kHz | ±2% | 5 MHz |
| MF6 (S, T) | Lowpass | Butterworth | 6th | ±1.0 | 0.1–20 kHz | N/A | N/A |
| MF5 (S) | Universal | Universal | 2nd | ±1.0% | 0.1–30 kHz | ±6% | 200 kHz |
| MF4 (S) | Lowpass | Butterworth | 4th | ±0.6% | 0.1–20 kHz | N/A | N/A |
| *LMF100 | Universal | Universal | 4th | ±0.6% | 40 kHz | ±2% | 1.8 MHz |
| *LMF60 | Lowpass | Butterworth | 6th | ±0.6% | 40 kHz | N/A | N/A |

**S** Surface Mount Available

**T** Extended Temperature Available

* Advance Information

National
Semiconductor
Corporation

# Analog Switch
# Definition of Terms

**$R_{ON}$**: Resistance between the output and the input of an addressed channel.

**$I_S$**: Current at any switch input. This is leakage current when the switch is ON.

**$I_D$**: Current at any switch input going into the switch. This is leakage current when the switch is OFF.

**$C_S$**: Capacitance between any open terminal "S" and ground.

**$C_D$**: Capacitance between any open terminal "D" and ground.

**$I_D - I_S$**: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current $I_D$ going into the switch and the current $I_S$ going out of the switch.

**$t_{RAN}$**: Delay time when switching from one address state to another.

**$t_{ON}$**: Delay time between the 50% points of an enable input and the switch ON condition.

**$t_{OFF}$**: Delay time between the 50% points of the enable input and the switch OFF condition.

# Analog Switch/Multiplexer Selection Guide

| Part Number | Function | Logic Input | $V_S$ (Typ) | $T_{ON}/T_{OFF}$ ns (Typ) | $R_{ON}$ Ω |
|---|---|---|---|---|---|
| AH5011 | QUAD SPST | TTL, CMOS | — | 150/300 | 100 |
| AH5012 | | TTL, CMOS | — | 150/300 | 150 |
| CD4016 | | CMOS | ±7.5 | 20/40 | 850 |
| CD4066 | | CMOS | ±7.5 | 25/50 | 280 |
| LF11201/LF13201 | | TTL | ±15 | 90/500 | 200 |
| LF11202/LF13202 | | TTL | ±15 | 90/500 | 200 |
| LF11331/LF13331 | | TTL | ±15 | 90/500 | 200 |
| LF11332/LF13332 | | TTL | ±15 | 90/500 | 200 |
| LF11333/LF13333 | | TTL | ±15 | 90/500 | 200 |
| MM74HC4016 | | CMOS | ±12 | 5/8 | 40 |
| AH5020 | DUAL SPDT | TTL, CMOS | — | 150/300 | 150 |
| CD4053 | TRIPLE SPDT | CMOS | ±7.5 | 160/75 | 300 |
| MM74HC4053 | | CMOS | ±6.0 | 15/16 | 40 |
| AH5009 | 4-CHANNEL | TTL, CMOS | — | 150/300 | 100 |
| AH5010 | | TTL, CMOS | — | 150/300 | 150 |
| CD4052 | 4-CHANNEL DIFFERENTIAL | CMOS | ±7.5 | 160/75 | 300 |
| CD4529B | | CMOS | ±7.5 | 50 | 350 |
| LF13509 | | TTL, CMOS | ±18 | 1600/200 | 350 |
| MM74HC4052 | | CMOS | ±6.0 | 15/16 | 40 |
| CD4051 | 8-CHANNEL | CMOS | ±7.5 | 160/75 | 300 |
| CD4529B | | CMOS | ±7.5 | 50 | 350 |
| LF13508 | | TTL, CMOS | ±18 | 1600/200 | 350 |
| MM74HC4051 | | CMOS | ±6.0 | 15/16 | 40 |

# Definition Of Terms
# A/D Converters

**Conversion Time:** The time required for a complete measurement by an analog-to-digital converter.

**DC Common-Mode Error:** This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

**Differential Nonlinearity:** Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

**Gain Error (Full Scale Error):** For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

**Gain Temperature Coefficient (Full Scale Temperature Coefficient):** Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

**Integral Nonlinearity (Linearity Error):** Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

**LSB (Least-Significant Bit):** In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by $2^n$, where n is the resolution of the converter.

**Missing Codes:** When an incremental increase or decrease in input voltage causes the converter to increment or decrement its numeric output by more than one LSB the converter is said to exhibit "missing codes". If there are missing codes, there is a numeric value on the output on the converter which cannot be reached by any input voltage value.

**Monotonicity:** A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

**MSB (Most Significant Bit):** In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

**Multiplying DAC:** In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by $2^n$ (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity four quadrant multiplication exists.

**Offset Error (Zero Error):** In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

**Power Supply Rejection (Power Supply Sensitivity):** The sensitivity of a converter to changes in the dc power supply voltages.

**Quantizing Error:** The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

**Ratiometric Operation:** Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

**Resolution:** The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to $2^n$. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

**Settling Time:** The time from a change in input code until a DAC's output signal remains within ±½ LSB (or some other specified tolerance) of the final value.

# A/D Converter Selection Guide

| Part No. | Resolution (Bits) | Absolute Accuracy (Max) | Conversion Time | Input Voltage Range | Output Logic Levels | Supplies (V) | Temperature Range* | | | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | M | I | C | | |
| **A/D CONVERTER** | | | | | | | | | | | |
| ADC0800 | 8 | ±2 LSB | 50 µs | ±5V | TTL, TRI-STATE | +5, −12 | • | | • | 18-Pin DIP | |
| ADC0801 | 8 | ±¼ LSB | 110 µs | 5V | TTL, TRI-STATE | +5 | • | • | | 20-Pin DIP | Differential Input |
| ADC0802 | 8 | ±½ LSB | 110 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin SO<br>20-Pin PCC | Differential Input |
| ADC0803 | 8 | ±½ LSB | 110 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin SO<br>20-Pin PCC | Differential Input |
| ADC0804 | 8 | ±1 LSB | 110 µs | 5V | TTL, TRI-STATE | +5 | | • | • | 20-Pin DIP<br>20-Pin SO<br>20-Pin PCC | Differential Input |
| ADC0805 | 8 | ±1 LSB | 110 µs | 5V | TTL, TRI-STATE | +5 | | • | | 20-Pin DIP | Ratiometric Operation |
| ADC0808 | 8 | ±½ LSB | 100 µs | 5V | TTL, TRI-STATE | +5 | • | • | | 28-Pin DIP<br>28-Pin PCC | 8-Channel MUX |
| ADC0809 | 8 | ±1 LSB | 100 µs | 5V | TTL, TRI-STATE | +5 | | • | | 28-Pin DIP<br>28-Pin PCC | 8-Channel MUX |
| ADC0811B | 8 | ±½ LSB | 32 µs | 5V | TTL | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | 11-Channel Serial I/O |
| ADC0811C | 8 | ±1 LSB | 32 µs | 5V | TTL | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | 11-Channel Serial I/O |
| ADC0816 | 8 | ±½ LSB | 100 µs | 5V | TTL, TRI-STATE | +5 | • | • | | 40-Pin DIP | 16-Channel MUX |
| ADC0817 | 8 | ±1 LSB | 100 µs | 5V | TTL, TRI-STATE | +5 | | • | | 40-Pin DIP | 16-Channel MUX |
| ADC0819B | 8 | ±½ LSB | 16 µs | 5V | TTL | +5 | | • | • | 28-Pin DIP<br>28-Pin PCC | 19-Channel Serial I/O |
| ADC0819C | 8 | ±1 LSB | 16 µs | 5V | TTL | +5 | | • | • | 28-Pin DIP<br>28-Pin PCC | 19-Channel Serial I/O |
| ADC0820B | 8 | ±½ LSB | 1.2 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin SO<br>20-Pin PCC | Built-In Track and Hold Function |
| ADC0820C | 8 | ±1 LSB | 1.2 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin SO<br>20-Pin PCC | Built-In Track and Hold Function |

## A/D Converter Selection Guide (Continued)

| Part No. | Resolution (Bits) | Absolute Accuracy (Max) | Conversion Time | Input Voltage Range | Output Logic Levels | Supplies (V) | Temperature Range* | | | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | M | I | C | | |
| **A/D CONVERTER** (Continued) | | | | | | | | | | | |
| ADC0829B | 8 | ± ½ LSB | 100 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | | 28-Pin DIP | Additional Digital Input Capability |
| ADC0829C | 8 | ± 1 LSB | 100 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | | 28-Pin DIP | Additional Digital Input Capability |
| ADC0831B | 8 | ± ½ LSB | 32 μs | 5V | TTL | +5 | | • | • | 8-Pin DIP | Serial I/O |
| ADC0831C | 8 | ± 1 LSB | 32 μs | 5V | TTL | +5 | | • | • | 8-Pin DIP | Serial I/O |
| ADC0832B | 8 | ± ½ LSB | 32 μs | 5V | TTL | +5 | | • | • | 8-Pin DIP | 2-Channel Serial I/O |
| ADC0832C | 8 | ± 1 LSB | 32 μs | 5V | TTL | +5 | | • | • | 8-Pin DIP | 2-Channel Serial I/O |
| ADC0833B | 8 | ± ½ LSB | 32 μs | 5V | TTL | +5 | | • | • | 14-Pin DIP | 4-Channel Serial I/O |
| ADC0833C | 8 | ± 1 LSB | 32 μs | 5V | TTL | +5 | | • | • | 14-Pin DIP | 4-Channel Serial I/O |
| ADC0834B | 8 | ± ½ LSB | 32 μs | 5V | TTL | +5 | | • | • | 14-Pin DIP | 4-Channel Serial I/O |
| ADC0834C | 8 | ± 1 LSB | 32 μs | 5V | TTL | +5 | | • | • | 14-Pin DIP | 4-Channel Serial I/O |
| ADC0838B | 8 | ± ½ LSB | 32 μs | 5V | TTL | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | 8-Channel Serial I/O |
| ADC0838C | 8 | ± 1 LSB | 32 μs | 5V | TTL | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | 8-Channel Serial I/O |
| ADC0841B | 8 | ± ½ LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | Differential Input, Internal Clock |
| ADC0841C | 8 | ± 1 LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 20-Pin DIP<br>20-Pin PCC | Differential Input, Internal Clock |
| ADC0844B | 8 | ± ½ LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 20-Pin DIP | 4-Channel MUX, Internal Clock |
| ADC0844C | 8 | ± 1 LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 20-Pin DIP | 4-Channel MUX, Internal Clock |
| ADC0848B | 8 | ± ½ LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 28-Pin DIP<br>28-Pin PCC | 8-Channel MUX, Internal Clock |
| ADC0848C | 8 | ± 1 LSB | 40 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 28-Pin DIP<br>28-Pin PCC | 8-Channel MUX, Internal Clock |
| ADC1001C | 10 | ± 1 LSB | 200 μs | 5V | TTL,<br>TRI-STATE | +5 | | • | • | 20-Pin DIP | 8-Bit Bus Compatible, Differential Input |
| ADC1005B | 10 | ± ½ LSB | 50 μs | 5V | TTL,<br>TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin PCC | 8-Bit Bus Compatible, Differential Input |

## A/D Converter Selection Guide (Continued)

| Part No. | Resolution (Bits) | Absolute Accuracy (Max) | Conversion Time | Input Voltage Range | Output Logic Levels | Supplies (V) | Temperature Range* | | | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | M | I | C | | |
| **A/D CONVERTER** (Continued) | | | | | | | | | | | |
| ADC1005C | 10 | ±1 LSB | 50 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 20-Pin DIP<br>20-Pin PCC | 8-Bit Bus Compatible, Differential Input |
| ADC1021C | 10 | ±1 LSB | 200 µs | 5V | TTL, TRI-STATE | +5 | | • | • | 24-Pin DIP | Differential Input |
| ADC1025B | 10 | ±½ LSB | 50 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 24-Pin DIP<br>28-Pin PCC | Differential Input |
| ADC1025C | 10 | ±1 LSB | 50 µs | 5V | TTL, TRI-STATE | +5 | • | • | • | 24-Pin DIP<br>28-Pin PCC | Differential Input |
| ADC1205B | 12+sign | ±½ LSB | 100 µs | ±5V | TTL, TRI-STATE | +5, ±5 | | • | • | 24-Pin DIP | 8-Bit Bus Compatible, Differential Input |
| ADC1205C | 12+sign | ±1 LSB | 100 µs | ±5V | TTL, TRI-STATE | +5, ±5 | | • | • | 24-Pin DIP | 8-Bit Bus Compatible, Differential Input |
| ADC1210 | 12 | ±¾ LSB | 200 µs | 10.2V | CMOS | +5 to ±15 | • | • | | 24-Pin DIP | |
| ADC1211 | 12 | ±2 LSB | 200 µs | 10.2V | CMOS | +5 to ±5 | • | • | | 24-Pin DIP | |
| ADC1225B | 12+sign | ±½ LSB | 100 µs | ±5V | TTL, TRI-STATE | +5, ±5 | | • | • | 28-Pin DIP | Differential Input |
| ADC1225C | 12+sign | ±1 LSB | 100 µs | ±5V | TTL, TRI-STATE | +5, ±5 | | • | • | 28-Pin DIP | Differential Input |
| ADC3511 | 3½-Digit | 0.05% | 200 ms | 2V | TTL, TRI-STATE | +5 | | | • | 24-Pin DIP | Integrating µP Compatible |
| ADC3711 | 3¾-Digit | 0.05% | 400 ms | 2V | TTL, TRI-STATE | +5 | | | • | 24-Pin DIP | Integrating µP Compatible |
| LM131 | V-F | 0.01% | N/A | $V_{CC}$ − 2V | Open Collector | +5 to +40 | • | • | • | 8-Pin DIP or TO-99 Can | Voltage-to-Frequency Converter 100 kHz Max |
| **DIGITAL VOLTMETER** | | | | | | | | | | | |
| ADD3501 | 3½-Digit | 0.05% | 200 ms | 2V | 7-Segment LED Drive | +5 | | | • | 28-Pin DIP | 3½-Digit LED DVM |
| ADD3701 | 3½-Digit | 0.05% | 400 ms | 2V | 7-Segment LED Drive | +5 | | | • | 28-Pin DIP | 3¾-Digit LED DVM |

*Temperature ranges: "M" is −55°C to +125°C ambient; "I" is −40°C to +85°C or −25°C to +85°C; "C" is 0°C to +70°C.

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# Definition of Terms
# D/A Converters

**Conversion Time:** The time required for a complete measurement by an analog-to-digital converter.

**DC Common-Mode Error:** This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

**Differential Nonlinearity:** Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

**Gain Error (Full Scale Error):** For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

**Gain Temperature Coefficient (Full Scale Temperature Coefficient):** Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

**Integral Nonlinearity (Linearity Error):** Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

**LSB (Least-Significant Bit):** In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by $2^n$, where n is the resolution of the converter.

**Monotonicity:** A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

**MSB (Most Significant Bit):** In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

**Multiplying DAC:** In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by $2^n$ (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity, four quadrant multiplication exists.

**Offset Error (Zero Error):** In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

**Power Supply Rejection (Power Supply Sensitivity):** The sensitivity of a converter to changes in the dc power supply voltages.

**Quantizing Error:** The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

**Ratiometric Operation:** Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion.** Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

**Resolution:** The smallest analog increment corresponding to a LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to $2^n$. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

**Settling Time:** The time from a change in input code until a DAC's output signal remains within ±½ LSB (or some other specified tolerance) of the final value.

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# D/A Converter Selection Guide

| Part No. | Resolution (Bits) | Linearity @ 25°C % (Max) | Settling Time (+½ LSB) | Supplies (V) | Temperature Range* | | | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | M | I | C | | |
| ADC0852 | 8 | 0.19 | | 5 | | • | • | 8-Pin DIP | DAC, Comparator, Serial Input |
| ADC0854 | 8 | 0.19 | | 5 | | • | • | 14-Pin DIP | DAC, Comparator, Serial Input |
| DAC0800 | 8 | 0.19 | 100 ns | ±5 to ±15 | • | | • | 16-Pin DIP<br>16-Pin S.O. | High-Speed Multiplying |
| DAC0801 | 8 | 0.39 | 100 ns | ±5 to ±15 | • | | • | 16-Pin DIP<br>16-Pin S.O. | High-Speed Multiplying |
| DAC0802 | 8 | 0.10 | 100 ns | ±5 to ±15 | • | | • | 16-Pin DIP<br>16-Pin S.O. | High-Speed Multiplying |
| DAC0806 | 8 | 0.78 | 150 ns | ±5 to ±15 | | | • | 16-Pin DIP<br>16-Pin S.O. | Multiplying |
| DAC0807 | 8 | 0.39 | 150 ns | ±5 to ±15 | | | • | 16-Pin DIP<br>16-Pin S.O. | Multiplying |
| DAC0808 | 8 | 0.19 | 150 ns | ±5 to ±15 | • | | • | 16-Pin DIP<br>16-Pin S.O. | Multiplying |
| DAC0830 | 8 | 0.05 | 1 μs | 5 to 15 | • | • | • | 20-Pin DIP<br>20-Pin S.O.<br>20-Pin PCC | μP Compatible 4-Quadrant Multiplying |
| DAC0831 | 8 | 0.10 | 1 μs | 5 to 15 | | | • | 20-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC0832 | 8 | 0.20 | 1 μs | 5 to 15 | | • | • | 20-Pin DIP<br>20-Pin S.O.<br>20-Pin PCC | μP Compatible 4-Quadrant Multiplying |
| DAC1000 | 10 | 0.05 | 500 ns | 5 to 15 | • | • | • | 24-Pin DIP | μP Compatible Double Buffered |
| DAC1001 | 10 | 0.1 | 500 ns | 5 to 15 | | | • | 24-Pin DIP | μP Compatible Double Buffered |
| DAC1002 | 10 | 0.2 | 500 ns | 5 to 15 | • | • | • | 24-Pin DIP | μP Compatible Double Buffered |
| DAC1006 | 10 | 0.05 | 500 ns | 5 to 15 | • | • | • | 20-Pin DIP | μP Compatible Double Buffered |
| DAC1007 | 10 | 0.1 | 500 ns | 5 to 15 | | • | • | 20-Pin DIP | μP Compatible Double Buffered |
| DAC1008 | 10 | 0.2 | 500 ns | 5 to 15 | • | • | • | 20-Pin DIP | μP Compatible Double Buffered |

## D/A Converter Selection Guide (Continued)

| Part No. | Resolution (Bits) | Linearity @ 25°C % (Max) | Settling Time (+½ LSB) | Supplies (V) | Temperature Range* | | | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | M | I | C | | |
| DAC1020 | 10 | 0.05 | 500 ns | 5 to 15 | ● | ● | ● | 16-Pin DIP | 4-Quadrant Multiplying |
| DAC1021 | 10 | 0.1 | 500 ns | 5 to 15 | ● | ● | ● | 16-Pin DIP | 4-Quadrant Multiplying |
| DAC1022 | 10 | 0.2 | 500 ns | 5 to 15 | ● | ● | ● | 16-Pin DIP | 4-Quadrant Multiplying |
| DAC1208 | 12 | 0.012 | 1 μs | 5 to 15 | | ● | ● | 24-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1209 | 12 | 0.024 | 1 μs | 5 to 15 | | ● | ● | 24-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1210 | 12 | 0.05 | 1 μs | 5 to 15 | | ● | ● | 24-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1218 | 12 | 0.012 | 1 μs | 5 to 15 | | ● | ● | 18-Pin DIP | 4-Quadrant Multiplying |
| DAC1219 | 12 | 0.024 | 1 μs | 5 to 15 | | ● | ● | 18-Pin DIP | 4-Quadrant Multiplying |
| DAC1220 | 12 | 0.05 | 500 ns | 5 to 15 | ● | ● | ● | 18-Pin DIP | 4-Quadrant Multiplying |
| DAC1221 | 12 | 0.1 | 500 ns | 5 to 15 | | | ● | 18-Pin DIP | 4-Quadrant Multiplying |
| DAC1222 | 12 | 0.2 | 500 ns | 5 to 15 | ● | ● | ● | 18-Pin DIP | 4-Quadrant Multiplying |
| DAC1230 | 12 | 0.012 | 1 μs | 5 to 15 | | ● | ● | 20-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1231 | 12 | 0.024 | 1 μs | 5 to 15 | | ● | ● | 20-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1232 | 12 | 0.05 | 1 μs | 5 to 15 | | ● | ● | 20-Pin DIP | μP Compatible 4-Quadrant Multiplying |
| DAC1265A | 12 | 0.006 | 200 ns | ±15 | ● | | ● | 24-Pin DIP | High-Speed |
| DAC1265 | 12 | 0.012 | 200 ns | ±15 | ● | | ● | 24-Pin DIP | High-Speed |
| DAC1266A | 12 | 0.006 | 200 ns | ±12 to ±15 | ● | | ● | 24-Pin DIP | High-Speed |
| DAC1266 | 12 | 0.012 | 200 ns | ±12 to ±15 | ● | | ● | 24-Pin DIP | High-Speed |

*Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" 0°C to +70°C.

# Sample and Hold Definition of Terms

**Acquisition Time:** The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Aperture Time:** The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

**Dynamic Sampling Error:** The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

**Gain Error:** The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

**Hold Settling Time:** The time required for the output to settle within 1 mV of final value after the "hold" logic command.

**Hold Step:** The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

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# Sample and Hold Selection Guide

| | LF198A | LF398A | LF198 | LF398 | LF298 | Units |
|---|---|---|---|---|---|---|
| Accuracy<br>Gain/Offset Error | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | % Max |
| Offset Voltage | 2 | 3 | 5 | 10 | 5 | mV Max |
| Droop Rate (25°C) | | | | | | |
| $C_S$ = 1000 pF | 30 | 30 | 30 | 30 | 30 | mV/sec |
| $C_S$ = 10000 pF | 3 | 3 | 3 | 3 | 3 | |
| Acquisition Time (25°C) | | | | | | |
| $C_S$ = 1000 pF | 4 | 4 | 4 | 4 | 4 | µs |
| $C_S$ = 10000 pF | 20 | 20 | 20 | 20 | 20 | |
| Aperture Time (25°C) | 25 | 25 | 25 | 25 | 25 | ns |
| Temperature Range | −55 to +125 | 0 to +70 | −55 to +125 | 0 to +70 | −25 to +85 | °C |
| Comment | Low Drift | Low Drift | General Purpose | General Purpose | Low Drift | |

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# Temperature Sensor Selection Guide

| Part | Temp. Range | *Accuracy | Output Scale |
|---|---|---|---|
| LM34A | −50°F to +300°F | ±2.0°F | 10 mV/°F |
| LM34 | −50°F to +300°F | ±3.0°F | 10 mV/°F |
| LM34CA | −40°F to +230°F | ±2.0°F | 10 mV/°F |
| LM34C | −40°F to +230°F | ±3.0°F | 10 mV/°F |
| LM34D | +32°F to +212°F | ±4.0°F | 10 mV/°F |
| LM35A | −55°C to +150°C | ±1.0°C | 10 mV/°C |
| LM35 | −55°C to +150°C | ±1.5°C | 10 mV/°C |
| LM35CA | −40°C to +110°C | ±1.0°C | 10 mV/°C |
| LM35C | −40°C to +110°C | ±1.5°C | 10 mV/°C |
| LM35D | 0°C to +100°C | ±2.0°C | 10 mV/°C |
| LM134-3 | −55°C to +125°C | ±3.0°C | $I_{SET} \propto {}^\circ k$ |
| LM134-6 | −55°C to +125°C | ±6.0°C | $I_{SET} \propto {}^\circ k$ |
| LM234-3 | −25°C to +100°C | ±3.0°C | $I_{SET} \propto {}^\circ k$ |
| LM234-6 | −25°C to +100°C | ±6.0°C | $I_{SET} \propto {}^\circ k$ |
| LM135A | −55°C to +150°C | ±1.3°C | 10 mV/°k |
| LM135 | −55°C to +150°C | ±2.0°C | 10 mV/°k |
| LM235A | −40°C to +125°C | ±1.3°C | 10 mV/°k |
| LM235 | −40°C to +125°C | ±2.0°C | 10 mV/°k |
| LM335A | −40°C to +100°C | ±2.0°C | 10 mV/°k |
| LM335 | −40°C to +100°C | ±4.0°C | 10 mV/°k |
| LM3911 | −25°C to +85°C | ±10.0°C | 10 mV/°k (or °F) |

***Note:** Accuracy is measured over T(Min) to T(Max) uncalibrated

**Note:** The LM134/234/334 3-Terminal Adjustable current sources Datasheet can be found in Linear 1, Section 1.

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# Voltage Reference Selection Guide

## Shunt Type

| Reverse Breakdown Voltage ($V_R$) | Device | Operating Temp. Range* | Voltage Tolerance Max, $T_A$ = 25°C | Temperature Drift | | Operating Current Range, $I_R$ | Output Dynamic Impedance (Typ) |
|---|---|---|---|---|---|---|---|
| | | | | ppm/°C (Max) | Over Range | | |
| 1.22 | LM113-2 | M | ±1% | 50 (Typ) | −55°C to +125°C | 500 μA to 20 mA | 0.8 |
| 1.22 | LM113-1 | M | ±2% | 50 (Typ) | −55°C to +125°C | 500 μA to 20 mA | 0.8 |
| 1.22 | LM113 | M | ±5% | 100 (Typ) | −55°C to +125°C | 500 μA to 20 mA | 0.8 |
| 1.22 | LM313 | C | ±5% | 100 (Typ) | 0°C to +70°C | 500 μA to 20 mA | 0.8 |
| 1.235 | LM185BX-1.2 | M | ±1% | 30 | −55°C to +125°C | 10 μA to 20 mA | 1 |
| 1.235 | LM185BY-1.2 | M | ±1% | 50 | −55°C to +125°C | 10 μA to 20 mA | 1 |
| 1.235 | LM185-1.2 | M | ±1% | 150 | −55°C to +125°C | 10 μA to 20 mA | 1 |
| 1.235 | LM285BX-1.2 | I | ±1% | 30 | −40°C to +85°C | 10 μA to 20 mA | 1 |
| 1.235 | LM285BY-1.2 | I | ±1% | 50 | −40°C to +85°C | 10 μA to 20 mA | 1 |
| 1.235 | LM285-1.2 | I | ±1% | 150 | −40°C to +85°C | 10 μA to 20 mA | 1 |
| 1.235 | LM385BX-1.2 | C | ±1% | 30 | 0°C to +70°C | 15 μA to 20 mA | 1 |
| 1.235 | LM385BY-1.2 | C | ±1% | 50 | 0°C to +70°C | 15 μA to 20 mA | 1 |
| 1.235 | LM385B-1.2 | C | ±1% | 150 | 0°C to +70°C | 15 μA to 20 mA | 1 |
| 1.235 | LM385-1.2 | C | +2%, −2.4% | 150 | 0°C to +70°C | 15 μA to 20 mA | 1 |
| 1.24 to 5.3 (Adj.) | LM185B | M | ±1% | 150 | −55°C to +125°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM185BX | M | ±1% | 50 | −55°C to +125°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM185BY | M | ±1% | 50 | −55°C to +125°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM285BX | I | ±1% | 30 | −40°C to +85°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM285BY | I | ±1% | 50 | −40°C to +85°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM285 | I | ±2% | 150 | −40°C to +85°C | 10 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM385BX | C | ±1% | 30 | 0°C to +70°C | 13 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM385BY | C | ±1% | 50 | 0°C to +70°C | 13 μA to 20 mA | 0.3 |
| 1.24 to 5.3 (Adj.) | LM385 | C | ±2% | 150 | 0°C to +70°C | 13 μA to 20 mA | 0.3 |
| 2.49 | LM136A | M | ±1% | 72 | −55°C to +125°C | 400 μA to 10 mA | 0.4 |
| 2.49 | LM136 | M | ±2% | 72 | −55°C to +125°C | 400 μA to 10 mA | 0.4 |
| 2.49 | LM236A | I | ±1% | 72 | −25°C to +85°C | 400 μA to 10 mA | 0.4 |
| 2.49 | LM236 | I | ±2% | 72 | −25°C to +85°C | 400 μA to 10 mA | 0.4 |
| 2.49 | LM336 | I | ±4% | 54 | 0°C to +70°C | 400 μA to 10 mA | 0.4 |
| 2.49 | LM336B | C | ±2% | 54 | 0°C to +70°C | 400 μA to 10 mA | 0.4 |
| 2.5 | LM185BX-2.5 | M | ±1.5% | 30 | −55°C to +125°C | 20 μA to 20 mA | 1 |
| 2.5 | LM185BY-2.5 | M | ±1.5% | 50 | −55°C to +125°C | 20 μA to 20 mA | 1 |
| 2.5 | LM185B-2.5 | M | ±1.5% | 150 | −55°C to +125°C | 20 μA to 20 mA | 1 |
| 2.5 | LM285BX-2.5 | I | ±1.5% | 30 | −40°C to +85°C | 20 μA to 20 mA | 1 |
| 2.5 | LM285BY-2.5 | I | ±1.5% | 50 | −40°C to +85°C | 20 μA to 20 mA | 1 |
| 2.5 | LM285-2.5 | I | ±1.5% | 150 | −40°C to +85°C | 20 μA to 20 mA | 1 |
| 2.5 | LM385BX-2.5 | C | ±1.5% | 30 | 0°C to +70°C | 20 μA to 20 mA | 1 |
| 2.5 | LM385BY-2.5 | C | ±1.5% | 50 | 0°C to +70°C | 20 μA to 20 mA | 1 |
| 2.5 | LM385B-2.5 | C | ±1.5% | 150 | 0°C to +70°C | 20 μA to 20 mA | 1 |
| 2.5 | LM385-2.5 | C | ±3% | 150 | 0°C to +70°C | 20 μA to 20 mA | 1 |

## Shunt Type (Continued)

| Reverse Breakdown Voltage ($V_R$) | Device | Operating Temp. Range* | Voltage Tolerance Max, $T_A$ = 25°C | Temperature Drift ppm/°C (Max) | Temperature Drift Over Range | Operating Current Range, $I_R$ | Output Dynamic Impedance (Typ) |
|---|---|---|---|---|---|---|---|
| 5.0 | LM136A | M | ±1% | 72 | −55°C to +125°C | 400 µA to 10 mA | 0.8 |
| 5.0 | LM136 | M | ±2% | 72 | −55°C to +125°C | 400 µA to 10 mA | 0.8 |
| 5.0 | LM236A | I | ±1% | 72 | −25°C to +85°C | 400 µA to 10 mA | 0.8 |
| 5.0 | LM236 | I | ±2% | 72 | −25°C to +85°C | 400 µA to 10 mA | 0.8 |
| 5.0 | LM336B | C | ±2% | 54 | 0°C to +70°C | 400 µA to 10 mA | 0.8 |
| 5.0 | LM336 | C | ±4% | 54 | 0°C to +70°C | 400 µA to 10 mA | 0.8 |
| 6.9 | LM129A | M | +3%, −2% | 10 | −55°C to +125°C | 600 µA to 15 mA | 0.6 |
| 6.9 | LM129B | M | +3%, −2% | 20 | −55°C to +125°C | 600 µA to 15 mA | 0.6 |
| 6.9 | LM129C | M | +3%, −2% | 50 | −55°C to +125°C | 600 µA to 15 mA | 0.6 |
| 6.9 | LM329B | C | ±5% | 50 | 0°C to +70°C | 600 µA to 15 mA | 0.8 |
| 6.9 | LM329C | C | ±5% | 20 | 0°C to +70°C | 600 µA to 15 mA | 0.8 |
| 6.9 | LM329D | C | ±5% | 100 | 0°C to +70°C | 600 µA to 15 mA | 0.8 |
| 6.95 | LM199A | M | ±2% | 0.5 | −55°C to +125°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM199A-20 | M | Same as LM199A with 20 ppm guaranteed long term drift. | | | | |
| 6.95 | LM199 | M | ±2% | 1.0 | −55°C to +125°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM299A | I | ±2% | 0.5 | −25°C to +85°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM299A-20 | I | Same as LM299A with 20 ppm guaranteed long term drift. | | | | |
| 6.95 | LM299 | I | ±2% | 1 | −25°C to +85°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM399A | C | ±5% | 1 | 0°C to +70°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM399A-50 | C | Same as LM399A with 50 ppm guaranteed long term drift. | | | | |
| 6.95 | LM399 | C | ±5% | 2 | 0°C to +70°C | 500 µA to 10 mA | 0.5 |
| 6.95 | LM3999 | C | ±5% | 5 | 0°C to +70°C | 600 µA to 10 mA | 0.6 |

*C (Commercial) = 0°C to 70°C, I (Industrial) = −25°C to +85°C for the LM236 and LM299, I = −40°C to +85°C for all others.
M (Military) = −55°C to +125°C

## Current References

| Output Current Range | Device | Operating Temperature Range | Set Current Error 2 µA to 10 µA | Set Current Error 10 µA to 1 mA | Set Current Error 1 mA to 5 mA | Operating Voltage Range | Set Current Temperature Dependence* |
|---|---|---|---|---|---|---|---|
| 2 µA to 10 mA | LM134 | −55°C to +125°C | ±8% | ±3% | ±5% | 1V to 40V | 0.96T to 0.104T |
| 2 µA to 10 mA | LM134-3 | −55°C to +125°C | N/A | ±1% | N/A | 1V to 40V | 0.98T to 0.102T |
| 2 µA to 10 mA | LM134-6 | −55°C to +125°C | N/A | ±2% | N/A | 1V to 40V | 0.97T to 0.103T |
| 2 µA to 10 mA | LM234 | −25°C to +100°C | ±8% | ±3% | ±5 | 1V to 40V | 0.96T to 0.104T |
| 2 µA to 10 mA | LM234-3 | −25°C to +100°C | N/A | ±1% | N/A | 1V to 40V | 0.98T to 0.102T |
| 2 µA to 10 mA | LM234-6 | −25°C to +100°C | N/A | ±2% | N/A | 1V to 40V | 0.97T to 0.103T |
| 2 µA to 10 mA | LM334 | 0°C to +70°C | ±12% | ±6% | ±8% | 1V to 40V | 0.96T to 0.104T |

*Set current changes linearly with temperature at a rate of 0.33%/°C.

## Series Type (Buffered Output)

| Output Voltage | Device | Oper. Temp. Range* | Voltage Tolerance Max, $T_A$ = 25°C | Temperature Drift | | Load Reg. ppm/mA | Over Current Range | Quiescent Current (mA) |
|---|---|---|---|---|---|---|---|---|
| | | | | ppm/°C (Max) | Over Range | | | |
| 2.5 | LM368Y-2.5 | C | ±0.2% | 20 | 0°C to +70°C | 25 | 0 mA to +10 mA | 0.55 |
| 2.5 | LM368-2.5 | C | ±0.2% | 30 | 0°C to +70°C | 25 | 0 mA to +10 mA | 0.55 |
| 5.0 | LM168BY-5.0 | M | ±0.05% | 10 | −55°C to +125°C | 10 | −10 mA to +10 mA | 0.35 |
| 5.0 | LM268BY-5.0 | I | ±0.05% | 15 | −40°C to +85°C | 10 | −10 mA to +10 mA | 0.35 |
| 5.0 | LM368BY-5.0 | C | ±0.1% | 20 | 0°C to +70°C | 10 | −10 mA to +10 mA | 0.35 |
| 5.0 | LM368-5.0 | C | ±0.1% | 30 | 0°C to +70°C | 10 | −10 mA to +10 mA | 0.35 |
| 10 | LM169B | M | ±0.05% | 3 | −55°C to +125°C | 8 | −10 mA to +10 mA | 1.8 |
| 10 | LM168BY-10 | M | ±0.05% | 10 | −55°C to +125°C | 10 | −10 mA to +10 mA | 0.35 |
| 10 | LH0070-2 | M | ±0.05% | 8 | −40°C to +85°C | 60 | 0 to 5 mA | 5 |
| 10 | LM169 | M | ±0.05% | 5 | −55°C to +125°C | 8 | −10 mA to +10 mA | 1.8 |
| 10 | LM581U | M | ±0.05% | 10 | −55°C to +125°C | 50 | 0 mA to 5 mA | 1.8 |
| 10 | LH0070-0 | M | ±0.1% | 40 | −40°C to +85°C | 60 | 0 mA to 5 mA | 5 |
| 10 | LM581T | M | ±0.1% | 10 | −55°C to +125°C | 50 | 0 mA to 5 mA | 1.8 |
| 10 | LH0070-1 | M | ±0.1% | 20 | −40°C to +85°C | 60 | 0 mA to 5 mA | 5 |
| 10 | LM581S | M | ±0.3% | 30 | −55°C to +125°C | 50 | 0 mA to 5 mA | 1.8 |
| 10 | LM268BY-10 | I | ±0.05% | 15 | −40°C to +85°C | 10 | −10 mA to +10 mA | 0.35 |
| 10 | LM581L | C | ±0.05% | 5 | 0°C to +70°C | 50 | 0 mA to 5 mA | 1.8 |
| 10 | LM369C | C | ±0.05% | 10 | 0°C to +70°C | 8 | −10 mA to +10 mA | 1.8 |
| 10 | LM369 | C | ±0.05% | 5 | 0°C to +70°C | 8 | −10 mA to +10 mA | 1.8 |
| 10 | LM369B | C | ±0.05% | 3 | 0°C to +70°C | 8 | −10 mA to +10 mA | 1.8 |
| 10 | LM581K | C | ±0.1% | 10 | 0°C to +70°C | 50 | 0 mA to 5 mA | 1.8 |
| 10 | LM368Y-10 | C | ±0.1% | 20 | 0°C to +70°C | 10 | −10 mA to +10 mA | 0.35 |
| 10 | LM368-10 | C | ±0.1% | 30 | 0°C to +70°C | 10 | −10 mA to +10 mA | 0.35 |
| 10 | LM369D | C | ±0.1% | 30 | 0°C to +70°C | 8 | −10 mA to +10 mA | 2 |
| 10 | LM581J | C | ±0.3% | 30 | 0°C to +70°C | 50 | 0 mA to 5 mA | 1.8 |
| 10.24 | LH0071-2 | M | ±0.05% | 8 | −40°C to +85°C | 60 | 0 mA to 5 mA | 5 |
| 10.24 | LH0071-1 | M | ±0.1% | 20 | −40°C to +85°C | 60 | 0 mA to 5 mA | 5 |
| 10.24 | LH0071-0 | M | ±0.1% | 30 | −40°C to +85°C | 60 | 0 mA to 5 mA | 5 |

*C (Commercial) = 0°C to 70°C, I (Industrial) = −40°C to +85°C, M (Military) = −55°C to +125°C

## Low Current Reference Diodes

| Output Voltage | Device | Operating Temp. Range* | Voltage Tolerance Max, $T_A$ = 25°C | Temperature Drift | | Operating Current Range, $I_R$ | Output Dynamic Impedance (Typ) |
|---|---|---|---|---|---|---|---|
| | | | | ppm/°C (Max) | Over Range | | |
| 3.0 | LM103-3.0 | M | ±10% | −1700 | −55°C to +125°C | 10 μA to 10 mA | 25 |
| 3.3 | LM103-3.3 | M | ±10% | −1500 | −55°C to +125°C | 10 μA to 10 mA | 25 |
| 3.6 | LM103-3.6 | M | ±10% | −1400 | −55°C to +125°C | 10 μA to 10 mA | 25 |
| 3.9 | LM103-3.9 | M | ±10% | −1300 | −55°C to +125°C | 10 μA to 10 mA | 25 |

*M (Military) = −55°C to +125°C

## "Reference Grade" Voltage Regulators*

| Output Voltage | Device | Operating Temperature Range | Voltage Tolerance Max, $T_A = 25°C$ | Output Variation Over Operating Range | Load Reg. ppm/mA | Line Reg. ppm/V | Output Current (Max) | Quiescent Current |
|---|---|---|---|---|---|---|---|---|
| Adjustable:<br>1.235V to 30V | LP2951 | −55°C to +150°C | ±0.5% | ±0.5% | 100 | 42 | 100 mA | 120 μA |
| | LP2951AC | −40°C to +125°C | ±0.5% | ±0.5% | 100 | 42 | 100 mA | 120 μA |
| | LP2951C | −40°C to +125°C | ±1% | ±1% | 200 | 83 | 100 mA | 120 μA |
| Programmable:<br>5V, 6V, 10V, 12V, 15V | LH0075 | −55°C to +125°C | ±0.5% | ±0.14% (Typ) | 15 | 200 | 200 mA | 8 mA |
| | LH0075C | 0°C to +70°C | ±1% | ±0.3% (Typ) | 25 | 400 | 200 mA | 10 mA |
| Programmable<br>−5V, −6V, −10V | LH0076 | −55°C to +125°C | ±0.5% | ±0.14% (Typ) | 15 | 200 | 200 mA | 15 mA |
| −10V, −15V | LH0076C | 0°C to +70°C | ±1% | ±0.3% (Typ) | 25 | 400 | 200 mA | 15 mA |
| 5V | LP2950AC | −40°C to +125°C | ±0.5% | ±0.5% | 100 | 42 | 100 mA | 120 μA |
| 5V | LP2950C | −40°C to +125°C | ±1% | ±1% | 200 | 83 | 100 mA | 120 μA |

*For more information on these circuits, refer to the Voltage Regulator section of the Databook.

# Linear 3 Databook

Selection Guides

Audio Circuits

Radio Circuits

Video Circuits

Motion Control

Special Functions

National Semiconductor Corporation

# Audio Circuits Definition of Terms

**Amplifier**

**Class A**

A class A transistor audio amplifier refers to an amplifier with a single output device that has a collector flowing for the full 360° of the input cycle.

**Class B**

The most common type of audio amplifier that basically consists of two output devices each of which conducts for 180° of the input cycle.

**Class C**

In a class C amplifier the collector current flows for less than 180°. Although highly efficient, high distortion results and the load is frequently tuned to minimize this distortion (primarily used in R.F. power amplifiers).

**Class D**

A switching or sampling amplifier with extremely high efficiency (approaching 100%). The output devices are used as switches, voltage appearing across them only while they are off, and current flowing only when they are saturated.

**Crossover Distortion**

Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current allowing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for I/Cs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion for negative going transition through zero at the higher audio frequencies.

**Dolby B**

Dolby B is a simplified version of the Dolby A professional quality noise reduction system. The amplitude of low level signals over a selected frequency range is increased prior to recording to enhance them above tape noise. On playback the original levels are restored causing a corresponding reduction in the audible tape noise. The major difference with Dolby A which used four frequency bands, is the use of a single variable frequency band with a cut-off frequency that increases in the presence of high level high frequency signals.

**Dolby Level**

Because of the complementary nature of the Dolby B noise reduction system, the audio channel between the encoder and the decoder must have a fixed gain such that the decoding signal level is within 2 dB of the encoding signal level. Also if recordings are interchangeable the signals in the noise reduction system must be related to the levels in the audio channel. Dolby level provides this reference and corresponds to a specified tape flux density when recorded with a 400 Hz tone. For reel to reel and eight track cartridge tapes this is 185 nWb/m, and for cassettes Dolby level is 200 nWb/m.

**Large-Signal Voltage Gain**

The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**Output Resistance**

The ratio of the change in output voltage to the change in output current with the output around zero.

**Output Voltage Swing**

The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Power Bandwidth**

The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated at 60 watts with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30 watts.

**Power Supply Rejection**

The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Slew Rate**

The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

**Supply Current**

The current required from the power supply to operate the amplifier with no load and the output at zero.

**Thermal Resistance ($R_{TH}$)**

An analogy for heat transfer where the ability of a heat conductive system to transfer heat is described in similar terms to those used in an electrical system for power dissipated in a resistor with a given applied voltage. The thermal resistance is given by the temperature differential established when a given amount of power is being dissipated ($\theta = T1 - T2/P_D$) with units of °C/watt.

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# Audio Selection Guide

## PREAMPLIFIERS

| | Application | | | Package | Voltage Range | Equivalent Input Noise | THD | PSR | Input Coupling | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Portable | Home | Auto | | | | | | | |
| LM381 | • | • | | 14 Pin DIP | 9V–40V | 0.5 µV | 0.1% | 120 dB | AC | Stereo |
| LM382 | • | • | • | 14 Pin DIP | 9V–40V | 0.8 µV | 0.1% | 120 dB | AC | Stereo |
| LM387 | • | • | • | 8 Pin DIP | 9V–30V | 0.65 µV | 0.1% | 110 dB | AC | Stereo |
| LM1818 | • | • | • | 20 Pin DIP | 3.5V–18V | 0.85 µV | 0.05% | 85 dB | AC | Tape System |
| LM1837 | • | • | • | 18 Pin DIP | 4V–18V | 0.6 µV† | 0.03% | 105 dB | DC | Autoreverse |
| LM1897 | • | • | • | 16 Pin DIP | 4V–18V | 0.6 µV† | 0.03% | 105 dB | DC | Few Externals |
| LM833<br>(Note 1) | | • | • | 8 Pin DIP<br>8 Pin SO | ±5V–±15V | 0.5 µV | 0.002% | 100 dB | DC | Low Noise<br>Dual Op Amp |
| LM837<br>(Note 1) | | • | • | 14 Pin DIP<br>14 Pin SO | ±5V–±15V | 0.5 µV | 0.002% | 100 dB | DC | Low Noise<br>Quad Op Amp<br>Drives 600Ω Load |

†CCIR/ARM in DIN circuit referred to unity gain at 2 kHz.

**Note 1:** Data sheet in Linear 1.

## AUDIO POWER AMPLIFIERS

| | Application | | | Package | Power* | | | @ Voltage | Bridgeable | THD* | Input Noise* | Single/ Dual | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Portable | Home | Auto | | 8Ω | 4Ω | 2Ω | | | | | | |
| LM380 | | • | | 8 Pin DIP<br>14 Pin DIP | 2.5W | | | 18V | | 0.2% | | Single | See AN-69 |
| LM383 | • | | • | 5 Pin TO-220 | | 5.5W | 8.6W | 14.4V | Yes | 0.2% | 2 µV | Single | Protected |
| LM384 | | • | | 14 Pin DIP | 5.5W | | | 22V | | 0.25% | | Single | Fixed Gain |
| LM386 | • | | | 8 Pin DIP<br>8 Pin SO | | 0.33W | | 6V | | 0.2% | | Single | 4V Operation |
| LM388 | • | | | 14 Pin DIP | 2.2W | | | 12V | Yes | 0.1% | | Single | Minimum Externals |
| LM389 | • | | | 18 Pin DIP | | 0.33W | | 6V | | 0.2% | | Single | Includes Transistor Array |
| LM390 | • | | | 14 Pin DIP | | 1W | | 6V | Yes | 0.2% | | Single | Battery Operation |
| LM391 | | • | | 16 Pin DIP | | | | 60V–100V | | 0.01% | 3 µV | Single | Power Driver |
| LM1877 | • | • | • | 14 Pin DIP | 3W | | | 20V | | 0.05% | 2.5 µV | Dual | 6V–24V |
| LM2877 | • | • | • | 11 Pin SIP | 4.5W | | | 20V | | 0.07% | 2.5 µV | Dual | Single-In-Line Package |
| LM1895 | • | • | • | 8 Pin DIP | | 1.1W | | 6V | | 0.2% | 1.4 µV | Single | Low AM Radiation |
| LM2895 | • | • | • | 11 Pin SIP | | 4.3W | | 12V | | 0.15% | 1.4 µV | Single | 3V–15V |

## AUDIO POWER AMPLIFIERS (Continued)

| | Application | | | Package | Power* | | | @ Voltage | Bridgeable | THD* | Input Noise* | Single/ Dual | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Portable | Home | Auto | | 8Ω | 4Ω | 2Ω | | | | | | |
| LM1896 | • | • | • | 14 Pin DIP | | 1.1W | | 6V | Yes | 0.1% | 1.4 µV | Dual | Low AM Radiation |
| LM2896 | • | • | • | 11 Pin SIP | | 2.5W | | 9V | Yes | 0.1% | 1.4 µV | Dual | No Pops |
| LM2002 | • | | • | 5 Pin TO-220 | | 5.2W | 8W | 14.4V | Yes | 0.1% | 2 µV | Single | Protected |
| LM2878 | | • | | 11 Pin SIP | 5.5W | | | 22V | Yes | 0.15% | 2.5 µV | Dual | 6V–32V |
| LM831 | • | | | 16 Pin DIP<br>20 Pin SO | 0.44W | | | 3V | Yes | 0.2% | 1.3 µV | Dual | 1.8V–6V |
| LM12 (Note 1) | | • | | TO-3 | 50W | 85W | | ±30V | | 0.01% | | Single | Power Op Amp |
| LM675 (Note 1) | | • | | 5 Pin TO-220 | 20W | | | ±25V | | | 3 µV | Single | Power Op Amp |
| LM1875 | | • | | 5 Pin TO-220 | 20W | | | ±25V | | 0.015% | 3 µV | Single | Low Crossover Distortion |
| LM2005 | | | • | 11 Pin TO-220 | | 20W | | 14.4V | Yes | 0.3% | 1.5 µV | Dual | Protected |
| LM2879 | | • | | 11 Pin TO-220 | 8W | | | 28V | Yes | 0.05% | 2.5 µV | Dual | 6V–32V |

*Note that all values shown are typical. Please refer to data sheets for test conditions.

**Note 1:** Data sheet in Linear 1.

## AUDIO CONTROLS

| | Application | | | Package | Voltage Range | Volume Control Range | Signal to Noise | THD | Separation | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | Portable | Home | Auto | | | | | | | |
| LM1035/ LM1036 | • | • | • | 20 Pin DIP | 8V–18V | 80 dB | 80 dB | 0.05% | 75 dB | Dual DC Controlled Tone/Volume/Balance |
| LM1037 | • | • | • | 18 Pin DIP | 5V–30V | | 100 dB | 0.04% | 100 dB | DC Audio Switch |
| LM1038 | • | • | • | 18 Pin DIP | 5V–30V | | 100 dB | 0.04% | 100 dB | BCD Logic Control |
| LM13600 (Note 1) | • | • | • | 16 Pin DIP | ±2V–±18V | | | 0.5% | 100 dB | Transconductance Amplifiers |
| LM13700 (Note 1) | • | • | • | 16 Pin SO | | | | | | |
| LM3080 (Note 1) | • | • | • | 8 Pin DIP | ±2V–±18V | | | | | Transconductance Amplifier |
| LM1040 | • | • | • | 24 Pin DIP | 9V–16V | 75 dB | 80 dB | 0.06% | 75 dB | Dual DC Controlled Tone/Volume/Balance Stereo Enhancement |
| LMC835 | | • | • | 28 Pin DIP | ±2.5V–±8V | | 114 dB | * | | 7 Band Graphic Equalizer MICROWIRE™ Controlled |
| LMC1992/ LMC1993 (Note 2) | | • | • | 28 Pin DIP | 7V–15V | 80 dB | 105 dB | 0.03% | 95 dB | Stereo Volume/ Tone/Fade/Select MICROWIRE™ Controlled |

*Distortion determined by external op amps.

**Note 1:** Data sheet in Linear 1.

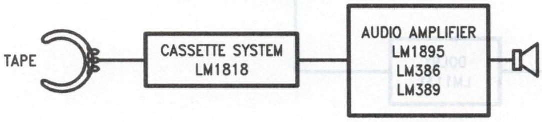
**Note 2:** LMC1992 selects 4 inputs.
LMC1993 selects 3 inputs and has a loudness control.

## NOISE REDUCTION

| | Application | | | Package | Voltage Range | NR Type | NR Effect* | Encoding Required | Single/ Dual/ | Decode S/N* | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Portable | Home | Auto | | | | | | | | |
| LM1131 | • | • | • | 18 Pin DIP | 7V–20V | Dolby | 10 dB | Yes | Dual | 90 dB | DC Switched |
| LM1894 | • | • | • | 14 Pin DIP, SO | 4.5V–18V | DNR | 12 dB | No | Dual | 76 dB | NSC System |
| LM1112 | • | • | • | 16 Pin DIP | 6V–20V | Dolby | 10 dB | Yes | Single | 83 dB | |
| LM1141 | • | • | • | 28 Pin DIP, Quad | 5V–16V | Dolby | | Yes | Single | | Dolby B/C |
| LM832 | • | | | 14 Pin DIP, SO | 1.5V–9V | DNR | 12 dB | No | Dual | 76 dB | NSC System |

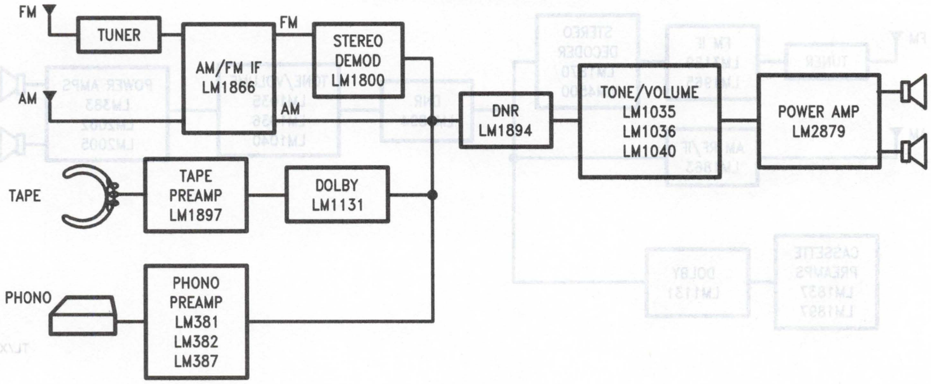
*Note that all values shown are typical. Please refer to data sheets for test conditions.

### Monaural Cassette Player


TAPE
CASSETTE SYSTEM
LM1818
AUDIO AMPLIFIER
LM1895
LM386
LM389

TL/XX/0013–1

### Home Stereo System (Audio Power < 10W)


FM
TUNER
AM/FM IF
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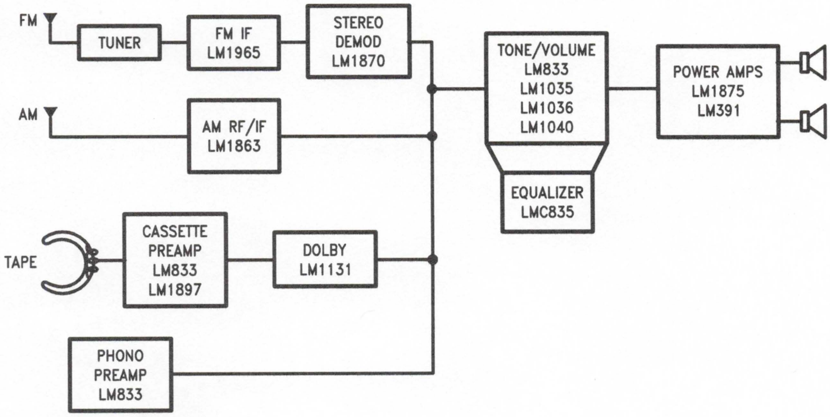
FM
STEREO
DEMOD
LM1800
AM
AM
DNR
LM1894
TONE/VOLUME
LM1035
LM1036
LM1040
POWER AMP
LM2879
TAPE
TAPE
PREAMP
LM1897
DOLBY
LM1131
PHONO
PHONO
PREAMP
LM381
LM382
LM387

TL/XX/0013–2

### Home Component Stereo (Audio Power > 10W)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FM IF
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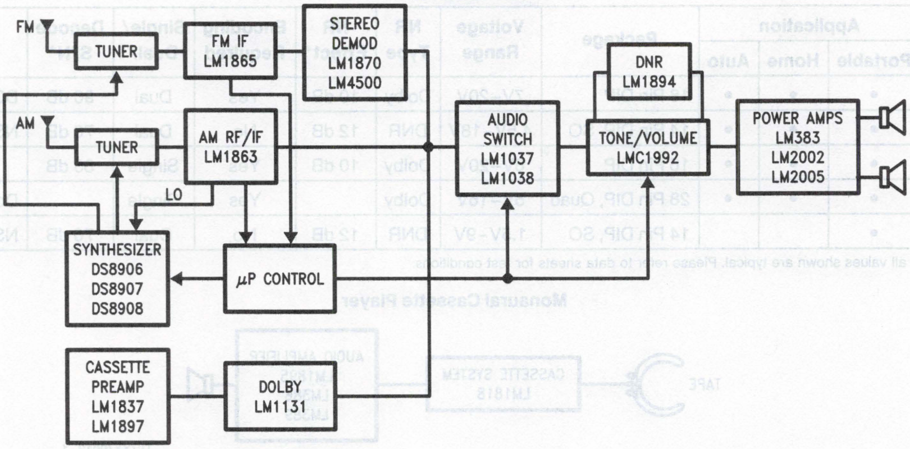
STEREO
DEMOD
LM1870
TONE/VOLUME
LM833
LM1035
LM1036
LM1040
POWER AMPS
LM1875
LM391
AM
AM RF/IF
LM1863
EQUALIZER
LMC835
TAPE
CASSETTE
PREAMP
LM833
LM1897
DOLBY
LM1131
PHONO
PREAMP
LM833

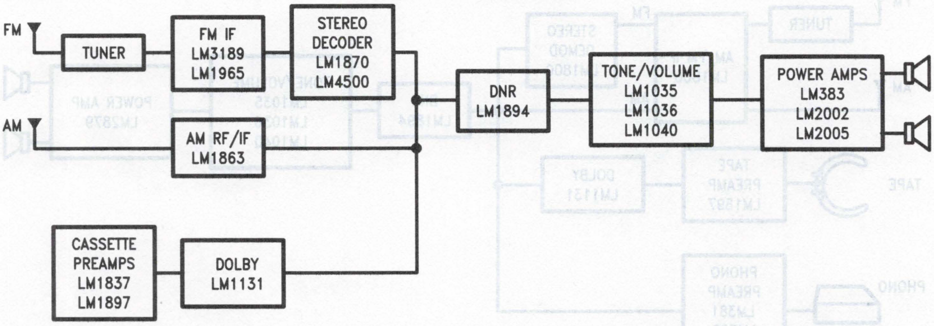
TL/XX/0013–3

## Automotive Radio (Electronically Tuned)


FM
TUNER
FM IF
LM1865
STEREO
DEMOD
LM1870
LM4500
AM
TUNER
AM RF/IF
LM1863
LO
AUDIO
SWITCH
LM1037
LM1038
DNR
LM1894
TONE/VOLUME
LMC1992
POWER AMPS
LM383
LM2002
LM2005
SYNTHESIZER
DS8906
DS8907
DS8908
µP CONTROL
CASSETTE
PREAMP
LM1837
LM1897
DOLBY
LM1131

TL/XX/0013–4

## Auto Radio (Manually Tuned)


FM
TUNER
FM IF
LM3189
LM1965
STEREO
DECODER
LM1870
LM4500
AM
AM RF/IF
LM1863
DNR
LM1894
TONE/VOLUME
LM1035
LM1036
LM1040
POWER AMPS
LM383
LM2002
LM2005
CASSETTE
PREAMPS
LM1837
LM1897
DOLBY
LM1131

TL/XX/0013–5

National Semiconductor Corporation

# Radio Circuits Definition of Terms

**AGC dc Output Shift:** The shift of the quiescent IC output voltage of the AGC section for a given change in AGC central voltage.

**AGC Figure of Merit:** The widest possible range of input signal level required to make the output signal drop by a specified amount from the specified maximum output level. Typical F.O.M. numbers are from 40 dB to 50 dB, for domestic radios and about 60 dB for automotive radios (for −10 dB output level change).

**AGC Input Current:** The current required to bias the central voltage input of the AGC section.

**AM Rejection Ratio:** The ratio of the recovered audio output produced by a desired FM signal of specified level and deviation to the recovered audio output produced by an unwanted AM signal of specified amplitude and modulating index.

**Channel Separation:** The level of output signal of an undriven amplifier with respect to the output level of an adjacent driven amplifier.

**Detection Bandwidth:** That frequency range about the free running frequency of the tone decoder/phase locked loop where a signal above a specified level will cause a detected signal condition at the output.

**Detection Bandwidth Skew:** The measure of how well the detection bandwidth is centered about the free running frequency. It is equal to the maximum detection bandwidth frequency plus the minimum detection bandwidth frequency minus twice the free running frequency.

**Hold In Range:** That range of frequencies about the free running frequency for which the phase locked loop will stay in lock if initially starting out in lock.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Input Sensitivity:** The minimum level of input signal at a specified frequency required to produce a specified signal-to-noise ratio at the recovered audio output.

**Input Voltage Range:** The range of voltages on the input terminals for which the amplifier operates within specifications.

**Large-Signal Voltage Gain:** The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**−3 dB Limiting Sensitivity:** In FM the input signal level which causes the recovered audio output level to drop 3 dB from the output level with a specified large signal input.

**Lock In Range:** That range of frequencies about the free running frequency for which the phase locked loop will come into lock if initially starting out of lock.

**Maximum Sweep Rate:** The maximum rate that the VCO may be made to vary its oscillating frequency over its Sweep Range.

**Output Resistance:** The ratio of the change in output voltage to the change in output current with the output around zero.

**Output Voltage Swing:** The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Phase Detector Sensitivity:** The change in the output voltage of the phase detector for a given change in phase between the two input signals to the phase detector.

**Power Bandwidth:** The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated a 60W with ≤0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

**Power Supply Rejection:** The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

**Supply Current:** The current required from the power supply to operate the amplifier with no load and the output at zero.

**Sweep Range:** That ratio of maximum oscillating frequency to minimum operating frequency produced by varying the central voltage of the VCO from its maximum value to its minimum value with fixed values of timing resistance and capacitance.

**VCO Sensitivity:** The change in operating frequency for a given change in VCO central voltage.

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# Radio Circuits Selection Guide

### AM RF/IF Detector

| | Portable | Home | Auto | Synthesized | Pin Count (Dip Package) | Supply Voltage | Supply Current | Input Sensitivity for 20 dB S/N Ratio | AM and FM IF | Audio Power Amplifier | Internal Detector | Meter Output |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM1863 | • | • | • | • | 20* | 7-16 | 8.3 mA | 30 $\mu$V | | | • | • |
| LM1866 | • | • | | | 20 | 3-15 | 15 mA | 25 $\mu$V | • | | • | • |
| LM1868 | • | • | | | 20 | 4.5-15 | 22 mA | 12 $\mu$V | • | • | • | |
| LM3820 | • | • | • | | 14 | 4.5-16 | 18 mA | 35 $\mu$V | | | | |

*SO Surface Mount Package Only

### Stereo Decoder

| | Portable | Home | Auto | Pin Count Dip Package | Supply Voltage | Supply Current | THD | Separation | Blend | High Cut | Lamp Driver | Output Buffer | ARI Interference Rejection |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM1800 | | • | | 16 | 10-18 | 21 mA | 0.4% | 45 dB | | | • | • | |
| LM1870 | • | • | • | 20 | 7-15 | 26 mA | 0.05% | 45 dB | • | • | • | • | |
| LM1884* | | | | 16 | 8-16 | 35 mA | 0.1% | — | | | • | • | |
| LM4500A | • | • | • | 16 | 8-16 | 35 mA | 0.1% | 40 dB | | | • | • | • |

*TV Stereo Decoder

### Radio Remote Control

| | Function | Pin Count (Dip Package) | Supply Voltage | Supply Current | Channels | | Frequency Range |
|---|---|---|---|---|---|---|---|
| | | | | | Analog | Digital | |
| LM1871 | Encoder/Transmitter | 18 | 4.5-15V | 14 mA | up to 6 | 2 | up to 72 MHz |
| LM1872 | Decoder/Receiver | 18 | 2.5-7V | 13 mA | 2 | 2 | up to 72 MHz |

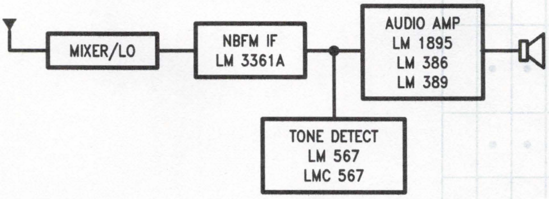
## FM IF/Detector

| | Portable | Home | Auto | Synthesized | Pin Count Dip | Pin Count S.O. | Supply Voltage | Supply Current | −3 dB Limiting Sensitivity | THD | Mute | AGC Outputs | AFC | Meter Output | AM/ FM IF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM1865 | | • | • | • | 20 | | 7.3-16 | 43 mA | 60 μV* | 0.1% | • | Reverse | • | • | |
| LM1965 | | • | • | | 20 | | 7.3-16 | 43 mA | 60 μV* | 0.1% | • | Reverse | • | • | |
| LM2065 | | • | • | • | 20 | | 7.3-16 | 43 mA | 60 μV* | 0.1% | • | Forward | • | • | |
| LM1866 | • | • | | | 20 | | 3-15 | 17 mA | 12 μV | 0.5% | • | • | • | • | • |
| LM1868 | • | • | | | 20 | | 4.5-15 | 19 mA | 15 μV | 1.1% | | | | | • |
| LM3089 | | • | • | | 16 | | 8-16 | 23 mA | 12 μV | 0.5% | • | • | • | • | |
| LM3189 | | • | • | | 16 | | 8-16 | 31 mA | 12 μV | 0.5% | • | • | • | • | |
| LM3361A† | • | | • | | 16 | 16 | 2-9 | 2.8 mA | 2 μV | - | • | | | | |

*Exclusive of 26 dB Buffer

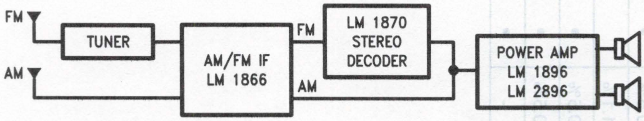
†Narrow-Band FM-IF

## Cordless Telephone Receiver


MIXER/LO
NBFM IF
LM 3361A
AUDIO AMP
LM 1895
LM 386
LM 389
TONE DETECT
LM 567
LMC 567

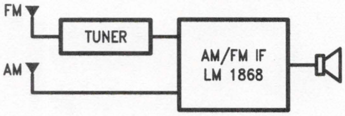
TL/XX/0011-1

## Portable Radio (Stereo)


FM
AM
TUNER
AM/FM IF
LM 1866
FM
AM
LM 1870
STEREO
DECODER
POWER AMP
LM 1896
LM 2896

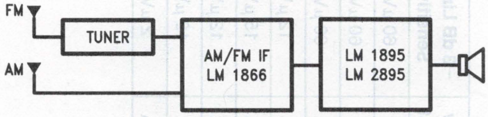
TL/XX/0011-2

## Portable Radio (Monaural)


FM
AM
TUNER
AM/FM IF
LM 1868

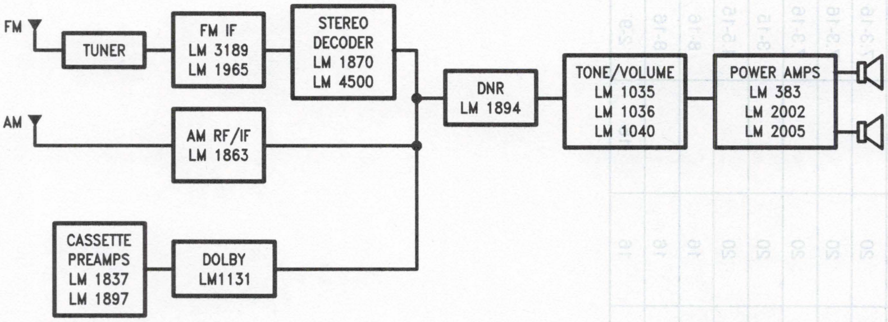
TL/XX/0011-3

## Table/Clock Radio


FM
AM
TUNER
AM/FM IF
LM 1866
LM 1895
LM 2895

TL/XX/0011-4

## Auto Radio (Manually Tuned)


FM
AM
TUNER
FM IF
LM 3189
LM 1965
STEREO
DECODER
LM 1870
LM 4500
AM RF/IF
LM 1863
CASSETTE
PREAMPS
LM 1837
LM 1897
DOLBY
LM1131
DNR
LM 1894
TONE/VOLUME
LM 1035
LM 1036
LM 1040
POWER AMPS
LM 383
LM 2002
LM 2005

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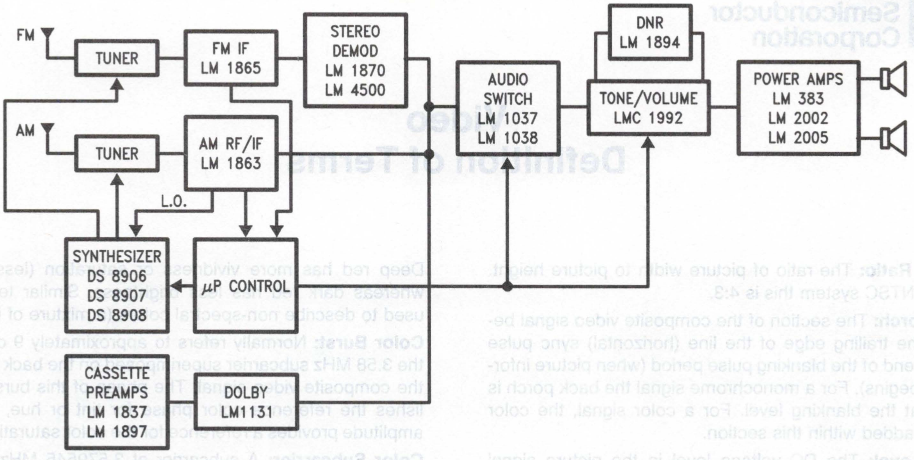
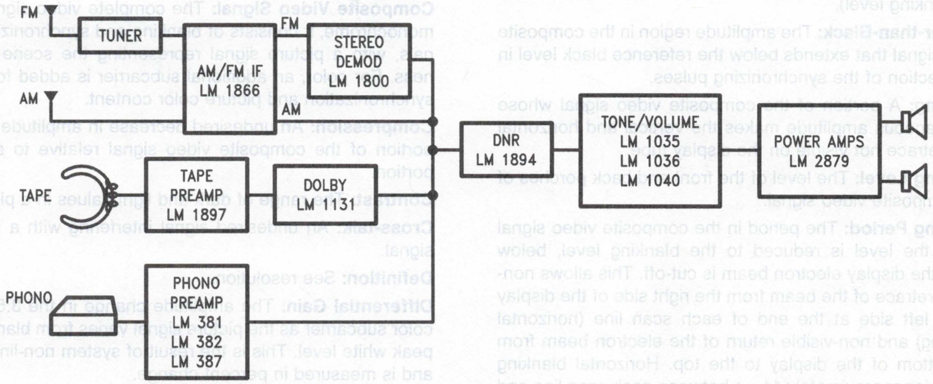
## Automotive Radio (Electronically Tuned)


FM
TUNER
FM IF
LM 1865
STEREO
DEMOD
LM 1870
LM 4500
DNR
LM 1894
AUDIO
SWITCH
LM 1037
LM 1038
TONE/VOLUME
LMC 1992
POWER AMPS
LM 383
LM 2002
LM 2005
AM
TUNER
AM RF/IF
LM 1863
L.O.
SYNTHESIZER
DS 8906
DS 8907
DS 8908
μP CONTROL
CASSETTE
PREAMPS
LM 1837
LM 1897
DOLBY
LM1131

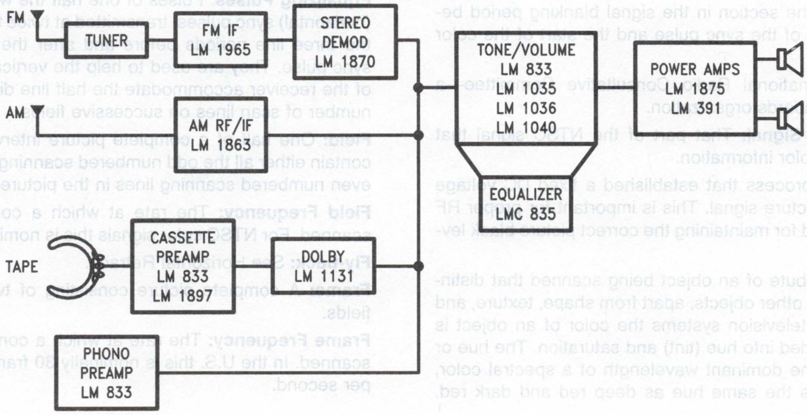
TL/XX/0011-6

## Home Stereo System (Audio Power < 10W)


FM
TUNER
FM
AM/FM IF
LM 1866
STEREO
DEMOD
LM 1800
AM
AM
DNR
LM 1894
TONE/VOLUME
LM 1035
LM 1036
LM 1040
POWER AMPS
LM 2879
TAPE
TAPE
PREAMP
LM 1897
DOLBY
LM 1131
PHONO
PHONO
PREAMP
LM 381
LM 382
LM 387

TL/XX/0011-7

## Home Component Stereo (Audio Power > 10W)


FM
TUNER
FM IF
LM 1965
STEREO
DEMOD
LM 1870
AM
AM RF/IF
LM 1863
TONE/VOLUME
LM 833
LM 1035
LM 1036
LM 1040
POWER AMPS
LM 1875
LM 391
EQUALIZER
LMC 835
TAPE
CASSETTE
PREAMP
LM 833
LM 1897
DOLBY
LM 1131
PHONO
PREAMP
LM 833

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# Video Definition of Terms

**Aspect Ratio:** The ratio of picture width to picture height. For the NTSC system this is 4:3.

**Back Porch:** The section of the composite video signal between the trailing edge of the line (horizontal) sync pulse and the end of the blanking pulse period (when picture information begins). For a monochrome signal the back porch is simply at the blanking level. For a color signal, the color burst is added within this section.

**Black Level:** The DC voltage level in the picture signal which corresponds to beam cut-off on the display tube. It can be at the blanking level (given by the back porch) or slightly higher (7.5% to 10% of the peak white signal above the blanking level).

**Blacker-than-Black:** The amplitude region in the composite video signal that extends below the reference black level in the direction of the synchronizing pulses.

**Blanking:** A portion of the composite video signal whose instantaneous amplitude makes the vertical and horizontal scan retrace not visible on the display tube.

**Blanking Level:** The level of the front and back porches of the composite video signal.

**Blanking Period:** The period in the composite video signal where the level is reduced to the blanking level, below which the display electron beam is cut-off. This allows non-visible retrace of the beam from the right side of the display to the left side at the end of each scan line (horizontal blanking) and non-visible return of the electron beam from the bottom of the display to the top. Horizontal blanking occurs for approximately 11 $\mu$s between each scan line and vertical blanking for 1.2 ms between each field.

**Blooming:** Defocussing of the picture in regions where the brightness is too high.

**Breezeway:** The section in the signal blanking period between the end of the sync pulse and the start of the color burst.

**C.C.I.R.:** International Radio Consultative Committee—a worldwide standards organization.

**Chrominance Signal:** That part of the NTSC signal that contains the color information.

**Clamping:** A process that established a fixed DC voltage level for the picture signal. This is important for proper RF modulation and for maintaining the correct picture black level.

**Color:** An attribute of an object being scanned that distinguishes it from other objects, apart from shape, texture, and brightness. In television systems the color of an object is further subdivided into hue (tint) and saturation. The hue or tint refers to the dominant wavelength of a spectral color, i.e., light red is the same hue as deep red and dark red. Deep red has more vividness or saturation (less white), whereas dark red has less brightness. Similar terms are used to describe non-spectral colors (a mixture of hues).

**Color Burst:** Normally refers to approximately 9 cycles of the 3.58 MHz subcarrier superimposed on the back porch of the composite video signal. The phase of this burst establishes the reference color phase for tint or hue, and the amplitude provides a reference for the color saturation level.

**Color Subcarrier:** A subcarrier at 3.579545 MHz (NTSC) whose modulation sidebands are added to a monochrome video signal to convey the color information. Similar subcarriers are used for SECAM and PAL.

**Composite Video Signal:** The complete video signal. For monochrome, it consists of blanking and synchronizing signals, with a picture signal representing the scene brightness. For color, an additional subcarrier is added for color synchronization and picture color content.

**Compression:** An undesired decrease in amplitude of one portion of the composite video signal relative to another portion.

**Contrast:** The range of dark and light values in a picture.

**Cross-talk:** An undesired signal interfering with a desired signal.

**Definition:** See resolution.

**Differential Gain:** The amplitude change in the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level. This is the result of system non-linearities and is measured in percent change.

**Differential Phase:** The phase change, measured in degrees, of the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level.

**Equalizing Pulses:** Pulses of one half the width of the line (horizontal) sync pulses, transmitted at twice the line rate for the three line periods before and after the field (vertical) sync pulse. They are used to help the vertical sync system of the receiver accommodate the half line difference in the number of scan lines on successive fields.

**Field:** One half of a complete picture interval. A field will contain either all the odd numbered scanning lines or all the even numbered scanning lines in the picture.

**Field Frequency:** The rate at which a complete field is scanned. For NTSC color signals this is nominally 59.94 Hz.

**Fly-back:** See Horizontal Retrace.

**Frame:** A complete picture consisting of two interlocking fields.

**Frame Frequency:** The rate at which a complete frame is scanned. In the U.S. this is nominally 30 frames or pictures per second.

**Front Porch:** The section of the composite video signal between the end of the picture information on a scan line (start of blanking) and the start of the line synchronization pulse.

**Horizontal Blanking:** The blanking signal at the end of each scan line that prevents the retrace of the display tube electron beam from being visible.

**Horizontal Retrace:** The rapid return of the scanning electron beam from the right side of the raster to the left side.

**Horizontal Hum Bars:** Relatively broad horizontal bars drifting slowly up the screen as a result of interference from the 60 Hz main frequency.

**Hue (Tint):** Describes the color that is being represented on the screen, i.e., red, blue, magenta, green, orange, etc.

**Interlace:** A scanning process in which each adjacent line belongs to the alternate field.

**I.R.E.:** Institute of Radio Engineers. Now combined with the AIEE to form the IEEE.

**I.R.E. Scale:** An oscilloscope scale calibrated for composite video and divided vertically into 140 units. The picture signal occupies the range from 0 to 100 with syncs in the range 0 to −40.

**Luminance:** The monochrome or brightness part of the color signal, composed of specific proportions of the three primary colors, red, blue, and green.

**N.T.S.C.:** National Television System Committee, used in reference to the system adopted for color television broadcasting in the U.S. at the end of 1953.

**Noise:** In a television picture, 'noise' refers to random interference producing a salt and pepper pattern over the picture. Heavy noise totally obscuring the picture is called "snow".

**Overshoot:** An (excessive) response to a unidirectional signal change. Overshoot is often used deliberately to enhance the luminance portion of a signal.

**Pairing:** A partial or complete failure of interlace in which scan lines of alternate fields fall in pairs, one on top of the other.

**Pedestal Level:** See Blanking Level.

**Percentage Sync:**

**Video:** The ratio in percent of the amplitude of the synchronizing pulse to the peak amplitude of the picture signal between blanking and reference white level. For a properly constituted composite video signal this is 40%.

**RF:** The ratio is a percent of the amplitude of the synchronizing pulse to the peak amplitude of the modulated RF signal. For correct modulation this is 25%.

**P.A.L.:** Phase Alternation Line. A variation of the NTSC system involving phase reversal of one of the color difference signals on a line by line basis, introduced into the U.K. and Germany in 1967.

**Picture Signal:** That portion of the composite video signal which is above the blanking level and contains the picture information.

**Pre-emphasis:** An increase in the level of a band of frequency components with respect to the remainder of the signal. For U.S. television, the audio signal is increased at a 6 db/octave rate above 2.1 kHz.

**Raster:** The area on the face of the display tube that is scanned by the electron beam. This is not always entirely visible since commercial receivers employ overscan so that the edges of the raster are hidden by the faceplate.

**Reference Signals:** See V.I.T.S. and V.I.R.S.

**Resolution (Horizontal):** The amount of resolvable detail in the horizontal direction of the picture. This depends on the high frequency and phase response of the transmission system and the receiver.

**Resolution (Vertical):** The amount of resolvable detail in the vertical direction of the picture. This depends primarily on the number of scan lines that are used and secondarily on the size (shape) of the electron scanning beam.

**Saturation (Color):** The amplitude of the chrominance signal. Increased saturation means increased chrominance signal level. Visibly, this refers to a color increasing from pale or pastel to deep.

**S.E.C.A.M.:** Sequential Couleur Avec Memoire. The color broadcasting system used predominantly in France which utilizes sequential transmission of the color difference signals, which are FM modulated on two separate subcarriers (1967).

**Setup:** The difference in level between the blanking level and the reference black level expressed as a percent of the reference white level.

**Smear:** Smear describes a picture condition where objects appear extended in the horizontal direction producing an ill-defined, blurry picture. This often occurs when the receiver is tuned slightly above the proper pix carrier frequency.

**Sync:** Abbreviation for synchronizing or synchronization.

**Sync Level:** The level of the synchronizing pulse tips.

**Vertical Blanking:** The blanking signal at the end of each field starting three lines before the vertical sync pulse.

**Vertical Retrace:** The return of the electron beam from the bottom of the display to the top after a complete field has been scanned.

**V.I.R.S.:** Vertical Interval Reference Signal. A quality control signal added to a horizontal scan line during the vertical blanking period. It is used to provide a chrominance, luminance and black level reference.

**V.I.T.S.:** Vertical Interval Test Signals. A series of test signals that are added to horizontal lines during the vertical blanking for in-service testing of the transmission equipment. They can be deleted or added at various points in the transmission link, unlike the VIRS, which is added at program origination and stays with the program material.

**Vestigal Sideband Transmission:** A broadcast transmission technique wherein only one side band of an amplitude modulated carrier is fully transmitted with the other sideband (usually lower) truncated.

**Video:** The visible portion of the transmitted signal representing the picture.

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# Video Selection Guide

## VIDEO AMPLIFIERS

| | Bandwidth | Gain | Package | Supply Voltage | Comments |
|---|---|---|---|---|---|
| LM592 | 120 MHz | 100, 400 | 14 Pin DIP<br>14 PIN SO | ±3V–±6V | Differential IN, Differential OUT |
| LM733 | 120 MHz | 10, 100, 400 | 14 Pin DIP | ±3V–±6V | Differential IN, Differential OUT |
| LM1201<br>(Advanced Information) | 100 MHz | 4–10 | 16 Pin DIP | +12V | Single Amplifier with Black Level and Contrast Control |
| LM1203 | 50 MHz | 4–10 | 28 Pin DIP | +12V | Triple Amplifier System with Black Level and Contrast Control |
| LM359<br>(Note 1) | 400 MHz GBW<br>30 MHz @ $A_V = 1$ | | 14 Pin DIP | 5V–22V | Dual Norton Amplifiers |

## VIDEO TIMING

| | Function | Package | Supply Voltage | Comments |
|---|---|---|---|---|
| LM1391 | PLL | 8 Pin DIP | Internal Shunt Zener | — |
| LM1880 | No-Holds Vert/Horiz | 14 Pin DIP | Internal Shunt Zener | |
| LM1881 | Sync Separator | 8 Pin DIP<br>8 Pin SO | 5V–15V | Outputs Provided:<br>Composite Sync<br>Vertical<br>Burst Gate<br>Odd/Even Field |

## VIDEO MODULATORS/DEMODULATORS

| | Function | Package | Comments |
|---|---|---|---|
| LM1496<br>(Note 2) | Balanced Modulator-Demodulator (Modulator—Suppressed Carrier, AM Demodulator—Synchronous, FM Phase Detection) | 14 Pin DIP<br>10 Pin TO-5<br>14 Pin SO | Operating Frequency to 100 MHz<br>Balanced Inputs and Outputs |
| LM1889 | Modulates Color Difference, Luminance, Audio onto Low-VHF Channels | 18 Pin DIP | DC Channel Switching<br>Chroma Reference |
| LM2889 | Modulates Composite Video, Audio onto Low-VHF Channels | 14 Pin DIP | DC Channel Switching, Low Distortion FM Sound Modulator, Video Clamp |

**Note 1:** Data sheet in Linear 1.

**Note 2:** Data sheet in Linear 3—Special Functions Chapter 5.

**VIDEO IFs**

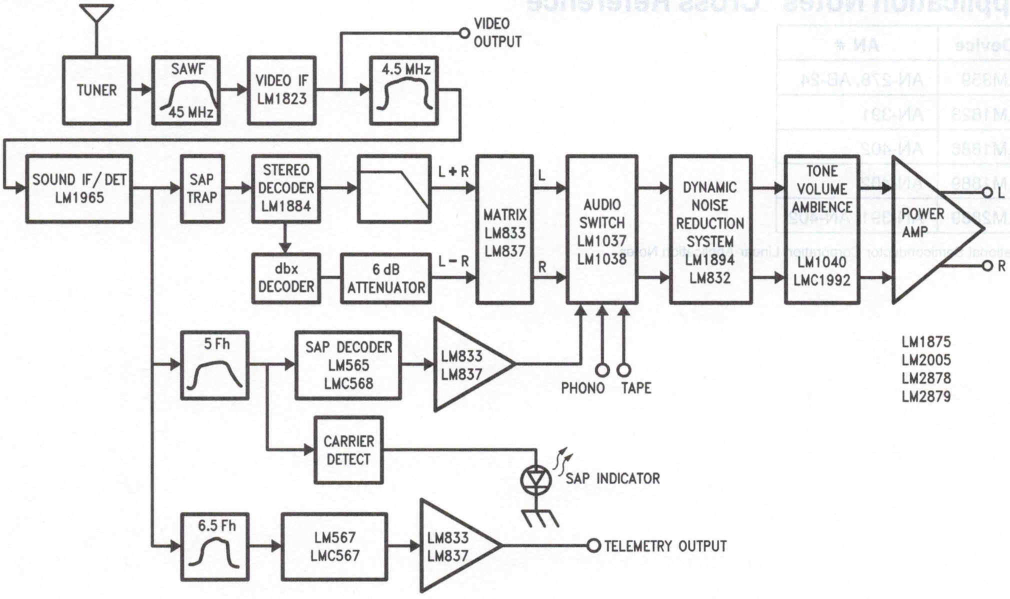
| | Application | Package | Comments |
|---|---|---|---|
| LM1211<br>(Note 3) | Broadband Demodulator | 20 Pin DIP | Operating Range 20 MHz–80 MHz<br>Quasi-Synchronous Detector<br>25 MHz Output Amplifier |
| LM1823 | Video IF | 28 Pin DIP | Operating Range 20 MHz–70 MHz<br>Synchronous Detector using PLL<br>9 MHz Output Amplifier |

**OTHER VIDEO PRODUCTS**

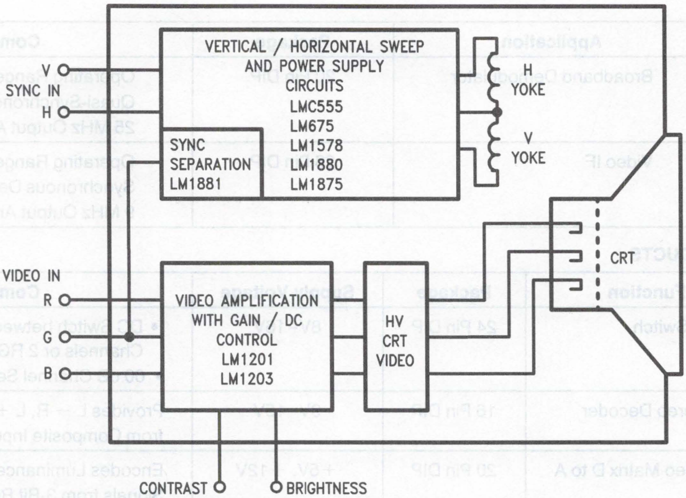
| | Function | Package | Supply Voltage | Comments |
|---|---|---|---|---|
| LM1044 | Video Switch | 24 Pin DIP | 8V–16V | • DC Switch between 3 Composite Video Channels or 2 RGB Channels<br>• 60 dB Channel Separation |
| LM1884<br>(Note 4) | TV Stereo Decoder | 16 Pin DIP | 9V–15V | Provides L − R, L + R Outputs from Composite Input |
| LM1886 | TV Video Matrix D to A | 20 Pin DIP | +5V, +12V | Encodes Luminance and Color Difference Signals from 3-Bit RGB Inputs |

**Note 3:** Data Sheet in Linear 3.

**Note 4:** Data Sheet in Linear 3.


VIDEO OUTPUT
TUNER
SAWF
45 MHz
VIDEO IF
LM1823
4.5 MHz
SOUND IF/DET
LM1965
SAP TRAP
STEREO DECODER
LM1884
L + R
L − R
dbx DECODER
6 dB ATTENUATOR
MATRIX
LM833
LM837
L
R
AUDIO SWITCH
LM1037
LM1038
DYNAMIC NOISE REDUCTION SYSTEM
LM1894
LM832
TONE VOLUME AMBIENCE
LM1040
LMC1992
POWER AMP
L
R
LM1875
LM2005
LM2878
LM2879
5 Fh
SAP DECODER
LM565
LMC568
LM833
LM837
PHONO
TAPE
CARRIER DETECT
SAP INDICATOR
6.5 Fh
LM567
LMC567
LM833
LM837
TELEMETRY OUTPUT

TL/XX/0012-1


V
SYNC IN
H
VERTICAL / HORIZONTAL SWEEP AND POWER SUPPLY CIRCUITS
LMC555
LM675
LM1578
LM1880
LM1875
SYNC SEPARATION
LM1881
H YOKE
V YOKE
CRT
VIDEO IN
R
G
B
VIDEO AMPLIFICATION WITH GAIN / DC CONTROL
LM1201
LM1203
HV CRT VIDEO
CONTRAST
BRIGHTNESS

TL/XX/0012-2

**FIGURE 1. Typical RGB Color Monitor Block Diagram**

## Application Notes* Cross Reference

| Device | AN # |
|---|---|
| LM359 | AN-278, AB-24 |
| LM1823 | AN-391 |
| LM1886 | AN-402 |
| LM1889 | AN-402 |
| LM2889 | AN-391, AN-402 |

*National Semiconductor Corporation Linear Application Notes

**National Semiconductor Corporation**

# Motion Control Selection Guide

## Dedicated Motor Control Functions

| Part Number | Function | Features |
|---|---|---|
| LM621 | Brushless D.C. Motor | Deadband Timer for Direction Reversal<br>40V Max. Operation<br>35 mA Outputs for Direct Drive of Bipolar Power Transistors |
| LM628 | High Performance Position Control for D.C. and Brushless D.C. Motors | On Board 32-Bit Incremental Shaft Encoder Interface<br>256 μs Loop Time<br>Automatic Trajectory Generator<br>Velocity Programmable "On-the-Fly"<br>Internal Programmable PID Filter<br>Convenient 8-Bit Host Interface<br>8-Bit or 12-Bit Port to DAC (LM628)<br>8-Bit PWM Output (LM629) |
| LM622 | P.W.M. Controller for Brushless and Brush D.C. Motors | Flexible Output Structure Drives H-Switches or Commutators<br>Precision On-Board Reference<br>Flexible Error Amp/Feedback Structure |

## H-Switches

| Output Current (Amps) | | Device | Supply Voltage (Max) | Full Current Saturation Voltage | | Operating Temp. Range | Package | Description |
|---|---|---|---|---|---|---|---|---|
| Peak (Typical) | Continuous (Max) | | | Source (Max) | Sink (Max) | | | |
| 4 | 2 | LM18298 | 50 | 2.8 | 2.6 | −40°C to +150°C | 15-Pin TO-220 | Quad ½ H Switch |
| 1.5 | 1 | LM18293 | 36 | 1.8 | 1.8 | −40°C to +125°C | 16-Pin DIP | Dual Full H Switch |

## Power Op-Amps*

| Output Current Amps | | Device | Supply Voltage (Max) | Input Offset Voltage (Max) | Quiescent Current | Slew Rate (Typical) | Operating Temp. Range | Package | Features |
|---|---|---|---|---|---|---|---|---|---|
| Peak (Typical) | Continous (Max) | | | | | | | | |
| 3 | 1.5 | LM675 | 60 | 10 mV | 50 mA | 8 V/μs | 0°C to +70°C | 5-Pin TO-220 | Thermal Parole |
| 15 | 10 | LM12L | 60 | 15 mV | 80 mA | 9 V/μs | −55°C to +125°C | 4-Pin TO-3 | Fully Protected |
| 15 | 10 | LM12CL | 60 | 20 mV | 120 mA | 9 V/μs | 0°C to +70°C | 4-Pin TO-3 | Fully Protected |
| 15 | 10 | LM12 | 80 | 15 mV | 80 mA | 9 V/μs | −55°C to +125°C | 4-Pin TO-3 | Fully Protected |
| 15 | 10 | LM12C | 80 | 20 mV | 120 mA | 9 V/μs | 0°C to +70°C | 4-Pin TO-3 | Fully Protected |
| 1 | 0.5 | LM18272 | 28 | 100 mV | 15 mA (Typ) | 0.5 V/μs | 0°C to +85°C | 8-Pin DIP | Dual (Bridge) |

*For more information on Power Amps, see the Amplifier section of the Linear Databook. For more High Power Amplifiers, refer to the Audio Amplifier section.

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# Building Blocks

## Communications-Related Building Blocks

### Modulators & Demodulators Selection Guide

| | LM1211 | LM1496 | LM1889 | LM2889 |
|---|---|---|---|---|
| Typical Application | Broadband Demodulator | Balanced Modulator-Demodulator | TV Video Modulator | TV Video Modulator |
| Key Features | • Configurable for AM or FM Based Signals<br>• 0 MHz–70 MHz Operating Frequency Range<br>• 25 MHz Detector Output Bandwidth<br>• Linear Output Phase Response | • Wide Frequency Response to 100 MHz<br>• Fully Balanced Inputs and Outputs<br>• Adjustable Gain and Signal Handling | • Input Signals<br>—Audio Modulation<br>—Color Difference<br>—Luminance<br>• Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output<br>• Companion Circuit to LM1886 TV Video Matrix D to A | • Input Signals<br>—Audio<br>—Composite Video<br>• Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output<br>• Video DC Restoration |

**PLL's AND TONE DECODERS**

General purpose PLL's and tone decoders are available for applications that include FSK demodulation, tone decoding, SAP and SCA demodulation, and telemetry reception. Both bipolar and CMOS devices are offered. Special purpose PLL's for TV synchronization and FM stereo demodulation are also available for use in other low frequency signal processing applications.

### PLL and Tone Decoder Selection Guide

| | LM565 | LM567 | LMC567* (CMOS LM567) | LMC568 | LM1391 | LM1800, LM1870, LM4500A |
|---|---|---|---|---|---|---|
| Typical Application | PLL | Tone Decoder | Tone Decoder | PLL | TV—Horizontal PLL | FM Stereo Demodulator PLL |
| Center Frequency Range | 15 Hz–500 kHz | 0.01 Hz–500 kHz | 0.01 Hz–500 kHz | 0.01 Hz–500 kHz | | |
| VCO Control Range | ±30% | ±7% | ±7% | ±30% | ±300 Hz | |
| Supply Voltage | ±5V to ±12V | 4.75V–9V | 2V–9V | 2V–9V | 8V–9.2V | Lowest: 7V<br>Highest: 16V<br>(See Datasheets) |
| Supply Current (Typ) | 8 mA | 12 mA | 0.8 mA | 1.2 mA | 20 mA | Lowest: 21 mA<br>Highest: 45 mA<br>(See Datasheet) |

*The CMOS LMC567 oscillator runs at twice the frequency of the bipolar LM567 oscillator. Refer to the datasheets for additional information.

**POWER LINE CARRIER**

The LM2893/LM1893 Carrier-Current Transceiver performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. Applications include energy management systems, inter-office control, fire alarm systems, security systems, telemetry, and remote meter reading.

**TIMERS**

General purpose timers are available for generating accurate time delays or oscillation. Both bipolar and CMOS devices are offered.

**Timer Selection Guide**

| | LM322 | LM2905 | LM555 | LMC555* (CMOS LM555) | LM556 (Dual LM555) |
|---|---|---|---|---|---|
| Trigger Pulse Relative to Output Pulse | Can Be Longer | Can Be Longer | Must Be Shorter | Must Be Shorter | Must Be Shorter |
| Typical Application | Monostable | Monostable | Astable | Astable | Astable |
| Supply Voltage | 4.5V–40V | 4.5V–40V | 4.5V–15V | 1.2V–12V | 4.5V–15V |
| Supply Current (Typical) | 2.5 mA | 2.5 mA | 10 mA | 0.15 mA | 10 mA (Each Timer Section) |

*The CMOS LMC555 can handle −10 mA to +50 mA of output current and the bipolar LM555 can handle up to ±200 mA of output current.

**VCO AND FUNCTION GENERATOR**

The LM566 is a general purpose voltage controlled oscillator which may be used to generate square and triangle waves. Typical applications include FM modulation, signal generation, function generation, frequency shift keying, and tone generation. The LM566 has very linear modulation characteristics.

## Drive-Related Building Blocks

**DISPLAY DRIVERS**

LED flasher/oscillator and dot/bar display drivers are offered.

**Display Driver Selection Guide**

| | LM3909 | LM3914 | LM3915 | LM3916 |
|---|---|---|---|---|
| Typical Application | Flasher/ Oscillator | Dot/Bar Display Driver | Dot/Bar Display Driver | Dot/Bar Display Driver |
| Display Scale | N/A | Linear | Log | VU Meter |
| Display Type | LED, Incandescent | LED, LCD, Vacuum Fluorescent | LED, LCD, Vacuum Fluorescent | LED, LCD, Vacuum Fluorescent |

**METER DRIVERS**

The LM1819 Air-Core Meter Driver is a function generator/driver for air-core (moving-magnet) meter movements in tachometers and ruggedized instruments. Driver outputs are self-centering and better than 2% linearity is guaranteed over a full 305° deflection range. Signal conditioning circuitry is included on chip.

**TEMPERATURE CONTROLLER**

The LM3911 (Note 1) is a temperature controller containing a precision temperature sensor, op amp, and reference. It is designed for temperature sensing and closed loop temperature control applications over the −25°C to +85°C range.

**Note 1:** See Linear 2 for datasheet.

# Precision-Related Building Blocks

## CHOPPER BLOCK

The LMC669 Auto Zero Block (Note 1) is a universal commutating auto-zero block that can be used with any operational amplifier to correct offset voltage.

**Note 1:** See Linear 2 for datasheet.

## TRANSISTOR ARRAYS

A variety of matched and power transistors are offered.

**Transistor Array Selection Guide**

| | LM394 | LM395 | LM3046 | LM3146 |
|---|---|---|---|---|
| Description | NPN Transistor Pair | Power Transistor | 5 NPN Transistors | 5 NPN Transistors |
| Key Features | • Emitter-Base Voltage Matched to 50 μV<br>• Current Gain Matched to 2% | • Collector Current: 1A<br>• Quiescent Current: 10 mA<br>• Switching Time: 2 μs<br>• Current Limit<br>• Thermal Limit<br>• Safe Area Protection | • Emitter-Base Voltage Matched to ±5 mV<br>• Breakdown Voltages<br>—$V_{(BR)(CBO)}$: 20V<br>—$V_{(BR)(CEO)}$: 15V<br>—$V_{(BR)(CIO)}$: 20V<br>—$V_{(BR)(EBO)}$: 5V<br>• DC—120 MHz | • Emitter-Base Voltage Matched to ±5 mV<br>• Breakdown Voltages<br>—$V_{(BR)(CBO)}$: 40V<br>—$V_{(BR)(CEO)}$: 30V<br>—$V_{(BR)(CIO)}$: 40V<br>—$V_{(BR)(EBO)}$: 5V<br>• DC—120 MHz |

# Sensing-Related Building Blocks

## LIQUID LEVEL SENSORS

A variety of liquid level sensing circuits are offered.

**Liquid Level Sensor Selection Guide**

| | LM903 | LM1042 | LM1812 | LM1830 |
|---|---|---|---|---|
| Output Type | Digital HI/LO | Analog | Pulse-Echo Timing | Digital HI/LO |
| Operation Method | Thermoresistive Probe | Thermoresistive Probe | Acoustic Transducer | Conductive Liquid |

## SPECIAL AMPLIFIERS

A variety of special sensor amplifiers are offered.

**Special Amplifiers Selection Guide**

| | LM1815 | LM1964 |
|---|---|---|
| Typical Application | Adaptive Sense Amplifier | Sensor Interface Amplifier |
| Sensor | Inductive Pickup | Lambda Sensor |
| Key Features | • Operates from 2.5V to 12V Supply<br>• Adaptive Hysteresis<br>• True Zero Crossing Timing Reference | • Normal Operation Guaranteed with Inputs up to 3V Below Ground on a Single Supply<br>• Fully Protected Inputs<br>• Input Open Circuit Detection |

## SPECIAL COMPARATOR

The LM1801 Battery Operated Power Comparator is an extremely low power comparator with a high current, open collector output stage. Typical applications include intrusion alarms, water leak detectors, gas leak detectors, overvoltage crowbars and battery operated monitors. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery.

## SPECIAL CONVERTERS

A variety of special converters for signal transformation applications are offered.

**Special Converters Selection Guide**

| | LH0091 (Note 1) | LH0094 (Note 1) | LM331 (Note 1) | LM2907, LM2917 |
|---|---|---|---|---|
| Converter Type | True RMS-to-DC | Multifunction | Voltage-to-Frequency | Frequency-to-Voltage |
| Key Features | • 0.1% Accuracy with External Trim<br>• Uncommitted Amplifier for Filtering, Gain or High Crest Factor Configuration<br>• True RMS Conversion | • $OUT = IN_Y \left(\frac{IN_Z}{IN_X}\right)^m$, $0.1 \leq m \leq 10$, m Continuously Adjustable<br>• Applications<br>—Precision Divider, Multiplier<br>—Square Root<br>—Square<br>—Trigonometric Function Generator<br>—Companding<br>—Linearization<br>—Control Systems<br>—Log Amp | • 1 Hz to 100 kHz Frequency Range<br>• Split or Single Supply Operation | • Operates Relay, Lamp or Other Load when Input Exceeds a Selected Rate<br>• Ground Referenced Tachometer Fully Protected from Damage Due to Swings Above Supply or Below Ground |

**Note 1:** See Linear 2 for datasheets.

## ULTRASONIC TRANSCEIVER

The LM1812 Ultrasonic Transceiver is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. Typical uses include liquid level measurement, sonar, surface profiling, data links, hydro-acoustic communications, non-contact sensing and industrial process control. Depending on the acoustic transducer, typical performance capabilities include 5 feet to 100 feet in water and 4 inches to 35 feet in air.

# Section 1
# Voltage Regulators

## Section 1 Contents

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***Devices Not Covered In Last Publication**

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# Voltage Regulators
# Definition of Terms

**Current-Limit Sense Voltage:** The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

**Feedback Sense Voltage:** The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

**Input Voltage Range:** The range of dc input voltages over which the regulator will operate within specifications.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

**Maximum Power Dissipation:** The maximum total device dissipation for which the regulator will operate within specifications.

**Output-Input Voltage Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

**Output Noise Voltage:** The RMS ac voltage at the output with constant load and no inut ripple, measured over a specified frequency range.

**Output Voltage Range:** The range of regulated output voltages over which the specifications apply.

**Output Voltage Scale Factor:** The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

**Quiescent Current:** That par of input current to the regulator that is not delivered to the load.

**Ripply Rejection:** The line regulation for ac inupt signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

**Standby Current Drain:** That part of the operating current of the regulator which does not contribute to the load current. (See Quiescent Current)

**Temperature Stability:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

**Thermal Regulation:** Percentage change in output voltage for a given change in power dissipation over a specified time period.

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# Voltage Regulators Selection Guide

### Adjustable Positive Voltage Regulators

| Amps | Device | Output Voltage | Package |
|---|---|---|---|
| 10.0 | LM196K | 1.25V–15V | TO-3 |
| | LM396K | 1.25V–15V | TO-3 |
| 5.0 | LM138K | 1.2V–32V | TO-3 |
| | LM338K | 1.2V–32V | TO-3 |
| 3.0 | LM150K | 1.2V–33V | TO-3 |
| | LM350K, T | 1.2V–33V | TO-3, TO-220 |
| 1.5 | LM117K | 1.2V–37V | TO-3 |
| | LM117HVK | 1.2V–57V | TO-3 |
| | LM2941CT | 5.0V–24V | TO-220 |
| | LM317K, T | 1.2V–37V | TO-3, TO-220 |
| | LM317HVK | 1.2V–57V | TO-3 |
| 0.5 | LM117H | 1.2V–37V | TO-39 |
| | LM117HVH | 1.2V–57V | TO-39 |
| | LM317H | 1.2V–57V | TO-39 |
| | LM317HVH | 1.2V–37V | TO-39 |
| | LM317MP | 1.2V–37V | TO-202 |
| 0.1 | LM317LZ, M | 1.2V–37V | TO-92, SO-8 |
| | LM2931CT | 3.0V–24V | TO-220, 5-LEAD |
| | LP2951CN, J, H, M | 1.24V–29V | DIP, CERDIP, HEADER, SO-8 |

### Adjustable Negative Voltage Regulators

| Amps | Device | Output Voltage | Package |
|---|---|---|---|
| 3.0 | LM133K | −1.2V – −32V | TO-3 |
| | LM333K, T | −1.2V – −32V | TO-3, TO-220 |
| 1.5 | LM137K | −1.2V – −37V | TO-3 |
| | LM137HVK | −1.2V – −47V | TO-3 |
| | LM337K, T | −1.2V – −37V | TO-3, TO-220 |
| | LM337HVK | −1.2V – −47V | TO-3 |
| 0.5 | LM137H | −1.2V – −37V | TO-39 |
| | LM137HVH | −1.2V – −47V | TO-39 |
| | LM337H | −1.2V – −37V | TO-39 |
| | LM337HVH | −1.2V – −47V | TO-39 |
| | LM337MP | −1.2V – −37V | TO-202 |
| 0.1 | LM337LZ, M | −1.2V – −37V | TO-92, SO-8 |

## Fixed Positive Voltage Regulators

| Amps | Device | Output Voltage | Package |
|---|---|---|---|
| 3.0 | LM123K | 5V | TO-3 |
| | LM2943CT* | 5V | TO-220 |
| | LM323K | 5V | TO-3 |
| 1.0 | LM109K | 5V | TO-3 |
| | LM140AK | 5V, 12V, 15V | TO-3 |
| | LM140K | 5V, 12V, 15V | TO-3 |
| | LM2940CT | 5V, 12V, 15V | TO-220 |
| | LM309K | 5V | TO-3 |
| | LM340AK, T | 5V, 12V, 15V | TO-3, TO-220 |
| | LM340K, T | 5V, 12V, 15V | TO-3, TO-220 |
| | LM78xxCK, T | 5V, 12V, 15V | TO-3, TO-220 |
| 0.5 | LM2984CT | 5V, 12V, 15V | TO-220, TO-202 |
| | LM341T, P | 5V, 12V, 15V | TO-220, TO-202 |
| | LM78MxxCT | 5V, 12V, 15V | TO-220 |
| 0.2 | LM109H | 5V | TO-39 |
| | LM309H | 5V | TO-39 |
| | LM342P | 5V, 12V, 15V | TO-202 |
| 0.15 | LM2930T | 5V, 8V | TO-220 |
| 0.1 | LM140LAH | 5V, 12V, 15V | TO-39 |
| | LM2931Z, T | 5V | TO-92, TO-220 |
| | LM340LZ, H | 5V, 12V, 15V | TO-92, TO-39 |
| | LM78LxxACZ, H, M | 5V, 12V, 15V | TO-92, TO-39, SO-8 |
| | LP2950CZ | 5V | TO-92 |

*Future Product

## Fixed Negative Voltage Regulators

| Amps | Device | Output Voltage | Package |
|---|---|---|---|
| 3.0 | LM145K | −5V, −5.2V | TO-3 |
| | LM345K | −5V, −5.2V | TO-3 |
| 1.5 | LM120K | −5V, −12V, −15V | TO-3 |
| | LM320K, T | −5V, −12V, −15V | TO-3, TO-220 |
| | LM79xxCT, K | −5V, −12V, −15V | TO-3, TO-220 |
| 0.5 | LM320MP | −5V, −12V, −15V | TO-220 |
| | LM79MxxCP, K | −5V, −12V, −15V | TO-202, TO-3 |
| 0.2 | LM120H | −5V, −12V, −15V | TO-39 |
| | LM320H | −5V, −12V, −15V | TO-39 |
| 0.1 | LM320LZ | −5V, −12V, −15V | TO-92 |
| | LM79LxxACZ, M | −5V, −12V, −15V | TO-92, SO-8 |

*The LM320 has better electrical characteristics than the LM79xx.

| | |
|---|---|
| LM100 Series | +55°C to +150°C |
| LM300 Series | 0°C to +125°C |

## Low Dropout Regulators

| Amps | Device | Output Voltage | Package |
|---|---|---|---|
| 0.100 | LM2931T, Z | 5V, ADJ | TO-220, TO-92 |
| | LP2950CZ | 5V | TO-92 |
| | LP2951N, J, H | ADJ | DIP, CERDIP, HEADER |
| 0.150 | LM2930T | 5V, 8V | TO-220 |
| 0.500 | LM2984CT | TRIPLE 5V + WATCHDOG | TO-220, 11-LEAD |
| 0.750 | LM2925T | 5V WITH DELAYED RESET | TO-220, 5-LEAD |
| | LM2935T | DUAL 5V | TO-220, 5-LEAD |
| 1.5 | LM2940CT | 5V, 12V, 15V | TO-220 |
| | LM2941CT* | ADJ | TO-220, 5-LEAD |
| 3.0 | LM2943CT* | 5V | TO-220 |

*Future Product

**National Semiconductor Corporation**

**PRELIMINARY**

# HS7067/HS7107 7 Amp, Multimode, High Efficiency Switching Regulator

## General Description

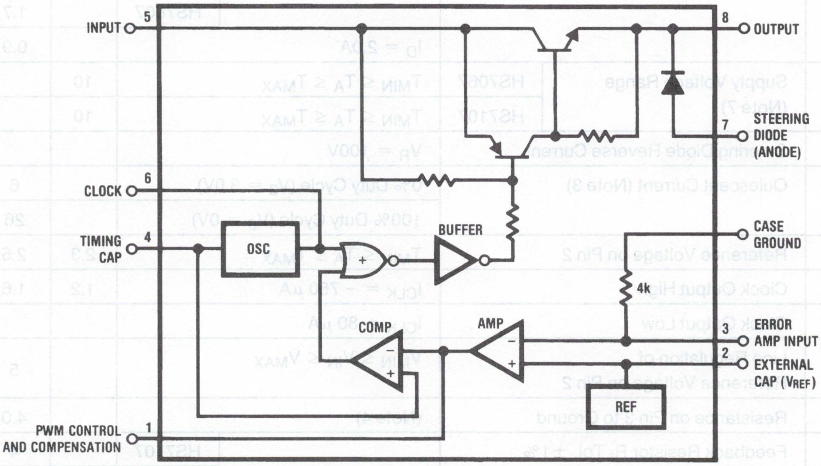
The HS7067/HS7107 is a hybrid high efficiency switching regulator with high output current capability. The device is housed in a standard TO-3 package containing a temperature compensated voltage reference, a pulse-width modulator with programmable oscillator frequency, error amplifier, high current, high voltage output switch and steering diode. The HS7067/HS7107 operates in a step-down, inverting, as well as in a transformer-coupled mode.

The HS7067/HS7107 can supply up to 7A of continuous output current over a wide range of input and output voltages.

## Features

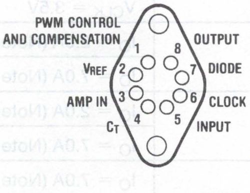
- HS7067—10V to 60V input
- HS7107—10V to 100V input
- 7A continuous output current
- Step-down, inverting, and transformer-coupled operation
- Frequency adjustable to 200 kHz
- High-efficiency (>75%)
- Standard 8-pin TO-3 package

## Block and Connection Diagrams


INPUT
5
8
OUTPUT
STEERING DIODE (ANODE)
7
CLOCK
6
TIMING CAP
4
OSC
BUFFER
CASE GROUND
4k
COMP
AMP
3
ERROR AMP INPUT
2
EXTERNAL CAP (VREF)
REF
PWM CONTROL AND COMPENSATION
1

TL/K/6746–1

**Metal Can Package**


PWM CONTROL AND COMPENSATION
1
OUTPUT
8
VREF
2
DIODE
7
AMP IN
3
CLOCK
6
CT
4
INPUT
5

TL/K/6746–2

**Top View**

Case is ground

**Order Number HS7067CK, HS7067K,**
**HS7107CK or HS7107K**
**See NS Package Number K08A**

1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$, Input Voltage | |
| HS7067 | 65V |
| HS7107 | 105V |
| $I_{OUT}$, Output Current | 8A |
| $T_J$, Operating Temperature | 150°C |
| $P_D$, Internal Power Dissipation | 25W |
| $T_A$, Operating Temperature Range | |
| HS7067C/7107C | −25°C to +85°C |
| HS7067/7107 | −55°C to +125°C |
| $T_{STG}$, Storage Temperature Range | −65°C to +150°C |
| $V_R(V_{8-7})$, Steering Diode Reverse Voltage | 105V |
| $I_D(I_{7-8})$, Steering Diode Forward Current | 8A |

## Electrical Characteristics $T_C = 25°C$, $V_{IN} = 20V$ (unless otherwise specified)

| Symbol | Parameter | | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}-V_{OUT}$ | Min $V_{IN}/V_{OUT}$ Differential | HS7067 | $10V \leq V_{IN} \leq V_{IN(MAX)}$ | | | 3.0 | | V |
| | | HS7107 | $I_{OUT} = 2A$ (Note 6) | | | 3.0 | | V |
| $V_S$ | Switch Saturation Voltage | | $I_C = 7.0A$, $V_{IN} = 10V$ | HS7107 | | 1.6 | TBD | V |
| | | | | HS7607 | | | 1.9 | V |
| | | | $I_C = 2.0A$, $V_{IN} = 10V$ | | | 1.0 | | V |
| $V_F$ | Steering Diode On Voltage | | $I_D = 7.0A$ | HS7107 | | 1.3 | TBD | V |
| | | | | HS7607 | | 1.7 | TBD | |
| | | | $I_D = 2.0A$ | | | 0.9 | | V |
| $V_{IN}$ | Supply Voltage Range (Note 7) | HS7067 | $T_{MIN} \leq T_A \leq T_{MAX}$ | | 10 | | 60 | V |
| | | HS7107 | $T_{MIN} \leq T_A \leq T_{MAX}$ | | 10 | | 100 | V |
| $I_R$ | Steering Diode Reverse Current | | $V_R = 100V$ | | | | 60 | μA |
| $I_Q$ | Quiescent Current (Note 3) | | 0% Duty Cycle ($V_3 = 3.0V$) | | | 6 | | mA |
| | | | 100% Duty Cycle ($V_3 = 0V$) | | | 26 | | mA |
| $V_2$ | Reference Voltage on Pin 2 | | $T_{MIN} \leq T_A \leq T_{MAX}$ | | 2.3 | 2.5 | 2.7 | V |
| $V_{CLK\,H}$ | Clock Output High | | $I_{CLK} = -750\ \mu A$ | | 1.2 | 1.6 | | V |
| $V_{CLK\,L}$ | Clock Output Low | | $I_{CLK} = 80\ \mu A$ | | | | 0.9 | V |
| $\Delta V_2$ | Line Regulation of Reference Voltage on Pin 2 | | $V_{MIN} \leq V_{IN} \leq V_{MAX}$ | | | 5 | | mV |
| $R_A$ | Resistance on Pin 3 to Ground | | (Note 4) | | | 4.0 | | kΩ |
| $V_{OUT}$ | Feedback Resistor $R_f$ Tol. ±1% | | | HS7107 | | 4 | TBD | % |
| | | | | HS7067 | | | 9 | |
| $V_4$ | Voltage Swing—Pin 4 | | | | | 3.0 | | V |
| $I_4$ | Charging Current—Pin 4 | | | | | 330 | | μA |
| $I_{CLK}$ | Clock Input Current — Pin 6 | | $V_{CLK} = 3.5V$ | | | 1.75 | 4 | mA |
| $t_r$ | Transistor Current Rise Time | | $I_O = 2.0A$ (Note 6) | | | 70 | | ns |
| | | | $I_O = 7.0A$ (Note 6) | | | 120 | | ns |
| $t_f$ | Transistor Current Fall Time | | $I_O = 2.0A$ (Note 6) | | | 100 | | ns |
| | | | $I_O = 7.0A$ (Note 6) | | | 160 | | ns |
| $t_s$ | Diode Storage Time | | $I_O = 7.0A$ (Note 6) | | | 120 | | ns |
| $t_d$ | Delay Time | | $I_O = 7.0A$ (Note 6) | | | 600 | | ns |
| $f_{MAX}$ | Max Clock Frequency | | (Note 5) | | | | 200 | kHz |

## Electrical Characteristics $T_C = 25°C, V_{IN} = 20V$ (unless otherwise specified) (Continued)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $Z_{PIN\ 1}$ | Impedance at Pin 1 | (Note 6) | | | 5 | | MΩ |
| $\eta$ | Efficiency | $V_{OUT} = 5V$<br>$I_{OUT} = 1A$ | $f_O = 25$ kHz (Note 6) | | 80 | | % |
| | | | $f_O = 200$ kHz (Note 5) | | 70 | | % |
| $\theta_{JC}$ | Thermal Resistance | (Note 1) | | | 4.0 | | °C/W |

**Note 1:** $\theta_{JA}$ is typically 35°C/W for natural convection cooling.

**Note 2:** $V_{OUT}$ and $I_{OUT}$ refer to the output DC voltage and output current of a switching supply after the output LC filter as shown in *Figure 1*.

**Note 3:** Quiescent current depends on the duty cycle of the switching translator.

**Note 4:** This test includes the input bias current of the error amplifier.

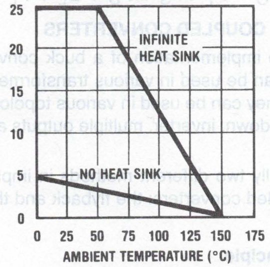
**Note 5:** Circuit configured as shown in *Figure 1*.

**Note 6:** These parameters are not tested. They are given for informational purposes only.

**Note 7:** Functionally tested at limits only (pass-fail).

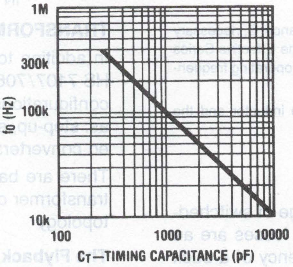
## Typical Performance Characteristics

**Power Derating Curve**



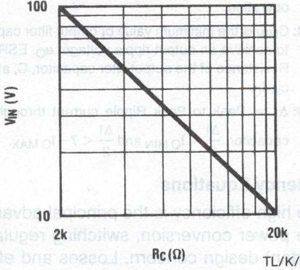
$$\theta_{JC} = 4°C/W$$
$$\theta_{JA} = 35°C/W$$

**Frequency vs Timing Capacitance**



$$f_O = \frac{1}{10k \times C_T}$$

**Typical Compensation Input Voltage vs $R_C$**



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$$R_C = \left[\frac{200k}{V_{IN(MAX)}}\right] Ω$$

$$C_C = \frac{\sqrt{LC} \times \sqrt{10}}{R_C} F$$

## Typical Applications

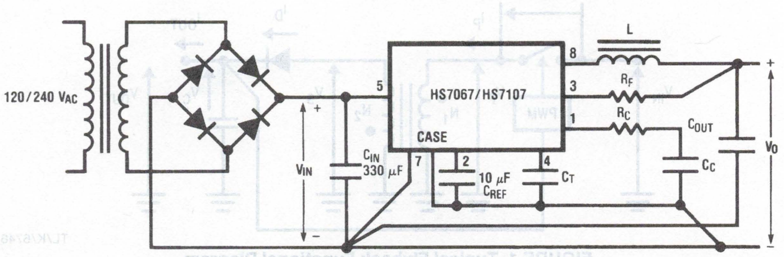
**THE BUCK CONVERTER (Step Down)**

The buck converter is the most common application in switching-power conversion. It allows to step down a voltage with a minimum of components and a maximum of efficiency (for further information on the theory of operation of a buck converter, see AN-343).

| $f_O$ | 25 kHz | 200 kHz |
|---|---|---|
| L | 86 µH | 21 µH |
| $C_T$ | 0.0039 µF | 330 pF |
| $C_C$ | 0.2 µF | 0.068 µF |
| $R_f$ | 4 kΩ | 4 kΩ |
| $R_C$ | 5.7 kΩ | 5.7 kΩ |
| $C_{OUT}$ | 1500 µF | 680 µF |

$V_{IN}$ = 10V to 35V
$V_{OUT}$ = 5V
$I_{OUT}$ = 1A to 6A

Load Regulation = 40 mV
Line Regulation = 5 mV



TL/K/6746–4

## Typical Applications (Continued)

Design equations:

Following are the design equations for a buck converter application using the HS 7107/7067:

$$C_T = \frac{1}{10^4 \times f_O}$$

$$L_{MIN} = \frac{(V_{IN(MAX)} - V_O)\, V_O}{V_{IN(MAX)} \times f_O \times \Delta I} \qquad \text{(Note 7, 9)}$$

$$C_{MIN} = \frac{\Delta I}{4\, f_O\, (e_O - \Delta I \times ESR)} \qquad \text{(Note 8, 9)}$$

$$C_C = \frac{\sqrt{10\, LC}}{R_C}$$

$$R_C = \frac{2 \times 10^5}{V_{IN(MAX)}}$$

$$R_f = 4k\left(\frac{V_O - 2.5}{2.5}\right)\Omega$$

**Note 7:** $L_{MIN}$ is the minimum value of output filter inductance, L, for stable operation.

**Note 8:** $C_{MIN}$ is the minimum value of output filter capacitance, C, necessary to achieve an output ripple voltage, $e_O$. ESR is the Effective Series Resistance of the output filter capacitor, C, at the operating frequency, $f_O$.

**Note 9:** $\Delta I$ = Peak to Peak Ripple current through the inductor and the capacitor. $\frac{\Delta I}{2} < I_{O\,MIN}$ and $\frac{\Delta I}{2} < 7 - I_{O\,MAX}$.

### Efficiency Equations

Since high efficiency is the principal advantage of switched-mode power conversion, switching regulator losses are an important design concern. Losses and efficiency of a buck converter can be calculated with the following equations.

**Note:** Pin 7 is grounded; $I_O$ = average output current at pin 8

Switching Period (T)

$$T = \frac{1}{f_O} = t_{ON} + t_{OFF}$$

Duty Cycle (D)

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_O + V_F}{V_{IN} - V_S + V_F}$$

Transistor DC Losses ($P_T$)

$$P_T = V_S \times I_O \times D$$

Transistor Switching Losses ($P_S$)

$$P_S = (V_{IN} + V_F) \times I_O \times \frac{(t_r + t_f + 2t_S)\, f_O}{2}$$

Capacitor Losses ($P_C$)

$$P_C = ESR \times \left(\frac{V_O\,(T - DT)}{4L}\right)^2$$

Diode DC Losses ($P_D$)

$$P_D = V_f \times I_O \times (1 - D)$$

Drive Circuit Losses ($D_L$)

$$D_L = 0.02 \times V_{IN} \times D$$

Inductor Losses ($P_L$)

$$P_L = I_O^2 \times R_L \text{ (DC winding resistance)}$$

Power Output ($P_O$)

$$P_O = \frac{((V_{IN} - V_S)\, t_{ON}) - ((V_F)\, t_{OFF})}{t_{ON} + t_{OFF}} \times I_O$$

Efficiency ($\eta$)

$$\eta = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_T + P_S + P_D + D_L + P_L + P_C}$$

### TRANSFORMER COUPLED CONVERTERS

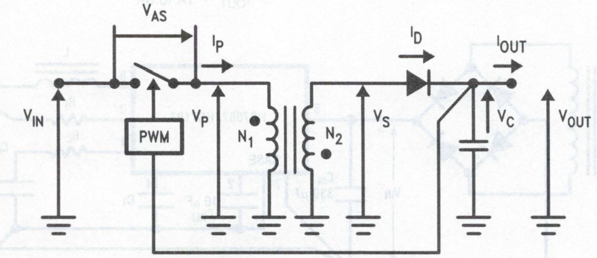
In addition to the implementation of a buck converter, the HS 7107/7067 can be used in various transformer coupled configurations. They can be used in various topologies such as: step-up, step-down, inverter, multiple outputs and isolated converters.

There are basically two different methods in implementing transformer coupled converters: the flyback and the foward topology

### The Flyback Principle

*Figure 1* shows a functional diagram of a flyback converter. Depending on the turn ratio N2/N1 and the feedback voltage, it can be implemented as a step-down or step-up converter.

When the switch is on, the current ($I_p$) flows through the primary winding creating a magnetic flux in the core and storing the energy. At this time, the voltage at the secondary keeps the same polarity (with respect to the dotted terminals), the diode is off and no current flows through it. When the switch is off, the voltage at the secondary and primary becomes reversed and the diode turns-on ($I_d$). The stored energy is then transferred to the load and the output filter capacitor. The energy stored in the capacitor will supply the load current during the next turn-on.



TL/K/6746-5

FIGURE 1. Typical Flyback Functional Diagram

## Typical Applications (Continued)

$V_p$ = Voltage at primary
$V_{as}$ = Voltage across the switch
$V_s$ = Voltage at the secondary
$I_p$ = Current at primary
$I_d$ = Current through diode
$I_c$ = Current through output cap
$I_{out}$ = Output current of the converter
$\Delta I$ = Ripple current
D = $T_{on}/(T_{off} + T_{on})$
F = Switching frequency
$V_{df}$ = Forward voltage drop of the diode
$V_1$ = $V_{out} \times N_1/N_2$  $V_2 = V_{in} + V_{out}\, N_1/N_2$
$V_3$ = Saturation voltage of the switch
$V_4$ = $V_{out} + V_{df}$  $V_5 = V_{in} \times N_2/N_1$

The load current is not supplied directly by the input source when the switch is on, but only by the energy stored in the output capacitor. The output voltage is monitored by the feedback loop which controls the duty cycle (D) through the PWM (Pulse Width Modulator) which in turn, modulates the amount of energy being transferred from the input to the output. *Figure 2* shows the waveforms of a continuous mode flyback converter (primary current $I_p$ is DC biased).

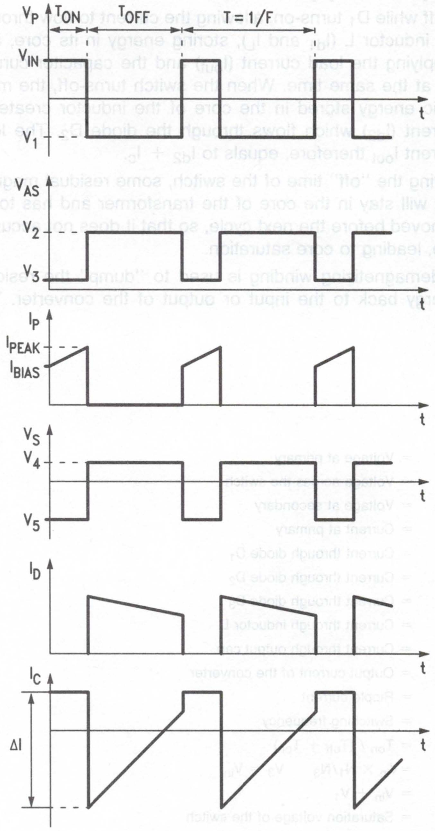


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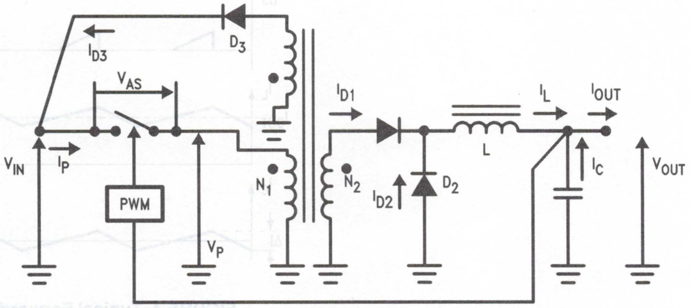
**FIGURE 2. Typical Flyback Waveforms**

### The Forward Principle

The forward converter is a little more complex and requires more components than the flyback, but the output ripple voltage is smaller. *Figure 3* shows a simplified diagram of a forward converter.

When the switch turns-on, a voltage $V_5 = V_1 \times N_2/N_1$ appears at the secondary of the transformer. The diode $D_2$



TL/K/6746–7

**FIGURE 3. Typical Forward Functional Diagram**

## Typical Applications (Continued)

is off while $D_1$ turns-on, allowing the current to flow through the inductor L ($I_{d1}$ and $I_L$), storing energy in its core, and supplying the load current ($I_{out}$) and the capacitor current ($I_c$) at the same time. When the switch turns-off, the magnetic energy stored in the core of the inductor creates a current ($I_{d2}$) which flows through the diode $D_2$. The load current $I_{out}$ therefore, equals to $I_{d2} + I_c$.

During the "off" time of the switch, some residual magnetism will stay in the core of the transformer and has to be removed before the next cycle, so that it does not accumulate, leading to core saturation.

A demagnetizing winding is used to "dump" the residual energy back to the input or output of the converter. The functional principle of the demagnetizing winding is similar to the flyback in the sense that, during the turn-off time, the residual magnetism will generate a reverse voltage at the demagnetizing winding (with respect to the dotted terminals) turning on the diode $D_3$.

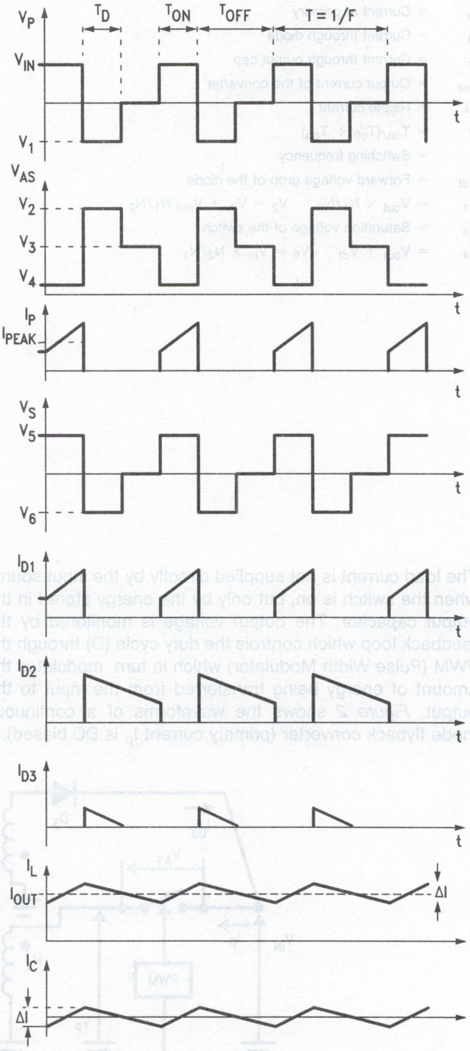
In the forward mode, when the switch is off, the load current is supplied by the energy stored in the output capacitor and the choke inductor but when the switch is on, it is supplied by the input source through the transformer. This accounts for the lower output ripple voltage.

The output voltage is monitored by the feedback loop, which controls the duty cycle through the PWM, which in turn modulates the amount of energy being transferred from the input to the output.

$V_p$ = Voltage at primary
$V_{as}$ = Voltage across the switch
$V_s$ = Voltage at secondary
$I_p$ = Current at primary
$I_{d1}$ = Current through diode $D_1$
$I_{d2}$ = Current through diode $D_2$
$I_{d3}$ = Current through diode $D_3$
$I_L$ = Current through inductor L
$I_c$ = Current through output cap
$I_{out}$ = Output current of the converter
$\Delta_I$ = Ripple current
F = Switching frequency
D = $T_{on} / (T_{off} + T_{on})$
$V_1 = V_{in} \times N_1/N_3$ $\quad V_3 = V_{in}$
$V_2 = V_{in} + V_1$
$V_4$ = Saturation voltage of the switch
$V_5 = V_{in} \times N_2/N_1$ $\quad V_6 = V_{in} \times N_2/N_3$

*Figure 4* shows the waveforms of the forward converter.

When the switch is off, $V_{as} = V_{in} + (V_{in} \times N_1/N_3)$ during the demagnetization time ($T_d$) and then, drops to $V_{as} = V_{in}$ as indicated in *Figure 4*.



TL/K/6746–8

**FIGURE 4. Typical Forward Waveforms**

## Typical Applications (Continued)

With both flyback and forward topologies, it is possible to design an inverting converter by using an external op-amp (*Figure 5*).

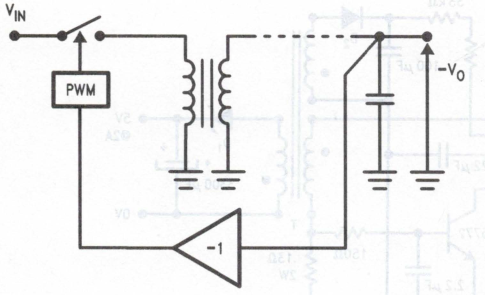


**FIGURE 5**

### Flyback Step-Up Application

*Figure 6* shows flyback converter in a step-up mode where an input voltage of +12V to +30V will be converted into a regulated output voltage of +50V.

**Performance Data**

| Parameter | Conditions | Result |
|---|---|---|
| Efficiency | $V_{out}$ = 50V @300 mA<br>$V_{in}$ = 15V | 82% |
| Line Regulation | $V_{out}$ = 50V @300 mA<br>$12V \le V_{in} \le 30V$ | 0.2% |
| Load Regulation | $V_{in}$ = 15V<br>$V_{out}$ = 50V<br>$50\ mA \le I_{out} \le 300\ mA$ | 0.2% |

### Isolated Flyback Converter

*Figure 7* shows an isolated flyback converter using a sense winding for feedback. Although, in practice the line regulation is acceptable, the load regulation can be marginal if the coupling between the windings is poor. However, the sense winding cannot detect any ohmic voltage drop in the main output so, a heavier gauge wire should be used to reduce this regulation error. Also, the sense winding will not sense the non-linear voltage drop across the diode, and this accounts for most of the load regulation inaccuracy. Therefore, the sense winding method is only recommended for applications where load variations are small.

*Figure 7* shows an isolated flyback converter with an output of 5V at 2A. The input voltage range is from +10V to +40V. The output can be adjusted to +5V by using the 5 kΩ trimpot.

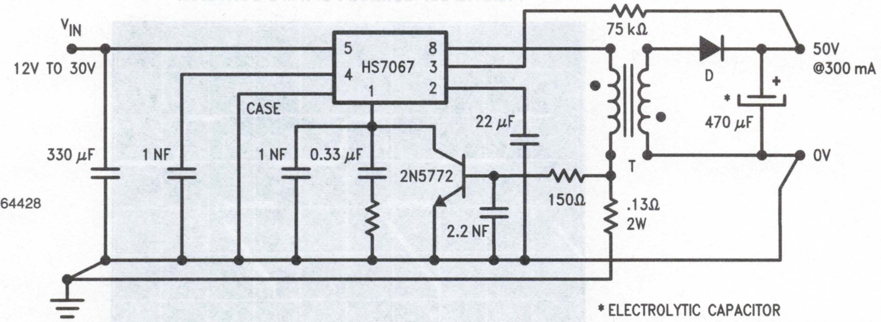
**Performance Data**

| Parameter | Conditions | Result |
|---|---|---|
| Efficiency | $V_{out}$ = 5V @ 2A<br>$V_{in}$ = 30V | 75% |
| Line Regulation | $V_{out}$ = 5V @ 2A<br>$10V \le V_{in} \le 40V$ | 5% |
| Load Regulation | $V_{in}$ = 30V<br>$1A \le I_{out} \le 2A$ | 7% |

### Isolated Forward Converter

As described previously, forward converters exhibit lower output ripple voltage and the opto-coupler feedback scheme provides good regulation as well as input to output isolation.

An opto-coupler feedback is usually difficult to implement because the transfer function of the opto-coupler is non-linear, the current transfer ratio changes with time and temperture and also from one unit to another. *Figure 8* shows the circuit diagram of a 5V @ 3A power converter with an input voltage range of +14V to +30V using an isolated forward topology.



D = Unitrode UES1302
T = Pulse Engineering PE64428
$f_o$ = 100 kHz
$I_{out\ (min)}$ = 50 mA

TL/K/6746–11

A 12V to 60V input Voltage Range is possible by replacing the HS7067 with a HS7107. The converter will operate in a discontinuous mode above 30V with a 300 mA load (the transformer's secondary current drops to zero before the switch turns on) and therefore, may generate more switching noise.

**FIGURE 6. Flyback Step-Up Converter**

## Typical Applications (Continued)

$D_1$ = International Rectifier 50SQ060
$D_2$ = 1N4148
$I_{out\ (min)}$ = 1A
$f_O$ = 100 kHz
T = Transformer made of a core Fenoxcube 1811PA2503B7
Primary = 8 turns with 5 strands #29
Secondary = 6 turns with 15 strands #30
Sense = 25 turns with 1 strand #30
windings should be interleaved in order to improve the coupling and regulation.

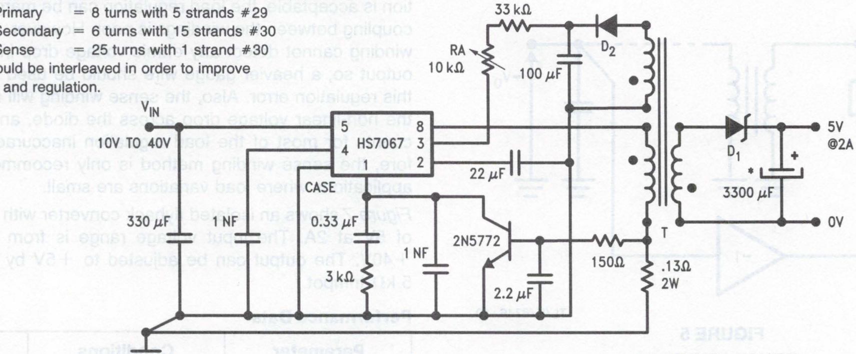

33 kΩ
RA
10 kΩ
100 µF
D2
V_IN
10V TO 40V
5
8
4
HS7067
3
2
CASE
22 µF
5V @2A
D1
*
3300 µF
0V
330 µF
1 NF
0.33 µF
1 NF
3 kΩ
2N5772
150Ω
T
.13Ω 2W
2.2 µF

**FIGURE 7. Isolated Flyback Converter**

* ELECTROLYTIC CAPACITOR

TL/K/6746-12

$D_1$ = $D_2$ = International Rectifier 50SQ060
$D_3$ = Unitode UES1302
T = Pulse Engineering PE64423
L = Pulse Engineering PE52711
$f_O$ = 50 kHz
$I_{out\ (min)}$ = 0.5A

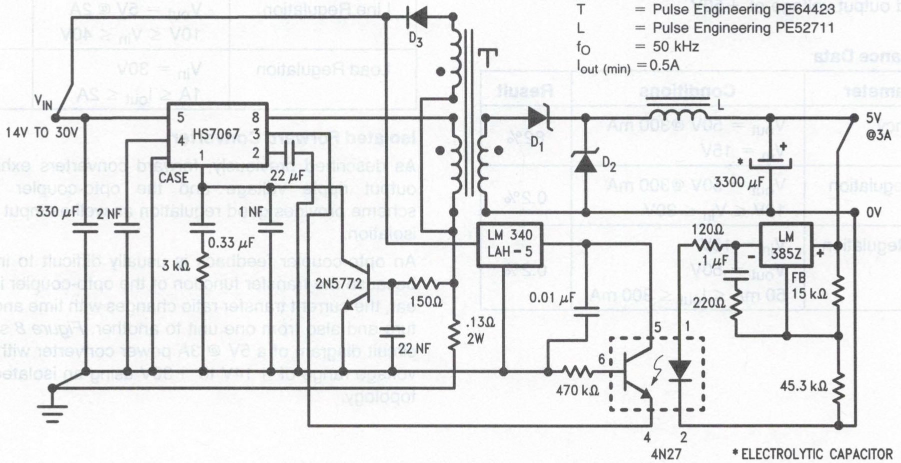
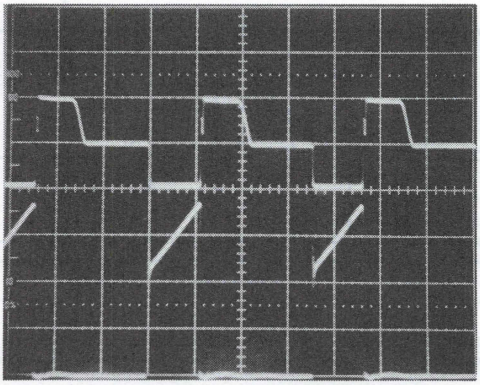

D3
T
V_IN
14V TO 30V
5
8
4
HS7067
3
2
CASE
22 µF
330 µF
2 NF
1 NF
0.33 µF
3 kΩ
2N5772
150Ω
.13Ω 2W
22 NF
L
D1
D2
*
3300 µF
5V @3A
0V
LM 340 LAH-5
120Ω
.1 µF
LM 385Z
FB
15 kΩ
220Ω
0.01 µF
470 kΩ
5
1
6
4
2
4N27
45.3 kΩ

**FIGURE 8a. Isolated Forward Converter**

* ELECTROLYTIC CAPACITOR

TL/K/6746-13



TL/K/6746-9

*Figure 8b* shows the typical forward converter waveforms in continuous mode which can be observed using the circuit from *Figure 8a.* Top waveform is the voltage across the switch (20V/div). Bottom waveform is the current throughout the switch (1A/dv). Horizontal Scale = 5 µS/dir. $V_{in}$ = 20V; $V_{out}$ = 5V @ 3A.

**Figure 8b.**

## Typical Applications (Continued)

An LM 385z (adjustable reference) is used as a comparator and error amplifier. This reference always wants to maintain 1.2V between pins 1 and 2 and will draw as much current as necessary from the opto-coupler to achieve this. Therefore, the feedback loop is virtually independent of the gain of the opto-coupler.

**Performance Data**

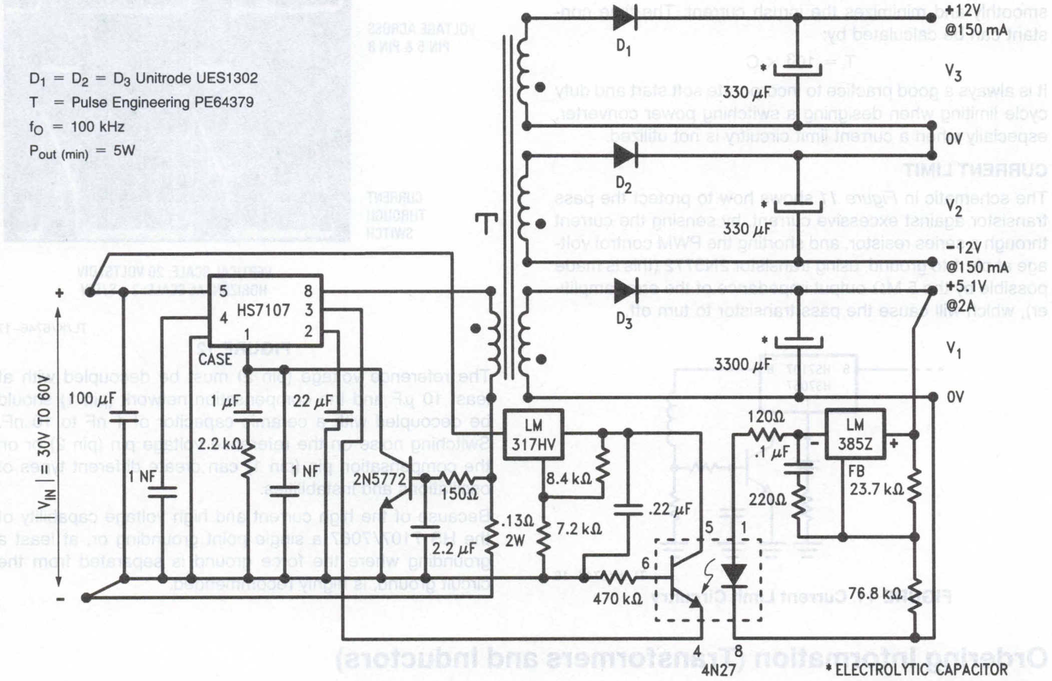
| Parameter | Conditions | Result |
|---|---|---|
| Efficiency | $V_{out} = 5V$ @ 3A<br>$V_{in} = 30V$ | 78% |
| Line Regulation | $V_{out} = 5V$ @ 3A<br>$14V \leq V_{in} \leq 30V$ | 0.1% |
| Load Regulation | $V_{out} = 5V$<br>$V_{in} = 20V$<br>$0.5A \leq I_{out} \leq 3A$ | 0.1% |

**Isolated Telecom Converter**

*Figure 9* shows an isolated triple output converter which will transform a positive or negative input voltage of 32V to 60V to an uncommitted triple output of +12V, −12V, and 5V, which may be later referenced to the system ground. This converter is ideal for a step down converter of high positive voltage or high negative voltage such as −48V used in telecom circuits.

**Performance Data**

| Parameter | Conditions | Result |
|---|---|---|
| Efficiency | $V_1 = 5.1V$ @ 2A<br>$V_2 = -12V$ @ 150 mA<br>$V_3 = 12V$ @ 100 mA<br>$\lvert V_{in} \rvert = 48V$ | 62% |
| Line Regulation on Main Secondary | $40V \leq \lvert V_{in} \rvert \leq 60V$<br>$V_1 = 5.1V$ @ 2A<br>$V_2 = -12V$ @ 150 mA<br>$V_3 = +12V$ @ 150 mA | 0.8% |
| Load Regulation on Main Secondary | $\lvert V_{in} \rvert = 48V$<br>$V_1 = 5.1V$<br>$V_2 = 12V$ @ 150 mA<br>$V_3 = 12V$ @ 150 mA<br>$0.5 \leq I_{out} \leq 2A$ | 1% |
| Load Regulation on 12V Secondary for Simultaneous Load Changes | $\lvert V_{in} \rvert = 48V$<br>$V_1 = 5.1V$ @ 2A<br>$V_2 = -12V$<br>$V_3 = 12V$<br>$75 mA \leq I_{out} \leq 150 mA$ | 5% |


D1 = D2 = D3 Unitrode UES1302
T = Pulse Engineering PE64379
fO = 100 kHz
Pout (min) = 5W
+12V
@150 mA
D1
330 µF
V3
0V
D2
T
V2
-12V
@150 mA
330 µF
+5.1V
@2A
D3
3300 µF
V1
0V
+
5
4
HS7107
8
3
1
2
CASE
VIN = 30V TO 60V
-
100 µF
1 NF
1 µF
2.2 kΩ
22 µF
1 NF
2N5772
150Ω
.13Ω
2W
2.2 µF
LM
317HV
8.4 kΩ
7.2 kΩ
.22 µF
5
1
6
470 kΩ
4
8
4N27
120Ω
.1 µF
220Ω
LM
385Z
FB
23.7 kΩ
76.8 kΩ
* ELECTROLYTIC CAPACITOR
TL/K/6746-14

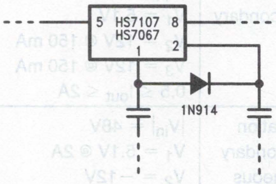
**Note 10:** An input voltage of −10V to −30V may cause the transformer to operate at a higher temperature at full load.

FIGURE 9. Telecom Flyback Converter

## Application Hints

### DUTY CYCLE LIMITING

In a flyback converter, the error amplifier sees 0V at the output of the converter during the initial turn-on, and forces the duty cycle to 100% until it sees the output voltage rising to the final value; but no voltage will appear if the switch does not turn off (see flyback principle). The result is that the core will saturate, reducing the effective impedance of the transformer to about 0Ω, and destroying the pass transistor. To prevent this, the duty cycle must be limited to a value at which the core does not saturate. A diode connected between pins 1 and 2 (*Figure 10*), will limit the duty cycle to about 80%.



TL/K/6746–15

**FIGURE 10. Duty Cycle Limiting Circuit**

### SOFT START

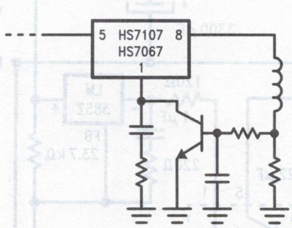
For any converter, connecting a large capacitor (20 to 200 μF) between pin 2 and the case is recommended to allow the reference voltage to slowly reach its final value after start-up. This allows the HS 7067/7107 to start-up smoothly and minimizes the inrush current. The time constant can be calculated by:

$$T = 10^3 \times C$$

It is always a good practice to incorporate soft start and duty cycle limiting when designing a switching power converter, especially when a current limit circuitry is not utilized.

### CURRENT LIMIT

The schematic in *Figure 11* shows how to protect the pass transistor against excessive current, by sensing the current through a series resistor, and shorting the PWM control voltage at pin 1 to ground, using transistor 2N5772 (this is made possible by the 5 MΩ output impedance of the error amplifier), which will cause the pass transistor to turn off.



TL/K/6746–16

**FIGURE 11. Current Limit Circuitry**

The sense resistor should be a low inductance type, otherwise the series inductance creates a high impedance at transients and activates the shutdown circuitry. If such a resistor cannot be found, a 0.1 μF connected in parallel with it will compensate the series inductance.

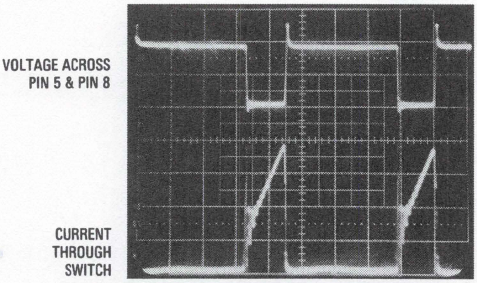
When such a circuitry is used, the duty cycle limiting diode becomes optional, but the soft start capacitor should still be at least 10 μF.

### DECOUPLING AND GROUNDING

Special attention should be given to the decoupling of the HS 7107/7067 itself at the input (pin 5), where the capacitor must be at least 100 μF and connected as close to the device as possible. Large switching spikes at the input of the pass transistor can cause breakdown of the junction and destroy the device. (See Figure 12.)

The waveform at the top of the picture represents the voltage across the switch of a typical BUCK (step down) converter. When the switch is turned off, the current in the inductor falls to zero (see waveform at the bottom) and a switching spike occurs across the switch. This spike can reach several tens of volts on top of the normally expected voltage across the switch and lead to stress on the device if the overall voltage exceeds the maximum rating.

The picture below shows a spike of about ten volts with a 330 μF capacitor of average quality.



VERTICAL SCALE: 20 VOLTS/DIV
HORIZONTAL SCALE: 2 μS/DIV

TL/K/6746–17

**FIGURE 12**

The reference voltage (pin 2) must be decoupled with at least 10 μF and the compensation network (pin 1) should be decoupled with a ceramic capacitor of 1 nF to 10 nF. Switching noise on the reference voltage pin (pin 2) or on the compensation pin (pin 1) can create different types of oscillations and instabilities.

Because of the high current and high voltage capability of the HS 7107/7067 a single point grounding or, at least a grounding where the force ground is separated from the circuit ground, is highly recommended.

## Ordering Information (Transformers and Inductors)

PULSE ENGINEERING INC.
7250 Convoy Court
San Diego, CA 92111
USA

Tel: (619) 268-2400
TWX: 910-335-1527
FAX: 619 268-2515

**National Semiconductor Corporation**

**PRELIMINARY**

# HS9151 Micro-Switching Off-Line Power Converter 120 $V_{AC}$/ +5V @ 3 Amps

## General Description

The HS9151—Micro-Switching Off-Line Power Converter is a hybrid power converter housed in a 3.5″ x 1.5″ x 0.44″ metal dual-in-line package.

The high efficiency of the Off-Line Converter is achieved by using advanced switching technology.

A 1 MHz PWM controller with current limiting and temperature protection is incorporated in the package. Also, the input and output rectifiers and magnetics are included as well as an internally adjusted opto-isolator feedback stage.

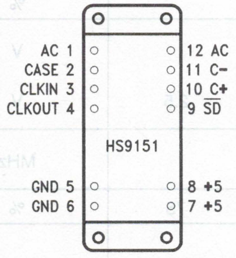
With a 120 $V_{AC}$ nominal input voltage, the HS9151 can supply 3 amps at +5 $V_{DC}$ over a temperature range of −25°C to +85°C and only requiring a heatsink for operation above 40°C.

The HS9151 provides access to the clock input pin for synchronization of several HS9151s from an external clock, or the internal clock of one unit can be used as a master clock for several units. The HS9151 also features softstart at power up.

## Features

- 120 $V_{AC}$ or 170 $V_{DC}$ nominal input
- +5 $V_{DC}$ output at 3 amps
- 3.5″ x 1.5″ x 0.44″ size
- 1000 $V_{RMS}$/1500 $V_{DC}$ Input/Output isolation
- Full 3A output current capability over temperature
- Synchronization
- Shortcircuit/temperature protection
- Softstart and remote shutdown
- 1 MHz switching frequency
- Isolated case

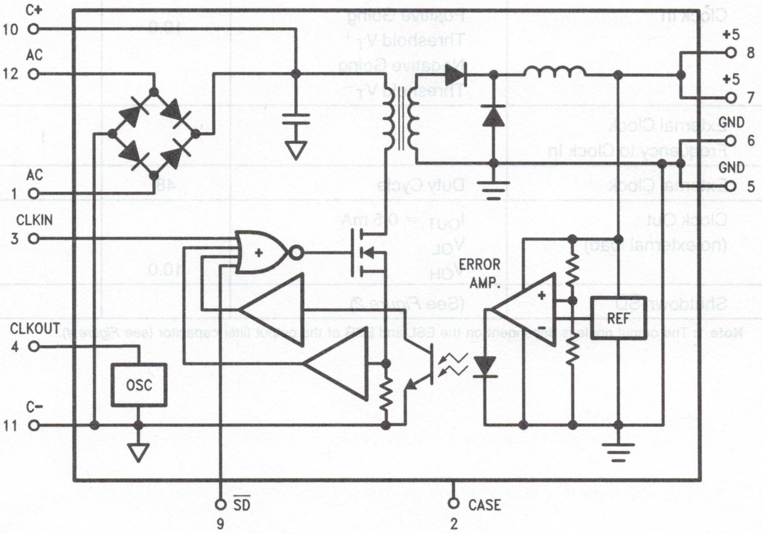
## Block and Connection Diagrams



TL/K/8502-1

**Top View**

**Order Number HS9151**



TL/K/8502-2

**Note 1:** Caution: this device is operated directly from the 115 Vrms AC line. An isolation transformer must be used when making measurements with test equipment, to prevent personnel exposure to lethal voltage potentials. Standard high voltage safety procedures should also be observed.

**Note 2:** Pin 2 is connected to case ground.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| $V_{IN}$, Input Voltage | |
| AC Voltage (Pin 1 to Pin 12) | 140 $V_{AC}$ |
| DC Voltage (Pin 10 to Pin 11) | 200 $V_{DC}$ |
| $I_{OUT}$, Output Short Circuit Duration | Continuous |

| | |
|---|---|
| $T_A$, Operating Temperature Range | −25°C to +85°C |
| $T_{CASE}$, Operating Case Temperature | 100°C |
| $T_{STG}$, Storage Temperature Range | −65°C to +150°C |
| Voltage Differential | |
| Input to Output (1 Min.) | 1500 $V_{DC}$ |
| Non-Repetitive Sinusoidal Surge through Bridge Rectifier (10 ms) | 20A |

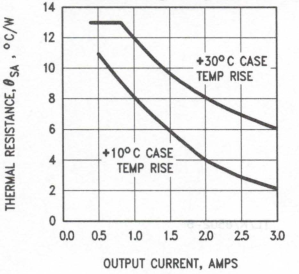
## Electrical Characteristics $T_A = 25°C$, $V_{IN} = 120\ V_{RMS}$ AC unless otherwise specified

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Voltage | $V_{IN} = 90$ to $130\ V_{AC}$ or<br>$V_{IN} = 115$ to $190\ V_{DC}$<br>$I_{OUT} = 0.5A$ to $3A$ | 4.875 | | 5.125 | $V_{DC}$ |
| Output Transient Recovery Time | $I_{OUT} = 2A$ to $3A$ | | 500 | | μs |
| Load Regulation | $I_{OUT} = 0.5A$ to $3A$ | | | ±1.0 | % |
| Line Regulation | $V_{IN} = 90$ to $130\ V_{AC}$ | | | ±0.25 | %<br>(0–120 Hz) |
| Peak to Peak Output Ripple | $I_{OUT} = 3A$<br>(Note 1) | | 50 | | mV<br>(0–20 MHz) |
| Input to Output Isolation | | 100 | | | MΩ |
| Efficiency | $I_{OUT} = 3A$<br>$I_{OUT} = 0.5A$ | | 75<br>50 | | %<br>% |
| Clock In | Positive Going Threshold $V_T+$<br>Negative Going Threshold $V_T-$ | 10.0 | | <br>2.5 | V<br>V |
| External Clock Frequency to Clock In | | | 1 | | MHz |
| External Clock | Duty Cycle | 48 | | 75 | % |
| Clock Out (no external load) | $I_{OUT} = 0.5$ mA<br>$V_{OL}$<br>$V_{OH}$ | <br><br>10.0 | | <br>0.5 | <br>V<br>V |
| Shutdown SD | (See *Figure 2*) | | | 2.5 | V |

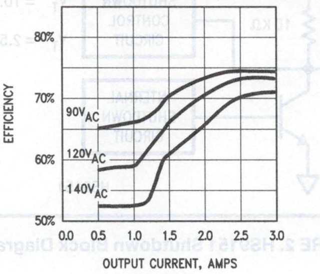
**Note 1:** The output ripple is dependent on the ESL and ESR of the output filter capacitor (see *Figure 4*).

## Typical Performance Characteristics

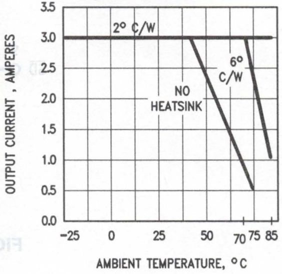
**Heatsinking Requirements**



**Efficiency vs. Output Current**



**Absolute Maximum Output Current**



TL/K/8502-3

**Note:** Case temperature should not exceed 100°C.

**Note:** Assumes $T_{CASE\ (MAX)} = 100°C$.

## Application Information

### IN-RUSH CURRENT LIMITING

During start up, the input of the HS9151 presents a very low impedance to the AC line, generally only the ESR of the input filter. If current limit is not provided at the input, the high in-rush current can destroy the input rectifier bridge.

A 10Ω (1 Watt) resistor should be placed in series with the input rectifier bridge and the AC line to limit the current to a non-destructive level. This scheme reduces the efficiency of the power converter by approximately 3% at full load due to the $I^2R$ loss in the resistor (see *Figure 4*).

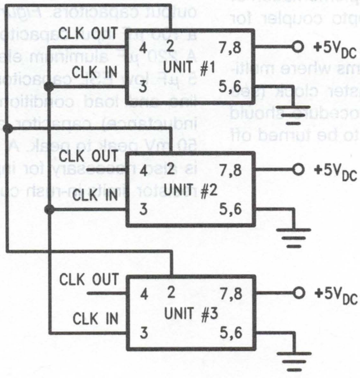
### CLKIN and CLKOUT

The HS9151 provides an internal 1 MHz clock, CLKOUT (pin 4), that allows several units to be synchronized to one master clock in applications where multiple units are used. The logic high is specified at 10.0V (min.) and logic low is specified at 0.5V (max.) when $I_{OUT} = \pm 1$ mA. The CLKIN (pin 3) allows the power converter to use an externally supplied 1 MHz clock instead of using the oscillator provided inside the HS9151. Isolation is required when using an external clock. In applications that do not require synchronization, the CLKIN and CLKOUT pins should be connected together.

*Figure 1* below, shows the connection scheme when three HS9151s are synchronized off the same master clock provided by unit #1.

### REMOTE SHUTDOWN $\overline{\text{SD}}$

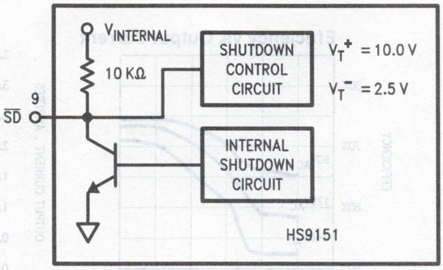
A remote shutdown function (pin 9) is also provided in the HS9151. This allows the switching converter to be disabled when pin 9 is brought below 2.5 volts. This feature allows proper power up sequencing of a complex system, and it also enables peripheral equipment to be turned on and off remotely. An input equivalent circuit of the $\overline{\text{SD}}$ pin is shown in *Figure 2*.



TL/K/8502-4

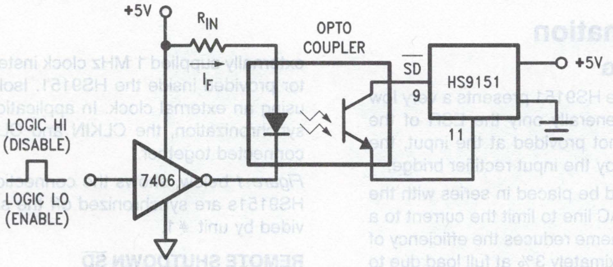
**FIGURE 1. HS9151 Synchronization**

## Application Information (Continued)


V_INTERNAL
10 KΩ
9
SD
SHUTDOWN CONTROL CIRCUIT
$V_T^+$ = 10.0 V
$V_T^-$ = 2.5 V
INTERNAL SHUTDOWN CIRCUIT
HS9151

TL/K/8502-5

**FIGURE 2. HS9151 Shutdown Block Diagram**


+5V
R_IN
OPTO COUPLER
I_F
LOGIC HI (DISABLE)
LOGIC LO (ENABLE)
7406
SD
9
HS9151
11
+5V

$$I_F = \frac{5V - V_{F(LED)} - V_{OL(7406)}}{R_{IN}}$$

TL/K/8502-6

**FIGURE 3. Remote Shutdown Using an Opto Coupler and +5V Logic**

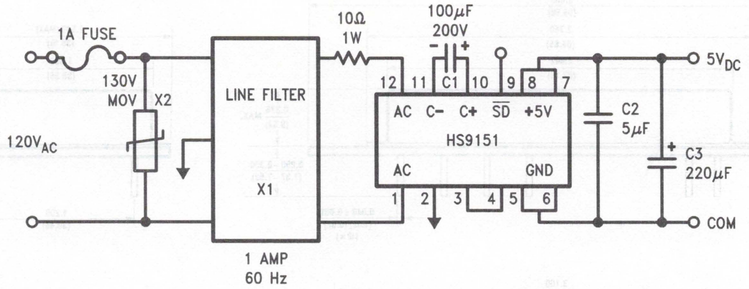
Because the shutdown control is located on the primary side of the power converter, it is recommended that the shutdown control signal, $\overline{SD}$, be isolated either optically or by other means. *Figure 3* shows a typical implementation of the remote shutdown function, using an opto coupler for isolation.

When the shutdown feature is used in systems where multiple HS9151s are synchronized from a master clock (see *Figure 1*) and sequenced, the shutdown procedure should be such that the master unit is the last unit to be turned off and the first one to be turned on.

## Typical Applications

The HS9151 can be configured into a complete 5V @ 3A power supply by simply adding an input capacitor and two output capacitors. *Figure 4* shows an implementation using a 100 μF input capacitor to provide a holdup time of 16 ms. A 220 μF aluminum electrolytic capacitor in parallel with a 5 μF low ESL capacitor guarantees loop stability under all line and load conditions. The low ESL (equivalent series inductance) capacitor also keeps the output ripple under 50 mV peak to peak. A 130 $V_{AC}$ metal oxide varistor (MOV) is also necessary for input protection and the 10Ω, 1 Watt resistor limits in-rush current to under 20A.

## Typical Applications (Continued)



TL/K/8502-7

**FIGURE 4. HS9151 Configured as a 15W Power Supply**

| | |
|---|---|
| X1 | SAE F15209 Line Filter, TRI-MAG G3-1 or equivalent |
| X2 | GE V130LA1 Metal Oxide Varistor |
| C1 | Mepco/Electra 3476 LK101M200 JMBS or equivalent<br>200V 100 µF Aluminum Electrolytic |
| C2 | Rel-Cap PPMF505KIR OR Electronic Concepts 5MC 22B 505K<br>100V, 5 µF Polypropylene 50V, 5 µF Polycarbonate |
| C3 | Mepco/Electra 3481 CE221V025 JDBS or equivalent<br>25V, 220 µF Aluminum Electrolytic |

Reliable Capacitors
12931 E. Sunnyside Place
Sante Fe Springs, CA 90670
(213) 946-8577

Electronic Concepts Inc.
P. O. Box 627
Eatontown, NJ 07724
(201) 542-7880

SAE Power Devices
340 Martin Ave.
Santa Clara, CA 95050-1997
(408) 988-0700

TRI-MAG, Inc.
8204 W. Doe St.
Visalia, CA. 93277
(209)651-2222

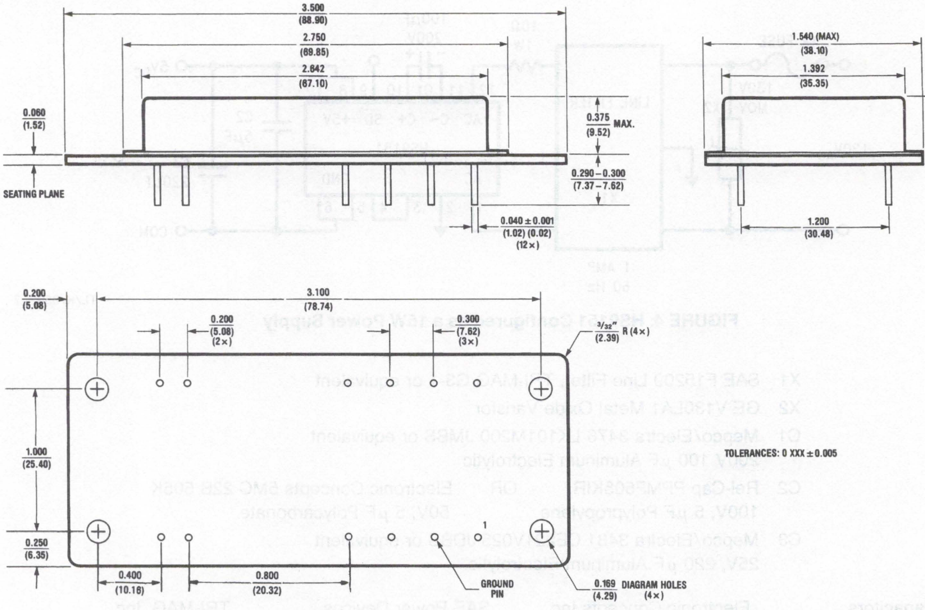
The efficiency of the power supply is a function of the input line voltage and the output load current. At maximum load current, the efficiency is the highest, approaching 75% with $V_{in}$ = 120 VAC. Also, the efficiency varies by less than ±2% when the line voltage changes from low line to high line at maximum output load current (see graph for efficiency versus output current).

### THERMAL CONSIDERATIONS

The HS9151 is housed in an all metal hybrid power package measuring only 3.5″ x 1.5″ x 0.44″. The low thermal resistance of this package allows the power converter to operate at full power (5V at 3A) without a heatsink up to an ambient temperature of 40°C. For operation beyond 40°C, some form of heat sinking is recommended. The rise in temperature of the internal components is dependent on the power delivered at the output. Under normal operating conditions, it is recommended that the case temperature of the HS9151 be kept below 90°C. Under these conditions, the junction temperature of the internal integrated circuits are kept below 115°C.

For selecting a proper heatsink consult the graph provided. This information greatly simplifies the task of selecting the proper heatsink for the HS9151 when it is operated at elevated temperatures. For example, when a load current of 3 amperes is drawn from the power converter, and a heatsink with a 2°C/W thermal resistance is used, the case temperature would increase by 10°C. Alternatively, if a 6°C/W heatsink were used, the case temperature would go up by 30°C.

## Physical Dimensions inches (millimeters)


3.500
(88.90)
2.750
(69.85)
2.642
(67.10)
0.060
(1.52)
SEATING PLANE
0.375
(9.52)
MAX.
0.290 – 0.300
(7.37 – 7.62)
0.040 ± 0.001
(1.02) (0.02)
(12×)
1.540 (MAX)
(38.10)
1.392
(35.35)
0.440
(11.18)
MAX.
1.200
(30.48)
0.200
(5.08)
3.100
(78.74)
0.200
(5.08)
(2×)
0.300
(7.62)
(3×)
3/32"
(2.39)
R (4×)
1.000
(25.40)
TOLERANCES: 0 XXX ± 0.005
1
0.250
(6.35)
0.400
(10.16)
0.800
(20.32)
GROUND
PIN
0.169
(4.29)
DIAGRAM HOLES
(4×)

TL/K/8502-8

**Bottom View**

**Order Number HS9151**

**National Semiconductor Corporation**

# LH0075 Positive Precision Programmable Regulator

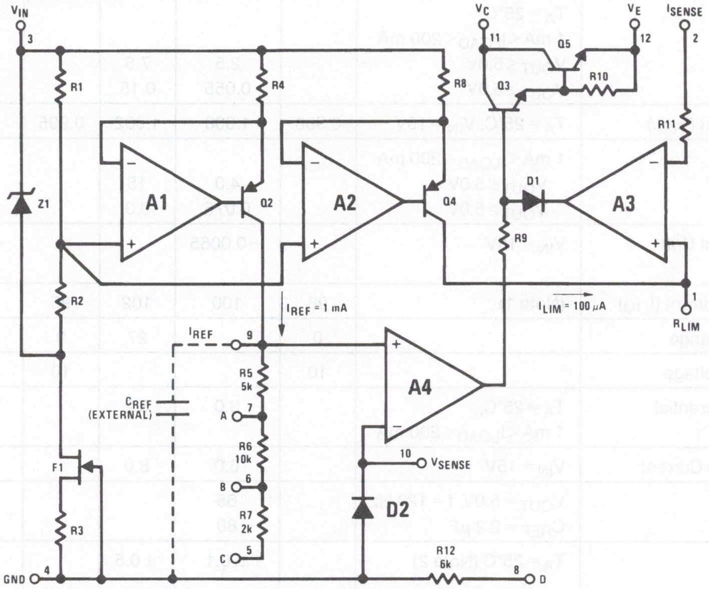
## General Description

The LH0075 is a precision programmable regulator for positive voltages. Regulated output voltages from 0 to 27V may be obtained using one external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V and 15V). The output current limit is adjustable from 0 to 200 mA using two external resistors. These features provide an inventory of precision regulated values in one package.

## Features

- Output adjustable to 0V
- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection of 80 dB
- Adjustable precision current limit
- Output currents to 200 mA
- Popular voltages available without external resistors

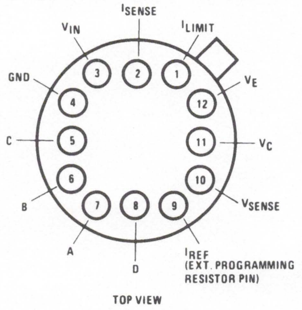
## Schematic Diagram



V<sub>IN</sub> 3
R1
R2
Z1
A1
Q2
R4
A2
Q4
R8
Q3
Q5
R10
V<sub>C</sub> 11
V<sub>E</sub> 12
I<sub>SENSE</sub> 2
R11
D1
A3
R9
I<sub>LIM</sub> = 100 μA
1
R<sub>LIM</sub>
I<sub>REF</sub> = 1 mA
I<sub>REF</sub> 9
C<sub>REF</sub> (EXTERNAL)
R5 5k
A 7
R6 10k
B 6
R7 2k
C 5
A4
10 V<sub>SENSE</sub>
D2
R12 6k
8 D
F1
R3
GND 4

## Connection Diagram

**TO-8 Metal Can Package**



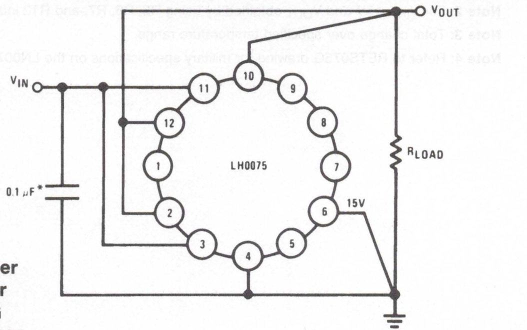
I<sub>SENSE</sub>
V<sub>IN</sub>
I<sub>LIMIT</sub>
GND
V<sub>E</sub>
C
V<sub>C</sub>
B
V<sub>SENSE</sub>
A
D
I<sub>REF</sub> (EXT. PROGRAMMING RESISTOR PIN)
1 2 3 4 5 6 7 8 9 10 11 12
TOP VIEW

Case is electrically isolated

**Order Number LH0075G or LH0075CG**
**See NS Package Number H12B**

## Typical Applications

**Precision 15V Reference Supply without Current Limit**



V<sub>OUT</sub>
V<sub>IN</sub>
LH0075
R<sub>LOAD</sub>
0.1 μF*
15V
1 2 3 4 5 6 7 8 9 10 11 12

TL/H/5549-1

*Needed if device is far from filter capacitors

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 4)**

| | |
|---|---|
| Input Voltage | 32V |
| Output Voltage | 27V |
| Output Current | 200 mA |
| Power Dissipation | See Curve |

| | |
|---|---|
| Operating Temperature Range | |
| LH0075 | −55°C to +125°C |
| LH0075C | 0°C to +70°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

## Electrical Characteristics

Conditions for $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted

| Parameter | Conditions | LH0075 | | | LH0075C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_A = 25°C$ | | 0.008 | 0.02 | | 0.008 | 0.04 | %/V |
| Load Regulation | $T_A = 25°C$,<br>$1\ mA < I_{LOAD} < 200\ mA$<br>$V_{OUT} \le 5.0V$<br>$V_{OUT} \ge 5.0V$ | | 2.5<br>0.055 | 7.5<br>0.15 | | 2.5<br>0.055 | 15<br>0.3 | mV<br>% |
| Reference Current ($I_{REF}$) | $T_A = 25°C$, $V_{IN} = 15V$ | 0.998 | 1.000 | 1.002 | 0.995 | 1.00 | 1.005 | mA |
| Load Regulation | $1\ mA < I_{LOAD} < 200\ mA$<br>$V_{OUT} \le 5.0V$<br>$V_{OUT} \ge 5.0V$ | | 4.0<br>0.075 | 15<br>0.3 | | 4.0<br>0.075 | 25<br>0.5 | mV<br>% |
| Reference Current Drift ($\Delta I_{REF}/\Delta Temp.$) | $V_{IN} = 15V$ | | −0.0065 | | | −0.0065 | | %/°C |
| Minimum Load Current ($I_{LIM}$) | (Note 1) | 98 | 100 | 102 | 95 | 100 | 105 | μA |
| Output Voltage Range | | 0 | | 27 | 0 | | 27 | V |
| Minimum Input Voltage | | 10 | | | 10 | | | V |
| Input-Output Differential Voltage | $T_A = 25°C$,<br>$1\ mA < I_{LOAD} < 200\ mA$ | | 3.0 | 3.2 | | 3.0 | 3.5 | V |
| Quiescent Supply Current | $V_{IN} = 15V$ | | 6.0 | 8.0 | | 6.5 | 10 | mA |
| Ripple Rejection | $V_{OUT} = 5.0V$, f = 120 Hz<br>$C_{REF} = 2.2\ \mu F$ | | 65<br>80 | | | 65<br>80 | | dB<br>dB |
| Output Voltage Tolerance | $T_A = 25°C$ (Note 2) | | ±0.1 | ±0.5 | | ±0.1 | ±1.0 | % |
| Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta Temp.$) | (Note 3) | | 0.003 | | | 0.003 | | %/°C |

**Note 1:** Minimum load current is established by $I_{LIM}$, the current from Q4 (see schematic). $I_{LIM}$ goes directly to the output if the current limit feature is used.

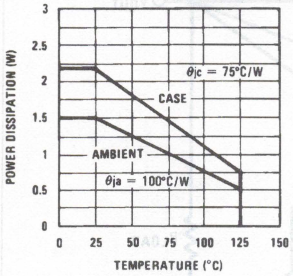
**Note 2:** For $V_{IN} = 15V$ and $V_{OUT}$ obtained by using R5, R6, R7, and R12 individually.

**Note 3:** Total change over specified temperature range.

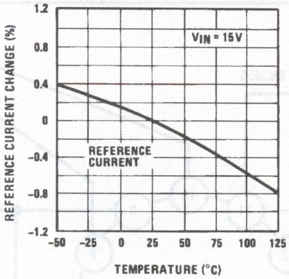
**Note 4:** Refer to RETS075G drawing for military specifications on the LN0075.

## Typical Performance Characteristics

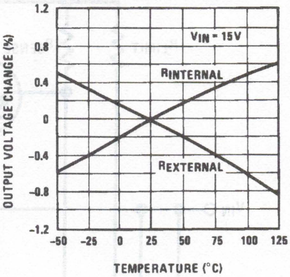
### Maximum Power Dissipation



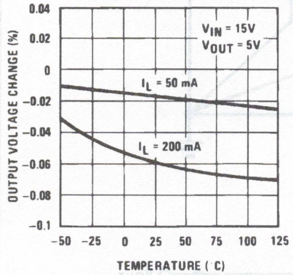
### Reference Current Change with Temperature (Normalized)



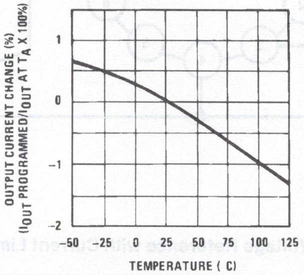
### Temperature Stability



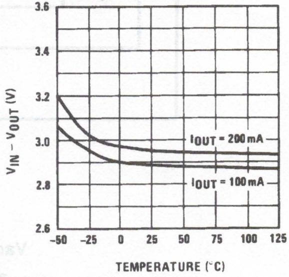
### Output Voltage Change with Temperature (Normalized)



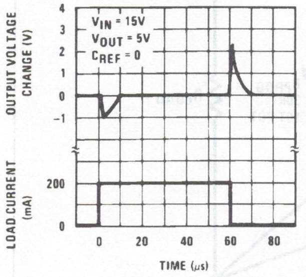
### Current Limit



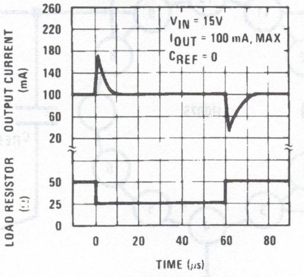
### Input-Output Differential Voltage



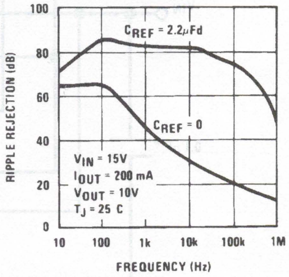
### Load Transient Response (Voltage Mode)



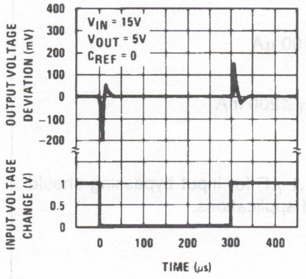
### Load Transient Response (Current Mode)



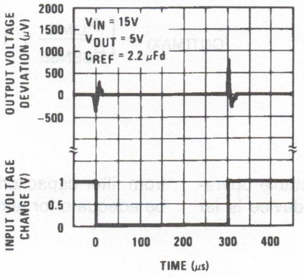
### Ripple Rejection



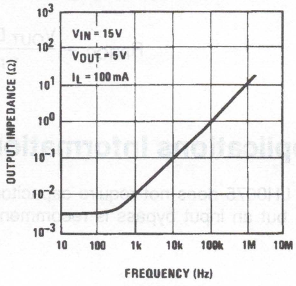
### Line Transient Response



### Line Transient Response



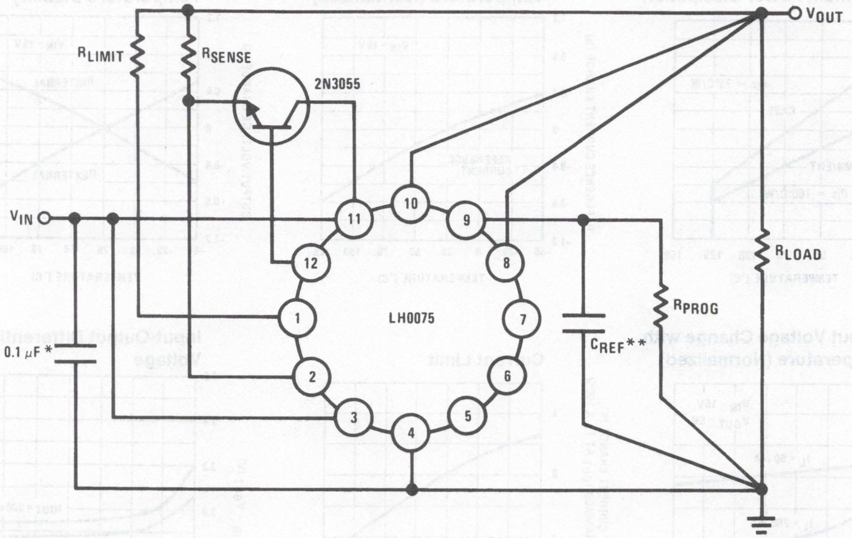
### Output Impedance



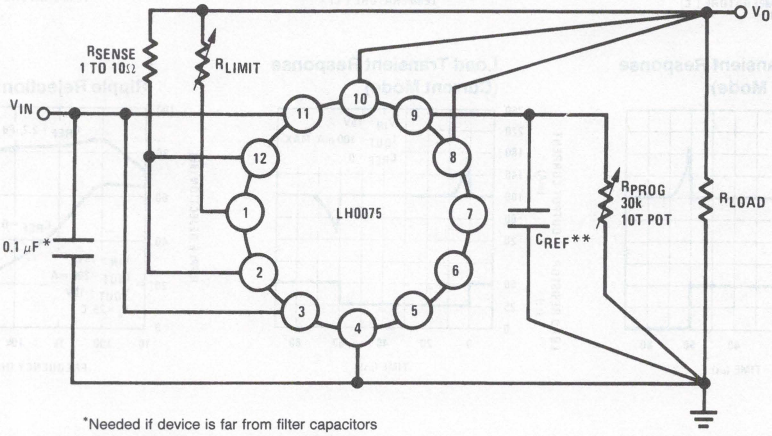
TL/H/5549-2

## Typical Applications (Continued)

### 2A Regulator with Current Limit


R_LIMIT
R_SENSE
2N3055
V_OUT
V_IN
0.1 µF*
LH0075
1
2
3
4
5
6
7
8
9
10
11
12
R_LOAD
R_PROG
C_REF**

### Variable Voltage Reference with Current Limit


R_SENSE
1 TO 10Ω
R_LIMIT
V_IN
V_OUT
0.1 µF*
LH0075
1
2
3
4
5
6
7
8
9
10
11
12
R_PROG
30k
10T POT
C_REF**
R_LOAD

*Needed if device is far from filter capacitors

**Optional—improves transient response

TL/H/5549-3

$$R_{PROG} = \frac{V_{OUT}\text{ Desired}}{1\text{ mA}}$$

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\ \mu A$$

$I_{OUT} \leq 200$ mA

## Applications Information

The LH0075 does not require capacitors for stable operation, but an input bypass is recommended if device is far from filter capacitors. A 0.1 µF for input bypassing should be adequate for almost all applications.

## Applications Information (Continued)

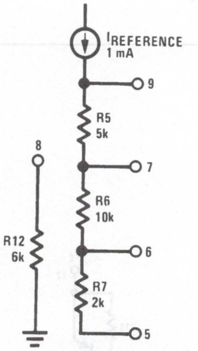
### DESCRIPTION OF OPTIONS

**Ripple Rejection Compensation. (Increases Ripple Rejection Typically to 80 dB)**

The ripple rejection may be improved by connecting an external capacitor between pin 9 and ground. (The typical performance curves show the rejection with a capacitance of 2.2 $\mu$Fd.)

**Internal Voltage Programming**

The LM0075 provides various precision output voltages simply by using one or more of the internal resistors. A particular voltage may be obtained by external connections as shown in Table I.



R5, R6, R7 and R12 are precision-trimmed to 0.1%.

TL/H/5549-4

**FIGURE 1**

**External Voltage Programming**

An external resistance can be connected between pin 9 and ground to obtain any voltage from 0 to 27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}}$$

The reference current ($I_{REF}$) has a typical temperature coefficient of −65 ppm/°C. Choosing a resistive material with a temperature coefficient of 65 ppm/°C will compensate the negative temperature coefficient, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is Nichrome, which has a typical temperature coefficient of 80 ppm/°C.

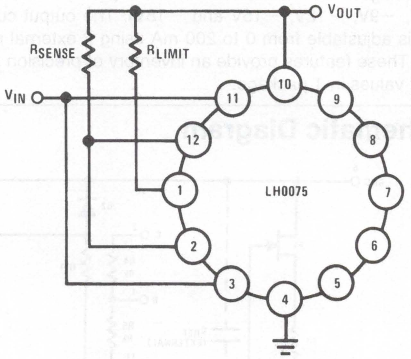
Since a current source is used as a reference, this makes remote voltage programming possible.

**Current Limit Programming**

The maximum current output of the device may be limited by adding two external resistors as shown below. The resistor values are easily calculated with the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\mu A$$

where $R_{SENSE} = 1$ to $10\Omega$.



TL/H/5549-5

**FIGURE 2. Current Limit Programmng**

This programmable current limit feature can be extended to make the LH0075 a programmable constant current source. This can be done by leaving pin 9 open and setting $R_{LIMIT}$ and $R_{SENSE}$ as desired.

For applications where the current limit is used, a minimum load current of 100 $\mu$A is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 $\mu$A, and it goes directly to the output of the LH0075. If the total current drawn from the output is less than the minimum, the output will rise.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. $R_{SENSE}$ must be placed as close to the output of the LH0075 as possible, but $R_{LIMIT}$ can be a fixed resistor or potentiometer located remotely from the device.

**TABLE I. Connection Scheme for Internal Available Output Voltages**

| OUTPUT VOLTAGE (V) | PIN 5 | PIN 6 | PIN 7 | PIN 8 | PIN 9 |
|---|---|---|---|---|---|
| 5 | | | Gnd | | |
| 6 | | | | ● | ● |
| 8 | ● | — | — | ● | |
| | | ● | — | — | ● |
| 10 | | Gnd | ● | — | ● |
| 12 | Gnd | | ● | — | ● |
| 15 | | Gnd | | | |
| 18 | | | ● | — | ● |
| | ● | — | — | ● | |

1

**National Semiconductor Corporation**

# LH0076 Negative Precision Programmable Regulator

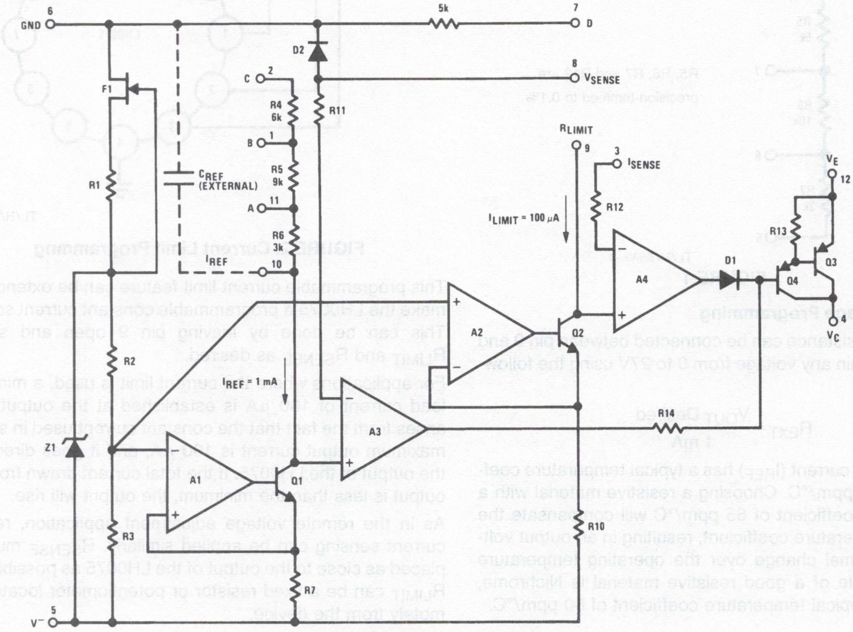
## General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200 mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

## Features

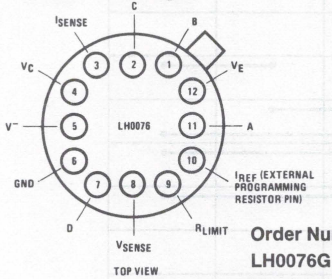
- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection-70 dB
- Output Adjustable to 0V
- Adjustable precision current limit
- Output current to 200 mA

## Schematic Diagram


6
GND
F1
R1
C_REF (EXTERNAL)
R2
Z1
R3
5
V⁻
D2
C 2
R4 6k
B 1
R5 9k
A 11
R6 3k
I_REF
10
R11
I_REF = 1 mA
A1
Q1
A3
R7
R8 5k
7 D
8 V_SENSE
R_LIMIT
9
3 I_SENSE
I_LIMIT = 100 μA
R12
A4
A2
Q2
D1
Q4
Q3
R13
V_E
12
4
V_C
R14
R10

## Connection Diagram

### Metal Can Package

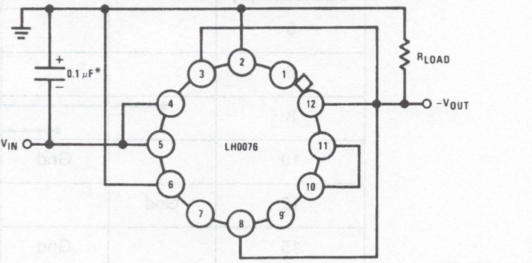

I_SENSE
C
B
V_C
V_E
V⁻
LH0076
A
GND
I_REF (EXTERNAL PROGRAMMING RESISTOR PIN)
D
V_SENSE
R_LIMIT
1
2
3
4
5
6
7
8
9
10
11
12
TOP VIEW

Case is electrically isolated

**Order Number**
**LH0076G**
**LH0076CG**
**See NS Package H12B**

## Typical Applications

### Precision −15V Reference Supply without Current Limit


0.1 μF*
+
−V_IN
LH0076
R_LOAD
−V_OUT
1
2
3
4
5
6
7
8
9
10
11
12

*Recommended if device is far from filter capacitors

TL/H/5548–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Input Voltage | −32V |
| Output Voltage | −27V |
| Output Current | 200 mA |
| Power Dissipation | See Curve |

| | |
|---|---|
| Operating Temperature Range | |
| LH0076 | −55°C to +125°C |
| LH0076C | 25°C to +85°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature<br>(Soldering, 10 seconds) | 300°C |

## Electrical Characteristics

Conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

| Parameter | Conditions | LH0076 | | | LH0076C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_A=25°C$ | | 0.005 | 0.02 | | 0.005 | 0.04 | %/V |
| Load Regulation | $T_A=25°C$,<br>$1\ mA<I_{LOAD}<200\ mA$<br>$V_{OUT} \geq -5.0V$<br>$V_{OUT} \leq -5.0V$ | | 0.02 | 7.5<br>0.15 | | 0.02 | 15<br>0.3 | mV<br>% |
| Reference Current ($I_{REF}$) | $T_A=25°C$, $V_{IN}=-15V$ | 0.998 | 1.000 | 1.002 | 0.995 | 1.000 | 1.005 | mA |
| Reference Current Drift ($\Delta I_{REF}/\Delta Temp.$) | $V_{IN}=-15V$ | | −0.0065 | | | −0.0065 | | %/°C |
| Minimum Load Current ($I_{LIM}$) | (Note 1) | 98 | 100 | 102 | 95 | 100 | 105 | μA |
| Output Voltage Range | | 0 | | −27 | 0 | | −27 | V |
| Minimum Input Voltage | | −10 | | | −10 | | | V |
| Input-Output Differential Voltage | $T_A=25°C$,<br>$1\ mA<I_{LOAD}<200\ mA$ | | 2.7 | 3.2 | | 2.7 | 3.5 | V |
| Quiescent Supply Current | $V_{IN}=-15V$ | | 11 | 15 | | 11 | 15 | mA |
| Ripple Rejection | $V_{OUT}=5.0V$, f=120 Hz | | 70 | | | 70 | | dB |
| Output Voltage Tolerance | $T_A=25°C$, (Note 2) | | ±0.1 | ±0.5 | | ±0.1 | ±1.0 | % |
| Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta Temp.$) | (Note 3) | | 0.003 | | | 0.003 | | %/°C |

**Note 1:** Minimum load current is established by $I_{LIM}$, the current to Q2 (see schematic.) $I_{LIM}$ draws directly from the output if the current limit feature is used.

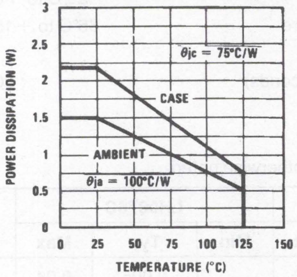
**Note 2:** For $V_{IN}=15V$ and $V_{OUT}$ obtained by using R4, R5, R6, and R8 individually.

**Note 3:** Total change over specified temperature range.

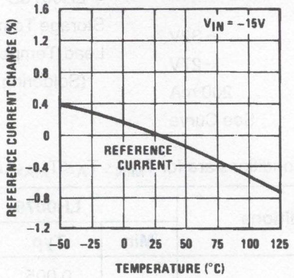
**Note 4:** Refer to RETS0076G for military specifications on the LH0076.

## Typical Performance Characteristics

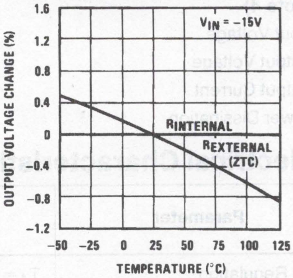
### Maximum Power Dissipation



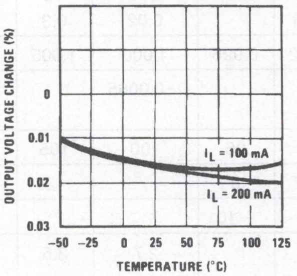
### Reference Current Change with Temperature (Normalized)



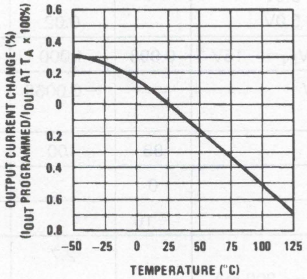
### Temperature Stability



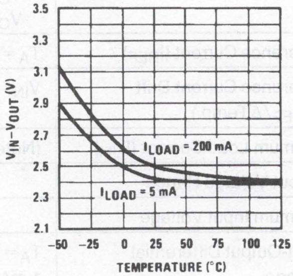
### Output Voltage Change with Temperature (Normalized)



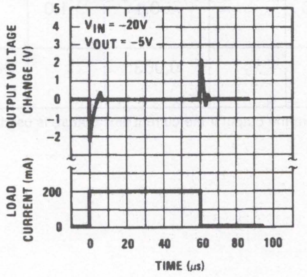
### Current Limit



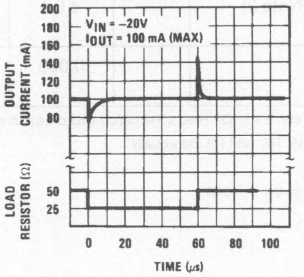
### Input-Output Differential Voltage



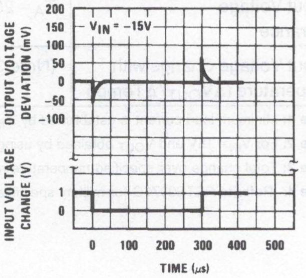
### Load Transient Response (Voltage Mode)



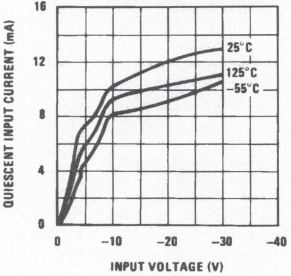
### Load Transient Response (Current Mode)



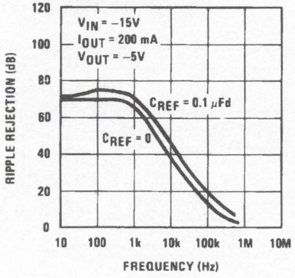
### Line Transient Response



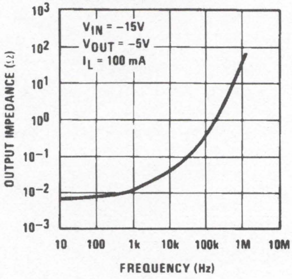
### Quiescent Input Current



### Ripple Rejection



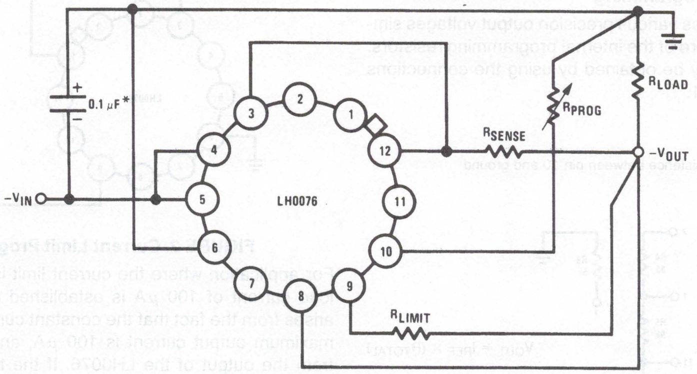
### Output Impedance



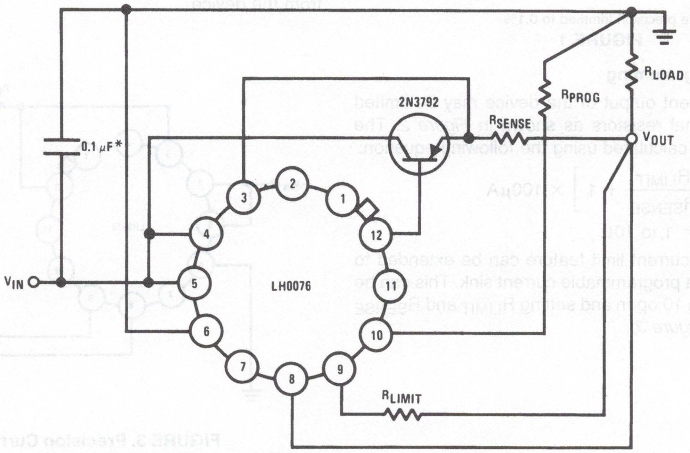
TL/H/5548–3

## Typical Applications (Continued)

**Variable Voltage Reference with Current Limit**


0.1 µF*
−VIN
LH0076
1
2
3
4
5
6
7
8
9
10
11
12
RSENSE
RPROG
RLOAD
−VOUT
RLIMIT

**2-Amp Regulator with Current Limit**


0.1 µF*
VIN
LH0076
2N3792
1
2
3
4
5
6
7
8
9
10
11
12
RSENSE
RPROG
RLOAD
VOUT
RLIMIT

TL/H/5548–4

*Recommended if device is far from filter capacitors

## Application Information

The LH0076 does not require external capacitors for stable operation. However, an input bypass is recommended if the device is far from filter capacitors. A 0.1 µF for input bypassing should be adequate for most applications.

### DESCRIPTION OF OPTIONS

### External Voltage Programming

An external resistance can be connected between pin 10 and ground to obtain any voltage from 0 to −27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\text{ desired}}{-1\text{ mA}}$$

The reference current ($I_{REF}$) has a typical temperature coefficient of −60 ppm/°C. Choosing a resistive material with a temperature coefficient of 60 ppm/°C will compensate the negative tempco of the reference current, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is nichrome, which has a typical tempco of 80 ppm/°C. Nichrome is the resistive material used in the LH0076, resulting in output voltage drift of 20 ppm/°C typically.

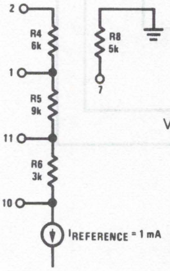
## Application Information (Continued)

Because a current source is used as a reference, remote voltage programming is possible.

### Internal Voltage Programming

The LH0076 provides various precision output voltages simply by using 1 or more of the internal programming resistors. These voltages may be obtained by using the connections as shown in Table 1.

$R_{TOTAL}$ is the total resistance between pin 10 and ground



$V_{OUT} = I_{REF} \times (R_{TOTAL})$

TL/H/5548-5

R4, R5, R6 and R8 are precision trimmed to 0.1%

FIGURE 1

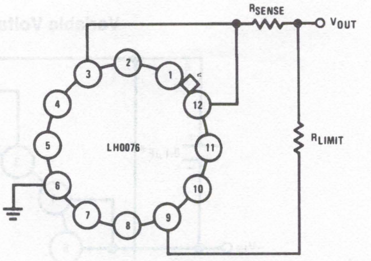
### Current Limit Programming

The maximum current output of the device may be limited by adding 2 external resistors as shown in *Figure 2.* The resistor values are calculated using the following equation:

$$I_{OUT(MAX)} = \left[ \frac{R_{LIMIT}}{R_{SENSE}} + 1 \right] \times 100\mu A$$

where $R_{SENSE} = 1$ to $10\Omega$

This programming current limit feature can be extended to make the LH0076 a programmable current sink. This can be done by leaving pin 10 open and setting $R_{LIMIT}$ and $R_{SENSE}$ as desired. (See *Figure 3).*

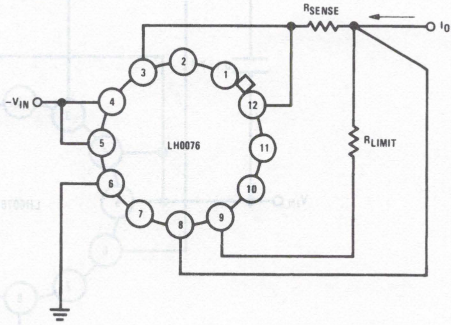


TL/H/5548-6

FIGURE 2. Current Limit Programming

For application where the current limit is used, a minimum load current of 100 µA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 µA, and it comes directly from the output of the LH0076. If the total current is less than this minimum current, the output will drop.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. $R_{SENSE}$ should be placed as close to the output of the LH0076 as possible, but $R_{LIMIT}$ can be a resistor or potentiometer located remotely from the device.



TL/H/5548-7

FIGURE 3. Precision Current Sink

TABLE 1. Connection Scheme for Internally Available Output Voltages

| OUTPUT VOLTAGE (V) | PIN 1 | PIN 2 | PIN 7 | PIN 10 | PIN 11 |
|---|---|---|---|---|---|
| −3 | | | | | GND |
| −5 | | | ● | ● | |
| −6 | ● | Gnd | ─ | ● | |
| −8 | | | ● | ─ | ● |
| −9 | Gnd | | | ● | ● |
| −12 | Gnd | | | | |
| −15 | | Gnd | | ● | ● |
| −18 | | Gnd | | | |

National
Semiconductor
Corporation

# LM104/LM204/LM304 Negative Regulator

## General Description

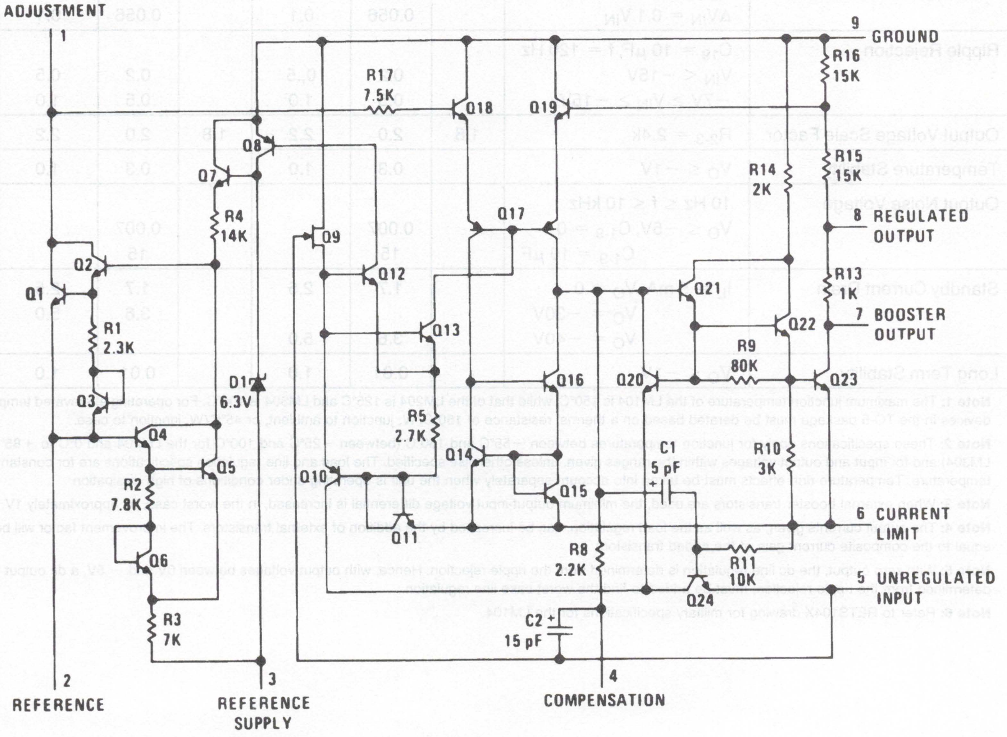
The LM104 series are precision voltage regulators which can be programmed by a single external resistor to supply any voltage from 40V down to zero while operating from a single unregulated supply. They can also provide 0.01-percent regulation in circuits using a separate, floating bias supply, where the output voltage is limited only by the breakdown of external pass transistors. Although designed primarily as linear, series regulators, the circuits can be used as switching regulators, current regulators or in a number of other control applications. Typical performance characteristics are:

- Subsurface zener reference
- 1 mV regulation no load to full load
- 0.01%/V line regulation
- 0.2 mV/V ripple rejection
- 0.3% temperature stability over military temperature range

The LM104 series is the complement of the LM105 positive regulator, intended for systems requiring regulated negative voltages which have a common ground with the unregulated supply. By themselves, they can deliver output currents to 25 mA, but external transistors can be added to get any desired current. The output voltage is set by external resistors, and either constant or foldback current limiting is made available.

The LM104 is specified for operation over the −55°C to +125°C military temperature range. The LM204 is specified for operation over the −25°C to +85°C temperature range. The LM304 is specified for operation from 0°C to +70°C.

## Schematic Diagram


ADJUSTMENT
1
9
GROUND
R16
15K
R17
7.5K
Q18
Q19
Q8
Q7
R15
15K
R14
2K
R4
14K
Q17
8 REGULATED
OUTPUT
Q9
Q2
Q12
R13
1K
Q1
Q21
R1
2.3K
Q13
7 BOOSTER
OUTPUT
Q22
R9
80K
D1
6.3V
Q16
Q20
Q23
Q3
R5
2.7K
Q4
Q14
C1
5 pF
R10
3K
Q5
Q10
R2
7.8K
Q15
Q11
6 CURRENT
LIMIT
Q6
R8
2.2K
R11
10K
5 UNREGULATED
INPUT
Q24
R3
7K
C2
15 pF
2
REFERENCE
3
REFERENCE
SUPPLY
4
COMPENSATION

TL/H/7754–1

# Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

**(Note 6)**

| | LM104/LM204 | LM304 |
|---|---|---|
| Input Voltage | 50V | 40V |
| Input-Output Voltage Differential | 50V | 40V |
| Power Dissipation (Note 1) | 500 mW | 500 mW |
| Operating Temperature Range | | |
| LM104 | −55°C to +125°C | |
| LM204 | −25°C to +85°C | |
| LM304 | | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C for plastic | 300°C for hermetic |

# Electrical Characteristics

| Parameter | Conditions | LM104/LM204 | | | LM304 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | | −50 | | −8 | −40 | | −8 | V |
| Output Voltage Range | | −40 | | −0.015 | −30 | | −0.035 | V |
| Output-Input Voltage Differential (Note 3) | $I_O = 20$ mA | 2.0 | | 50 | 2.0 | | 40 | V |
| | $I_O = 5$ mA | 0.5 | | 50 | 0.5 | | 40 | V |
| Load Regulation (Note 4) | $0 \leq I_O \leq 20$ mA<br>$R_{SC} = 15\Omega$ | | 1 | 5 | | 1 | 5 | mV |
| Line Regulation (Note 5) | $V_{OUT} \leq -5V$<br>$\Delta V_{IN} = 0.1 V_{IN}$ | | 0.056 | 0.1 | | 0.056 | 0.1 | % |
| Ripple Rejection | $C_{19} = 10\ \mu F$, f = 120 Hz<br>$V_{IN} < -15V$ | | 0.2 | 0,.5 | | 0.2 | 0.5 | mV/V |
| | $-7V \geq V_{IN} \geq -15V$ | | 0.5 | 1.0 | | 0.5 | 1.0 | mV/V |
| Output Voltage Scale Factor | $R_{2\text{-}3} = 2.4k$ | 1.8 | 2.0 | 2.2 | 1.8 | 2.0 | 2.2 | V/kΩ |
| Temperature Stability | $V_O \leq -1V$ | | 0.3 | 1.0 | | 0.3 | 1.0 | % |
| Output Noise Voltage | 10 Hz ≤ f ≤ 10 kHz<br>$V_O \leq -5V, C_{1\text{-}9} = 0$ | | 0.007 | | | 0.007 | | % |
| | $C_{1\text{-}9} = 10\ \mu F$ | | 15 | | | 15 | | μV |
| Standby Current Drain | $I_L = 5$ mA, $V_O = 0$ | | 1.7 | 2.5 | | 1.7 | 2.5 | mA |
| | $V_O = -30V$ | | | | | 3.6 | 5.0 | mA |
| | $V_O = -40V$ | | 3.6 | 5.0 | | | | mA |
| Long Term Stability | $V_O \leq -1V$ | | 0.01 | 1.0 | | 0.01 | 1.0 | % |

**Note 1:** The maximum junction temperature of the LM104 is 150°C, while that of the LM204 is 125°C and LM304 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

**Note 2:** These specifications apply for junction temperatures between −55°C and 150°C (between −25°C and 100°C for the LM204 and 0°C to +85°C for the LM304) and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

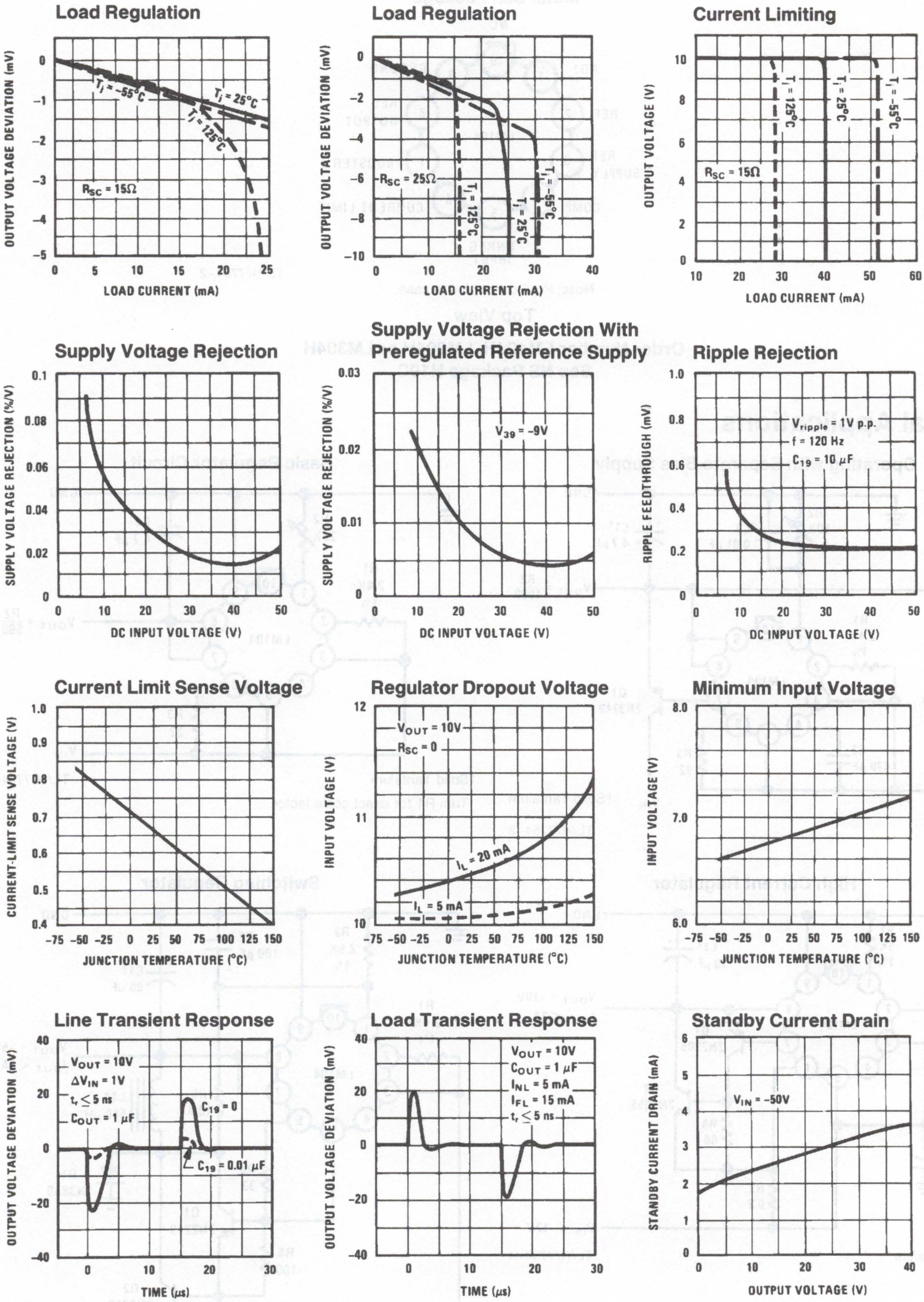
**Note 3:** When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1V.

**Note 4:** The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

**Note 5:** With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and − 5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

**Note 6:** Refer to RETS104X drawing for military specifications for the LM104.

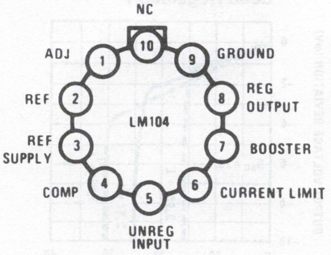
## Typical Performance Characteristics


Load Regulation; Load Regulation; Current Limiting; Supply Voltage Rejection; Supply Voltage Rejection With Preregulated Reference Supply; Ripple Rejection; Current Limit Sense Voltage; Regulator Dropout Voltage; Minimum Input Voltage; Line Transient Response; Load Transient Response; Standby Current Drain

TL/H/7754-7

## Connection Diagram

**Metal Can Package**


NC
10
ADJ
1
GROUND
9
REF
2
REG OUTPUT
8
LM104
REF SUPPLY
3
BOOSTER
7
COMP
4
CURRENT LIMIT
6
5
UNREG INPUT

TL/H/7754–2

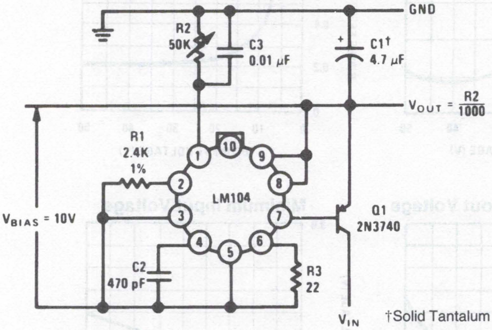
**Note:** Pin 5 connected to case.

**Top View**

**Order Number LM104H, LM204H or LM304H**
**See NS Package H10C**

## Typical Applications

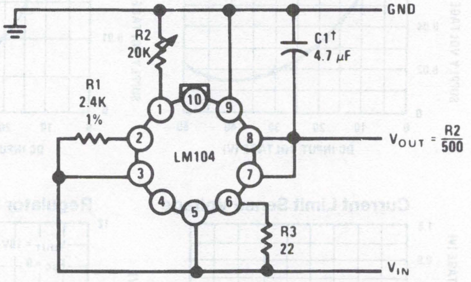
### Operating with Separate Bias Supply


GND
R2
50K
C3
0.01 µF
C1†
4.7 µF
VOUT = R2/1000
R1
2.4K
1%
LM104
VBIAS = 10V
Q1
2N3740
C2
470 pF
R3
22
VIN

†Solid Tantalum

TL/H/7754–3

### Basic Regulator Circuit

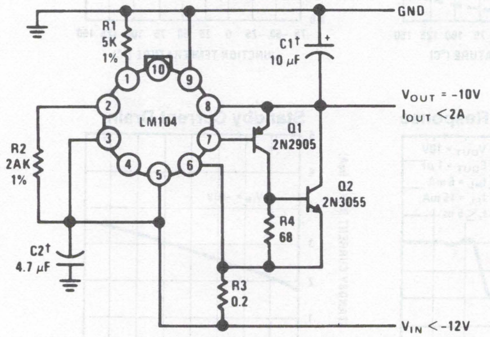

GND
R2
20K
C1†
4.7 µF
R1
2.4K
1%
LM104
VOUT = R2/500
R3
22
VIN

†Solid Tantalum

Trim R1 for exact scale factor.

TL/H/7754–5

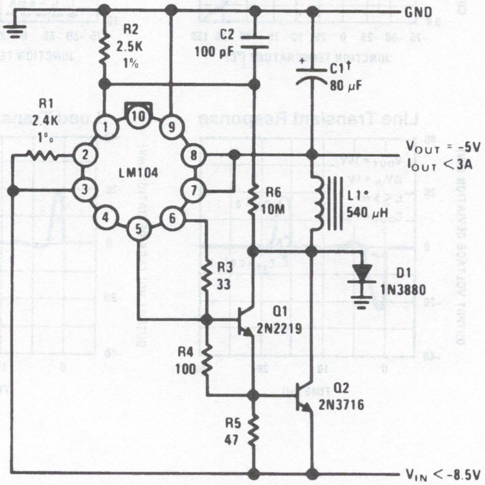
### High Current Regulator


GND
R1
5K
1%
C1†
10 µF
VOUT = -10V
IOUT < 2A
LM104
Q1
2N2905
R2
2.4K
1%
Q2
2N3055
R4
68
C2†
4.7 µF
R3
0.2
VIN < -12V

†Solid Tantalum

TL/H/7754–4

### Switching Regulator


GND
R2
2.5K
1%
C2
100 pF
C1†
80 µF
R1
2.4K
1%
LM104
VOUT = -5V
IOUT < 3A
R6
10M
L1*
540 µH
R3
33
D1
1N3880
Q1
2N2219
R4
100
Q2
2N3716
R5
47
VIN < -8.5V

†Solid Tantalum

TL/H/7754–6

*60 turns #20 on Arnold Engineering A930157-2 Molybdenum Permalloy Core.

**National Semiconductor Corporation**

# LM105/LM205/LM305/LM305A, LM376 Voltage Regulators

## General Description

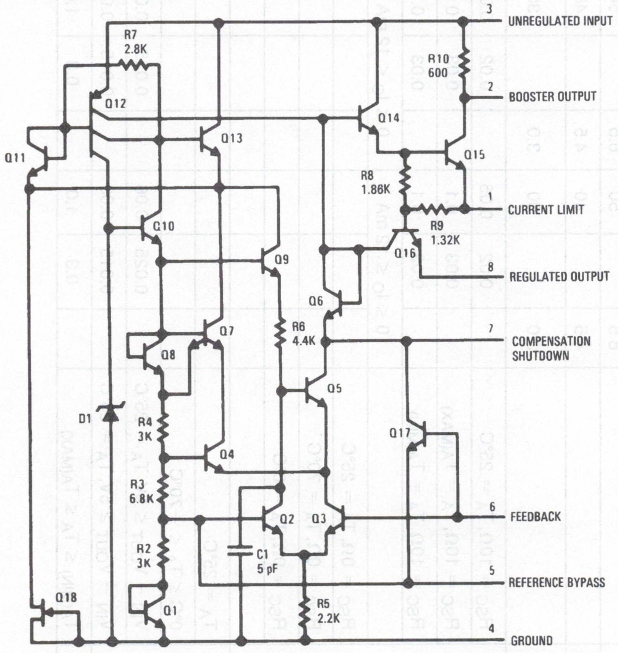
The LM105 series are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection on 0.01%V
- 45 mA output current without external pass transistor (LM305A)

Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in either an 8-lead, TO-5 header or a 1/4″ x 1/4″ metal flat package.

The LM105 is specified for operation for $-55°C \le T_A \le +125°C$, the LM205 is specified for $-25°C \le T_A \le +85°C$, and the LM305/LM305A, LM376 is specified for $0°C \le T_A \le +70°C$.

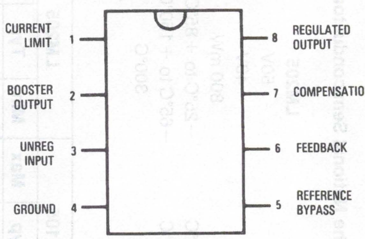
## Schematic and Connection Diagrams


R7
2.8K
Q12
Q11
Q13
Q14
R10
600
Q15
R8
1.86K
R9
1.32K
Q16
Q10
Q9
Q6
R6
4.4K
Q7
Q8
Q5
D1
R4
3K
Q17
Q4
R3
6.8K
Q2
Q3
C1
5 pF
R2
3K
R5
2.2K
Q18
Q1
3 UNREGULATED INPUT
2 BOOSTER OUTPUT
1 CURRENT LIMIT
8 REGULATED OUTPUT
7 COMPENSATION SHUTDOWN
6 FEEDBACK
5 REFERENCE BYPASS
4 GROUND

TL/H/7755–1

Pin connections shown are for metal can.

**Dual-In-Line Package**

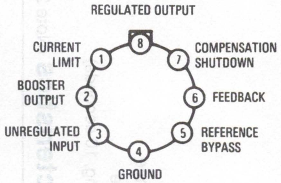

CURRENT LIMIT 1
BOOSTER OUTPUT 2
UNREG INPUT 3
GROUND 4
8 REGULATED OUTPUT
7 COMPENSATION
6 FEEDBACK
5 REFERENCE BYPASS

TL/H/7755–2

**Top View**

**Order Number LM376N**
**See NS Package Number N08E**

**Metal Can Package**


REGULATED OUTPUT
8
CURRENT LIMIT 1
BOOSTER OUTPUT 2
UNREGULATED INPUT 3
4
GROUND
7 COMPENSATION SHUTDOWN
6 FEEDBACK
5 REFERENCE BYPASS

TL/H/7755–3

**Top View**

**Order Number LM105H, LM205H, LM305H or LM305AH**
**See NS Package Number H08C**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)**

| | LM105 | LM205 | LM305 | LM305A | LM376 |
|---|---|---|---|---|---|
| Input Voltage | 50V | 50V | 40V | 50V | 40V |
| Input-Output Differential | 40V | 40V | 40V | 40V | 40V |
| Power Dissipation (Note 1) | 800 mW | 800 mW | 800 mW | 800 mW | 400 mW |
| Operating Temperature Range | −55°C to +125°C | −25°C to +85°C | −0°C to +70°C | 0°C to +70°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 300°C | 300°C | 300°C | 260°C |

## Electrical Characteristics (Note 2)

| Parameter | Conditions | LM105 | | | LM205 | | | LM305 | | | LM305A | | | LM376 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | | 8.5 | | 50 | 8.5 | | 50 | 8.5 | | 40 | 8.5 | | 50 | 9.0 | | 40 | V |
| Output Voltage Range | | 4.5 | | 40 | 4.5 | | 40 | 4.5 | | 30 | 4.5 | | 40 | 5.0 | | 37 | V |
| Input-Output Voltage Differential | | 3.0 | | 30 | 3.0 | | 30 | 3.0 | | 30 | 3.0 | | 30 | 3.0 | | 30 | V |
| Load Regulation (Note 3) | $R_{SC} = 10\Omega$, $T_A = 25°C$ | | 0.02 | 0.05 | | 0.02 | 0.05 | | 0.02 | 0.05 | | | | | | | % |
| | $R_{SC} = 10\Omega$, $T_A = T_{A(MAX)}$ | | 0.03 | 0.1 | | 0.03 | 0.1 | | 0.03 | 0.1 | | | | | | | % |
| | $R_{SC} = 10\Omega$, $T_A = T_{A(MIN)}$ | | 0.03 | 0.1 | | 0.03 | 0.1 | | 0.03 | 0.1 | | | | | | | % |
| | | $0 \leq I_O \leq 12$ mA | | | $0 \leq I_O \leq 12$ mA | | | $0 \leq I_O \leq 12$ mA | | | | | | | | | |
| | $R_{SC} = 0\Omega$, $T_A = 25°C$ | | | | | | | | | | | 0.02 | 0.2 | | | 0.2 | % |
| | $R_{SC} = 0\Omega$, $T_A = 70°C$ | | | | | | | | | | | 0.03 | 0.4 | | | 0.5 | % |
| | $R_{SC} = 0\Omega$, $T_A = 0°C$ | | | | | | | | | | | 0.03 | 0.4 | | | 0.5 | % |
| | | | | | | | | | | | $0 \leq I_O \leq 45$ mA | | | $0 \leq I_O \leq 25$ mA | | | |
| Line Regulation | $T_A = 25°C$ | | | | | | | | | | | | | | | 0.03 | %/V |
| | $0°C \leq T_A \leq +70°C$ | | | | | | | | | | | | | | | 0.1 | %/V |
| | $V_{IN} - V_{OUT} \leq 5V$, $T_A = 25°C$ | | 0.025 | 0.06 | | 0.025 | 0.06 | | 0.025 | 0.06 | | 0.025 | 0.06 | | | | %/V |
| | $V_{IN} - V_{OUT} \geq 5V$, $T_A = 25°C$ | | 0.015 | 0.03 | | 0.015 | 0.03 | | 0.015 | 0.03 | | 0.015 | 0.03 | | | | %/V |
| Temperature Stability | $T_{A(MIN)} \leq T_A \leq T_{A(MAX)}$ | | 0.3 | 1.0 | | 0.3 | 1.0 | | 0.3 | 1.0 | | 0.3 | 1.0 | | | | % |

## Electrical Characteristics (Note 2) (Continued)

| Parameter | Conditions | LM105 | | | LM205 | | | LM305 | | | LM305A | | | LM376 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Feedback Sense Voltage | | 1.63 | 1.7 | 1.81 | 1.63 | 1.7 | 1.81 | 1.63 | 1.7 | 1.81 | 1.55 | 1.7 | 1.85 | 1.60 | 1.72 | 1.80 | V |
| Output Noise Voltage | 10 Hz ≤ f ≤ 10 kHz | | | | | | | | | | | | | | | | |
| | $C_{REF} = 0$ | | 0.005 | | | 0.005 | | | 0.005 | | | 0.005 | | | | | % |
| | $C_{REF} = 0.1\ \mu F$ | | 0.002 | | | 0.002 | | | 0.002 | | | 0.002 | | | | | % |
| Standby Current Drain | $V_{IN} = 30V$, $T_A = 25°C$ | | | | | | | | | | | | | | | 2.5 | mA |
| | $V_{IN} = 40V$ | | | | | | | | 0.8 | 2.0 | | | | | | | mA |
| | $V_{IN} = 50V$ | | 0.8 | 2.0 | | 0.8 | 2.0 | | | | | 0.8 | 2.0 | | | | mA |
| Current Limit Sense Voltage | $T_A = 25°C$, $R_{SC} = 10\Omega$, $V_{OUT} = 0V$, (Note 4) | 225 | 300 | 375 | 225 | 300 | 375 | 225 | 300 | 375 | 225 | 300 | 375 | | 300 | | mV |
| Long Term Stability | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | | | % |
| Ripple Rejection | $C_{REF} = 10\ \mu F$, f = 120 Hz | | 0.003 | | | 0.003 | | | 0.003 | | | 0.003 | | | | | %/V |
| $\theta_{JA}$ | Epoxy Dual-In-Line Package | | | | | | | | | | | | | | 140 | | °C/W |
| $\theta_{JA}$ | TO-5 Board Mount in Still Air | | 230 | | | 230 | | | 230 | | | 230 | | | | | °C/W |
| $\theta_{JA}$ | TO-5 Board Mount in 400 LF/Min Air Flow | | 92 | | | 92 | | | 92 | | | 92 | | | | | °C/W |
| $\theta_{JC}$ | TO-5 | | 25 | | | 25 | | | 25 | | | 25 | | | | | °C/W |

**Note 1:** The maximum junction temperature of the LM105 and LM305A is 150°C, the LM205 and LM376 is 100°C, and the LM305 is 85°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 231°C/W junction to ambient, or 25°C/W junction to case. For the epoxy dual-in-line package, derating is based on a thermal resistance of 138°C/W junction to ambient. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power average over a five second interval for the LM105 and LM205, and averaged over a two second interval for the LM305.

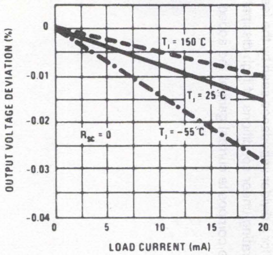
**Note 2:** Unless otherwise specified, these specifications apply for temperatures within the operating temperature range, for input and output voltages within the range given, and for a divider impedance seen by the feedback terminal of 2 kΩ. Load and line regulation specifications are for a constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

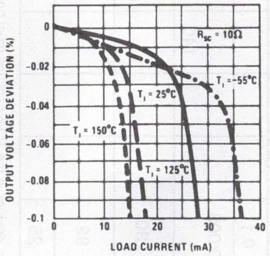
**Note 3:** The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

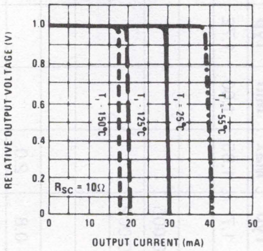
**Note 4:** With no external pass transistor.

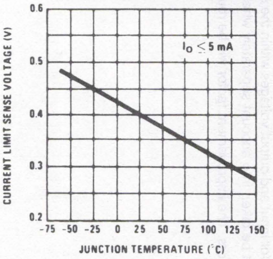
**Note 5:** Refer to RETS105X Drawing for military specifications for the LM105.

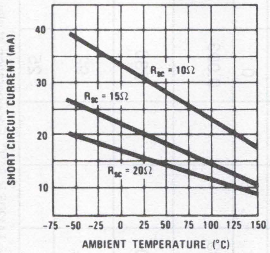
## Typical Performance Characteristics LM105/LM205/LM305/LM305A

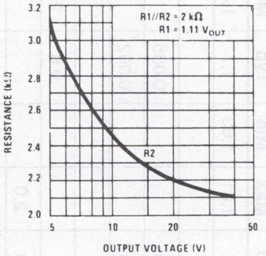

Load Regulation

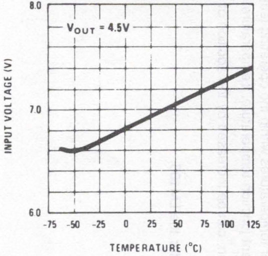

Load Regulation

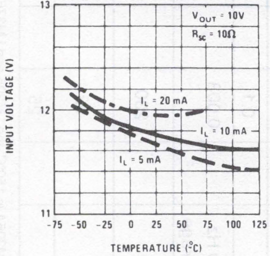

Current Limiting Characteristics

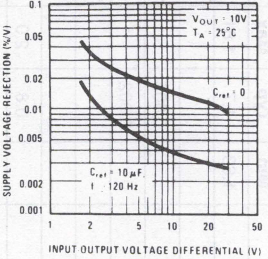

Current Limit Sense Voltage

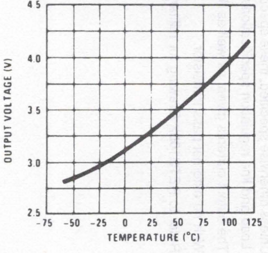

Short Circuit Current

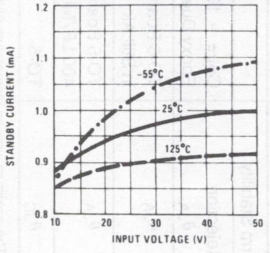

Optimum Divider Resistance Values

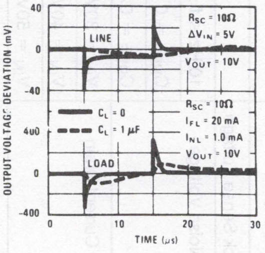

Minimum Input Voltage


Regulator Dropout Voltage


Supply Voltage Rejection


Minimum Output Voltage

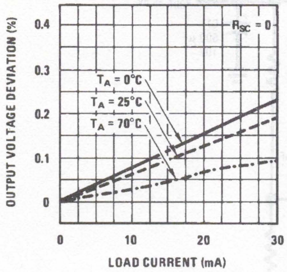

Standby Current Drain


Transient Response

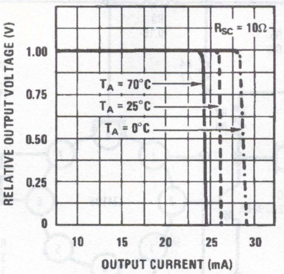
TL/H/7755–6

# Typical Performance Characteristics LM376

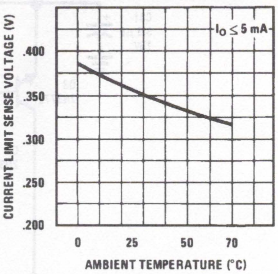
### Load Regulation



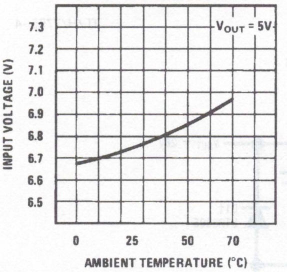
### Current Limiting Characteristics



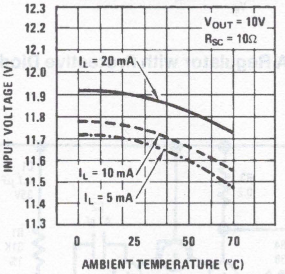
### Current Limiting Sense Voltage



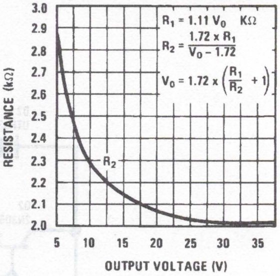
### Minimum Input Voltage



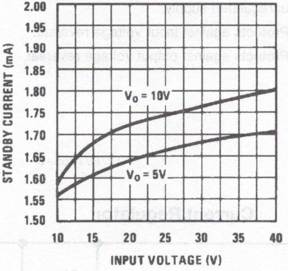
### Regulator Dropout Voltage



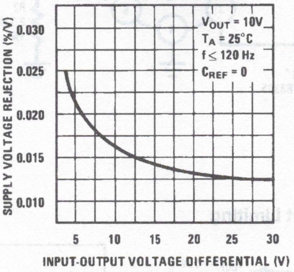
### Optimum Divider Resistance



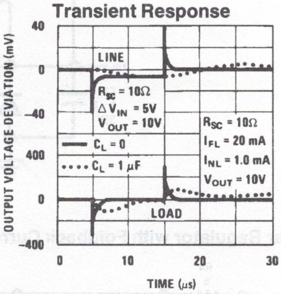
### Standby Current Drain $T_A = 25°C$



### Supply Voltage Rejection



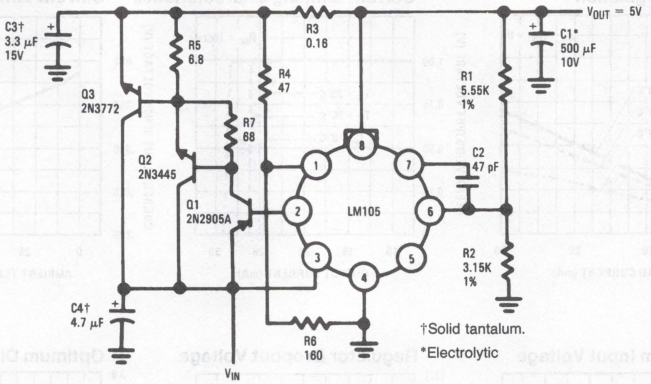
### Transient Response



TL/H/7755-7

## Typical Applications

### 10A Regulator with Foldback Current Limiting

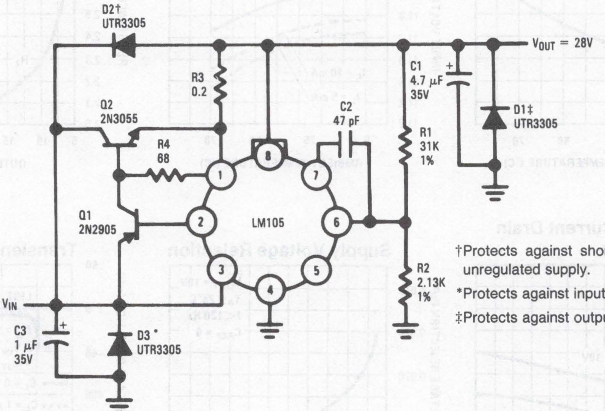

C3†
3.3 μF
15V
Q3
2N3772
R5
6.8
R4
47
R3
0.16
$V_{OUT}$ = 5V
C1*
500 μF
10V
R7
68
Q2
2N3445
Q1
2N2905A
LM105
1
2
3
4
5
6
7
8
R1
5.55K
1%
C2
47 pF
R2
3.15K
1%
C4†
4.7 μF
R6
160
$V_{IN}$

†Solid tantalum.

*Electrolytic

TL/H/7755-4

### 1.0A Regulator with Protective Diodes


D2†
UTR3305
$V_{OUT}$ = 28V
R3
0.2
Q2
2N3055
R4
68
C2
47 pF
C1
4.7 μF
35V
D1‡
UTR3305
R1
31K
1%
Q1
2N2905
LM105
1
2
3
4
5
6
7
8
R2
2.13K
1%
$V_{IN}$
C3
1 μF
35V
D3*
UTR3305

†Protects against shorted input or inductive leads on unregulated supply.

*Protects against input voltage reversal.

‡Protects against output voltage reversal.

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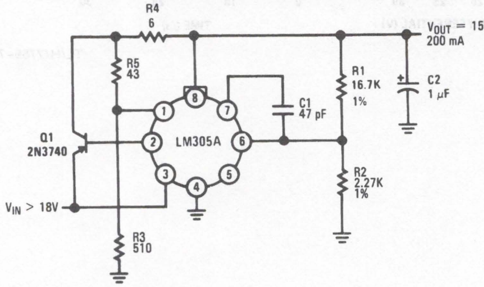
### Linear Regulator with Foldback Current Limiting


R4
6
$V_{OUT}$ = 15V
200 mA
R5
43
R1
16.7K
1%
C2
1 μF
C1
47 pF
Q1
2N3740
LM305A
1
2
3
4
5
6
7
8
$V_{IN}$ > 18V
R2
2.27K
1%
R3
510

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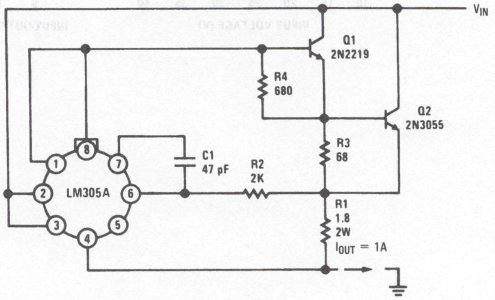
### Current Regulator


$V_{IN}$
Q1
2N2219
R4
680
Q2
2N3055
R3
68
C1
47 pF
R2
2K
LM305A
1
2
3
4
5
6
7
8
R1
1.8
2W
$I_{OUT}$ = 1A

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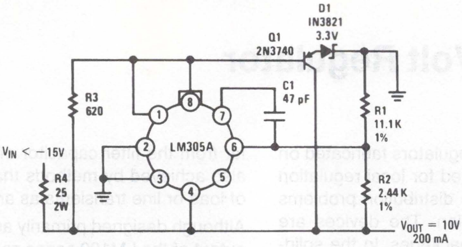
## Typical Applications (Continued)

### Shunt Regulator


D1
1N3821
3.3V
Q1
2N3740
C1
47 pF
R3
620
R1
11.1K
1%
LM305A
$V_{IN}$ < 15V
R4
25
2W
R2
2.44 K
1%
$V_{OUT}$ = 10V
200 mA
1
2
3
4
5
6
7
8

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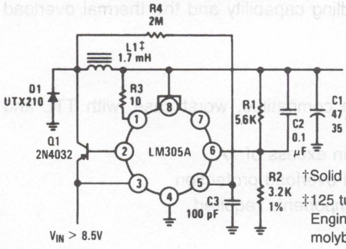
### Switching Regulator


R4
2M
L1‡
1.7 mH
$V_{OUT}$ = 5V
D1
UTX210
R3
10
R1
5.6K
C1
47 μF
35 V
C2
0.1
μF
Q1
2N4032
LM305A
R2
3.2K
1%
C3
100 pF
$V_{IN}$ > 8.5V
1
2
3
4
5
6
7
8

†Solid tantaium.

‡125 turns = 22 on Arnold Engineering A262123-2 molybdenum permally core.

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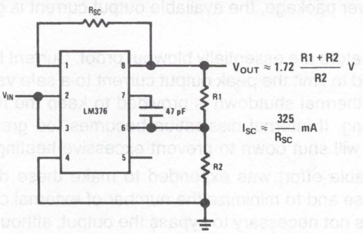
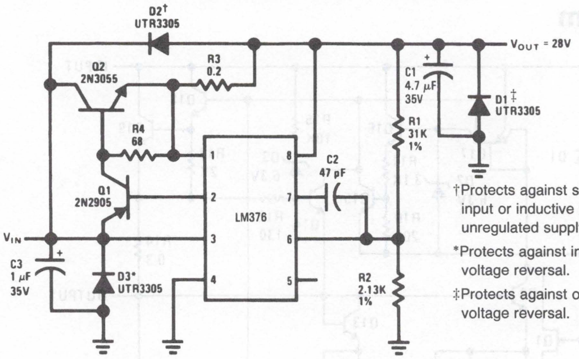
### Basic Positive Regulator with Current Limiting


$R_{SC}$
$V_{OUT} \approx 1.72 \frac{R1 + R2}{R2}$ V
$V_{IN}$
LM376
47 pF
R1
$I_{SC} \approx \frac{325}{R_{SC}}$ mA
R2
1
2
3
4
5
6
7
8

TL/H/7755-12

### 1.0A Regulator with Protective Diodes


D2†
UTR3305
$V_{OUT}$ = 28V
Q2
2N3055
R3
0.2
C1
4.7 μF
35V
D1‡
UTR3305
R4
68
R1
31K
1%
C2
47 pF
Q1
2N2905
LM376
$V_{IN}$
C3
1 μF
35V
D3*
UTR3305
R2
2.13K
1%
1
2
3
4
5
6
7
8

†Protects against shorted input or inductive loads on unregulated supply.

*Protects against input voltage reversal.

‡Protects against output voltage reversal.

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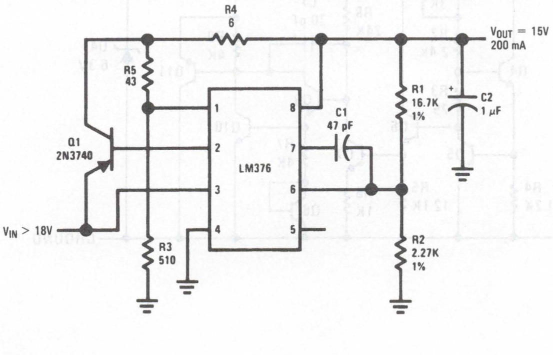
### Linear Regulator with Foldback Current Limiting


R4
6
$V_{OUT}$ = 15V
200 mA
R5
43
R1
16.7K
1%
C2
1 μF
Q1
2N3740
C1
47 pF
LM376
$V_{IN}$ > 18V
R3
510
R2
2.27K
1%
1
2
3
4
5
6
7
8

TL/H/7755-14

**National Semiconductor Corporation**

# LM109/LM309 5-Volt Regulator

## General Description

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

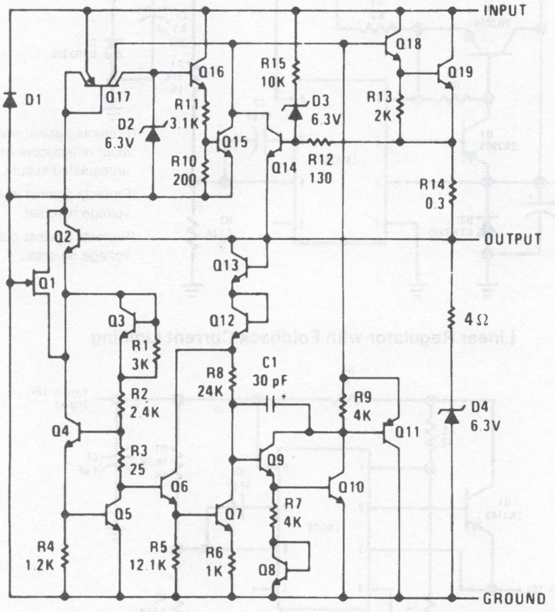
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

## Features

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

## Schematic Diagram



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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Input Voltage | 35V |
| Power Dissipation | Internally Limited |
| Operating Junction Temperature Range | |
| LM109 | −55°C to +150°C |
| LM309 | 0°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM109 | | | LM309 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_j = 25°C$ | 4.7 | 5.05 | 5.3 | 4.8 | 5.05 | 5.2 | V |
| Line Regulation | $T_j = 25°C$<br>$7.10V \le V_{IN} \le 25V$ | | 4.0 | 50 | | 4.0 | 50 | mV |
| Load Regulation | $T_j = 25°C$ | | | | | | | |
| TO-5 Package | $5\ mA \le I_{OUT} \le 0.5A$ | | 15 | 50 | | 15 | 50 | mV |
| TO-3 Package | $5\ mA \le I_{OUT} \le 1.5A$ | | 15 | 100 | | 15 | 100 | mV |
| Output Voltage | $7.40V \le V_{IN} \le 25V$,<br>$5\ mA \le I_{OUT} \le I_{MAX}$,<br>$P < P_{MAX}$ | 4.6 | | 5.4 | 4.75 | | 5.25 | V |
| Quiescent Current | $7.40V \le V_{IN} \le 25V$ | | 5.2 | 10 | | 5.2 | 10 | mA |
| Quiescent Current Change | $7.40V \le V_{IN} \le 25V$<br>$5\ mA \le I_{OUT} \le I_{MAX}$ | | | 0.5<br>0.8 | | | 0.5<br>0.8 | mA<br>mA |
| Output Noise Voltage | $T_A = 25°C$<br>$10\ Hz \le f \le 100\ kHz$ | | 40 | | | 40 | | μV |
| Long Term Stability | | | 10 | | | 20 | | mV |
| Ripple Rejection | $T_j = 25°C$ | 50 | | | 50 | | | dB |
| Thermal Resistance, Junction to Case | (Note 2) | | | | | | | |
| TO-5 Package | | | 15 | | | 15 | | °C/W |
| TO-3 Package | | | 2.5 | | | 2.5 | | °C/W |

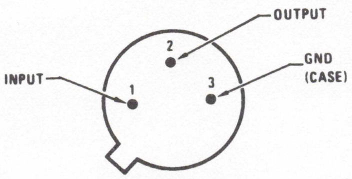
**Note 1:** Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM109 and $0°C \le T_j \le +125°C$ for the LM309; $V_{IN} = 10V$; and $I_{OUT} = 0.1A$ for the TO-39 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-39 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$.

**Note 2:** Without a heat sink, the thermal resistance of the TO-39 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

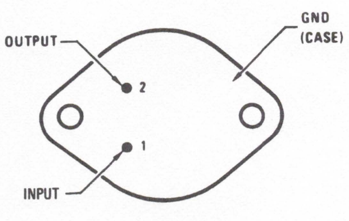
**Note 3:** Refer to RETS109H drawing for LM109H or RETS109K drawing for LM109K military specifications.

## Connection Diagrams

**Metal Can Packages**



**Order Number LM109H or LM309H**
**See NS Package Number H03A**



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**Order Number LM109K STEEL or LM309K STEEL**
**See NS Package Number K02A**

**Order Number LM309K (ALUMINUM)**
**See NS Package Number KC02A**

## Application Hints

**a. Bypass the input** of the LM109 to ground with ≥ 0.2 μF ceramic or solid tantalum capacitor if main filter capacitor is more than 4 inches away.

**b. Use steel package** instead of aluminum if more than 5,000 thermal cycles are expected. (ΔT ≥ 50°C)

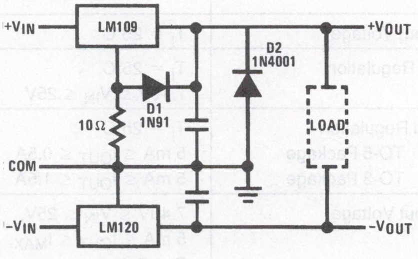
**c. Avoid insertion of regulator into "live" socket** if input voltage is greater than 10V. The output will rise to within 2V of the unregulated input if the ground pin does not make contact, possibly damaging the load. The LM109 may also be damaged if a large output capacitor is charged up, then discharged through the internal clamp zener when the ground pin makes contact.

**d. The output clamp zener** is designed to absorb transients only. It will not clamp the output effectively if a failure occurs in the internal power transistor structure. Zener dynamic impedance is ≈ 4Ω. Continuous RMS current into the zener should not exceed 0.5A.

**e. Paralleling of LM109s** for higher output current is not recommended. Current sharing will be almost nonexistent, leading to a current limit mode operation for devices with the highest initial output voltage. The current limit devices may also heat up to the thermal shutdown point (≈ 175°C). Long term reliability cannot be guaranteed under these conditions.

**f. Preventing latchoff** for loads connected to negative voltage:

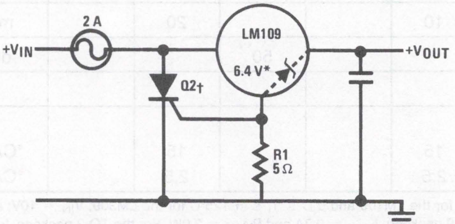
If the output of the LM109 is pulled negative by a high current supply so that the output pin is more than 0.5V negative with respect to the ground pin, the LM109 can latch off. This can be prevented by clamping the ground pin to the output pin with a germanium or Schottky diode as shown. A silicon diode (1N4001) at the output is also needed to keep the positive output from being pulled too far negative. The 10Ω resistor will raise $+V_{OUT}$ by ≈ 0.05V.



TL/H/7138-7

## Crowbar Overvoltage Protection

### Input Crowbar



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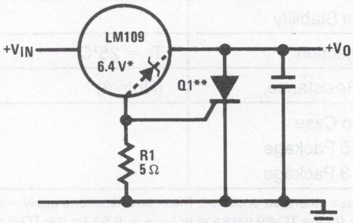
### Output Crowbar



TL/H/7138-9

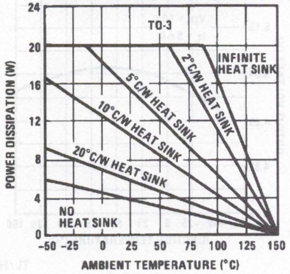
*Zener is internal to LM109.

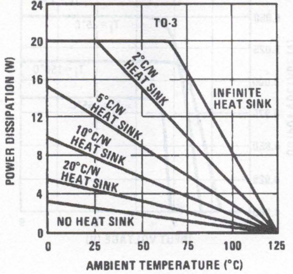
**Q1 must be able to withstand 7A continuous current if fusing is not used at regulator input. LM109 bond wires will fuse at currents above 7A.

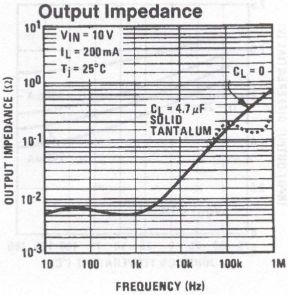
†Q2 is selected for surge capability. Consideration must be given to filter capacitor size, transformer impedance, and fuse blowing time.

††Trip point is ≈ 7.5V.

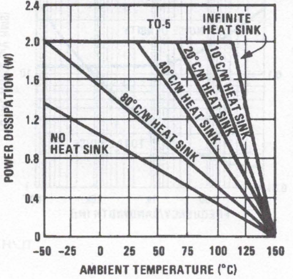
## Typical Performance Characteristics

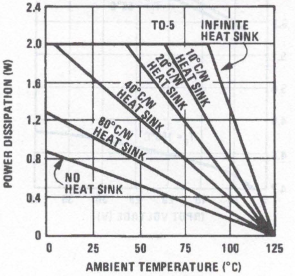

Maximum Average Power Dissipation (LM109K)

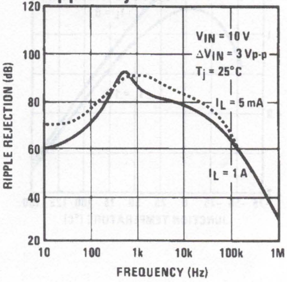

Maximum Average Power Dissipation (LM309K)


Output Impedance

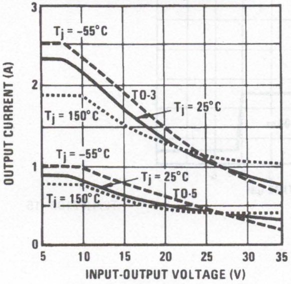
TL/H/7138-10

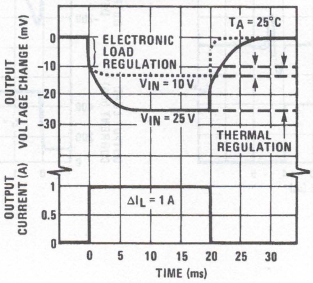

Maximum Average Power Dissipation (LM109H)

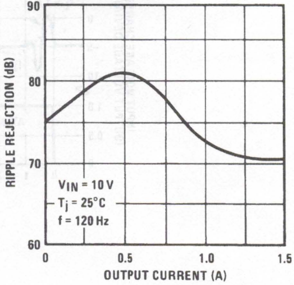

Maximum Average Power Dissipation (LM309H)


Ripple Rejection

TL/H/7138-11


Current Limit Characteristics (Note 1)


Thermally Induced Output Voltage Variation


Ripple Rejection

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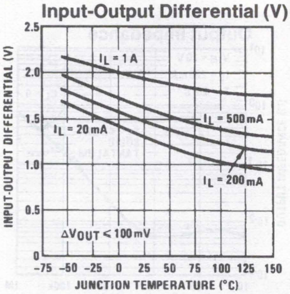
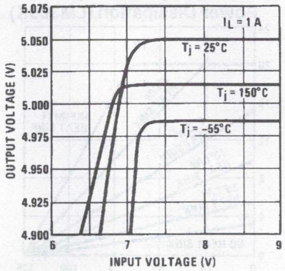
**Note 1:** Current limiting foldback characteristics are determined by input output differential, not by output voltage.

## Typical Performance Characteristics (Continued)

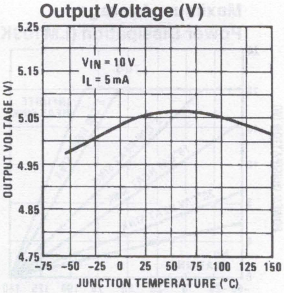
Input-Output Differential (V)



Output Voltage (V)

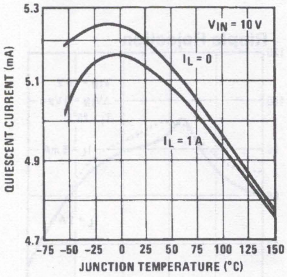


Output Voltage (V)

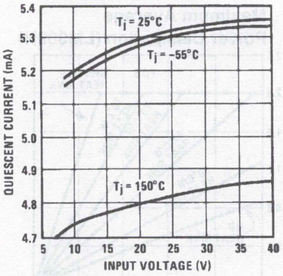


TL/H/7138–13

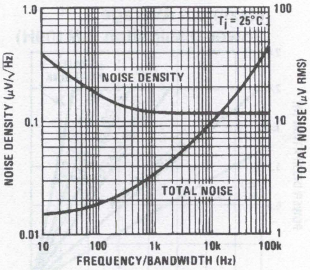
Quiescent Current



Quiescent Current

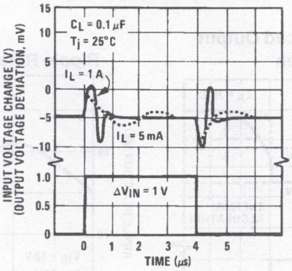


Output Voltage Noise

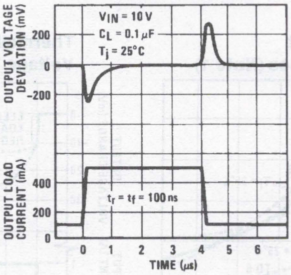


TL/H/7138–14

Line Transient Response



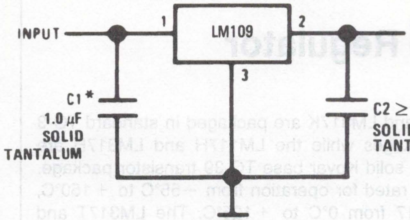
Load Transient Response



TL/H/7138–15

## Typical Applications

### Fixed 5V Regulator


INPUT
1
LM109
2
OUTPUT
5V
3
C1*
1.0 µF
SOLID
TANTALUM
C2 ≥ 1.0µF†
SOLID
TANTALUM

TL/H/7138-2

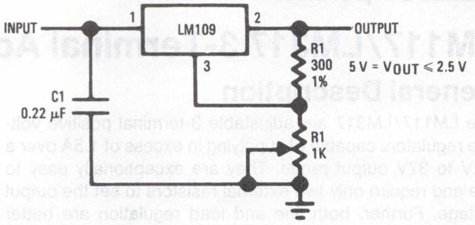
*Required if regulator is located more than 4″ from power supply filter capacitor.

†Although no output capacitor is needed for stability, it does improve transient response.

C2 should be used whenever long wires are used to connect to the load, or when transient response is critical.

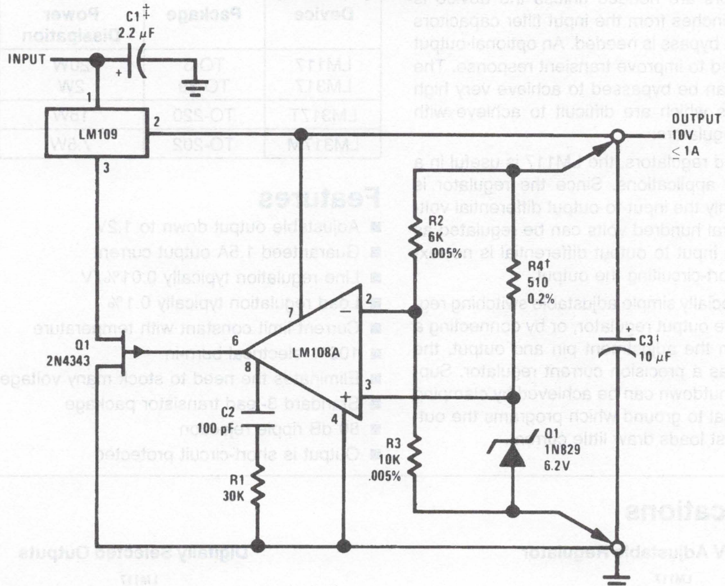
**Note:** Pin 3 electrically connected to case.

### Adjustable Output Regulator


INPUT
1
LM109
2
OUTPUT
3
R1
300
1%
5 V = VOUT ≤ 2.5 V
C1
0.22 µF
R1
1K

TL/H/7138-4

### High Stability Regulator*


C1‡
2.2 µF
INPUT
+
1
LM109
2
3
OUTPUT
10V
≤1A
R2
6K
.005%
R4†
510
0.2%
2
7
−
6
8
LM108A
Q1
2N4343
+
3
4
C2
100 pF
R1
30K
R3
10K
.005%
C3†
10 µF
+
Q1
1N829
6.2V

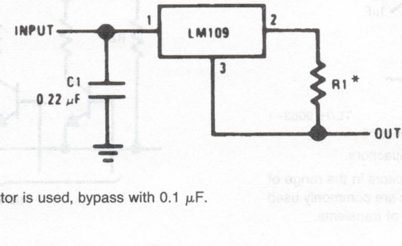
TL/H/7138-5

*Regulation better than 0.01%, load, line and temperature, can be obtained.

†Determines zener current. May be adjusted to minimize thermal drift.

‡Solid tantalum.

### Current Regulator


INPUT
1
LM109
2
3
R1*
C1
0.22 µF
OUTPUT

TL/H/7138-6

*Determines output current. If wirewound resistor is used, bypass with 0.1 µF.

National Semiconductor Corporation

# LM117/LM317 3-Terminal Adjustable Regulator

## General Description

The LM117/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K and LM317K are packaged in standard TO-3 transistor packages while the LM117H and LM317H are packaged in a solid Kovar base TO-39 transistor package. The LM117 is rated for operation from −55°C to +150°C, and the LM317 from 0°C to +125°C. The LM317T and LM317MP, rated for operation over a 0°C to +125°C range, are available in a TO-220 plastic package and a TO-202 package, respectively.

For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

**LM117 Series Packages and Power Capability**

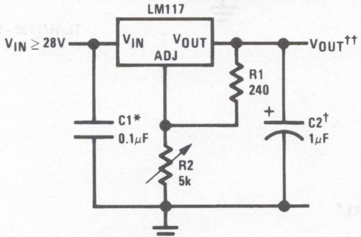
| Device | Package | Rated Power Dissipation | Design Load Current |
|---|---|---|---|
| LM117<br>LM317 | TO-3<br>TO-39 | 20W<br>2W | 1.5A<br>0.5A |
| LM317T | TO-220 | 15W | 1.5A |
| LM317M | TO-202 | 7.5W | 0.5A |

## Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected

## Typical Applications

### 1.2V–25V Adjustable Regulator



TL/H/9063-1

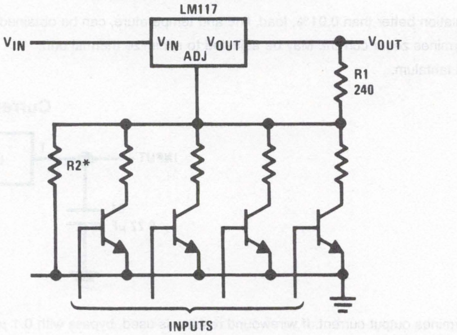
Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$††V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

### Digitally Selected Outputs



TL/H/9063-2

*Sets maximum $V_{OUT}$

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Power Dissipation | Internally limited |
| Input—Output Voltage Differential | +40V, −0.3V |
| Operating Junction Temperature Range | |
| LM117 | −55°C to +150°C |
| LM317 | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering) | |
| Metal Package | 300°C, 10 seconds |
| Plastic Package | 260°C, 4 seconds |
| ESD rating | 2k Volts |

## Preconditioning

| | |
|---|---|
| Burn-In in Thermal Limit | 100% All Devices |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM117 | | | LM317 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_j = 25°C$, $3V \le (V_{IN} - V_{OUT}) \le 40V$ (Note 2), $I_L = 10$ mA | | 0.01 | 0.02 | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_J = 25°C$, $10\text{ mA} \le I_{OUT} \le I_{MAX}$ | | 0.1 | 0.3 | | 0.1 | 0.5 | % |
| Thermal Regulation | $T_J = 25°C$, 20 ms Pulse | | 0.03 | 0.07 | | 0.04 | 0.07 | %/W |
| Adjustment Pin Current | | | 50 | 100 | | 50 | 100 | μA |
| Adjustment Pin Current Change | $10\text{ mA} \le I_L \le I_{MAX}$<br>$3V \le (V_{IN} - V_{OUT}) \le 40V$ | | 0.2 | 5 | | 0.2 | 5 | μA |
| Reference Voltage | $3V \le (V_{IN} - V_{OUT}) \le 40V$, (Note 3)<br>$10\text{ mA} \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation | $3V \le (V_{IN} - V_{OUT}) \le 40V$, (Note 2) | | 0.02 | 0.05 | | 0.02 | 0.07 | %/V |
| Load Regulation | $10\text{ mA} \le I_{OUT} \le I_{MAX}$ (Note 2) $I_L = 10$ mA | | 0.3 | 1 | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \le T_j \le T_{MAX}$ | | 1 | | | 1 | | % |
| Minimum Load Current | $(V_{IN} - V_{OUT}) = 40V$ | | 3.5 | 5 | | 3.5 | 10 | mA |
| Current Limit | $(V_{IN} - V_{OUT}) \le 15V$ | | | | | | | |
| | K and T Package | 1.5 | 2.2 | 3.4 | 1.5 | 2.2 | 3.4 | A |
| | H and P Package | 0.5 | 0.8 | 1.8 | 0.5 | 0.8 | 1.8 | A |
| | $(V_{IN} - V_{OUT}) = 40V$, $T_j = +25°C$ | | | | | | | |
| | K and T Package | 0.30 | 0.4 | | 0.15 | 0.4 | | A |
| | H and P Package | 0.15 | 0.07 | | 0.075 | 0.07 | | A |
| RMS Output Noise, % of $V_{OUT}$ | $T_J = 25°C$, $10\text{ Hz} \le f \le 10\text{ kHz}$ | | 0.003 | | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = 10V$, $f = 120$ Hz | | 65 | | | 65 | | dB |
| | $C_{ADJ} = 10\ \mu F$ | 66 | 80 | | 66 | 80 | | dB |
| Long-Term Stability | $T_J = 125°C$ | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | H Package | | 12 | 15 | | 12 | 15 | °C/W |
| | K Package | | 2.3 | 3 | | 2.3 | 3 | °C/W |
| | T Package | | | | | 4 | | °C/W |
| | P Package | | | | | 7 | | °C/W |
| Thermal Resistance, Junction to Ambient (No heat sink) | H Package | | 140 | | | 140 | | °C/W |
| | K Package | | 35 | | | 35 | | °C/W |
| | T Package | | | | | 50 | | °C/W |
| | P Package | | | | | 80 | | °C/W |

**Note 1:** Unless otherwise specified, these specifications apply: $-55°C \le T_j \le +150°C$ for the LM117, and $0°C \le T_J \le +125°C$ for the LM317; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202, and 20W for the TO-3 and TO-220. $I_{MAX}$ is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39 and TO-202 packages.

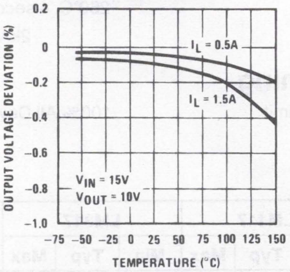
**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

**Note 3:** Refer to RETS117H drawing for LM117H or RETS117K drawing for LM117K military specifications.

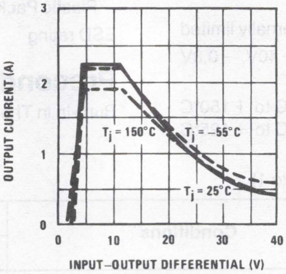
## Typical Performance Characteristics (K and T Packages)

Output Capacitor = 0 unless otherwise noted

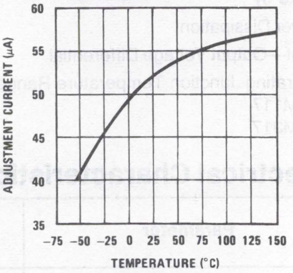
### Load Regulation



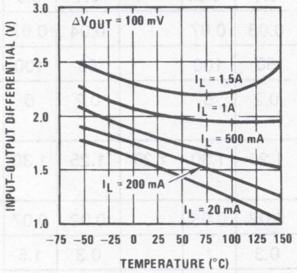
### Current Limit



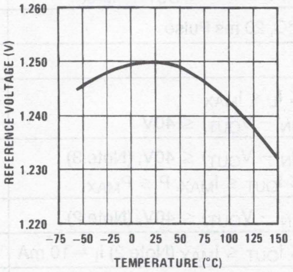
### Adjustment Current



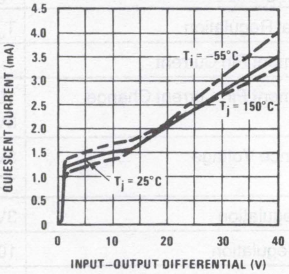
### Dropout Voltage



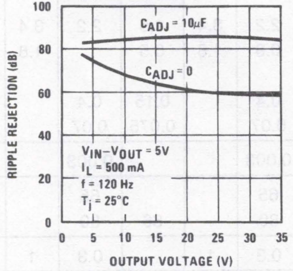
### Temperature Stability



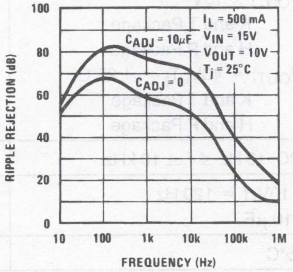
### Minimum Operating Current



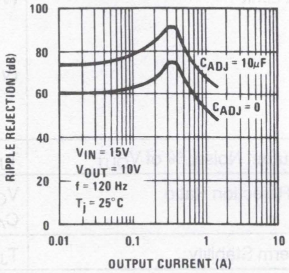
### Ripple Rejection



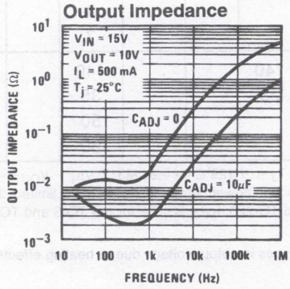
### Ripple Rejection



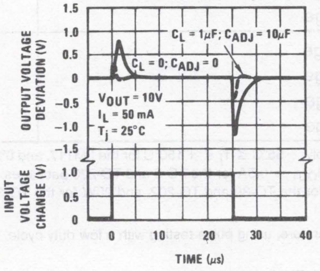
### Ripple Rejection



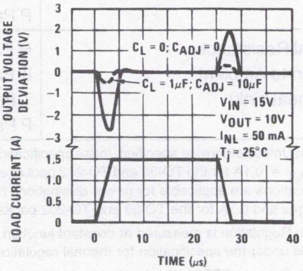
### Output Impedance



### Line Transient Response



### Load Transient Response

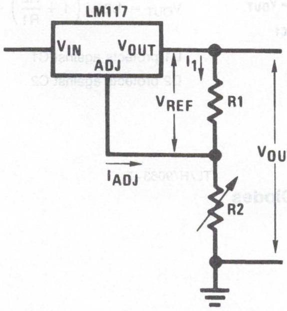


TL/H/9063–4

## Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, $V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9063–5

**FIGURE 1**

Since the 100 $\mu$A current from the adjustment terminal represents an error term, the LM117 was designed to minimize $I_{ADJ}$ and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

### External Capacitors

An input bypass capacitor is recommended. A 0.1 $\mu$F disc or 1 $\mu$F solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 $\mu$F bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 $\mu$F do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

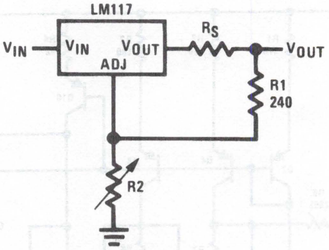
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 $\mu$F in aluminum electrolytic to equal 1 $\mu$F solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 $\mu$F disc may seem to work better than a 0.1 $\mu$F disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 $\mu$F solid tantalum (or 25 $\mu$F aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 $\mu$F will merely improve the loop stability and output impedance.

### Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × $I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

*Figure 2* shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9063–6

**FIGURE 2. Regulator with Line Resistance in Output Lead**

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

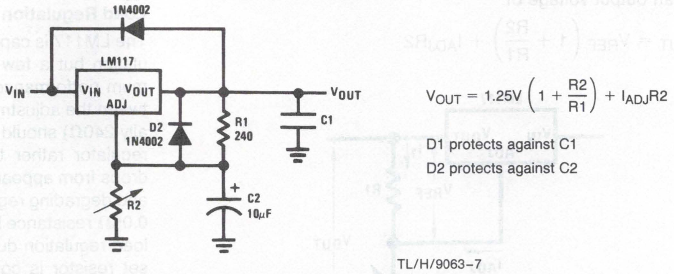
### Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 $\mu$F capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{IN}$. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 $\mu$F or less, there is no need to use diodes.

## Application Hints (Continued)

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.


D1
1N4002
LM117
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
D2
1N4002
R1
240
R2
C1
C2
10μF
$V_{OUT}$
TL/H/9063-7

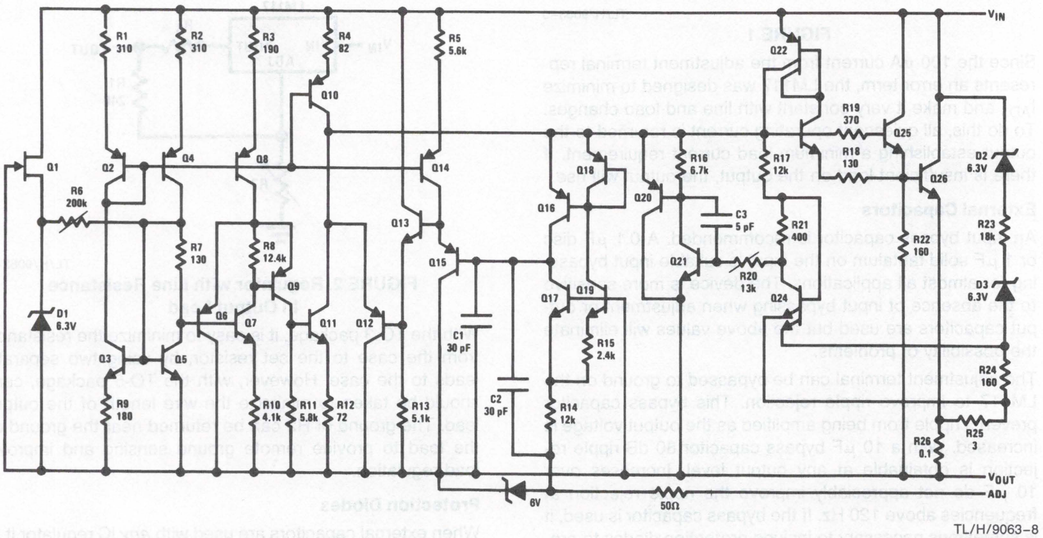
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1

D2 protects against C2

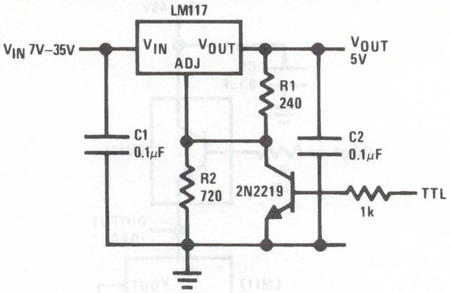
**FIGURE 3. Regulator with Protection Diodes**

## Schematic Diagram


$V_{IN}$
R1 310
R2 310
R3 190
R4 82
R5 5.6k
Q10
Q1
Q2
Q4
Q8
Q14
R6 200k
R7 130
R8 12.4k
Q13
Q15
Q9
D1 6.3V
Q6
Q7
Q11
Q12
C1 30 pF
Q3
Q5
R9 180
R10 4.1k
R11 5.8k
R12 72
R13 5.1k
C2 30 pF
Q22
R19 370
Q25
R18 130
Q18
R16 6.7k
R17 12k
D2 6.3V
Q20
Q26
Q16
C3 5 pF
R21 400
R23 18k
Q21
R22 160
R20 13k
Q17
Q19
Q24
D3 6.3V
R15 2.4k
R14 12k
R24 160
R25 3
R26 0.1
6V
50Ω
$V_{OUT}$
ADJ
TL/H/9063-8

## Typical Applications (Continued)

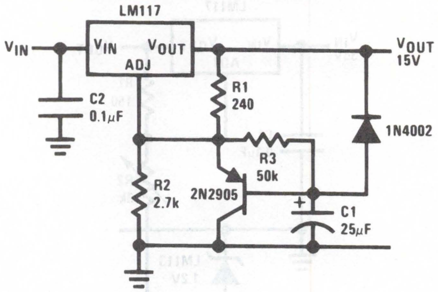
### 5V Logic Regulator with Electronic Shutdown*


LM117
VIN 7V–35V
VIN
VOUT
ADJ
VOUT
5V
R1
240
C1
0.1μF
C2
0.1μF
R2
720
2N2219
TTL
1k

*Min. output ≈ 1.2V

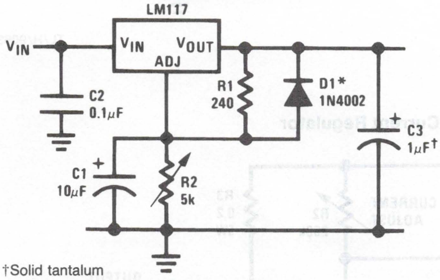
TL/H/9063–3

### Slow Turn-On 15V Regulator


LM117
VIN
VIN
VOUT
ADJ
VOUT
15V
C2
0.1μF
R1
240
1N4002
R3
50k
R2
2.7k
2N2905
C1
25μF

TL/H/9063–9

### Adjustable Regulator with Improved Ripple Rejection

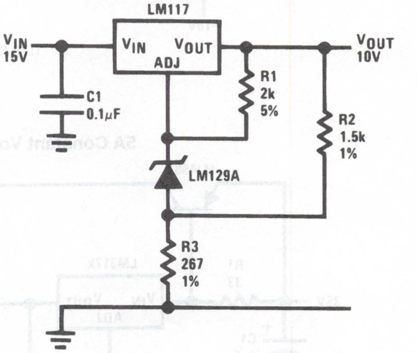

LM117
VIN
VIN
VOUT
ADJ
C2
0.1μF
R1
240
D1*
1N4002
C3
1μF†
C1
10μF
R2
5k

†Solid tantalum

*Discharges C1 if output is shorted to ground

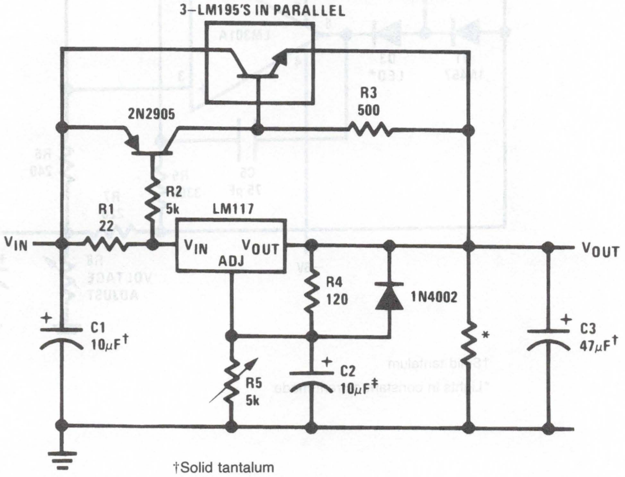
TL/H/9063–10

### High Stability 10V Regulator


LM117
VIN
15V
VIN
VOUT
ADJ
VOUT
10V
C1
0.1μF
R1
2k
5%
R2
1.5k
1%
LM129A
R3
267
1%

TL/H/9063–11

### High Current Adjustable Regulator


3–LM195'S IN PARALLEL
2N2905
R3
500
R2
5k
R1
22
LM117
VIN
VIN
VOUT
ADJ
VOUT
R4
120
1N4002
C1
10μF†
*
C3
47μF†
R5
5k
C2
10μF‡

†Solid tantalum

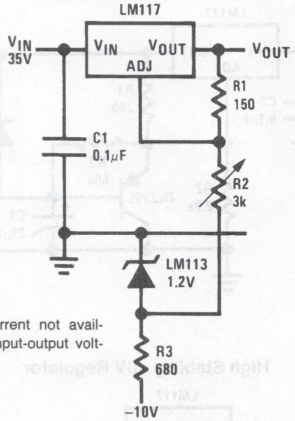
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

TL/H/9063–12

## Typical Applications (Continued)

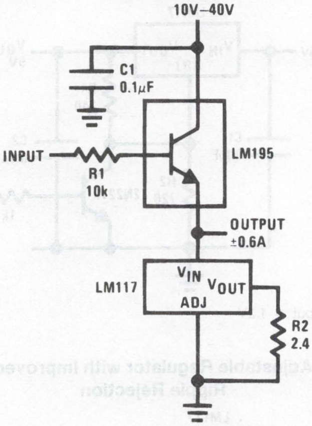
### 0 to 30V Regulator


LM117
$V_{IN}$ 35V
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R1 150
C1 0.1μF
R2 3k
LM113 1.2V
R3 680
−10V

Full output current not available at high input-output voltages

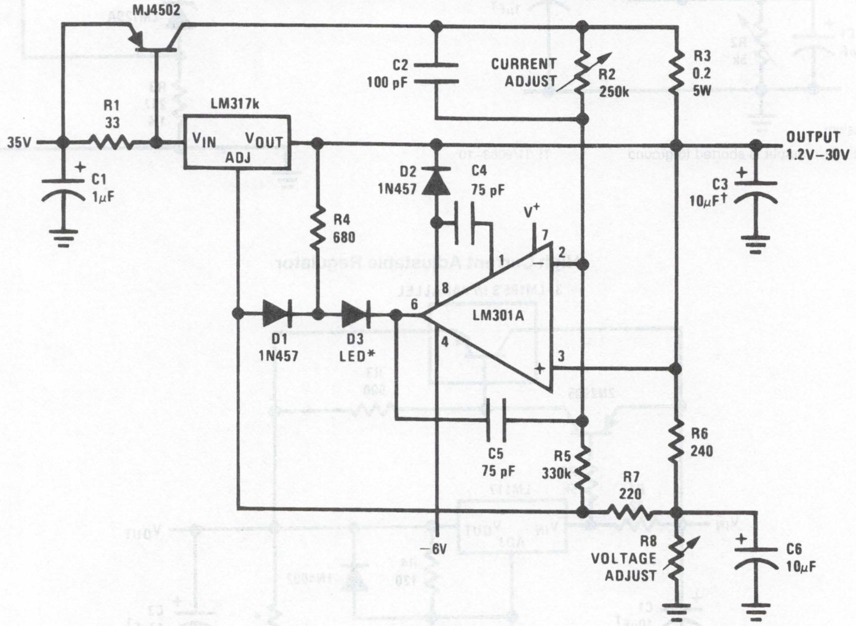
TL/H/9063-13

### Power Follower


10V–40V
C1 0.1μF
INPUT
R1 10k
LM195
OUTPUT ±0.6A
LM117
$V_{IN}$
$V_{OUT}$
ADJ
R2 2.4

TL/H/9063-14

### 5A Constant Voltage/Constant Current Regulator


MJ4502
R1 33
LM317k
35V
$V_{IN}$
$V_{OUT}$
ADJ
C1 1μF
C2 100 pF
CURRENT ADJUST
R2 250k
R3 0.2 5W
OUTPUT 1.2V–30V
C3 10μF†
D2 1N457
C4 75 pF
V+
7
2
R4 680
8
6
LM301A
4
3
D1 1N457
D3 LED*
C5 75 pF
R5 330k
R6 240
R7 220
−6V
R8 VOLTAGE ADJUST
C6 10μF

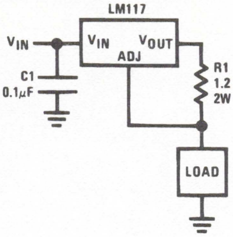
†Solid tantalum

*Lights in constant current mode

TL/H/9063-15

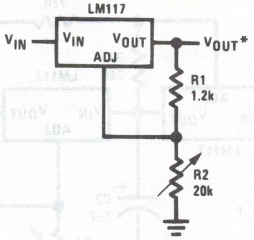
## Typical Applications (Continued)

### 1A Current Regulator


LM117
VIN
VIN
VOUT
ADJ
C1
0.1μF
R1
1.2
2W
LOAD

TL/H/9063-16

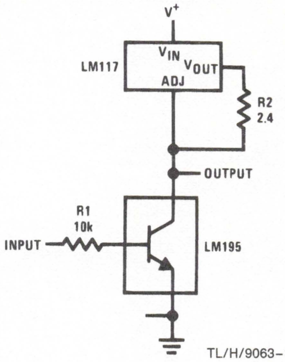
### 1.2V–20V Regulator with Minimum Program Current


LM117
VIN
VIN
VOUT
ADJ
VOUT*
R1
1.2k
R2
20k

TL/H/9063-17

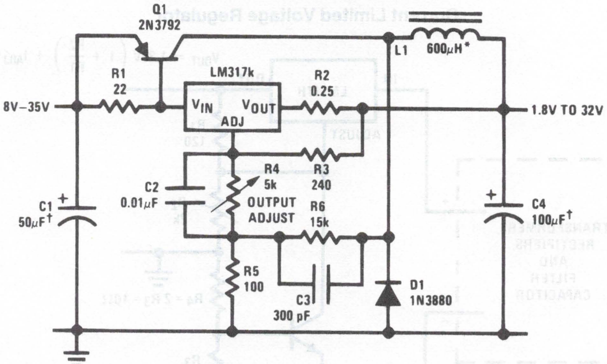
*Minimum load current ≈ 4 mA

### High Gain Amplifier


V+
LM117
VIN
VOUT
ADJ
R2
2.4
OUTPUT
R1
10k
INPUT
LM195

TL/H/9063-18

### Low Cost 3A Switching Regulator

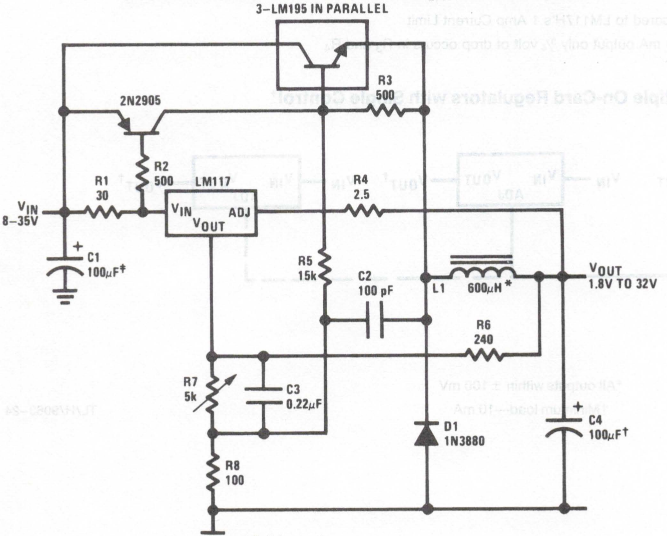

Q1
2N3792
L1
600μH*
R1
22
LM317k
R2
0.25
8V–35V
VIN
VOUT
ADJ
1.8V TO 32V
R3
240
C2
0.01μF
R4
5k
OUTPUT ADJUST
R6
15k
C1
50μF†
C4
100μF†
R5
100
C3
300 pF
D1
1N3880

†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063-19

### 4A Switching Regulator with Overload Protection

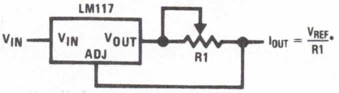

3-LM195 IN PARALLEL
R3
500
2N2905
R2
500
R1
30
LM117
R4
2.5
VIN
8–35V
VIN
VOUT
ADJ
C1
100μF‡
R5
15k
C2
100 pF
L1
600μH*
VOUT
1.8V TO 32V
R6
240
R7
5k
C3
0.22μF
D1
1N3880
C4
100μF†
R8
100

†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063-20

### Precision Current Limiter

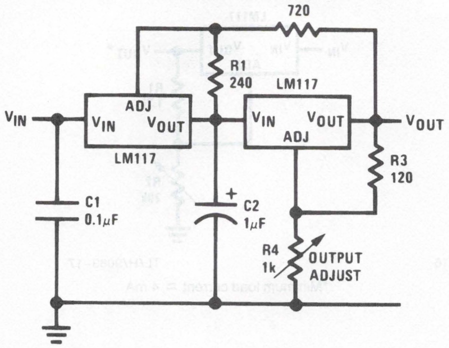

LM117
VIN
VIN
VOUT
ADJ
R1
$I_{OUT} = \frac{V_{REF}}{R1}$*

*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9063-21

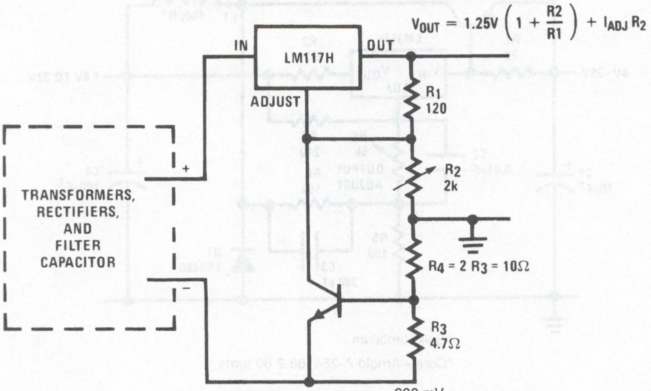
## Typical Applications (Continued)

### Tracking Preregulator


R2
720
R1
240
LM117
ADJ
$V_{IN}$
$V_{IN}$
$V_{OUT}$
LM117
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R3
120
C1
0.1μF
C2
1μF
R4
1k
OUTPUT
ADJUST

TL/H/9063-22

### Current Limited Voltage Regulator


IN
LM117H
OUT
ADJUST
$R_1$
120
$R_2$
2k
TRANSFORMERS,
RECTIFIERS,
AND
FILTER
CAPACITOR
+
−
$R_4 = 2\ R_3 = 10\Omega$
$R_3$
4.7Ω

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R_2$$

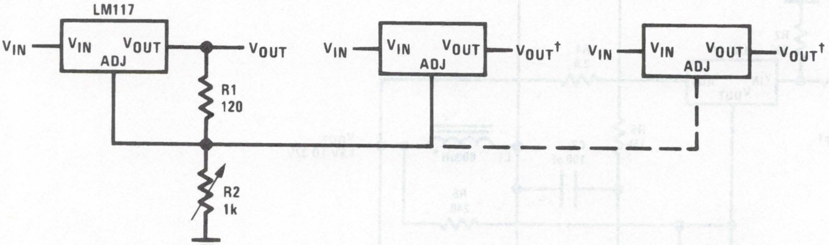
TL/H/9063-23

–Short circuit current is approximately $\frac{600\text{ mV}}{R3}$, or 120 mA

(Compared to LM117H's 1 Amp Current Limit

–(At 50 mA output only ¾ volt of drop occurs in $R_3$ and $R_4$

### Adjusting Multiple On-Card Regulators with Single Control*


LM117
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R1
120
R2
1k
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†

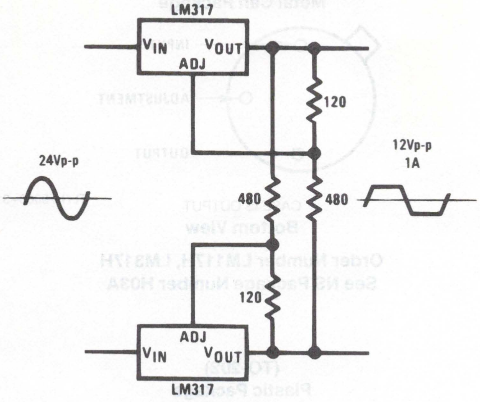
*All outputs within ± 100 mV

†Minimum load—10 mA

TL/H/9063-24

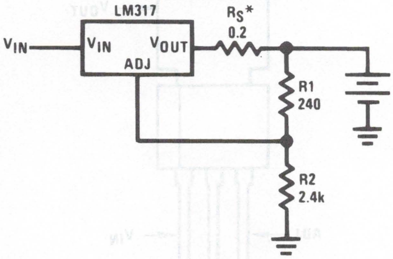
## Typical Applications (Continued)

### AC Voltage Regulator


LM317
VIN
VOUT
ADJ
120
24Vp-p
12Vp-p
1A
480
480
120
ADJ
VIN
VOUT
LM317

TL/H/9063-25

### 12V Battery Charger

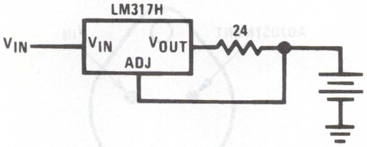

LM317
RS*
0.2
VIN
VIN
VOUT
ADJ
R1
240
R2
2.4k

TL/H/9063-26

*$R_S$—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

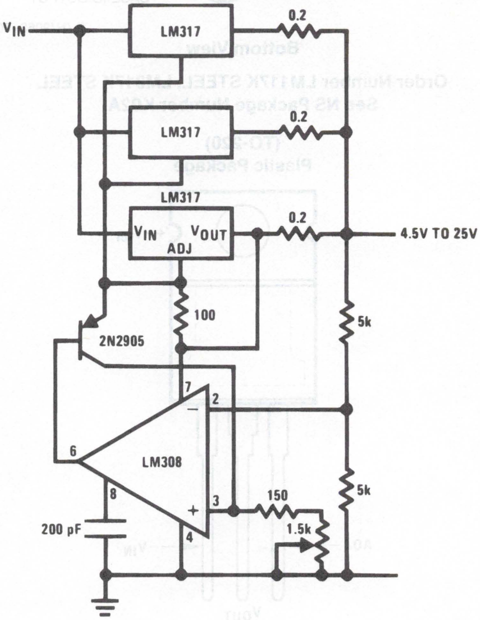
Use of $R_S$ allows low charging rates with fully charged battery.

### 50 mA Constant Current Battery Charger


LM317H
VIN
VIN
VOUT
ADJ
24

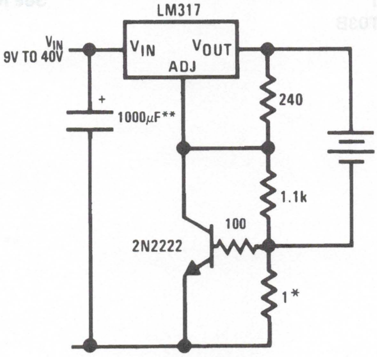
TL/H/9063-27

### Adjustable 4A Regulator


VIN
LM317
0.2
LM317
0.2
LM317
VIN
VOUT
ADJ
0.2
4.5V TO 25V
100
2N2905
5k
7
2
6
LM308
8
3
150
5k
200 pF
4
1.5k

TL/H/9063-28

### Current Limited 6V Charger


LM317
VIN
9V TO 40V
VIN
VOUT
ADJ
+
1000μF**
240
1.1k
100
2N2222
1*

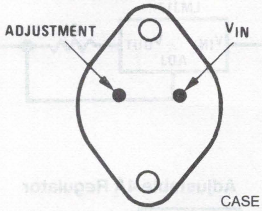
*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

TL/H/9063-29

## Connection Diagrams (See Physical Dimension section for further information)

**(TO-3 Steel)**
**Metal Can Package**


ADJUSTMENT
$V_{IN}$

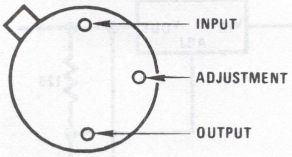
CASE IS OUTPUT

TL/H/9063-30

**Bottom View**

**Order Number LM117K STEEL, LM317K STEEL**
**See NS Package Number K02A**

**(TO-39)**
**Metal Can Package**


INPUT
ADJUSTMENT
OUTPUT

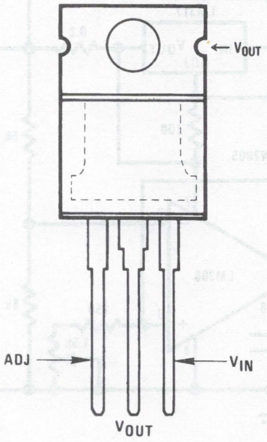
CASE IS OUTPUT

TL/H/9063-31

**Bottom View**

**Order Number LM117H, LM317H**
**See NS Package Number H03A**

**(TO-220)**
**Plastic Package**

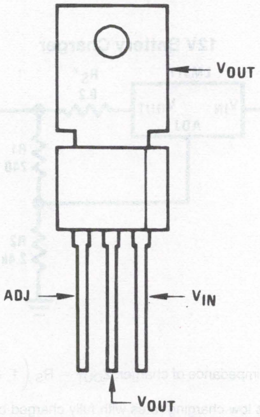

$V_{OUT}$
ADJ
$V_{IN}$
$V_{OUT}$

TL/H/9063-32

**Front View**

**Order Number LM317T**
**See NS Package Number T03B**

**(TO-202)**
**Plastic Package**


$V_{OUT}$
ADJ
$V_{IN}$
$V_{OUT}$

TL/H/9063-33

**Front View**

**Order Number LM317MP**
**See NS Package Number P03A**

**National Semiconductor Corporation**

# LM117HV/LM317HV 3-Terminal Adjustable Regulator

## General Description

The LM117HV/LM317HV are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 57V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117HV is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117HV series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117HV is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e. do not short the output to ground.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117HV can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

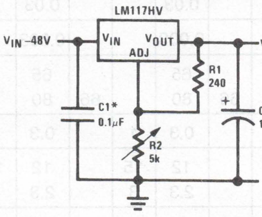
The LM117HVK STEEL, and LM317HVK STEEL are packaged in standard TO-3 transistor packages while the LM117HVH, and LM317HVH are packaged in a solid Kovar base TO-39 transistor package. The LM117HV is rated for operation from −55°C to +150°C, and the LM317HV from 0°C to +125°C.

## Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected

## Typical Applications

### 1.2V–45V Adjustable Regulator



TL/H/9062-1

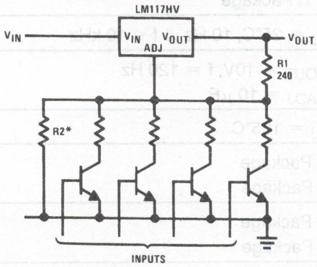
Full output current not available at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25\text{V}\left(1 + \frac{R2}{R1}\right) + I_{ADJ} R_2$$

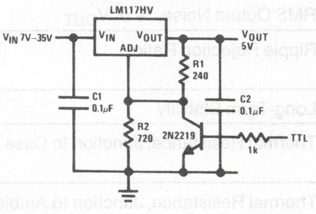
### Digitally Selected Outputs



TL/H/9062-2

*Sets maximum $V_{OUT}$

### 5V Logic Regulator with Electronic Shutdown*



TL/H/9062-3

*Min. output ≈ 1.2V

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 3)**

| | |
|---|---|
| Power Dissipation | Internally limited |
| Input—Output Voltage Differential | +60V, −0.3V |
| Operating Junction Temperature Range | |
| LM117HV | −55°C to +150°C |
| LM317HV | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| Preconditioning Burn-In in Thermal Limit | 100% All Devices |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM117HV | | | LM317HV | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_J = 25°C, 3V \le V_{IN} - V_{OUT} \le 60V$ (Note 2) $I_L = 10$ mA | | 0.01 | 0.02 | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_J = 25°C, 10 \text{ mA} \le I_{OUT} \le I_{MAX}$ | | 0.1 | 0.3 | | 0.1 | 0.5 | % |
| Thermal Regulation | $T_J = 25°C$, 20 ms Pulse | | 0.03 | 0.07 | | 0.04 | 0.07 | %/W |
| Adjustment Pin Current | | | 50 | 100 | | 50 | 100 | $\mu$A |
| Adjustment Pin Current Change | $10 \text{ mA} \le I_L \le I_{MAX}$<br>$3.0 V \le (V_{IN} - V_{OUT}) \le 60V$ | | 0.2 | 5 | | 0.2 | 5 | $\mu$A |
| Reference Voltage | $3.0 V \le (V_{IN} - V_{OUT}) \le 60V$, (Note 3)<br>$10 \text{ mA} \le I_{OUT} \le I_{MAX}, P \le P_{MAX}$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation | $3.0V \le (V_{IN} - V_{OUT}) \le 60V, I_L = 10$ mA, (Note 2) | | 0.02 | 0.05 | | 0.02 | 0.07 | %/V |
| Load Regulation | $10 \text{ mA} \le I_{OUT} \le I_{MAX}$ (Note 2) | | 0.3 | 1 | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \le T_J \le T_{MAX}$ | | 1 | | | 1 | | % |
| Minimum Load Current | $(V_{IN} - V_{OUT}) = 60V$ | | 3.5 | 7 | | 3.5 | 12 | mA |
| Current Limit | $(V_{IN} - V_{OUT}) \le 15V$ | | | | | | | |
| | K Package | 1.5 | 2.2 | 3.5 | 1.5 | 2.2 | 3.7 | A |
| | H Package | 0.5 | 0.8 | 1.8 | 0.5 | 0.8 | 1.9 | A |
| | $(V_{IN} - V_{OUT}) \le 60V$ | | | | | | | |
| | K Package | | 0.1 | | | 0.1 | | A |
| | H Package | | 0.03 | | | 0.03 | | A |
| RMS Output Noise, % of $V_{OUT}$ | $T_J = 25°C, 10 \text{ Hz} \le f \le 10 \text{ kHz}$ | | 0.003 | | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = 10V, f = 120$ Hz | | 65 | | | 65 | | dB |
| | $C_{ADJ} = 10\ \mu F$ | 66 | 80 | | 66 | 80 | | dB |
| Long-Term Stability | $T_J = 125°C$ | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | H Package | | 12 | 15 | | 12 | 15 | °C/W |
| | K Package | | 2.3 | 3 | | 2.3 | 3 | °C/W |
| Thermal Resistance, Junction to Ambient (no heat sink) | H Package | | 140 | | | 140 | | °C/W |
| | K Package | | 35 | | | 35 | | °C/W |

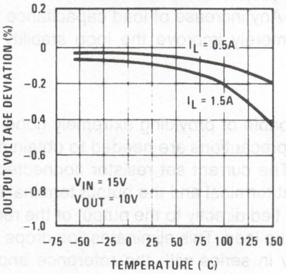
**Note 1:** Unless otherwise specified, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM117HV, and $0°C \le T_J \le +125°C$ for the LM317HV; $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. $I_{MAX}$ is 1.5A for the TO-3 and 0.5A for the TO-39 package.

**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

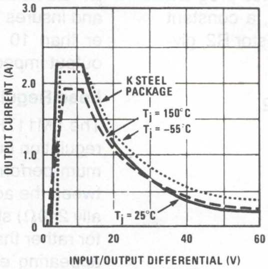
**Note 3:** Refer to RETS117HVH for LM117HVH or RETS117HVK for LM117HVK military specificatioins.

## Typical Performance Characteristics (K Package)

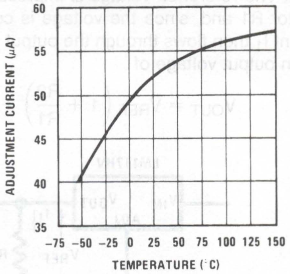
### Load Regulation



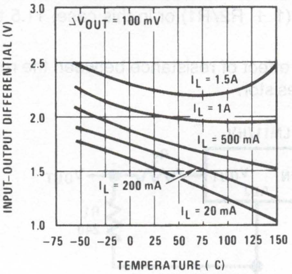
### Current Limit



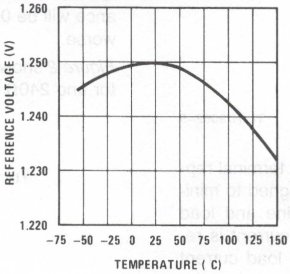
### Adjustment Current



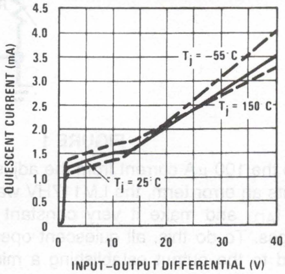
### Dropout Voltage



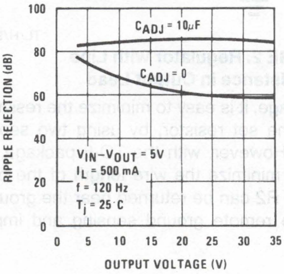
### Temperature Stability



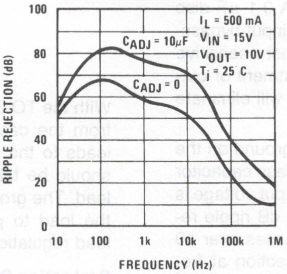
### Minimum Operating Current



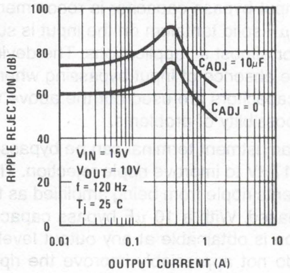
### Ripple Rejection



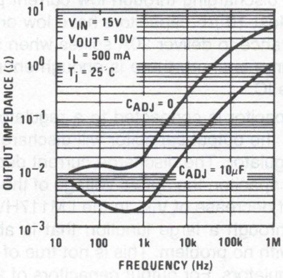
### Ripple Rejection



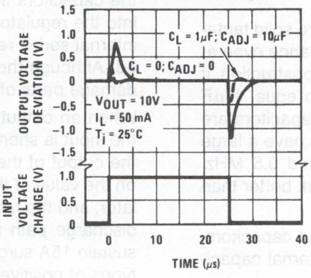
### Ripple Rejection



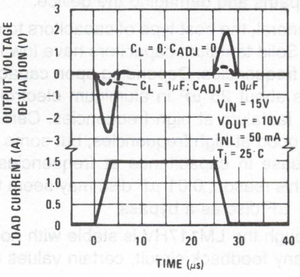
### Output Impedance



### Line Transient Response



### Load Transient Response

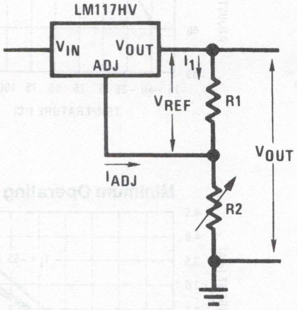


TL/H/9062–4

## Application Hints

In operation, the LM117HV develops a nominal 1.25V reference voltage, $V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9062-5

**FIGURE 1**

Since the 100 $\mu$A current from the adjustment terminal represents an error term, the LM117HV was designed to minimize $I_{ADJ}$ and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

### External Capacitors

An input bypass capacitor is recommended. A 0.1 $\mu$F disc or 1 $\mu$F solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM117HV to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 $\mu$F bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 $\mu$F do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

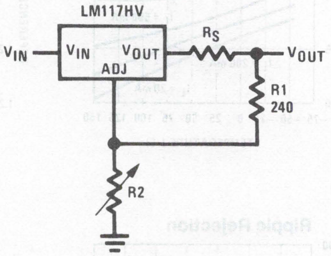
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 $\mu$F in aluminum electrolytic to equal 1 $\mu$F solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 $\mu$F disc may seem to work better than a 0.1 $\mu$F disc as a bypass.

Although the LM117HV is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 $\mu$F solid tantalum (or 25 $\mu$F aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of load capacitance larger than 10 $\mu$F will merely improve the loop stability and output impedance.

### Load Regulation

The LM117HV is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × $I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

*Figure 2* shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9062-6

**FIGURE 2. Regulator with Line Resistance in Output Lead**

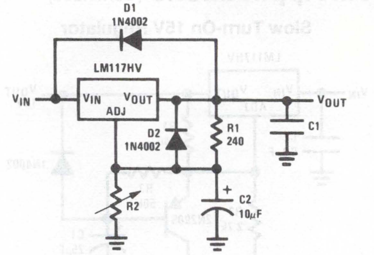
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

### Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 $\mu$F capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{IN}$. In the LM117HV, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 $\mu$F or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117HV is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117HV with protection diodes included for use with outputs greater than 25V and high values of output capacitance.


D1
1N4002
LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
D2
1N4002
R1
240
C1
$V_{OUT}$
R2
+
C2
10μF

TL/H/9062-7

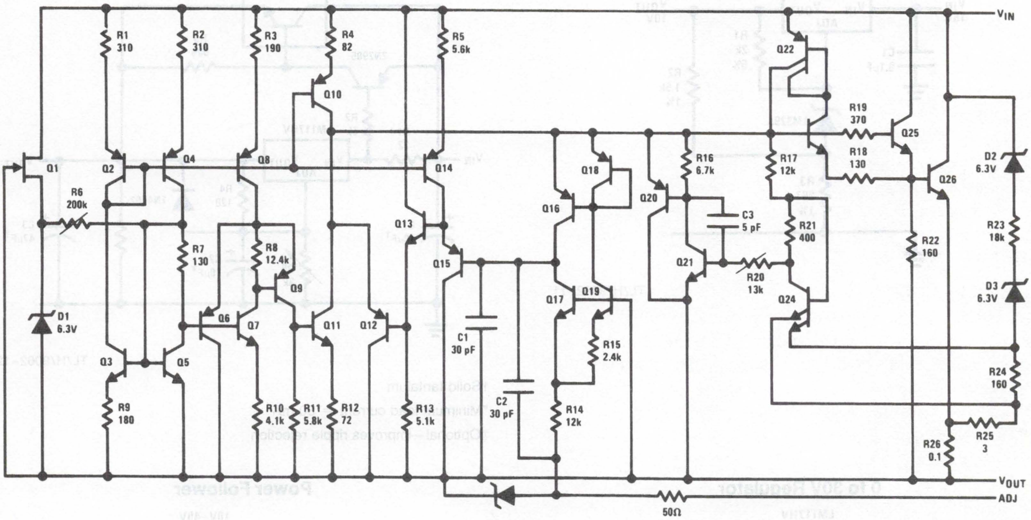
**FIGURE 3. Regulator with Protection Diodes**

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1

D2 protects against C2

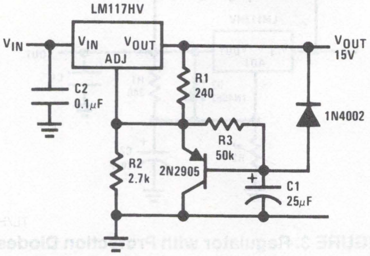
## Schematic Diagram


$V_{IN}$
R1 310
R2 310
R3 190
R4 82
R5 5.6k
Q10
Q22
R19 370
Q25
Q1
Q2
Q4
Q8
Q14
Q18
R16 6.7k
R17 12k
R18 130
D2 6.3V
Q26
R6 200k
Q16
Q20
C3 5 pF
Q13
R21 400
R7 130
R8 12.4k
R22 160
R23 18k
Q15
Q21
Q9
R20 13k
Q19
Q17
Q24
D3 6.3V
D1 6.3V
Q6
Q7
Q11
Q12
C1 30 pF
Q3
Q5
R15 2.4k
R24 160
R9 180
R10 4.1k
R11 5.8k
R12 72
R13 5.1k
C2 30 pF
R14 12k
R25 3
R26 0.1
$V_{OUT}$
ADJ
50Ω

TL/H/9062-8

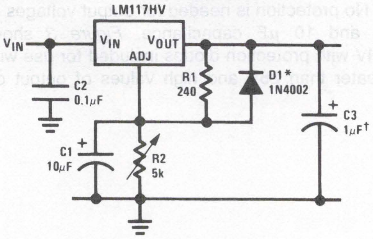
## Typical Applications (Continued)

### Slow Turn-On 15V Regulator


LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
15V
C2
0.1µF
R1
240
1N4002
R3
50k
R2
2.7k
2N2905
C1
25µF

TL/H/9062-9

### Adjustable Regulator with Improved Ripple Rejection

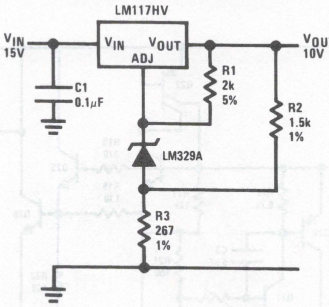

LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
C2
0.1µF
R1
240
D1*
1N4002
C3
1µF†
C1
10µF
R2
5k

TL/H/9062-10

†Solid tantalum

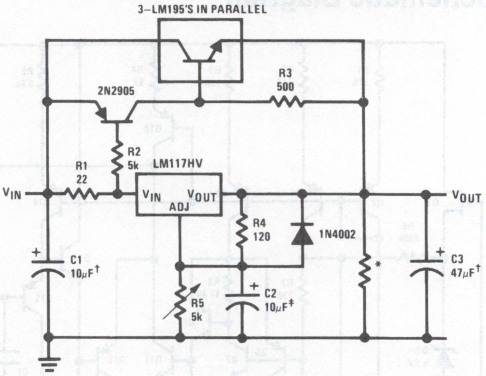
*Discharges C1 if output is shorted to ground

### High Stability 10V Regulator


LM117HV
$V_{IN}$
15V
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
10V
C1
0.1µF
R1
2k
5%
R2
1.5k
1%
LM329A
R3
267
1%

TL/H/9062-11

### High Current Adjustable Regulator


3–LM195'S IN PARALLEL
R3
500
2N2905
R2
5k
LM117HV
R1
22
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R4
120
1N4002
C1
10µF†
C3
47µF†
*
R5
5k
C2
10µF‡

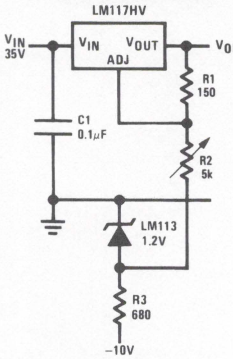
TL/H/9062-12

†Solid tantalum

*Minimum load current = 30 mA

‡Optional—improves ripple rejection

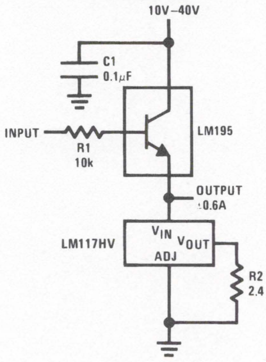
### 0 to 30V Regulator


LM117HV
$V_{IN}$
35V
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R1
150
C1
0.1µF
R2
5k
LM113
1.2V
R3
680
−10V

TL/H/9062-13

Full output current not available at high input-output voltages

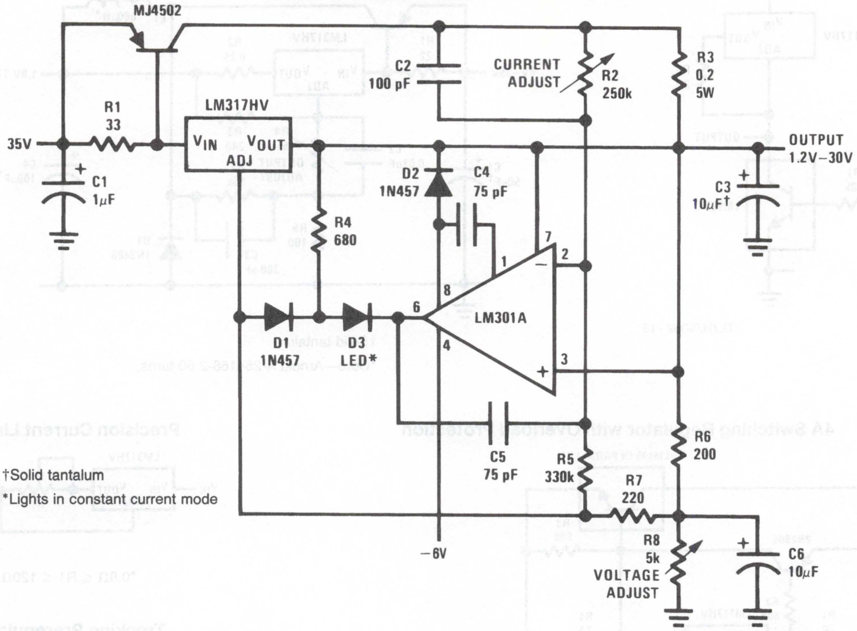
### Power Follower


10V–40V
C1
0.1µF
INPUT
R1
10k
LM195
OUTPUT
±0.6A
LM117HV
$V_{IN}$
$V_{OUT}$
ADJ
R2
2.4

TL/H/9062-14

## Typical Applications (Continued)

### 5A Constant Voltage/Constant Current Regulator

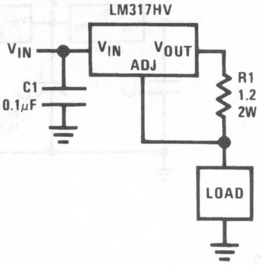

MJ4502
R1
33
35V
C1
1µF
LM317HV
VIN
VOUT
ADJ
C2
100 pF
CURRENT
ADJUST
R2
250k
R3
0.2
5W
OUTPUT
1.2V–30V
C3
10µF†
D2
1N457
C4
75 pF
R4
680
7
1
2
8
6
LM301A
4
3
D1
1N457
D3
LED*
C5
75 pF
R5
330k
R6
200
R7
220
R8
5k
VOLTAGE
ADJUST
C6
10µF
−6V

†Solid tantalum

*Lights in constant current mode

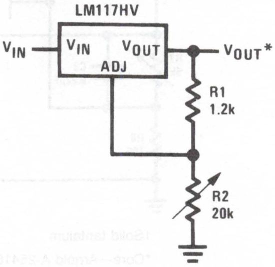
TL/H/9062-15

### 1A Current Regulator


LM317HV
VIN
VIN
VOUT
ADJ
C1
0.1µF
R1
1.2
2W
LOAD

TL/H/9062-16

### 1.2V–20V Regulator with Minimum Program Current

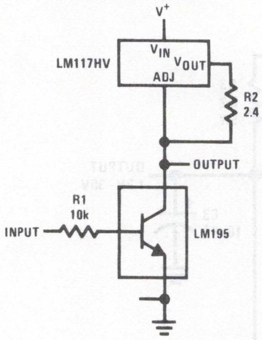

LM117HV
VIN
VIN
VOUT
ADJ
VOUT*
R1
1.2k
R2
20k

TL/H/9062-17

*Minimum load current ≈ 4 mA

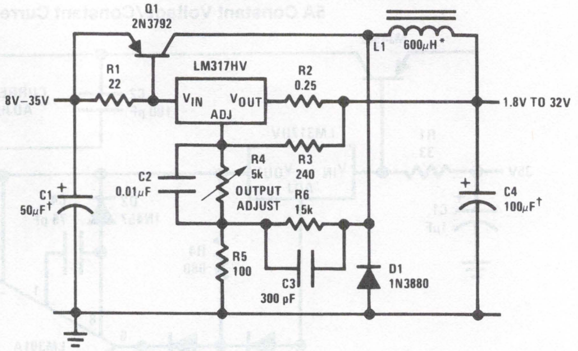
## Typical Applications (Continued)

### High Gain Amplifier


$V^+$
LM117HV
$V_{IN}$
$V_{OUT}$
ADJ
R2
2.4
OUTPUT
R1
10k
INPUT
LM195

TL/H/9062–18

### Low Cost 3A Switching Regulator

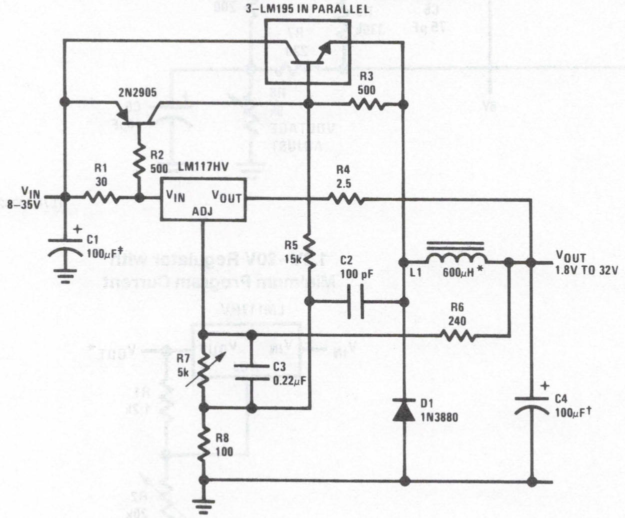

Q1
2N3792
L1
600μH*
LM317HV
R1
22
R2
0.25
8V–35V
$V_{IN}$
$V_{OUT}$
ADJ
1.8V TO 32V
R4
5k
OUTPUT
ADJUST
R3
240
C2
0.01μF
C1
50μF†
R6
15k
C4
100μF†
R5
100
C3
300 pF
D1
1N3880

†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–19

### 4A Switching Regulator with Overload Protection

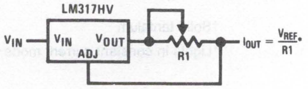

3–LM195 IN PARALLEL
2N2905
R3
500
R2
500
LM117HV
R1
30
$V_{IN}$
8–35V
$V_{IN}$
$V_{OUT}$
ADJ
R4
2.5
C1
100μF†
R5
15k
C2
100 pF
L1
600μH*
$V_{OUT}$
1.8V TO 32V
R6
240
R7
5k
C3
0.22μF
D1
1N3880
C4
100μF†
R8
100

†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–20

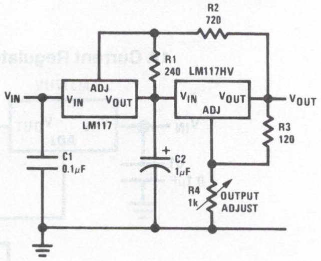
### Precision Current Limiter


LM317HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
R1
$I_{OUT} = \frac{V_{REF}}{R1}$*

TL/H/9062–21

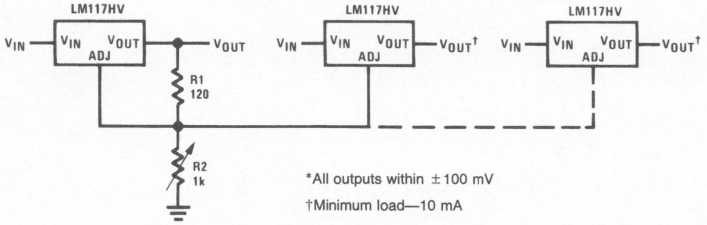
*0.8Ω ≤ R1 ≤ 120Ω

### Tracking Preregulator


R2
720
R1
240
LM117HV
ADJ
$V_{IN}$
$V_{IN}$
$V_{OUT}$
LM117
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
C1
0.1μF
C2
1μF
R3
120
R4
1k
OUTPUT
ADJUST

TL/H/9062–22

### Adjustable Multiple On-Card Regulators with Single Control*


LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R1
120
R2
1k
LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†
LM117HV
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†

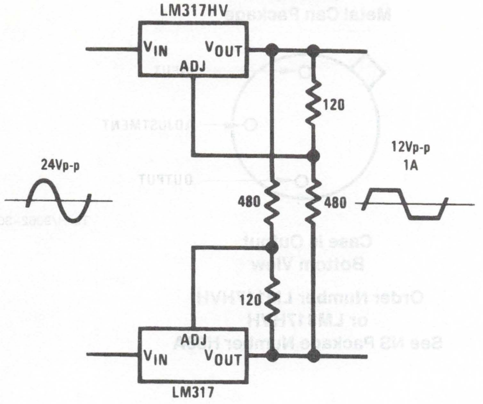
*All outputs within ±100 mV

†Minimum load—10 mA

TL/H/9062–23

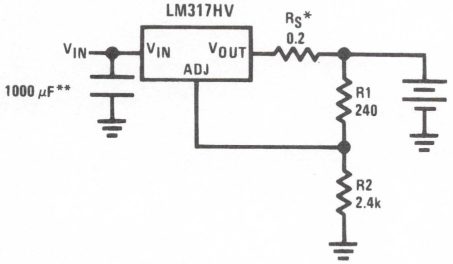
## Typical Applications (Continued)

### AC Voltage Regulator


LM317HV
VIN
VOUT
ADJ
120
24Vp-p
12Vp-p
1A
480
480
120
ADJ
VIN
VOUT
LM317

TL/H/9062–24

### 12V Battery Charger


LM317HV
VIN
VIN
VOUT
ADJ
RS*
0.2
1000 μF**
R1
240
R2
2.4k

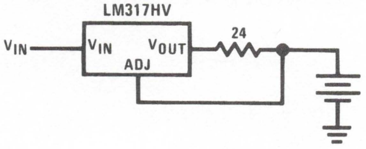
TL/H/9062–25

*$R_S$—sets output impedance of charger $Z_{OUT} = R_S\left(1+\frac{R2}{R1}\right)$

Use of $R_S$ allows low charging rates with fully charged battery.

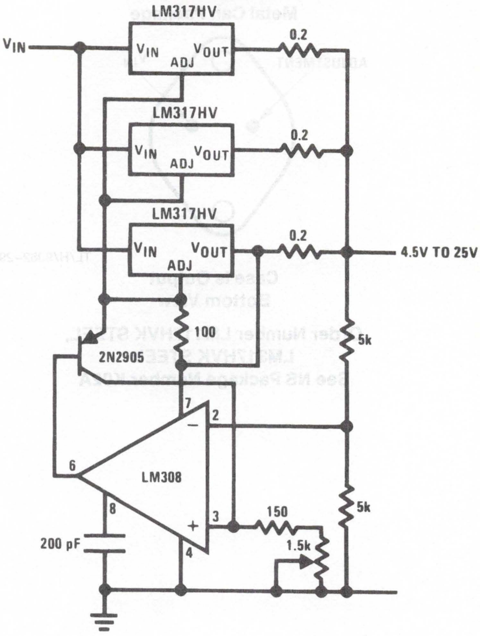
**The 1000 μF is recommended to filter out input transients

### 50 mA Constant Current Battery Charger


LM317HV
VIN
VIN
VOUT
ADJ
24

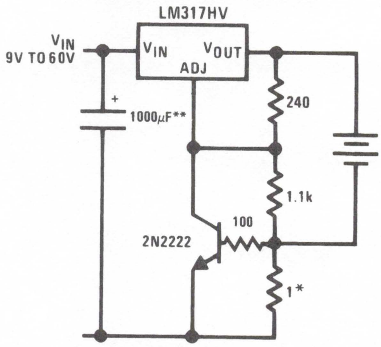
TL/H/9062–26

### Adjustable 4A Regulator


LM317HV
VIN
VIN
ADJ
VOUT
0.2
LM317HV
VIN
ADJ
VOUT
0.2
LM317HV
VIN
VOUT
ADJ
0.2
4.5V TO 25V
100
2N2905
5k
7
2
6
LM308
8
3
150
5k
200 pF
4
1.5k

TL/H/9062–27

### Current Limited 6V Charger


LM317HV
VIN
9V TO 60V
VIN
VOUT
ADJ
+
1000μF**
240
1.1k
100
2N2222
1*

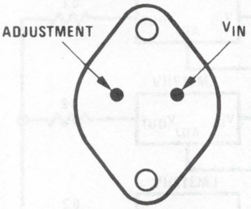
TL/H/9062–28

*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

## Connection Diagrams (See Physical Dimension section for further information)

**(TO-3 Steel)**
**Metal Can Package**

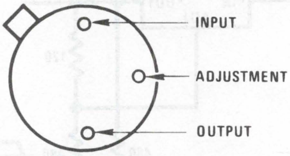

ADJUSTMENT
$V_{IN}$

TL/H/9062-29

**Case is Output**
**Bottom View**

**Order Number LM117HVK STEEL,**
**LM317HVK STEEL**
**See NS Package Number K02A**

**(TO-39)**
**Metal Can Package**


INPUT
ADJUSTMENT
OUTPUT

TL/H/9062-30

**Case is Output**
**Bottom View**

**Order Number LM117HVH,**
**or LM317HVH**
**See NS Package Number H03A**

**National Semiconductor Corporation**

# LM120/LM320 Series 3-Terminal Negative Regulators

## General Description

The LM120 series are three-terminal negative regulators with a fixed output voltage of −5V, −12V, and −15V, and up to 1.5A load current capability. Where other voltages are required, the LM137 series provides an output voltage range of −1.2V to −4.7V.

The LM120 need only one external component—a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

## Features

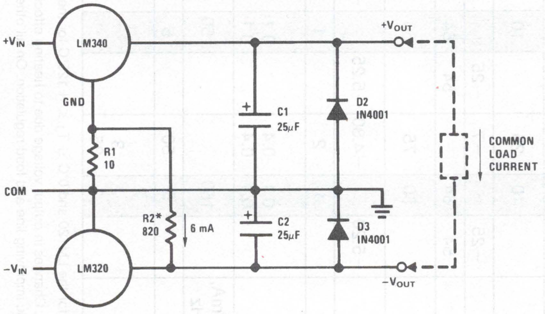
- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- Low temperature drift
- Easily adjustable to higher output voltage

**LM120 Series Packages and Power Capability**

| Device | Package | Rated Power Dissipation | Design Load Current |
|---|---|---|---|
| LM120 | TO-3 | 20W | 1.5A |
| LM320 | TO-39 | 2W | 0.5A |
| LM320T | TO-220 | 15W | 1.5A |
| LM320M | TO-202 | 7.5W | 0.5A |

## Typical Applications

### Preventing Positive Regulator Latch-Up

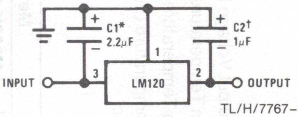


TL/H/7767–1

R1 & D1 allow the positive regulator to "start-up" when $+V_{IN}$ is delayed relative to $-V_{IN}$ and a heavy load is drawn between the outputs. Without R1 & D1, most three-terminal regulators will not start with heavy (0.1A–1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

*R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT} \approx 60$ mV if R2 is omitted.

### Fixed Regulator



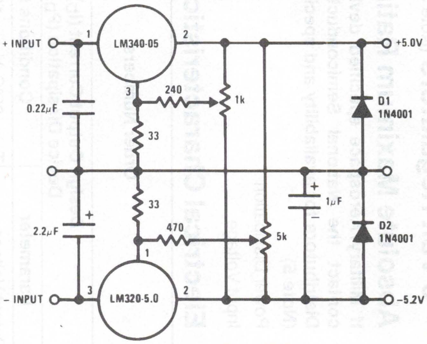
TL/H/7767–2

*Required if regulator is separated from filter capacitor by more than 3″. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may substituted. Values given may be increased without limit.

For output capacitance in excess of 100 μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

### Dual Trimmed Supply



TL/H/7767–3

# −5 Volt Regulators (Note 3)

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input Voltage | −25V |
| Input-Output Voltage Differential | 25V |
| Junction Temperatures | See Note 1 |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| Plastic | 260°C |

## Electrical Characteristics

| Order Numbers | | Metal Can Package | | | | | | | | | | | | Power Plastic Package | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | LM120K-5.0 (TO-3) | | | LM320K-5.0 (TO-3) | | | LM120H-5.0 (TO-39) | | | LM320H-5.0 (TO-39) | | | LM320T-5.0 (TO-220) | | | LM320MP-5.0 (TO-202) | | | |
| Design Output Current ($I_D$)<br>Device Dissipation ($P_D$) | | 1.5A<br>20W | | | 1.5A<br>20W | | | 0.5A<br>2W | | | 0.5A<br>2W | | | 1.5A<br>15W | | | 0.5A<br>7.5W | | | |
| Parameter | Conditions (Note 1) | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_J$ = 25°C, $V_{IN}$ = 10V, $I_{LOAD}$ = 5 mA | −5.1 | −5 | −4.9 | −5.2 | −5 | −4.8 | −5.1 | −5 | −4.9 | −5.2 | −5 | −4.8 | −5.2 | −5 | −4.8 | −5.2 | −5 | −4.8 | V |
| Line Regulation | $T_J$ = 25°C, $I_{LOAD}$ = 5 mA, $V_{MIN} \leq V_{IN} \leq V_{MAX}$ | | 10 | 25 | | 10 | 40 | | 10 | 25 | | 10 | 40 | | 10 | 40 | | 10 | 40 | mV |
| Input Voltage | | −25 | | −7 | −25 | | −7 | −25 | | −7 | −−25 | | −7 | −25 | | −7.5 | −25 | | −7.5 | V |
| Ripple Rejection | f = 120 Hz | 54 | 64 | | 54 | 64 | | 54 | 64 | | 54 | 64 | | 54 | 64 | | 54 | 64 | | dB |
| Load Regulation, (Note 2) | $T_J$ = 25°C, $V_{IN}$ = 10V, 5 mA $\leq I_{LOAD} \leq I_D$ | | 50 | 75 | | 60 | 100 | | 30 | 50 | | 30 | 50 | | 50 | 100 | | 40 | 100 | mV |
| Output Voltage, (Note 1) | −7.5V $\leq V_{IN} \leq V_{MAX}$, 5 mA $\leq I_{LOAD} \leq I_D$, $P \leq P_D$ | −5.20 | | −4.80 | −5.25 | | −4.75 | −5.20 | | −4.80 | −5.25 | | −4.75 | −5.25 | | −4.75 | −5.25 | −5 | −4.75 | V |
| Quiescent Current | $V_{MIN} \leq V_{IN} \leq V_{MAX}$ | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | mA |
| Quiescent Current Change | $T_J$ = 25°C<br>$V_{MIN} \leq V_{IN} \leq V_{MAX}$<br>5 mA $\leq I_{LOAD} \leq I_D$ | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.04 | 0.4<br>0.4 | | 0.05<br>0.04 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.04 | 0.3<br>0.25 | mA<br>mA |
| Output Noise Voltage | $T_A$ = 25°C, $C_L$ = 1 µF, $I_L$ = 5 mA, $V_{IN}$ = 10V, 10 Hz $\leq f \leq$ 100 kHz | | 150 | | | 150 | | | 150 | | | 150 | | | 150 | | | 150 | | µV |
| Long Term Stability | | | 5 | 50 | | 5 | 50 | | 5 | 50 | | 5 | 50 | | 10 | | | 10 | | mV |
| Thermal Resistance<br>Junction to Case<br>Junction to Ambient | | | | 3<br>35 | | | 3<br>35 | | | Note 4<br>Note 4 | | | Note 4<br>Note 4 | | 4<br>50 | | | 12<br>70 | | °C/W<br>°C/W |

**Note 1:** This specification applies over −55°C ≤ $T_J$ ≤ +150°C for the LM120 and 0°C ≤ $T_J$ ≤ +125°C for the LM320.

**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to $P_D$.

**Note 3:** For −5V 3 amp regulators, see LM145 data sheet.

**Note 4:** Thermal resistance of typically 85°C/W (in 400 linear feet air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

**Note 5:** Refer to RETS120-5H drawing for LM120H-5.0 or RETS120-5K drawing for LM120-5K military specifications.

## −12 Volt Regulators

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input Voltage | −35V |
| Input-Output Voltage Differential | 30V |
| Junction Temperatures | See Note 1 |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics

| | | Metal Can Package | | | | | | | | | | | | Power Plastic Package | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Order Numbers | | LM120K-12 (TO-3) | | | LM320K-12 (TO-3) | | | LM120H-12 (TO-39) | | | LM320H-12 (TO-39) | | | LM320T-12 (TO-220) | | | LM320MP-12 (TO-202) | | | Units |
| Design Output Current ($I_D$) | | | 1A | | | 1A | | | 0.2A | | | 0.2A | | | 1A | | | 0.5A | | |
| Device Dissipation ($P_D$) | | | 20W | | | 20W | | | 2W | | | 2W | | | 15W | | | 7.5W | | |
| Parameter | Conditions (Note 1) | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_J = 25°C$, $V_{IN} = 17V$, $I_{LOAD} = 5$ mA | −12.3 | −12 | −11.7 | −12.4 | −12 | −11.6 | −12.3 | −12 | −11.7 | −12.4 | −12 | −11.6 | −12.4 | −12 | −11.6 | −12.5 | −12 | −11.5 | V |
| Line Regulation | $T_J = 25°C$, $I_{LOAD} = 5$ mA, $V_{MIN} \le V_{IN} \le V_{MAX}$ | | 4 | 10 | | 4 | 20 | | 4 | 10 | | 4 | 20 | | 4 | 20 | | 4 | 24 | mV |
| Input Voltage | | −32 | | −14 | −32 | | −14 | −32 | | −14 | −32 | | −14 | −32 | | −14.5 | −32 | | −14.5 | V |
| Ripple Rejection | f = 120 Hz | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | dB |
| Load Regulation, (Note 2) | $T_J = 25°C$, $V_{IN} = 17V$, $5\text{ mA} \le I_{LOAD} \le I_D$ | | 30 | 80 | | 30 | 80 | | 10 | 25 | | 10 | 40 | | 30 | 80 | | 40 | 100 | mV |
| Output Voltage, (Note 1) | $14.5V \le V_{IN} \le V_{MAX}$, $5\text{ mA} \le I_{LOAD} \le I_D$, $P \le P_D$ | −12.5 | | −11.5 | −12.6 | | −11.4 | −12.5 | | −11.5 | −12.6 | | −11.4 | −12.6 | | −11.4 | −12.6 | | −11.4 | V |
| Quiescent Current | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | mA |
| Quiescent Current Change | $T_J = 25°C$<br>$V_{MIN} \le V_{IN} \le V_{MAX}$<br>$5\text{ mA} \le I_{LOAD} \le I_D$ | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.03 | 0.4<br>0.4 | | 0.05<br>0.03 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.04 | 0.3<br>0.25 | mA<br>mA |
| Output Noise Voltage | $T_A = 25°C$, $C_L = 1\ \mu F$, $I_L = 5$ mA, $V_{IN} = 17V$, $10\text{ Hz} \le f \le 100\text{ kHz}$ | | 400 | | | 400 | | | 400 | | | 400 | | | 400 | | | 400 | | μV |
| Long Term Stability | | | 12 | 120 | | 12 | 120 | | 12 | 120 | | 12 | 120 | | 24 | | | 24 | | mV |
| Thermal Resistance<br>Junction to Case<br>Junction to Ambient | | | | 3<br>35 | | | 3<br>35 | | | Note 3<br>Note 3 | | | Note 3<br>Note 3 | | 4<br>50 | | | 12<br>70 | | °C/W<br>°C/W |

**Note 1:** This specification applies over $-55°C \le T_J \le +150°C$ for the LM120 and $0°C \le T_J \le +125°C$ for the LM320.

**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to $P_D$.

**Note 3:** Thermal resistance of typically 85°C/W (in 400 linear feet/min air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

**Note 4:** Refer to RETS120H-12 drawing for LM120H-12 or RETS120-12K drawing for LM120K-12 military specifications.

# −15 Volt Regulators

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 4)**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input Voltage | |
| LM120/LM320 | −40V |
| LM320T/LM320MP | −35V |
| Input-Output Voltage Differential | 30V |
| Junction Temperatures | See Note 1 |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics

| | | Metal Can Package | | | | | | | | | | | | Power Plastic Package | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Order Numbers | | LM120K-15 (TO-3) | | | LM320K-15 (TO-3) | | | LM120H-15 (TO-39) | | | LM320H-15 (TO-39) | | | LM320T-15 (TO-220) | | | LM320MP-15 (TO-202) | | | |
| Design Output Current ($I_D$)<br>Device Dissipation ($P_D$) | | 1A<br>20W | | | 1A<br>20W | | | 0.2A<br>2W | | | 0.2A<br>2W | | | 1A<br>15W | | | 0.5A<br>7.5W | | | |
| **Parameter** | **Conditions (Note 1)** | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_J = 25°C$, $V_{IN} = 20V$, $I_{LOAD} = 5$ mA | −15.3 | −15 | −14.7 | −15.4 | −15 | −14.6 | −15.3 | −15 | −14.7 | −15.4 | −15 | −14.6 | −15.5 | −15 | −14.5 | −15.6 | −15 | −14.4 | V |
| Line Regulation | $T_J = 25°C$, $I_{LOAD} = 5$ mA, $V_{MIN} \le V_{IN} \le V_{MAX}$ | | 5 | 10 | | 5 | 20 | | 5 | 10 | | 5 | 20 | | 5 | 20 | | 5 | 30 | mV |
| Input Voltage | | −35 | | −17 | −35 | | −17 | −35 | | −17 | −35 | | −17 | −35 | | −17.5 | −35 | | −17.5 | V |
| Ripple Rejection | f = 120 Hz | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | 56 | 80 | | dB |
| Load Regulation, (Note 2) | $T_J = 25°C$, $V_{IN} = 20V$, $5\text{ mA} \le I_{LOAD} \le I_D$ | | 30 | 80 | | 30 | 80 | | 10 | 25 | | 10 | 40 | | 30 | 80 | | 40 | 100 | mV |
| Output Voltage, (Note 1) | $17.5V \le V_{IN} \le V_{MAX}$, $5\text{ mA} \le I_{LOAD} \le I_D$, $P \le P_D$ | −15.5 | | −14.5 | −15.6 | | −14.4 | −15.5 | | −14.5 | −15.6 | | −14.4 | −15.7 | | −14.3 | −15.7 | | −14.3 | V |
| Quiescent Current | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | | 2 | 4 | mA |
| Quiescent Current Change | $T_J = 25°C$<br>$V_{MIN} \le V_{IN} \le V_{MAX}$<br>$5\text{ mA} \le I_{LOAD} \le I_D$ | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.03 | 0.4<br>0.4 | | 0.05<br>0.03 | 0.4<br>0.4 | | 0.1<br>0.1 | 0.4<br>0.4 | | 0.05<br>0.04 | 0.3<br>0.25 | mA<br>mA |
| Output Noise Voltage | $T_A = 25°C$, $C_L = 1\ \mu F$, $I_L = 5$ mA, $V_{IN} = 20V$, $10\text{ Hz} \le f \le 100\text{ kHz}$ | | 400 | | | 400 | | | 400 | | | 400 | | | 400 | | | 400 | | μV |
| Long Term Stability | | | 15 | 150 | | 15 | 150 | | 15 | 150 | | 15 | 150 | | 30 | | | 30 | | mV |
| Thermal Resistance<br>Junction to Case<br>Junction to Ambient | | | | 3<br>35 | | | 3<br>35 | | | Note 3<br>Note 3 | | | Note 3<br>Note 3 | | 4<br>50 | | | 12<br>70 | | °C/W<br>°C/W |

**Note 1:** This specification applies over −55°C ≤ $T_J$ ≤ +150°C for the LM120 and 0°C ≤ $T_J$ ≤ +125°C for the LM320.

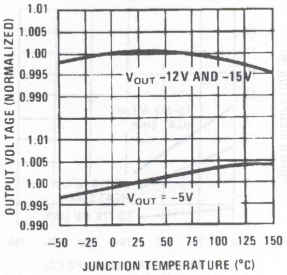
**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to $P_D$.

**Note 3:** Thermal resistance of typically 85°C/W (in 400 linear feet/min air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

**Note 4:** Refer to RETS120-15H drawing for LM120H-15 or RETS120-15K drawing for LM120K-15 military specifications.

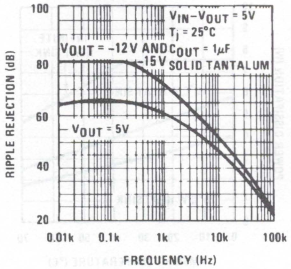
## Typical Performance Characteristics

**Output Voltage vs Temperature**

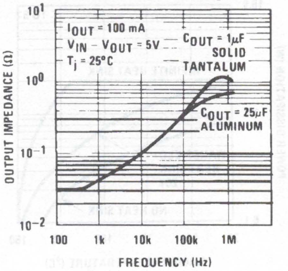


**Note:** Shaded portion refers to LM320 series regulators.

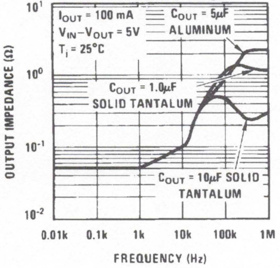
**Ripple Rejection (All Types)**



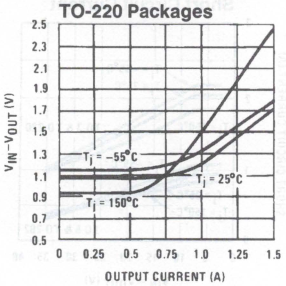
**Output Impedance TO-3 and TO-220 Packages**



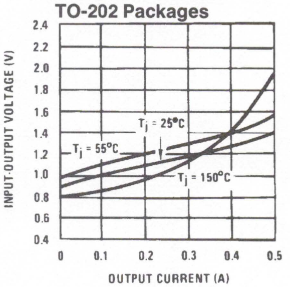
**Output Impedance TO-5 and TO-202 Packages**



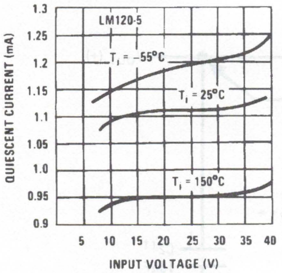
**Minimum Input-Output Differential TO-3 and TO-220 Packages**



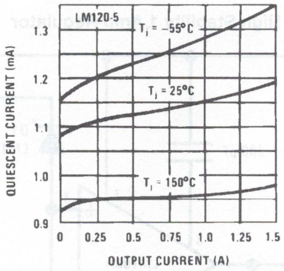
**Minimum Input-Output Differential TO-5 and TO-202 Packages**



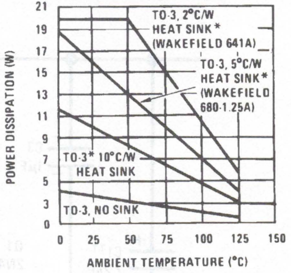
**Quiescent Current vs Input Voltage**



**Quiescent Current vs Load Current**



**Maximum Average Power Dissipation (TO-3)**



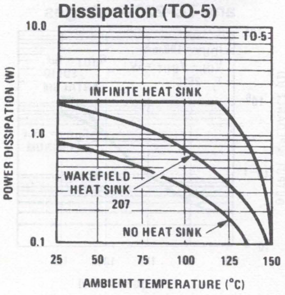
TL/H/7767–4

**Note:** Shaded area shows operating range of TO-5 and TO-202 packages.

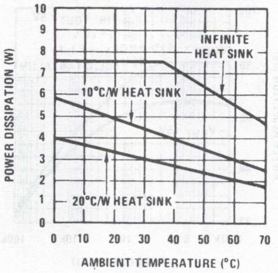
*These curves for LM120 and LM220. Derate 25°C further for LM320.

## Typical Performance Characteristics (Continued)

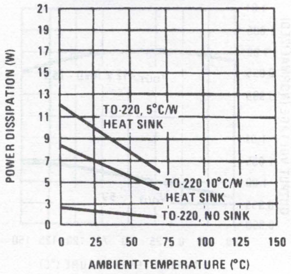
### Maximum Average Power Dissipation (TO-5)



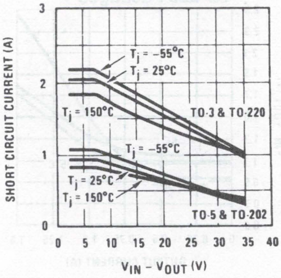
### Maximum Average Power Dissipation (TO-202)



### Maximum Average Power Dissipation (TO-220)



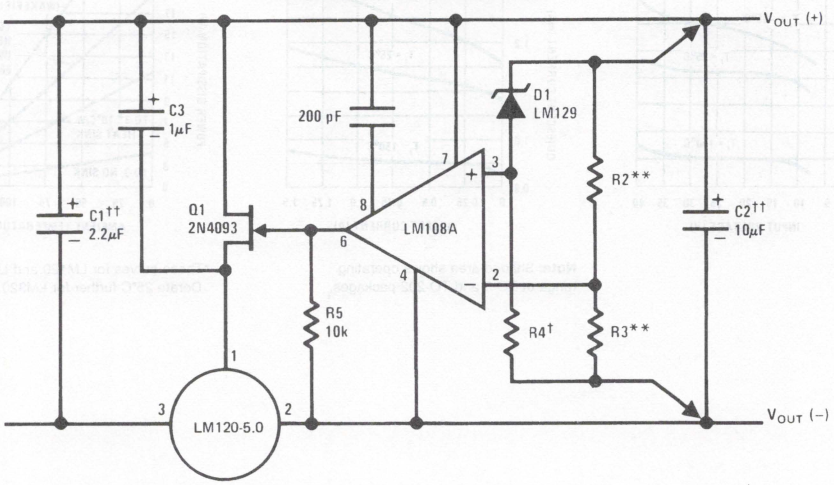
### Short Circuit Current



TL/H/7767–5

## Typical Applications (Continued)

### High Stability 1 Amp Regulator



$V_{OUT}$ (+)
C3 1μF
200 pF
D1 LM129
7
3
+
R2**
Q1 2N4093
8
LM108A
6
4
−
2
C1†† 2.2μF
C2†† 10μF
R5 10k
R4†
R3**
1
3
2
LM120-5.0
$V_{OUT}$ (−)

TL/H/7767–6

Lead and line regulation — 0.01% temperature stability — 0.2%

†Determines Zener current.

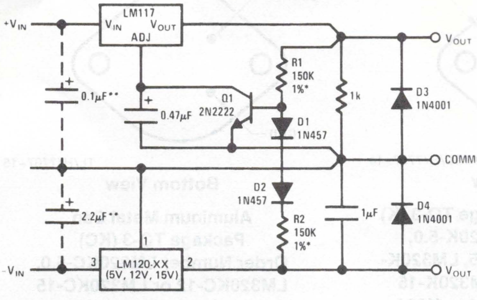
††Solid tantalum.

An LM120-12 or LM120-15 may be used to permit higher input voltages, but the regulated output voltage must be at least −15V when using the LM120-12 and −18V for the LM120-15.

**Select resistors to set output voltage. 2 ppm/°C tracking suggested.

## Typical Applications (Continued)

### Wide Range Tracking Regulator


+V_IN
LM117
V_IN
V_OUT
ADJ
V_OUT
0.1μF**
0.47μF
Q1
2N2222
R1
150K
1%*
1k
D3
1N4001
D1
1N457
COMMON
D2
1N457
2.2μF**
R2
150K
1%*
1μF
D4
1N4001
-V_IN
LM120-XX
(5V, 12V, 15V)
V_OUT

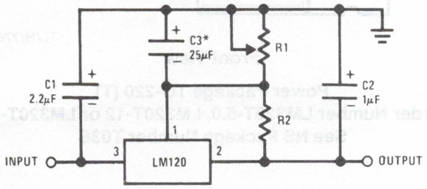
TL/H/7767-7

*Resistor tolerance of R1 and R2 determine matching of (+) and (−) inputs.

**Necessary only if raw supply capacitors are more than 3″ from regulators

An LM3086N array may substitute for Q1, D1 and D2 for better stability and tracking. In the array diode transistors Q5 and Q4 (in parallel) make up D2; similarly, Q1 and Q2 become D1 and Q3 replaces the 2N2222.

### Variable Output


C3*
25μF
R1
C1
2.2μF
C2
1μF
R2
INPUT
LM120
OUTPUT

TL/H/7767-9

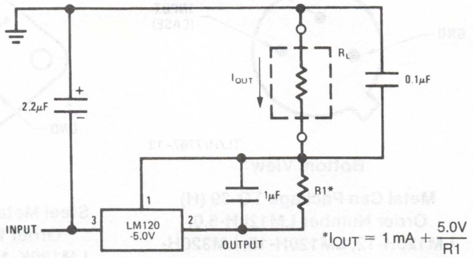
*Optional. Improves transient response and ripple rejection.

$$V_{OUT} = V_{SET}\frac{R1+R2}{R2}$$

**SELECT R2 AS FOLLOWS:**

| | |
|---|---|
| **LM120-5** | **−300Ω** |
| **LM120-12** | **−750Ω** |
| **LM120-15** | **−1k** |

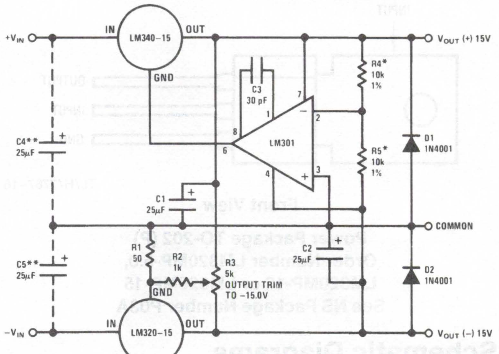
### Current Source


R_L
I_OUT
0.1μF
2.2μF
1μF
R1*
INPUT
LM120
-5.0V
OUTPUT

$$^{*}I_{OUT} = 1\text{ mA} + \frac{5.0V}{R1}$$

TL/H/7767-8

### ±15V, 1 Amp Tracking Regulators


+V_IN
IN
LM340-15
OUT
GND
V_OUT (+) 15V
R4*
10k
1%
C3
30 pF
LM301
D1
1N4001
R5*
10k
1%
C4**
25μF
C1
25μF
COMMON
C5**
25μF
R1
50
R2
1k
C2
25μF
R3
5k
OUTPUT TRIM
TO −15.0V
GND
D2
1N4001
-V_IN
IN
LM320-15
OUT
V_OUT (−) 15V

TL/H/7767-12

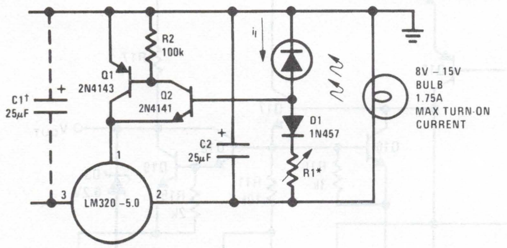
### Performance (Typical)

| | | |
|---|---|---|
| Load Regulation at $\Delta I_L = 1A$ | 10 mV | 1 mV |
| Output Ripple, $C_{IN} = 3000\ \mu F$, $I_L = 1A$ | 100 μVrms | 100 μVrms |
| Temperature Stability | +50 mV | +50 mV |
| Output Noise 10 Hz ≤ f ≤ 10 kHz | 150 μVrms | 150 μVrms |

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 2″ from regulators.

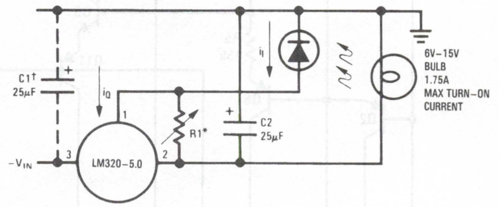
### Light Controllers Using Silicon Photo Cells


R2
100k
Q1
2N4143
Q2
2N4141
i_l
8V − 15V
BULB
1.75A
MAX TURN-ON
CURRENT
C1†
25μF
D1
1N457
C2
25μF
R1*
LM320-5.0

TL/H/7767-10

*Lamp brightness increases until $i_l = 5V/R1$ ($i_l$ can be set as low as 1 μA).

†Necessary only of raw supply filter capacitor is more than 2″ from LM320MP.

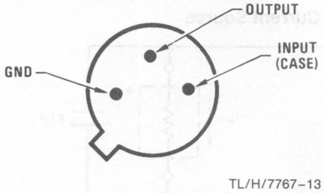

C1†
25μF
i_l
i_Q
6V−15V
BULB
1.75A
MAX TURN-ON
CURRENT
R1*
C2
25μF
-V_IN
LM320-5.0

TL/H/7767-11

*Lamp brightness increases until $i_l = i_Q$ (1 mA) + 5V/R1.

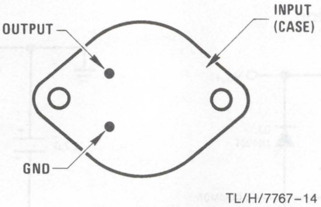
†Necessary only if raw supply filter capacitor is more than 2″ from LM320.

## Connection Diagrams


OUTPUT
INPUT (CASE)
GND
TL/H/7767-13

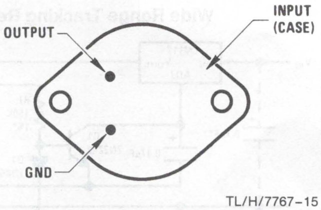
**Bottom View**

**Metal Can Package TO-39 (H)**
**Order Number LM120H-5.0, LM120H-12, LM120H-15, LM320H-5.0, LM320H-12 or LM320H-15**
**See NS Package Number H03A**


OUTPUT
INPUT (CASE)
GND
TL/H/7767-14

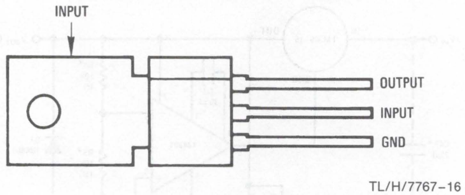
**Bottom View**

**Steel Metal Can Package TO-3 (K)**
**Order Number LM120K-5.0, LM120K-12, LM120K-15, LM320K-5.0, LM320K-12 or LM320K-15**
**See NS Package Number K02A**


OUTPUT
INPUT (CASE)
GND
TL/H/7767-15

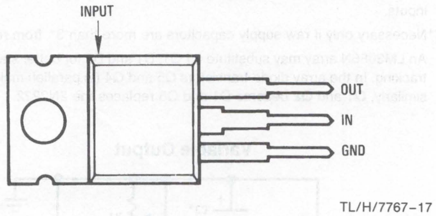
**Bottom View**

**Aluminum Metal Can Package TO-3 (KC)**
**Order Number LM320KC-5.0, LM320KC-12 or LM320KC-15**
**See NS Package Number KC02A**


INPUT
OUTPUT
INPUT
GND
TL/H/7767-16

**Front View**

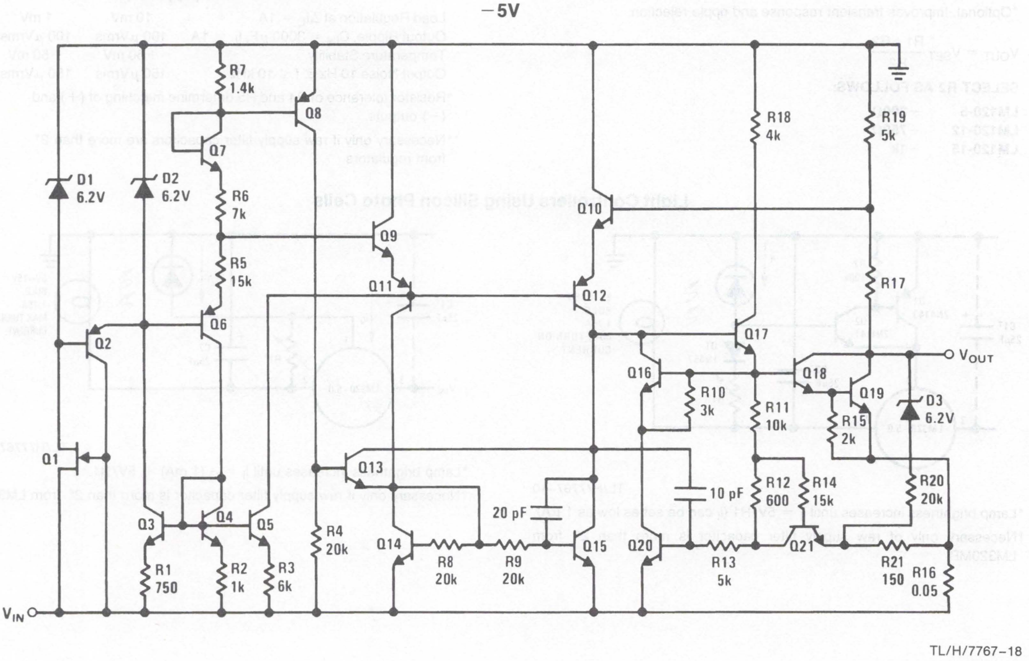
**Power Package TO-202 (P)**
**Order Number LM320MP-5.0, LM320MP-12 or LM320MP-15**
**See NS Package Number P03A**


INPUT
OUT
IN
GND
TL/H/7767-17

**Front View**

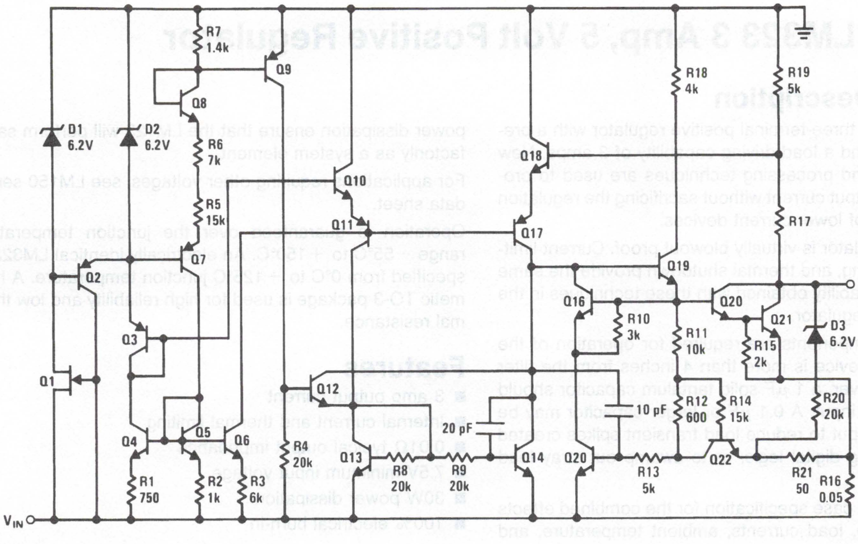
**Power Package TO-220 (T)**
**Order Number LM320T-5.0, LM320T-12 or LM320T-15**
**See NS Package Number T03B**

## Schematic Diagrams


−5V
R7 1.4k
Q8
Q7
D1 6.2V
D2 6.2V
R6 7k
R5 15k
Q9
Q10
Q11
Q12
Q6
Q2
Q17
R18 4k
R19 5k
R17
V_OUT
Q16
R10 3k
R11 10k
Q18
Q19
R15 2k
D3 6.2V
Q1
Q13
10 pF
20 pF
R12 600
R14 15k
R20 20k
Q3
Q4
Q5
R4 20k
Q14
R8 20k
R9 20k
Q15
Q20
R13 5k
Q21
R21 150
R16 0.05
R1 750
R2 1k
R3 6k
V_IN
TL/H/7767-18

## Schematic Diagrams (Continued)

−12V and −15V


R7
1.4k
Q9
Q8
D1
6.2V
D2
6.2V
R6
7k
Q10
R5
15k
Q11
Q7
Q2
Q3
Q1
Q12
Q4
Q5
Q6
20 pF
R4
20k
Q13
R8
20k
R9
20k
R1
750
R2
1k
R3
6k
V_IN
R18
4k
R19
5k
Q18
R17
Q17
Q19
V_OUT
Q16
Q20
Q21
D3
6.2V
R10
3k
R11
10k
R15
2k
10 pF
R12
600
R14
15k
R20
20k
Q14
Q20
R13
5k
Q22
R21
50
R16
0.05

TL/H/7767–19

**National Semiconductor Corporation**

# LM123/LM323 3 Amp, 5 Volt Positive Regulator

## General Description

The LM123 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3 amp regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1 amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1 μF solid tantalum capacitor should be used on the input. A 0.1 μF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature, and power dissipation ensure that the LM123 will perform satisfactorily as a system element.

For applications requiring other voltages, see LM150 series data sheet.

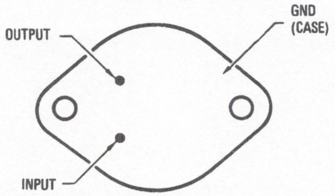
Operation is guaranteed over the junction temperature range −55°C to +150°C. An electrically identical LM323 is specified from 0°C to +125°C junction temperature. A hermetic TO-3 package is used for high reliability and low thermal resistance.

## Features

- 3 amp output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5V minimum input voltage
- 30W power dissipation
- 100% electrical burn-in

## Connection Diagram

**Metal Can Package**

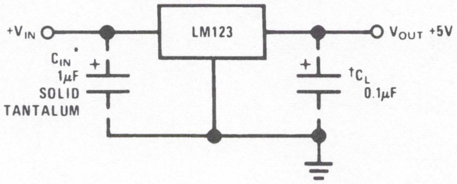


TL/H/7771-2

**Order Number LM123K STEEL or LM323K STEEL**
**See NS Package Number K02A**

## Typical Applications

**Basic 3 Amp Regulator**



TL/H/7771-3

*Required if LM123 is more than 4″ from filter capacitor.

†Regulator is stable with no load capacitor into resistive loads.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Input Voltage | 20V |
| Power Dissipation | Internally Limited |
| Operating Junction Temperature Range | |
| LM123 | −55°C to +150°C |
| LM323 | 0°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Preconditioning

| | |
|---|---|
| **Burn-In in Thermal Limit** | **100% All Devices** |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM123 | | | LM323 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_j = 25°C$<br>$V_{IN} = 7.5V$, $I_{OUT} = 0A$ | 4.7 | 5 | 5.3 | 4.8 | 5 | 5.2 | V |
| | $7.5V \leq V_{IN} \leq 15V$<br>$0A \leq I_{OUT} \leq 3A$, $P \leq 30W$ | 4.6 | | 5.4 | 4.75 | | 5.25 | V |
| Line Regulation (Note 3) | $T_j = 25°C$<br>$7.5V \leq V_{IN} \leq 15V$ | | 5 | 25 | | 5 | 25 | mV |
| Load Regulation (Note 3) | $T_j = 25°C$, $V_{IN} = 7.5V$,<br>$0A \leq I_{OUT} \leq 3A$ | | 25 | 100 | | 25 | 100 | mV |
| Quiescent Current | $7.5V \leq V_{IN} \leq 15V$,<br>$0A \leq I_{OUT} \leq 3A$ | | 12 | 20 | | 12 | 20 | mA |
| Output Noise Voltage | $T_j = 25°C$<br>$10\ Hz \leq f \leq 100\ kHz$ | | 40 | | | 40 | | μVrms |
| Short Circuit Current Limit | $T_j = 25°C$<br>$V_{IN} = 15V$<br>$V_{IN} = 7.5V$ | | 3<br>4 | 4.5<br>5 | | 3<br>4 | 4.5<br>5 | A<br>A |
| Long Term Stability | | | | 35 | | | 35 | mW |
| Thermal Resistance Junction to Case (Note 2) | | | 2 | | | 2 | | °C/W |

**Note 1:** Unless otherwise noted, specifications apply for $-55°C \leq T_j \leq +150°C$ for the LM123 and $0°C \leq T_j \leq +125°C$ for the LM323. Although power dissipation is internally limited, specifications apply only for $P \leq 30W$.

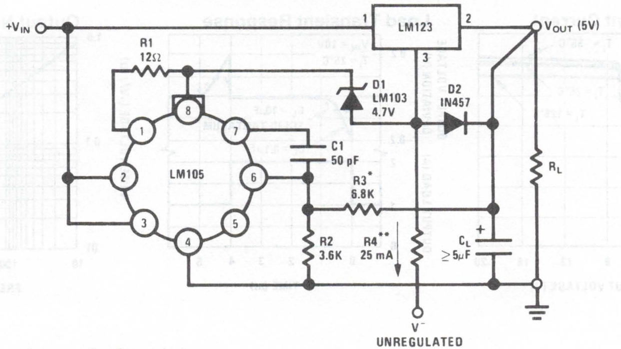
**Note 2:** Without a heat sink, the thermal resistance of the TO-3 package is about 35°C/W. With a heat sink, the effective thermal resistance can only approach the specified values of 2°C/W, depending on the efficiency of the heat sink.

**Note 3:** Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%.

**Note 4:** Refer to RETS123K drawing for military specifications for the LM123K.

## Typical Applications (Continued)

### Adjustable Output 5V–10V 0.1% Regulation



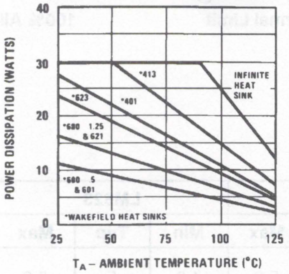
*Select to Set Output Voltage

**Select to Draw 25 mA from V⁻

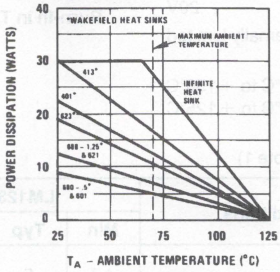
TL/H/7771–4

## Typical Performance Characteristics

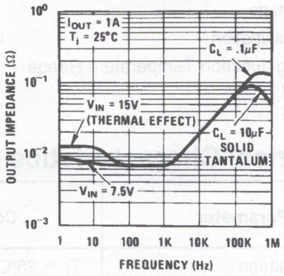
### Maximum Average Power Dissipation for LM123



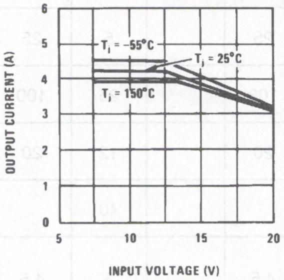
### Maximum Average Power Dissipation for LM323



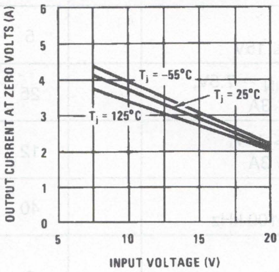
### Output Impedance



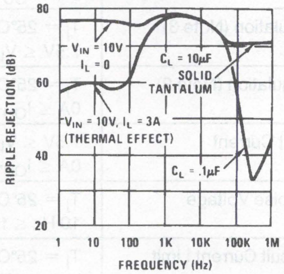
### Peak Available Output Current



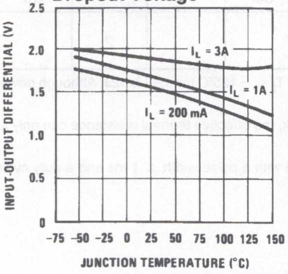
### Short Circuit Current



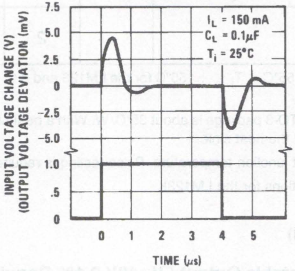
### Ripple Rejection



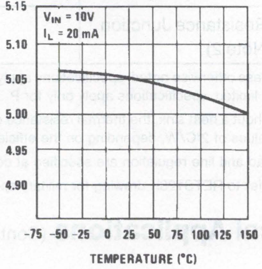
### Dropout Voltage



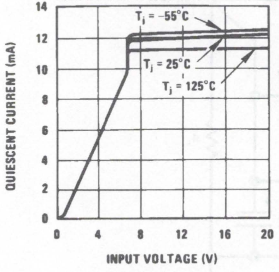
### Line Transient Response



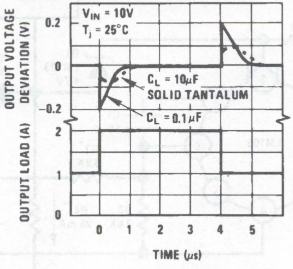
### Output Voltage



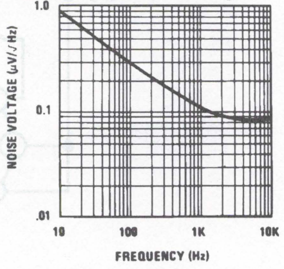
### Quiescent Current



### Load Transient Response



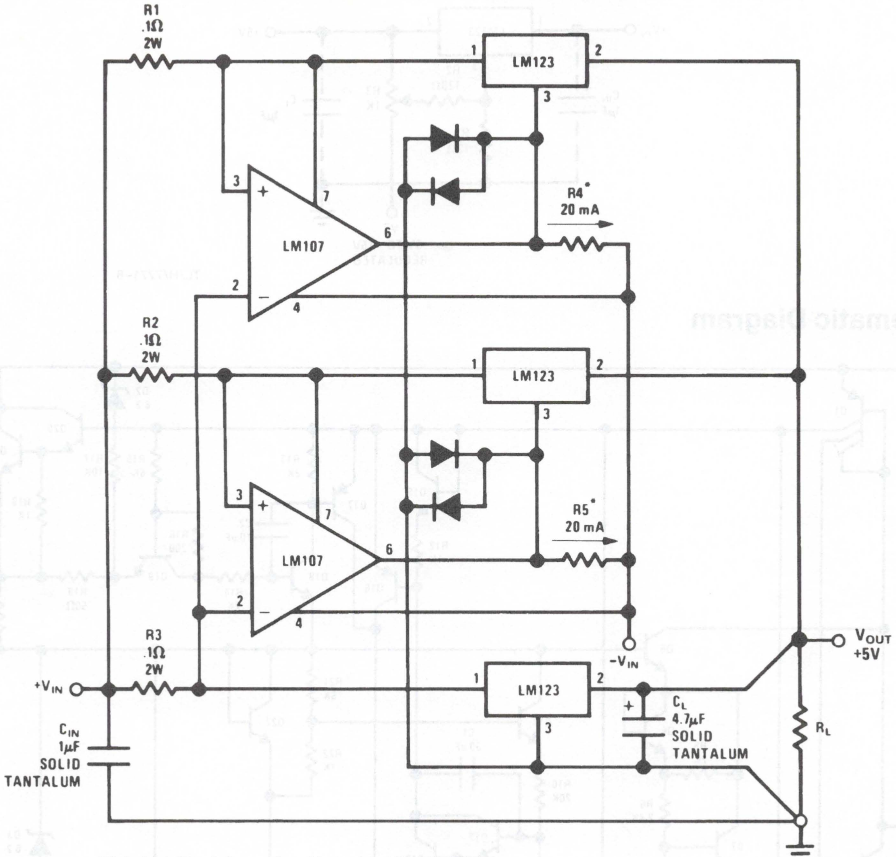
### Output Noise Voltage



TL/H/7771–5

# Typical Applications (Continued)

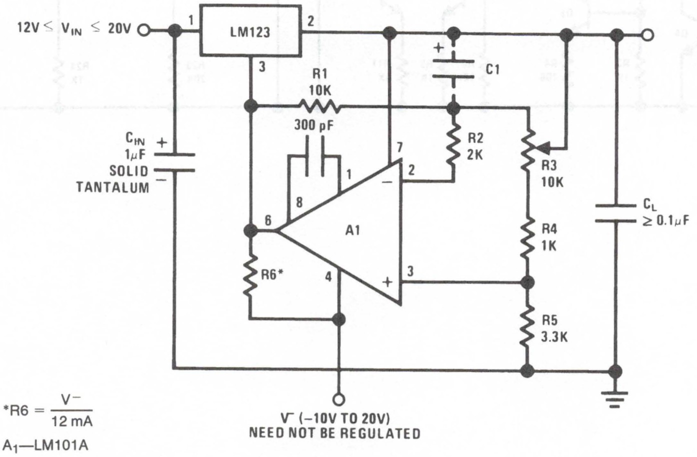
### 10 Amp Regulator with Complete Overload Protection


R1
.1Ω
2W
LM123
1
2
3
LM107
3
+
7
6
2
−
4
R4*
20 mA
R2
.1Ω
2W
LM123
1
2
3
LM107
3
+
7
6
2
−
4
R5*
20 mA
−V_IN
R3
.1Ω
2W
+V_IN
LM123
1
2
3
C_IN
1μF
SOLID
TANTALUM
+
C_L
4.7μF
SOLID
TANTALUM
V_OUT
+5V
R_L

*Select for 20 mA Current from Unregulated Negative Supply

TL/H/7771-6

### Adjustable Regulator 0V−10V @ 3A


12V ≤ V_IN ≤ 20V
1
LM123
2
3
R1
10K
300 pF
+
C1
R2
2K
R3
10K
C_IN
1μF
SOLID
TANTALUM
+
−
7
1
8
6
A1
−
2
+
3
4
R6*
R4
1K
R5
3.3K
C_L
≥ 0.1μF
V⁻ (−10V TO 20V)
NEED NOT BE REGULATED

$*R6 = \frac{V^-}{12\ mA}$

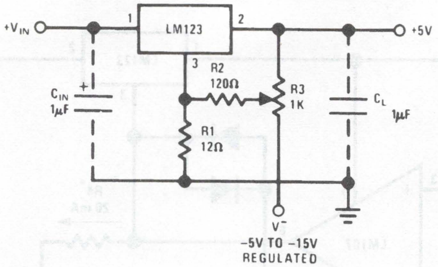
$A_1$—LM101A

$C_1$—2 μF Optional—Improves Ripple Rejection, Noise, and Transient Response

TL/H/7771-7

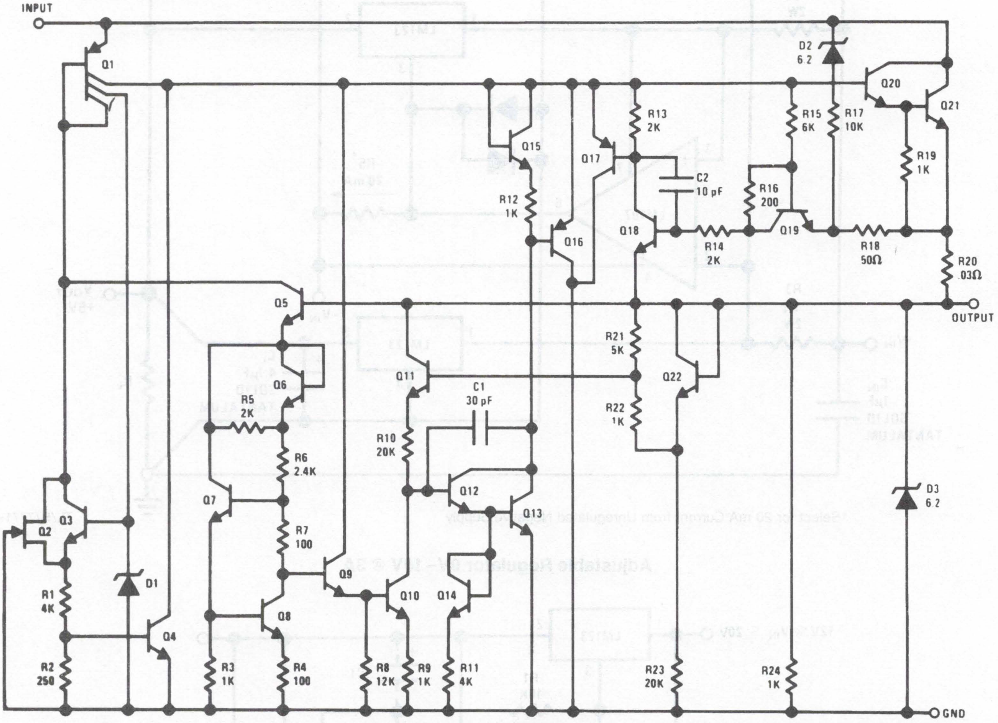
## Typical Applications (Continued)

### Trimming Output to 5V


+V_IN
1
LM123
2
+5V
3
C_IN
1µF
R2
120Ω
R3
1K
C_L
1µF
R1
12Ω
V⁻
−5V TO −15V
REGULATED

TL/H/7771-8

## Schematic Diagram


INPUT
Q1
D2
6.2
Q20
Q21
R13
2K
R15
6K
R17
10K
R19
1K
Q15
Q17
C2
10 pF
R16
200
R12
1K
Q16
Q18
R14
2K
Q19
R18
50Ω
R20
.03Ω
OUTPUT
Q5
R21
5K
Q22
Q6
Q11
C1
30 pF
R5
2K
R22
1K
R10
20K
R6
2.4K
Q12
Q7
Q13
D3
6.2
Q2
Q3
R7
100
R1
4K
D1
Q9
Q10
Q14
Q8
Q4
R2
250
R3
1K
R4
100
R8
12K
R9
1K
R11
4K
R23
20K
R24
1K
GND

TL/H/7771-1

**National Semiconductor Corporation**

# LM125/LM325/LM325A, LM126/LM326 Voltage Regulators

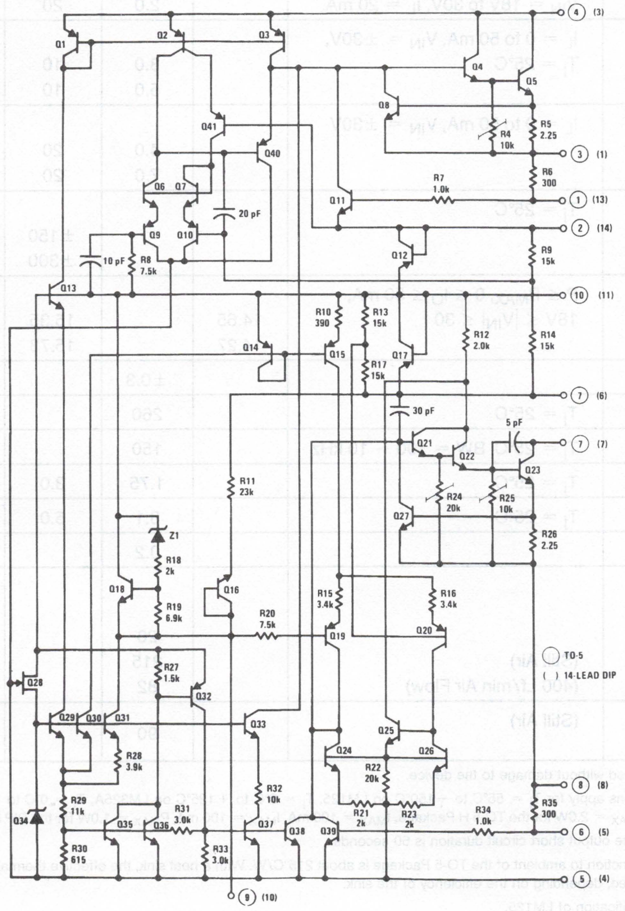
## General Description

These are dual polarity tracking regulators designed to provide balanced positive and negative output voltages at current up to 100 mA, the devices are set for ±15V and ±12V outputs respectively. Input voltages up to ±30V can be used and there is provision for adjustable current limiting. These devices are available in three package types to accommodate various power requirements and temperature ranges.

## Features

- ±15V and ±12V tracking outputs
- Output current to 100 mA
- Output voltage balanced to within 1% (LM125, LM126, LM325A)
- Line and load regulation of 0.06%
- Internal thermal overload protection
- Standby current drain of 3 mA
- Externally adjustable current limit
- Internal current limit

## Schematic and Connection Diagrams



Q1
Q2
Q3
Q4
Q5
Q8
Q41
Q40
Q6
Q7
Q9
Q10
20 pF
10 pF
R8 7.5k
Q13
Q11
Q12
R4 10k
R5 2.25
R6 300
R7 1.0k
R9 15k
R10 390
R13 15k
R12 2.0k
R14 15k
Q14
Q15
Q17
R17 15k
30 pF
5 pF
Q21
Q22
Q23
R11 23k
R24 20k
R25 10k
Q27
R26 2.25
Z1
R18 2k
R19 6.9k
Q18
Q16
R15 3.4k
R16 3.4k
R20 7.5k
Q19
Q20
R27 1.5k
Q28
Q32
Q29
Q30
Q31
Q33
Q25
Q24
Q26
R28 3.9k
R22 20k
R29 11k
R32 10k
R35 300
Q34
Q35
Q36
R31 3.0k
Q37
Q38
Q39
R21 2k
R23 2k
R34 1.0k
R30 615
R33 3.0k
4 (3)
3 (1)
1 (13)
2 (14)
10 (11)
7 (6)
7 (7)
8 (8)
6 (5)
5 (4)
9 (10)
TO-5
( ) 14-LEAD DIP

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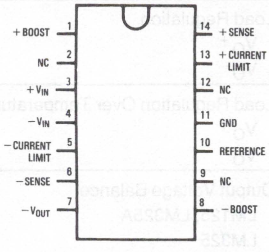
**Dual-In-Line Package**



+BOOST 1
NC 2
+V_IN 3
−V_IN 4
−CURRENT LIMIT 5
−SENSE 6
−V_OUT 7
14 +SENSE
13 +CURRENT LIMIT
12 NC
11 GND
10 REFERENCE
9 NC
8 −BOOST

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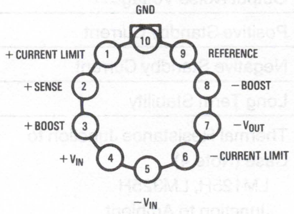
**Top View**

**Order Number LM325AN, LM325N or LM326N**

**See NS Package Number N14A**

**Metal Can Package**



GND
10
+CURRENT LIMIT 1
9 REFERENCE
+SENSE 2
8 −BOOST
+BOOST 3
7 −V_OUT
+V_IN 4
6 −CURRENT LIMIT
5
−V_IN

Case connected to $-V_{IN}$

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**Top View**

**Order Number LM125H, LM325H, LM126H or LM326H**

**See NS Package Number H10C**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 5)**

| | |
|---|---|
| Input Voltage | ±30V |
| Forced $V_O^+$ (Min) (Note 1) | −0.5V |
| Forced $V_O^-$ (Max) (Note 1) | +0.5V |
| Power Dissipation (Note 2) | $P_{MAX}$ |
| Output Short-Circuit Duration (Note 3) | Indefinite |

## Operating Conditions

| | |
|---|---|
| Operating Free Temperature Range | |
| LM125 | −55°C to +125°C |
| LM325, LM325A | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics LM125/LM325/LM325A (Note 2)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Voltage | $T_j$ = 25°C | | | | |
| LM125/LM325A | | 14.8 | 15 | 15.2 | V |
| LM325 | | 14.5 | 15 | 15.5 | V |
| Input-Output Differential | | 2.0 | | | V |
| Line Regulation | $V_{IN}$ = 18V to 30V, $I_L$ = 20 mA, $T_j$ = 25°C | | 2.0 | 10 | mV |
| Line Regulation Over Temperature Range | $V_{IN}$ = 18V to 30V, $I_L$ = 20 mA, | | 2.0 | 20 | mV |
| Load Regulation | $I_L$ = 0 to 50 mA, $V_{IN}$ = ±30V, $T_j$ = 25°C | | | | |
| $V_O^+$ | | | 3.0 | 10 | mV |
| $V_O^-$ | | | 5.0 | 10 | mV |
| Load Regulation Over Temperature Range | $I_L$ = 0 to 50 mA, $V_{IN}$ = ±30V | | | | |
| $V_O^+$ | | | 4.0 | 20 | mV |
| $V_O^-$ | | | 7.0 | 20 | mV |
| Output Voltage Balance | $T_j$ = 25°C | | | | |
| LM125, LM325A | | | | ±150 | mV |
| LM325 | | | | ±300 | mV |
| Output Voltage Over Temperature Range | $P \le P_{MAX}$, $0 \le I_O \le 50$ mA, $18V \le \lvert V_{IN} \rvert \le 30$ | | | | |
| LM125, LM325A | | 14.65 | | 15.35 | V |
| LM325 | | 14.27 | | 15.73 | V |
| Temperature Stability of $V_O$ | | | ±0.3 | | % |
| Short Circuit Current Limit | $T_j$ = 25°C | | 260 | | mA |
| Output Noise Voltage | $T_j$ = 25°C, BW = 100 − 10 kHz | | 150 | | μVrms |
| Positive Standby Current | $T_j$ = 25°C | | 1.75 | 3.0 | mA |
| Negative Standby Current | $T_j$ = 25°C | | 3.1 | 5.0 | mA |
| Long Term Stability | | | 0.2 | | %/kHr |
| Thermal Resistance Junction to Case (Note 4) | | | | | |
| LM125H, LM325H | | | 20 | | °C/W |
| Junction to Ambient | (Still Air) | | 215 | | °C/W |
| Junction to Ambient | (400 Lf/min Air Flow) | | 82 | | °C/W |
| Junction to Ambient<br>LM325AN, LM325N | (Still Air) | | 90 | | °C/W |

**Note 1:** That voltage to which the output may be forced without damage to the device.

**Note 2:** Unless otherwise specified these specifications apply for $T_j$ = 55°C to +150°C on LM125, $T_j$ = 0°C to +125°C on LM325A, $T_j$ = 0°C to +125°C on LM325, $V_{IN}$ = ±20V, $I_L$ = 0 mA, $I_{MAX}$ = 100 mA, $P_{MAX}$ = 2.0W for the TO-5 H Package. $I_{MAX}$ = 100 mA. $I_{MAX}$ = 100 mA, $P_{MAX}$ = 1.0W for the DIP N Package.

**Note 3:** If the junction temperature exceeds 150°C, the output short circuit duration is 60 seconds.

**Note 4:** Without a heat sink, the thermal resistance junction to ambient of the TO-5 Package is about 215°C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.

**Note 5:** Refer to RETS125X drawing for military specification of LM125.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Input Voltage | ±30V |
| Forced $V_O^+$ (Min) (Note 1) | −0.5V |
| Forced $V_O^-$ (Max) (Note 1) | +0.5V |
| Power Dissipation (Note 2) | Internally Limited |
| Output Short-Circuit Duration (Note 3) | Indefinite |

## Operating Conditions

| | |
|---|---|
| Operating Free Temperature Range | |
| LM126 | −55°C to +125°C |
| LM326 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics LM126/LM326 (Note 2)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Voltage<br>LM126/LM326 | $T_j = 25°C$ | 11.8<br>11.5 | 12 | 12.2<br>12.5 | V<br>V |
| Input-Output Differential | | 2.0 | | | V |
| Line Regulation | $V_{IN} = 15V$ to $30V$<br>$I_L = 20$ mA, $T_j = 25°C$ | | 2.0 | 10 | mV |
| Line Regulation Over Temperature Range | $V_{IN} = 15V$ to $30V$, $I_L = 20$ mA | | 2.0 | 20 | mV |
| Load Regulation<br>$V_O^+$<br>$V_O^-$ | $I_L = 0$ to $50$ mA, $V_{IN} = \pm 30V$,<br>$T_j = 25°C$ | | 3.0<br>5.0 | 10<br>10 | mV<br>mV |
| Load Regulation Over Temperature Range<br>$V_O^+$<br>$V_O^-$ | $I_L = 0$ to $50$ mA, $V_{IN} = \pm 30V$ | | 4.0<br>7.0 | 20<br>20 | mV<br>mV |
| Output Voltage Balance<br>LM126, LM326 | $T_j = 25°C$ | | | ±125<br>±250 | mV<br>mV |
| Output Voltage Over Temperature Range<br>LM126<br>LM326 | $P \le P_{MAX}$, $0 \le I_O \le 50$ mA,<br>$15V \le \lvert V_{IN} \rvert \le 30$ | 11.68<br>11.32 | | 12.32<br>12.68 | V<br>V |
| Temperature Stability of $V_O$ | | | ±0.3 | | % |
| Short Circuit Current Limit | $T_j = 25°C$ | | 260 | | mA |
| Output Noise Voltage | $T_j = 25°C$, BW $= 100 - 10$ kHz | | 100 | | μVrms |
| Positive Standby Current | $T_j = 25°C$, $I_L = 0$ | | 1.75 | 3.0 | mA |
| Negative Standby Current | $T_j = 25°C$, $I_L = 0$ | | 3.1 | 5.0 | mA |
| Long Term Stability | | | 0.2 | | %/kHr |
| Thermal Resistance Junction to Case (Note 4)<br>LM126H, LM326H<br>Junction to Ambient<br>Junction to Ambient | <br>(Still Air)<br>(400 Lf/min Air Flow) | | 20<br>215<br>82 | | °C/W<br>°C/W<br>°C/W |
| Junction to Ambient LM326N | | | 150 | | °C/W |

**Note 1:** That voltage to which the output may be forced without damage to the device.

**Note 2:** Unless otherwise specified these specifications apply for $T_j = 55°C$ to $+150°C$ on LM126, $T_j = 0°C$ to $+125°C$ on LM326, $V_{IN} = \pm 20V$, $I_L = 0$ mA, $I_{MAX} = 100$ mA, $P_{MAX} = 2.0W$ for the TO-5 H Package. $I_{MAX} = 100$ mA. $I_{MAX} = 100$ mA, $P_{MAX} = 1.0W$ for the DIP N Package.

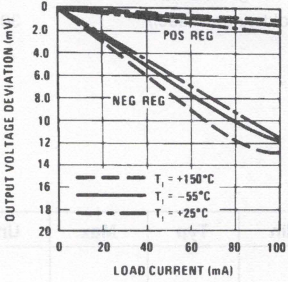
**Note 3:** If the junction temperature exceeds 150°C, the output short circuit duration is 60 seconds.

**Note 4:** Without a heat sink, the thermal resistance junction to ambient of the TO-5 Package is about 215°C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.

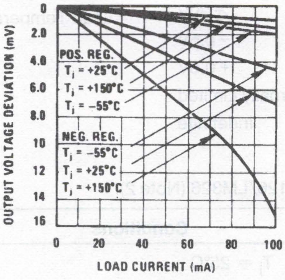
**Note 5:** Refer to RETS126X drawing for military specification of LM126.

## Typical Performance Characteristics

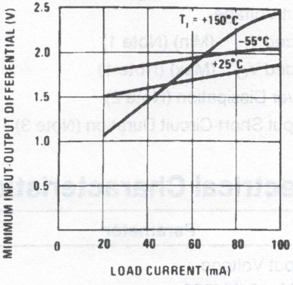
**LM125 Load Regulation**



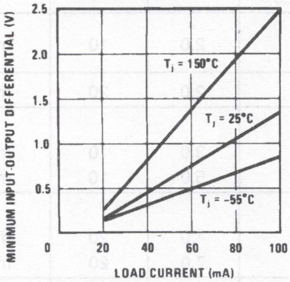
**LM126 Load Regulation**



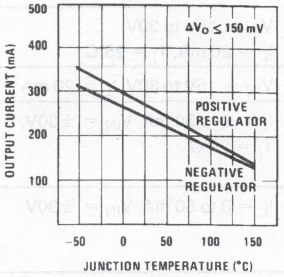
**LM125/126 Regulator Dropout Voltage for Positive Regulator**



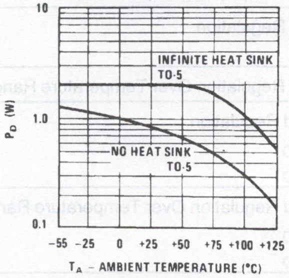
**LM125/126 Regulator Dropout Voltage for Negative Regulator**



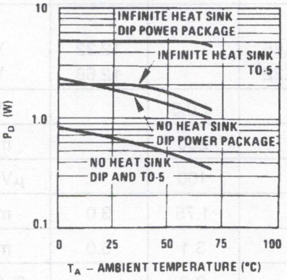
**LM125/126 Peak Output Current vs Junction Temperature**



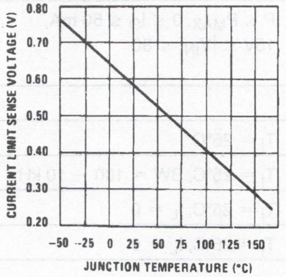
**LM125/126 Maximum Average Power Dissipation vs Ambient Temperature**



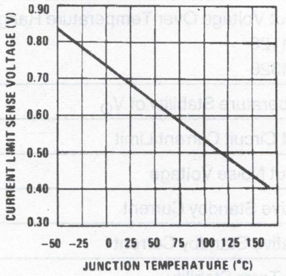
**LM325/326 Maximum Average Power Dissipation vs Ambient Temperature**



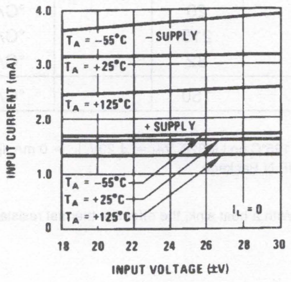
**LM125/126 Current Limit Sense Voltage vs Temperature for Negative Regulator**



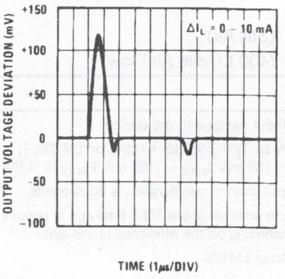
**LM125/126 Current Limit Sense Voltage vs Temperature for Positive Regulator**



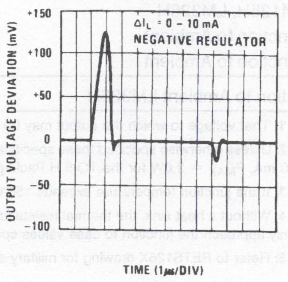
**LM125/126 Standby Current Drain**



**LM125 Load Transient Response for Negative Regulator**



**LM126 Load Transient Response**



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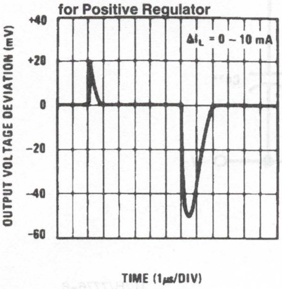
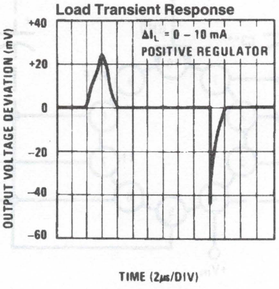
## Typical Performance Characteristics (Continued)

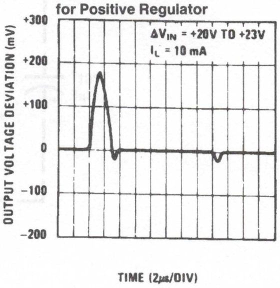
**LM125**
**Load Transient Response for Positive Regulator**



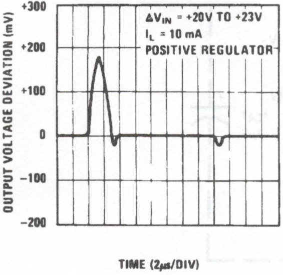
**LM126**
**Load Transient Response**



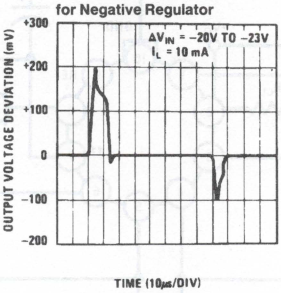
**LM125**
**Line Transient Response for Positive Regulator**



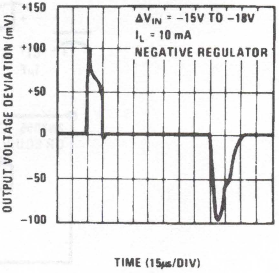
**LM126**
**Line Transient Response**



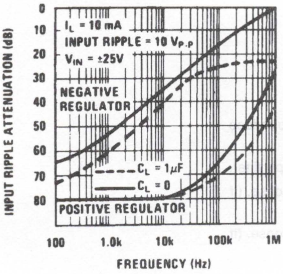
**LM125**
**Line Transient Response for Negative Regulator**



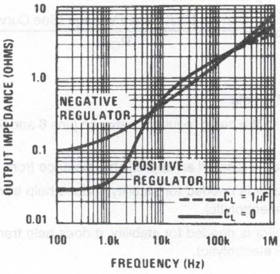
**LM126**
**Line Transient Response**



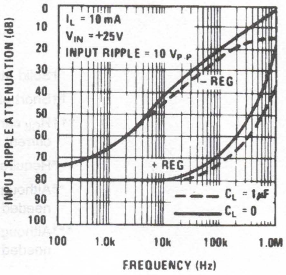
**LM125**
**Ripple Rejection**



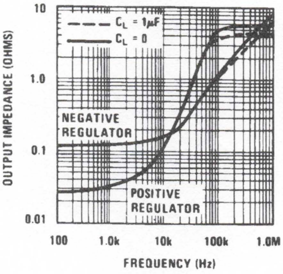
**LM125**
**Output Impedance vs Frequency**



**LM126**
**Ripple Rejection**



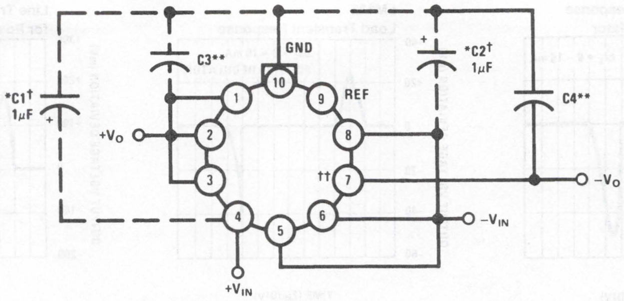
**LM126**
**Output Impedance vs Frequency**



TL/H/7776–5

## Typical Applications

### Basic Regulator†††


GND
C3**
*C2†
1μF
*C1†
1μF
REF
C4**
+VO
1
2
3
4
5
6
7
8
9
10
††
−VO
−VIN
+VIN

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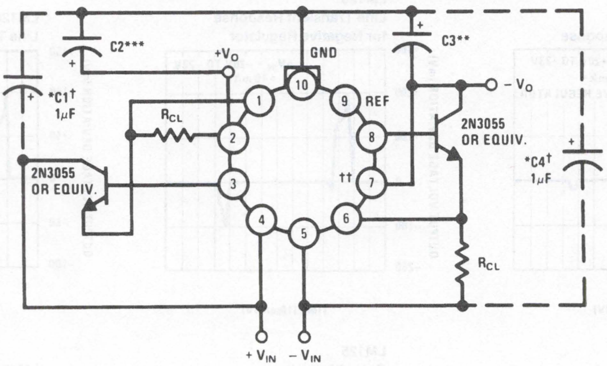
### 2.0 Amp Boosted Regulator With Current Limit


C2***
+VO
GND
C3**
*C1†
1μF
− VO
RCL
REF
2N3055
OR EQUIV.
2N3055
OR EQUIV.
*C4†
1μF
††
1
2
3
4
5
6
7
8
9
10
RCL
+ VIN
− VIN

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**Note:** Metal can (H) packages shown.

$$I_{CL} = \frac{\text{Current Limit Sense Voltage (See Curve)}}{R_{CL}}$$

†Solid tantalum

††Short pins 6 and 7 on dip

†††$R_{CL}$ can be added to the basic regulator between pins 6 and 5, 1 and 2 to reduce current limit.

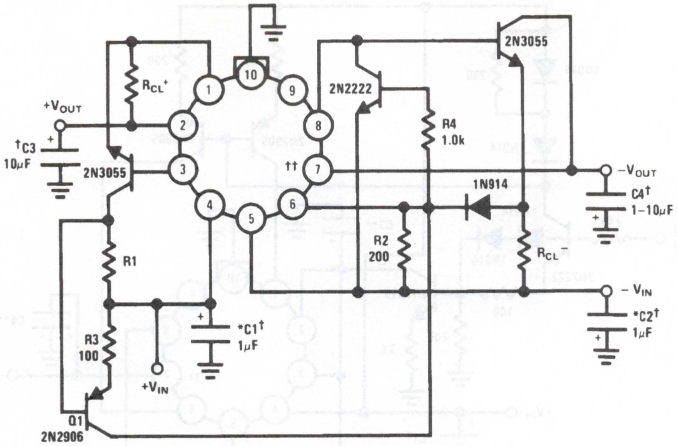
*Required if regulator is located an appreciable distance from power supply filter.

**Although no capacitor is needed for stability, it does help transient response. (If needed use 1 μF electrolytic).

***Although no capacitor is needed for stability, it does help transient response. (If needed use 10 μF electrolytic).

## Typical Applications (Continued)

### Positive Current Dependent Simultaneous Current Limiting


10
R<sub>CL</sub>+
1
9
2N2222
2N3055
+V<sub>OUT</sub>
2
8
R4
1.0k
†C3
10µF
2N3055
3
††
7
−V<sub>OUT</sub>
1N914
C4†
1–10µF
4
6
5
R2
200
R<sub>CL</sub>−
R1
− V<sub>IN</sub>
*C2†
1µF
*C1†
1µF
R3
100
+V<sub>IN</sub>
Q1
2N2906

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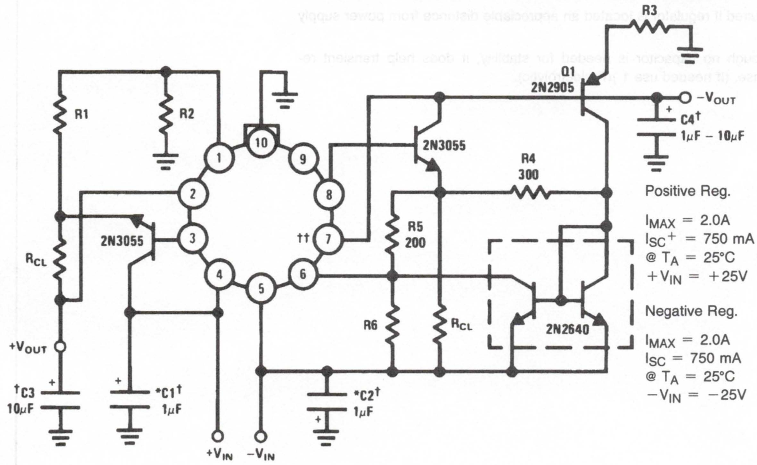
$$I_{CL}{}^{+} = \frac{\dfrac{V_{\text{SENSE NEG}}}{2} + V_{BEQ1}}{R1}$$

$$I_{CL}{}^{+} = \frac{V_{\text{SENSE NEG}} + V_{DIODE}}{R_{CL}{}^{-}}$$

$$R_{CL}{}^{+} = \frac{V_{SENSE}{}^{+}}{1.1\, I_{CL}{}^{+}}$$

$I_{CL}{}^{+}$ Controls Both Sides of the Regulator.

### Boosted Regulator With Foldback Current Limit


R3
Q1
2N2905
−V<sub>OUT</sub>
C4†
1µF – 10µF
R1
R2
10
9
1
2N3055
R4
300
2
8
2N3055
3
††
7
R5
200
R<sub>CL</sub>
4
5
6
R6
R<sub>CL</sub>
2N2640
+V<sub>OUT</sub>
†C3
10µF
*C1†
1µF
*C2†
1µF
+V<sub>IN</sub>
−V<sub>IN</sub>

Positive Reg.

$I_{MAX}$ = 2.0A
$I_{SC}{}^{+}$ = 750 mA
@ $T_A$ = 25°C
$+V_{IN}$ = +25V

Negative Reg.

$I_{MAX}$ = 2.0A
$I_{SC}$ = 750 mA
@ $T_A$ = 25°C
$-V_{IN}$ = −25V

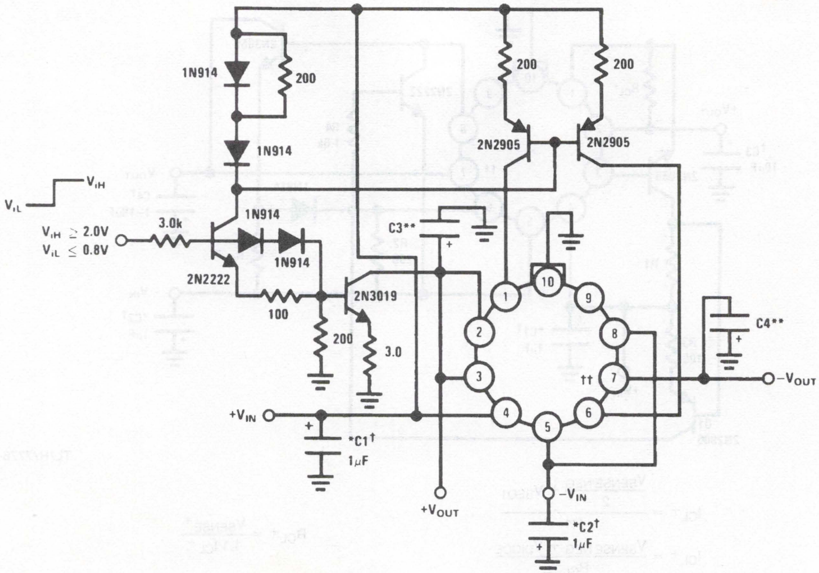
TL/H/7776–9

**Resistor Values**

| | 125 | 126 |
|---|---|---|
| R1 | 18 | 20 |
| R2 | 310 | 180 |
| R3 | 2.4k | 1.35k |
| R6 | 300 | 290 |
| $R_{CL}$ | 0.7 | 0.9 |

## Typical Applications (Continued)

### Electric Shutdown


1N914
200
1N914
200
200
2N2905
2N2905
$V_{IL}$
$V_{IH}$
$V_{IH} \geq 2.0V$
$V_{IL} \leq 0.8V$
3.0k
1N914
1N914
2N2222
C3**
100
2N3019
200
3.0
1
2
3
4
5
6
7
8
9
10
††
C4**
$-V_{OUT}$
$+V_{IN}$
*C1†
1µF
$+V_{OUT}$
$-V_{IN}$
*C2†
1µF

TL/H/7776-10

†Solid tantalum

††Short pins 6 and 7 on dip

*Required if regulator is located an appreciable distance from power supply filter.

**Although no capacitor is needed for stability, it does help transient response. (If needed use 1 µF electrolytic).

**National Semiconductor Corporation**

# LM133/LM333 3-Ampere Adjustable Negative Regulators

## General Description

The LM133/LM333 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −3.0A over an output voltage range of −1.2V to −32V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low themal transients. Further, the LM133 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

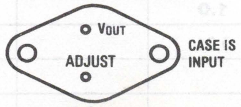
The LM133/LM333 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM133/LM333 are ideal complements to the LM150/LM350 adjustable positive regulators.

## Features

- Output voltage adjustable from −1.2V to −32V
- 3.0A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output is short circuit protected

## Connection Diagrams

**TO-3**
**Metal Can Package**

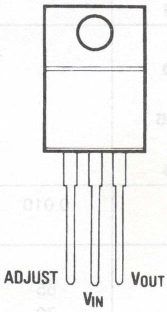


TL/H/9065–1

**Bottom View**

**Steel TO-3 Metal Can Package (K STEEL)**
**Order Number LM133K STEEL or LM333K STEEL**
**See NS Package Number K02A**

**TO-220**
**Plastic Package**



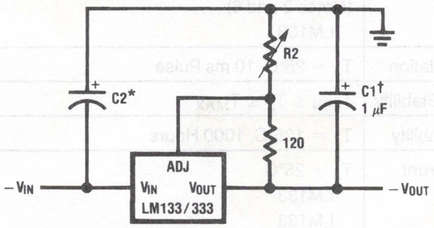
TL/H/9065–2

**Bottom View**

**3-Lead TO-220 Plastic Package (T)**
**Order Number LM333T**
**See NS Package Number T03B**

## Typical Applications

**Adjustable Negative Voltage Regulator**



TL/H/9065–3

Full output current not available at high input-output voltages.

$$-V_{OUT} = -1.25V\left(1+\frac{R2}{120\Omega}\right)+\left(-I_{ADJ}\times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4″ from power supply filter capacitor.

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input-Output Voltage Differential | 35V |
| Operating Junction Temperature Range | $T_{MIN}$ to $T_{MAX}$ |
| LM133 | −55°C to +150°C |
| LM333 | −40°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | |
| TO-3 Package | 300°C |
| TO-220 Package | 260°C |

## Preconditioning

| | |
|---|---|
| Burn-In In Thermal Limit | 100% All Devices |

## Electrical Characteristics LM133 (Note 1) (Note 5)

| Parameter | Conditions | Typical | Tested Limit (Note 3) | Design Limit (Note 4) | Units (Max Unless Noted) |
|---|---|---|---|---|---|
| Reference Voltage | $T_J = 25°C, I_L = 10\ mA$ | −1.250 | −1.238<br>−1.262 | | V(MIN)<br>V(MAX) |
| | $T_{MIN} \le T_J \le T_{MAX}, 3V \le \lvert V_{IN} - V_{OUT} \rvert \le 35V,$<br>$10\ mA \le I_L \le 3A, P \le P_{MAX}$<br>LM133<br>LM133 | **−1.250** | **−1.225**<br>**−1.275** | | V(MIN)<br>V(MAX) |
| Line Regulation | $T_J = 25°C, 3V \le \lvert V_{IN} - V_{OUT} \rvert \le 35V,$<br>$I_{OUT} = 50\ mA$ (Note 2) | 0.01 | 0.02 | | % /V |
| | LM133 | **0.02** | **0.05** | | % /V |
| Load Regulation | $T_J = 25°C, 10\ mA \le I_{OUT} \le 3A, P \le P_{MAX}$<br>(Notes 2 and 6) | 0.2 | 0.5 | | % |
| | LM133 | **0.4** | **1.0** | | % |
| Thermal Regulation | $T_J = 25°C$, 10 ms Pulse | 0.002 | 0.01 | | % /W |
| Temperature Stability | $T_{MIN} \le T_J \le T_{MAX}$ | 0.4 | | | % |
| Long Term Stability | $T_J = 125°C$, 1000 Hours | 0.15 | | 0.8 | % |
| Adjust Pin Current | $T_J = 25°C$ | | | | |
| | LM133 | 65 | 90 | | μA |
| | LM133 | **70** | **100** | | μA |
| Adjust Pin Current Change | $T_J = 25°C, 10\ mA \le I_L \le 3A$ | 2 | 5 | **6** | μA |
| | $T_J = 25°C, 3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 35V$ | 2 | 5 | **6** | μA |
| Minimum Load Current | $\lvert V_{IN} - V_{OUT} \rvert \le 35V, T_J = 25°C$<br>LM133 | **2.5** | **5.0** | | mA |
| | $\lvert V_{IN} - V_{OUT} \rvert \le 10V, T_J = 25°C$<br>LM133 | **1.2** | **2.5** | | mA |
| Current Limit (Note 6) | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 10V, T_J = 25°C$<br>LM133 | **3.9** | **3.0** | | A(MIN) |
| | $\lvert V_{IN} - V_{OUT} \rvert = 20V, T_J = 25°C$<br>LM133 | **2.4** | **1.25** | | A(MIN) |
| | $\lvert V_{IN} - V_{OUT} \rvert = 30V, T_J = 25°C$<br>LM133 | 0.4 | **0.3** | | A(MIN) |
| Output Noise (% of $V_{OUT}$) | 10 Hz to 10 kHz, $T_J = 25°C$ | 0.003 | | 0.010 | % (rms) |
| Ripple Rejection | $V_{OUT} = 10V, f = 120\ Hz, T_J = 25°C$ | | | | |
| | $C_{ADJ} = 0\ \mu F$ | 60 | | 55 | dB |
| | $C_{ADJ} = 10\ \mu F$ | 77 | | 70 | dB |
| Thermal Resistance | TO-3 Package (K STEEL) | 1.2 | | 1.8 | °C/W |
| | TO-220 Package (T) | 3 | | 4 | °C/W |
| Thermal Shutdown Temperature | LM133 | 163 | 150 | | °C(MIN) |
| | LM133 | | | 190 | °C(MAX) |

## Electrical Characteristics LM133 (Note 1) **(Note 5)**

| Parameter | Conditions | Typical | Tested Limit (Note 3) | Design Limit (Note 4) | Units (Max Unless Noted) | |
|---|---|---|---|---|---|---|
| Reference Voltage | $T_J = 25°C, I_L = 10$ mA<br>$T_{MIN} \leq T_J \leq T_{MAX}, 3V \leq \lvert V_{IN} - V_{OUT} \rvert \leq 35V$, $10 \text{ mA} \leq I_L \leq 3A, P \leq P_{MAX}$ | −1.250<br>**−1.250** | −1.225<br>−1.275 | **−1.213**<br>**−1.287** | V(MIN)<br>V(MAX)<br>V(MIN)<br>V(MAX) | |
| Line Regulation | $T_J = 25°C, 3V \leq \lvert V_{IN} - V_{OUT} \rvert \leq 35V$, $I_{OUT} = 50$ mA (Note 2) | 0.001<br>**0.02** | 0.004 | **0.07** | % /V<br>% /V | |
| Load Regulation | $T_J = 25°C, 10 \text{ mA} \leq I_{OUT} \leq 3A, P \leq P_{MAX}$ (Notes 2 and 6) | 0.2<br>**0.4** | 1.0 | **1.5** | %<br>% | |
| Thermal Regulation | $T_J = 25°C$, 10 ms Pulse | 0.002 | 0.02 | | % /W | |
| Temperature Stability | $T_{MIN} \leq T_J \leq T_{MAX}$ | 0.5 | | | % | |
| Long Term Stability | $T_J = 125°C$, 1000 Hours | 0.2 | | 0.8 | % | |
| Adjust Pin Current | $T_J = 25°C$ | 65<br>**70** | 95 | **100** | $\mu$A<br>$\mu$A | |
| Adjust Pin Current Change | $T_J = 25°C, 10 \text{ mA} \leq I_L \leq 3A$<br>$T_J = 25°C, 3.0V \leq \lvert V_{IN} \leq \leq 35V$ | 2.5<br>2.5 | 7<br>7 | **8**<br>**8** | $\mu$A<br>$\mu$A | 7 |
| Minimum Load Current | $\lvert V_{IN} - V_{OUT} \rvert \leq 35V, T_J = 25°C$<br>$\lvert V_{IN} - V_{OUT} \rvert \leq 10V, T_J = 25°C$ | **2.5**<br>**1.5** | 10<br>5.0 | **10**<br>**5.0** | mA<br>mA | |
| Current Limit (Note 6) | $3V \leq \lvert V_{IN} - V_{OUT} \rvert \leq 10V, T_J = 25°C$<br>$\lvert V_{IN} - V_{OUT} \rvert = 20V, T_J = 25°C$<br>$\lvert V_{IN} - V_{OUT} \rvert = 30V, T_J = 25°C$ | **3.9**<br>**2.4**<br>0.4 | 2.0<br>1.0<br>0.20 | **3.0**<br>**1.0**<br>**0.2** | A(MIN)<br>A(MIN)<br>A(MIN) | |
| Output Noise (% of $V_{OUT}$) | 10 Hz to 10 kHz, $T_J = 25°C$ | 0.003 | | 0.010 | % (rms) | |
| Ripple Rejection | $V_{OUT} = 10V, f = 120 \text{ Hz}, T_J = 25°C$<br>$C_{ADJ} = 0\ \mu F$<br>$C_{ADJ} = 10\ \mu F$ | 60<br>77 | | 50<br>66 | dB<br>dB | |
| Thermal Resistance Junction to Case | TO-3 Package (K STEEL)<br>TO-220 Package (T) | 1.2<br>3 | | 1.8<br>4 | °C/W<br>°C/W | |
| Thermal Shutdown Temperature | | 163 | | 150<br>190 | °C(MIN)<br>°C(MAX) | |
| Thermal Resistance Junction to Ambient (No Heatsink) | K Package<br>T Package | 35<br>50 | | | °C/W<br>°C/W | |

**Note 1:** Unless otherwise specified, these specifications apply: $-55°C \leq T_J \leq +150°C$ for the LM133; and $-40°C \leq T_J + 125°C$ for the LM333; $\lvert V_{IN} - V_{OUT} \rvert = 5V$; and $I_{OUT} = 0.5A$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 30W.

**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8″ below the base of the TO-3 package.

**Note 3:** Testing limits are guaranteed and 100% tested in production.

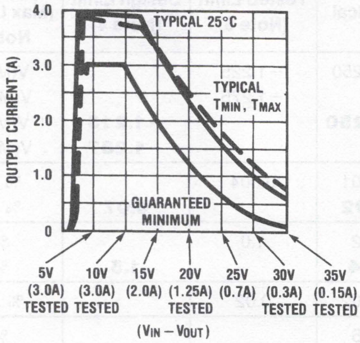
**Note 4:** Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

**Note 5:** Specifcations in **boldface** apply over the full rated temperature range.

**Note 6:** The output capability of the LM333 is guaranteed at 3A in the range of $3V \leq \lvert V_{IN} - V_{OUT} \rvert \leq 10V$. At voltages above 10V, the available output current decreases, but in the range $10V \leq \lvert V_{IN} - V_{OUT} \rvert \leq 15V$, the available current is $30W - \lvert V_{IN} - V_{OUT} \rvert$. At voltages higher than 15V, refer to graphs for actual guaranteed output current available.

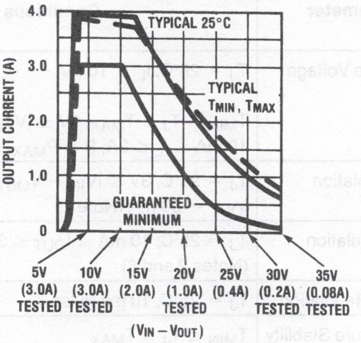
## Guaranteed Performance Characteristics

**LM133 Guaranteed Output Current**



TL/H/9065–4

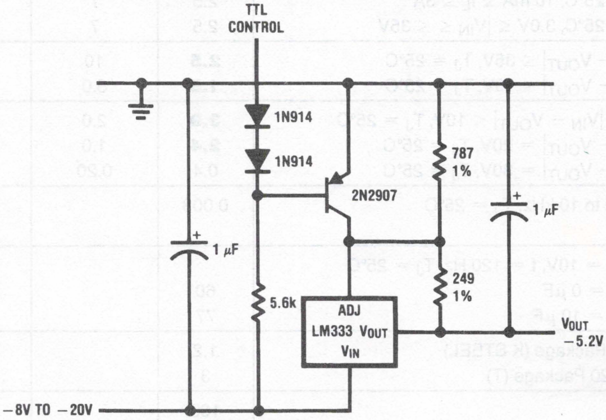
**LM333 Guaranteed Output Current**



TL/H/9065–5

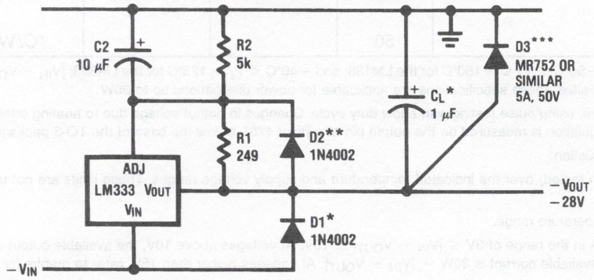
## Typical Applications (Continued)

**−5.2V Regulator with Electronic Shutdown***


TTL
CONTROL
1N914
1N914
2N2907
787
1%
1 μF
1 μF
5.6k
249
1%
ADJ
LM333 VOUT
VIN
VOUT
–5.2V
–8V TO –20V

TL/H/9065–6

**Negative Regulator with Protection Diodes**


C2
10 μF
R2
5k
R1
249
D2**
1N4002
D1*
1N4002
CL*
1 μF
D3***
MR752 OR
SIMILAR
5A, 50V
ADJ
LM333 VOUT
VIN
–VOUT
–28V
–VIN

*When $C_L$ is larger than 20 μF, D1 protects the LM133 in case the input supply is shorted.

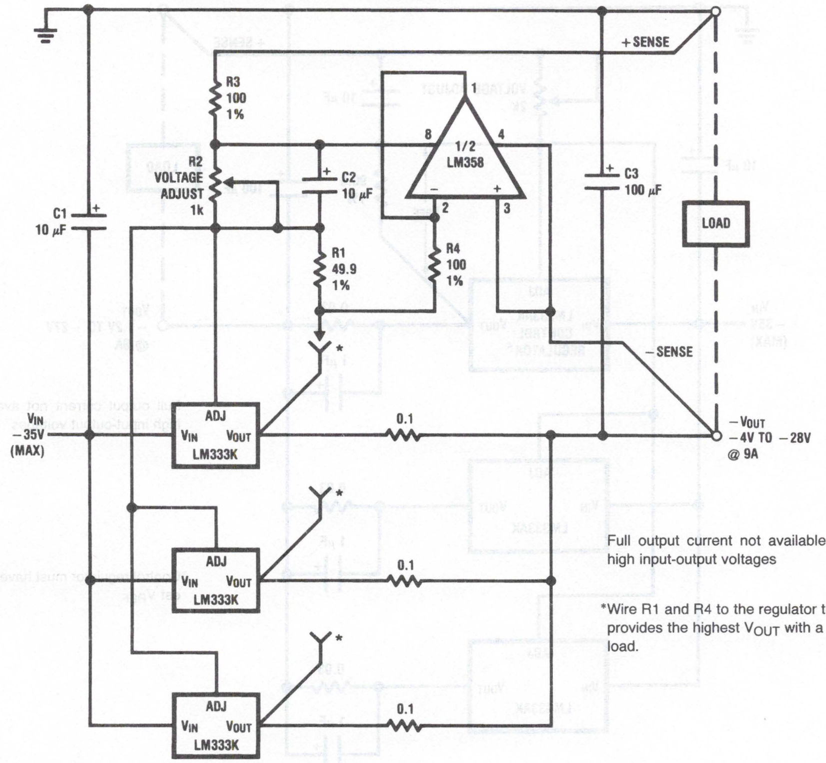
**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protect the LM133 in case the output is shorted.

***In case $V_{OUT}$ is shorted to a positive supply, D3 protects the LM133 from overvoltage, and protects the load from reversed voltage.

TL/H/9065–7

## Typical Applications (Continued)

### High-Performance 9-Ampere Adjustable Regulator

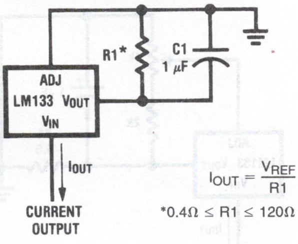

+SENSE
R3
100
1%
R2
VOLTAGE
ADJUST
1k
C2
10 μF
1/2
LM358
1
8
4
2
3
C3
100 μF
LOAD
C1
10 μF
R1
49.9
1%
R4
100
1%
*
−SENSE
V_IN
−35V
(MAX)
ADJ
V_IN
V_OUT
LM333K
0.1
−V_OUT
−4V TO −28V
@ 9A

Full output current not available at high input-output voltages

*Wire R1 and R4 to the regulator that provides the highest $V_{OUT}$ with a 3A load.

TL/H/9065-8

### Current Regulator

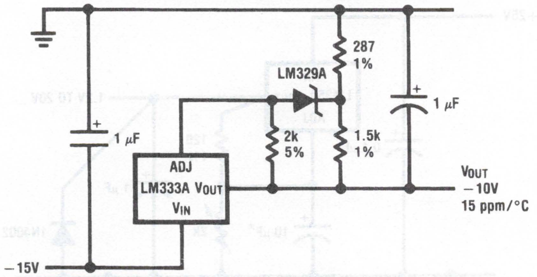

ADJ
LM133 V_OUT
V_IN
R1*
C1
1 μF
I_OUT
CURRENT
OUTPUT

$I_{OUT} = \frac{V_{REF}}{R1}$

*0.4Ω ≤ R1 ≤ 120Ω

TL/H/9065-9

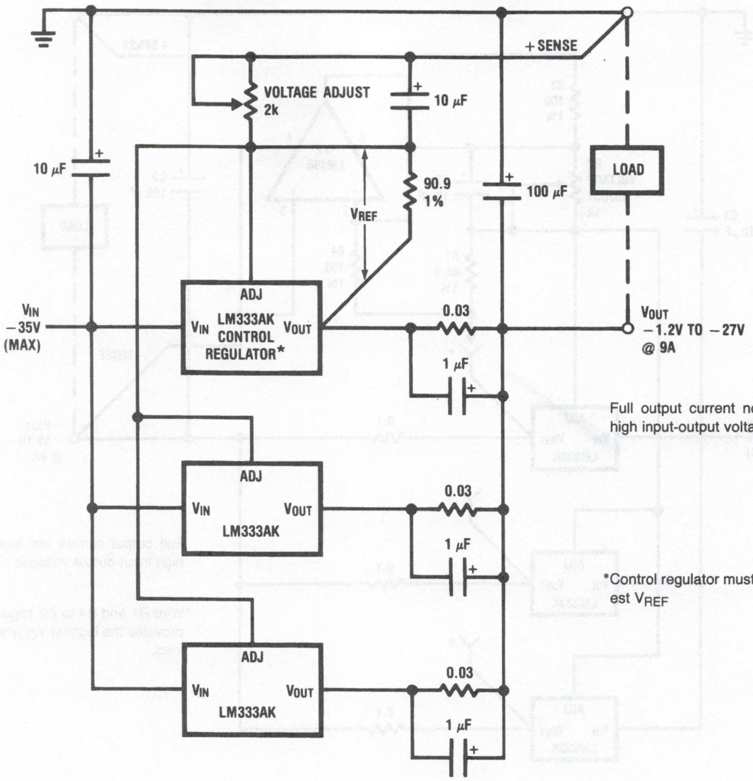
### High Stability—10V Regulator


287
1%
LM329A
1 μF
1 μF
2k
5%
1.5k
1%
ADJ
LM333A V_OUT
V_IN
−15V
V_OUT
−10V
15 ppm/°C

TL/H/9065-10

## Typical Applications (Continued)

### High-Current Adjustable Regulator

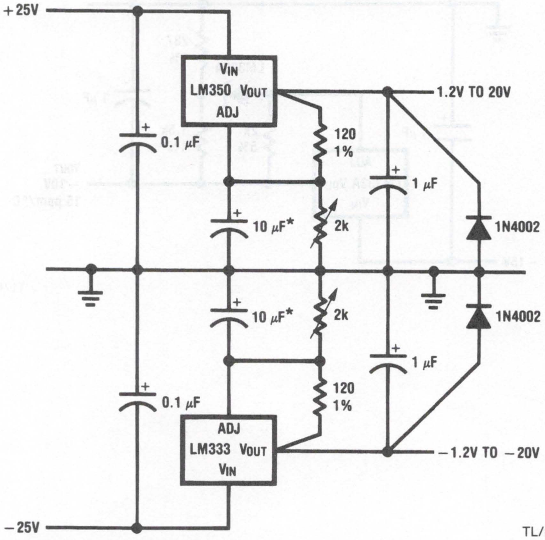

+SENSE
VOLTAGE ADJUST
2k
10 μF
10 μF
90.9
1%
VREF
100 μF
LOAD
VIN
−35V
(MAX)
ADJ
VIN
LM333AK
CONTROL
REGULATOR*
VOUT
0.03
1 μF
VOUT
−1.2V TO −27V
@ 9A
ADJ
VIN
VOUT
LM333AK
0.03
1 μF
ADJ
VIN
VOUT
LM333AK
0.03
1 μF

Full output current not available at high input-output voltages

*Control regulator must have the largest $V_{REF}$

TL/H/9065–11

### Adjutable Lab Voltage Regulator

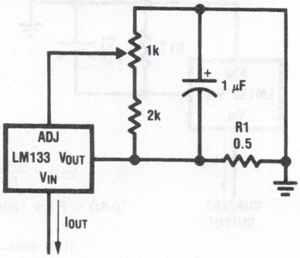

+25V
VIN
LM350
VOUT
ADJ
1.2V TO 20V
0.1 μF
120
1%
1 μF
10 μF*
2k
1N4002
10 μF*
2k
1N4002
1 μF
0.1 μF
120
1%
ADJ
LM333
VOUT
VIN
−1.2V TO −20V
−25V

TL/H/9065–12

Full output current not available at high input-output voltages.

*The 10 μF capacitors are optional to improve ripple rejection.

### Adjustable Current Regulator


1k
1 μF
2k
ADJ
LM133
VOUT
VIN
R1
0.5
IOUT

TL/H/9065–13

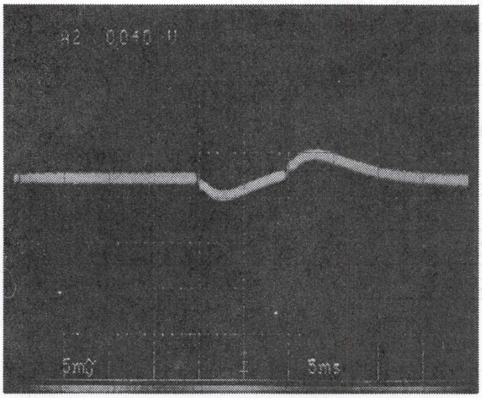
$$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\% \text{ adjustable}$$

## Typical Applications (Continued)

### THERMAL REGULATION

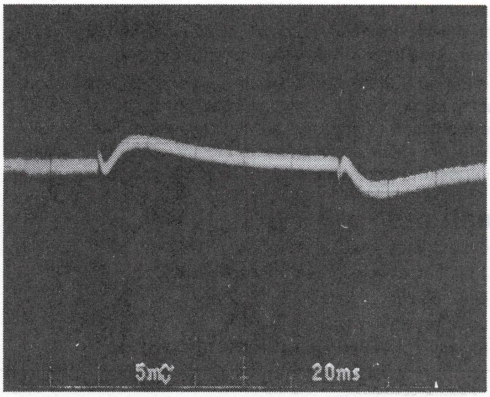
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since the power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of $V_{OUT}$, per watt, within the first 10 rms after a step of power is applied. The LM133's specification is 0.01%/W, max.

In *Figure 1,* a typical LM133's output drifts only 2 mV (or 0.02% of $V_{OUT} = -10V$) when a 20W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.01%/W×20W = 0.2% max. When the 20W pulse is ended, the thermal regulation again shows a 2 mV step as the LM133 chip cools off. Note that the load regulation error of about 1 mV (0.01%) is additional to the thermal regulation error. In *Figure 2,* when the 20W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



TL/H/9065–14

**FIGURE 1**



TL/H/9065–15

**FIGURE 2**

National
Semiconductor
Corporation

# LM137/LM337 3-Terminal Adjustable Negative Regulators

## General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

## Features

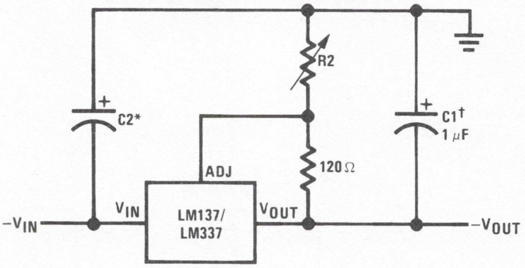
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output is short circuit protected

**LM137 Series Packages and Power Capability**

| Device | Package | Rated Power Dissipation | Design Load Current |
|---|---|---|---|
| LM137/337 | TO-3<br>TO-39 | 20W<br>2W | 1.5A<br>0.5A |
| LM337T | TO-220 | 15W | 1.5A |
| LM337M | TO-202 | 7.5W | 0.5A |

## Typical Applications

**Adjustable Negative Voltage Regulator**



TL/H/9067-1

Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1+\frac{R2}{120\Omega}\right)+\left(-I_{ADJ}\times R2\right)$$

†C1 = 1 µF solid tantalum or 10 µF aluminum electrolytic required for stability

*C2 = 1 µF solid tantalum is required only if regulator is more than 4″ from power-supply filter capacitor

Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input-Output Voltage Differential | 40V |
| Operating Junction Temperature Range | |
| LM137 | −55°C to +150°C |
| LM337 | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| Plastic Package (Soldering, 4 sec.) | 260°C |
| ESD Rating | 2k Volts |

## Preconditioning

| | |
|---|---|
| **Burn-In in Thermal Limit** | **100% All Devices** |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM137 | | | LM337 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_j = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2) $I_L = 10$ mA | | 0.01 | 0.02 | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_j = 25°C$, $10\text{ mA} \le I_{OUT} \le I_{MAX}$ | | 0.3 | 0.5 | | 0.3 | 1.0 | % |
| Thermal Regulation | $T_j = 25°C$, 10 ms Pulse | | 0.002 | 0.02 | | 0.003 | 0.04 | %/W |
| Adjustment Pin Current | | | 65 | 100 | | 65 | 100 | μA |
| Adjustment Pin Current Charge | $10\text{ mA} \le I_L \le I_{MAX}$<br>$3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$,<br>$T_A = 25°C$ | | 2 | 5 | | 2 | 5 | μA |
| Reference Voltage | $T_j = 25°C$ (Note 3) | −1.225 | −1.250 | −1.275 | −1.213 | −1.250 | −1.287 | V |
| | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3)<br>$10\text{ mA} \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$ | −1.200 | −1.250 | −1.300 | −1.200 | −1.250 | −1.300 | V |
| Line Regulation | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2) | | 0.02 | 0.05 | | 0.02 | 0.07 | %/V |
| Load Regulation | $10\text{ mA} \le I_{OUT} \le I_{MAX}$, (Note 2) | | 0.3 | 1 | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \le T_j \le T_{MAX}$ | | 0.6 | | | 0.6 | | % |
| Minimum Load Current | $\lvert V_{IN} - V_{OUT} \rvert \le 40V$ | | 2.5 | 5 | | 2.5 | 10 | mA |
| | $\lvert V_{IN} - V_{OUT} \rvert \le 10V$ | | 1.2 | 3 | | 1.5 | 6 | mA |
| Current Limit | $\lvert V_{IN} - V_{OUT} \rvert \le 15V$ | | | | | | | |
| | K and T Package | 1.5 | 2.2 | 3.5 | 1.5 | 2.2 | 3.7 | A |
| | H and P Package | 0.5 | 0.8 | 1.8 | 0.5 | 0.8 | 1.9 | A |
| | $\lvert V_{IN} - V_{OUT} \rvert = 40V$, $T_j = 25°C$ | | | | | | | |
| | K and T Package | 0.24 | 0.4 | | 0.15 | 0.4 | | A |
| | H and P Package | 0.15 | 0.17 | | 0.10 | 0.17 | | A |
| RMS Output Noise, % of $V_{OUT}$ | $T_j = 25°C$, $10\text{ Hz} \le f \le 10\text{ kHz}$ | | 0.003 | | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = -10V$, $f = 120$ Hz | | 60 | | | 60 | | dB |
| | $C_{ADJ} = 10\ \mu F$ | 66 | 77 | | 66 | 77 | | dB |
| Long-Term Stability | $T_j = 125°C$, 1000 Hours | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | H Package | | 12 | 15 | | 12 | 15 | °C/W |
| | K Package | | 2.3 | 3 | | 2.3 | 3 | °C/W |
| | T Package | | | | | 4 | | °C/W |
| | P Package | | | | | 7 | | °C/W |
| Thermal Resistance, Junction to Ambient (No Heat Sink) | H Package | | 140 | | | 140 | | °C/W |
| | K Package | | 35 | | | 35 | | °C/W |
| | T Package | | | | | 50 | | °C/W |
| | P Package | | | | | 80 | | °C/W |

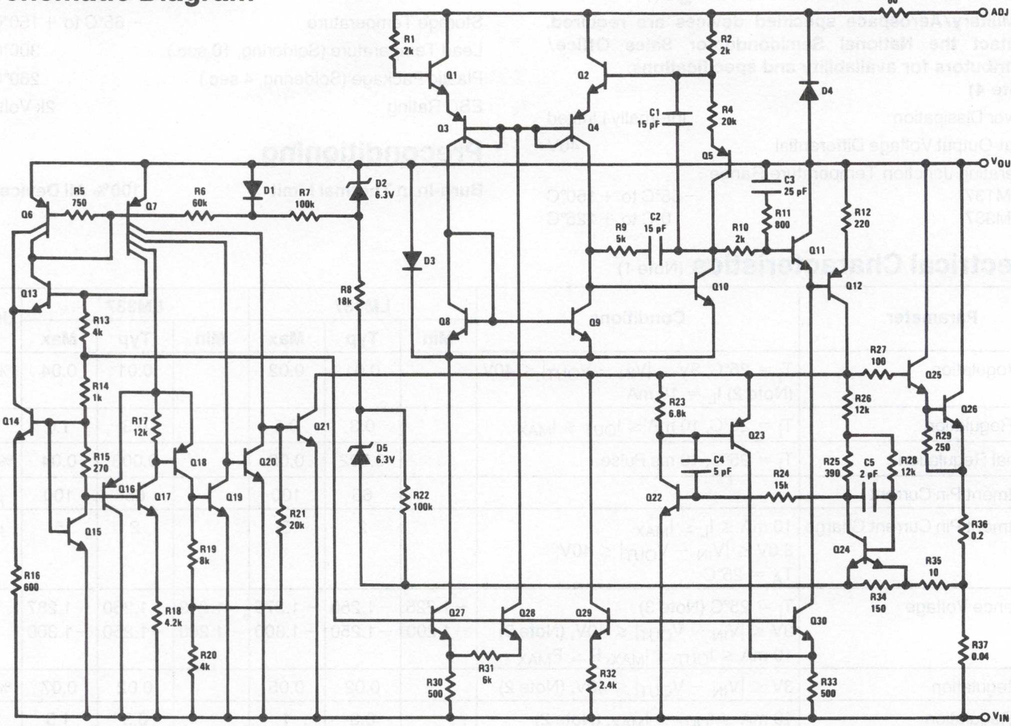
**Note 1:** Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202 and 20W for the TO-3 and TO-220. $I_{MAX}$ is 1.5A for the TO-3 and TO-220 packages, and 0.5A for the TO-202 package and 0.2A for the TO-39 package.

**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point ⅛″ below the base of the TO-3 and TO-39 packages.

**Note 3:** Selected devices with tightened tolerance reference voltage available.

**Note 4:** Refer to RETS137H drawing for LM137H or RETS137K drawing for LM137K military specifications.

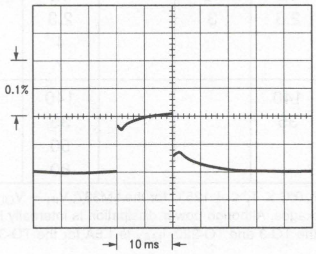
## Schematic Diagram


R1 2k
Q1
R2 2k
Q2
R3 60
ADJ
D4
C1 15 pF
R4 20k
Q3
Q4
Q5
VOUT
C3 25 pF
R11 800
R12 220
R10 2k
Q11
R9 5k
C2 15 pF
Q10
Q12
Q6
R5 750
Q7
R6 60k
D1
R7 100k
D2 6.3V
D3
R8 18k
Q8
Q9
Q13
R13 4k
R14 1k
Q14
R17 12k
R15 270
Q16
Q17
Q18
Q19
Q20
Q21
D5 6.3V
R21 20k
R22 100k
R23 6.8k
C4 5 pF
Q23
Q22
R24 15k
R27 100
Q25
Q26
R26 12k
R29 250
R25 390
C5 2 pF
R28 12k
R36 0.2
Q24
R35 10
R34 150
Q15
R16 600
R19 8k
R18 4.2k
R20 4k
Q27
Q28
Q29
Q30
R31 6k
R30 500
R32 2.4k
R33 500
R37 0.04
VIN

TL/H/9067-2

## Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of $V_{OUT}$, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

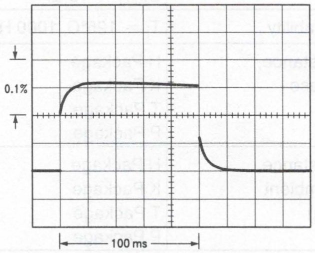


TL/H/9067-3

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_{IL} = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

**FIGURE 1**

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W × 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step at the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



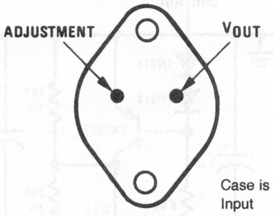
TL/H/9067-4

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

**FIGURE 2**

## Connection Diagrams

### TO-3
### Metal Can Package

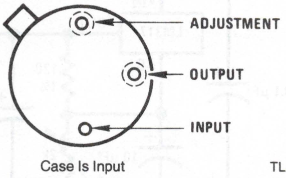

ADJUSTMENT
$V_{OUT}$
Case is Input

TL/H/9067-5

**Bottom View**

**Order Number LM137K STEEL or LM337K STEEL**
**See NS Package Number K02A**

### TO-39
### Metal Can Package

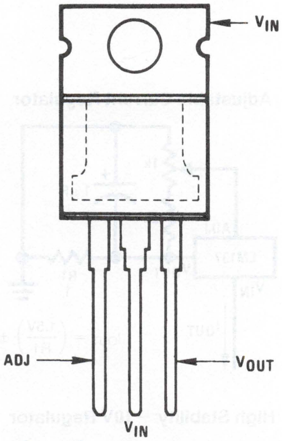

ADJUSTMENT
OUTPUT
INPUT
Case Is Input

TL/H/9067-6

**Bottom View**

**Order Number LM137H or LM337H**
**See NS Package Number H03B**

### TO-220
### Plastic Package

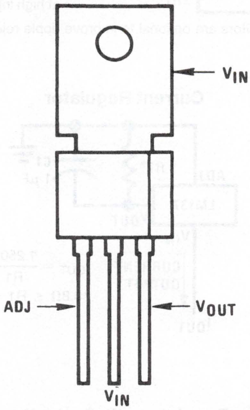

$V_{IN}$
ADJ
$V_{OUT}$
$V_{IN}$

TL/H/9067-7

**Front View**

**Order Number LM337T**
**See NS Package Number T03B**

### TO-202
### Plastic Package


$V_{IN}$
ADJ
$V_{OUT}$
$V_{IN}$

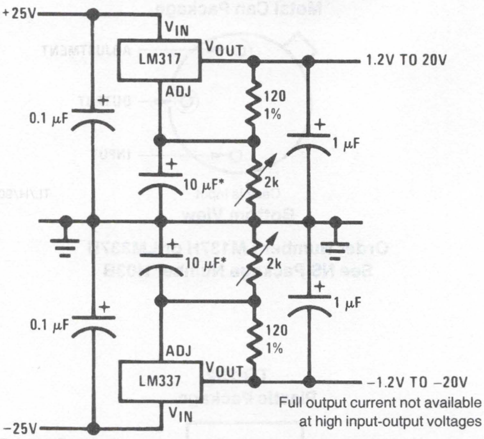
TL/H/9067-8

**Front View**

**Order Number LM337MP**
**See NS Package Number P03A**

## Typical Applications (Continued)

### Adjustable Lab Voltage Regulator

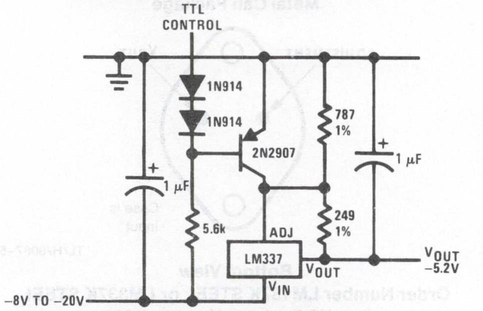

+25V
V_IN
LM317
V_OUT
ADJ
1.2V TO 20V
0.1 µF
120
1%
1 µF
10 µF*
2k
10 µF*
2k
1 µF
0.1 µF
120
1%
ADJ
LM337
V_OUT
V_IN
−1.2V TO −20V
−25V

Full output current not available at high input-output voltages

*The 10 µF capacitors are optional to improve ripple rejection

TL/H/9067–9

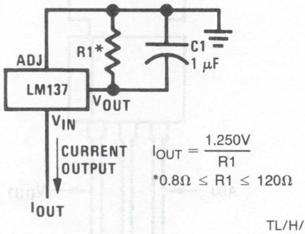
### −5.2V Regulator with Electronic Shutdown*


TTL
CONTROL
1N914
1N914
2N2907
787
1%
1 µF
1 µF
5.6k
249
1%
ADJ
LM337
V_OUT
V_IN
V_OUT
−5.2V
−8V TO −20V

TL/H/9067–10

*Minimum output ≅ −1.3V when control input is low

### Current Regulator

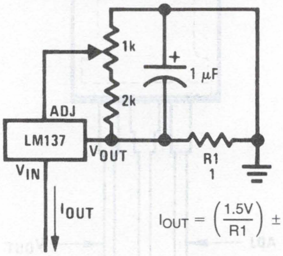

R1*
C1
1 µF
ADJ
LM137
V_OUT
V_IN
CURRENT
OUTPUT
I_OUT

$I_{OUT} = \frac{1.250V}{R1}$

*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9067–11

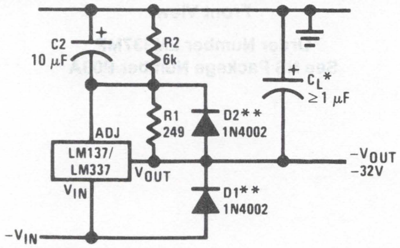
### Adjustable Current Regulator


1k
1 µF
2k
ADJ
LM137
V_OUT
V_IN
R1
1
I_OUT

$I_{OUT} = \left(\frac{1.5V}{R1}\right)$ ±15% adjustable

TL/H/9067–12

### Negative Regulator with Protection Diodes

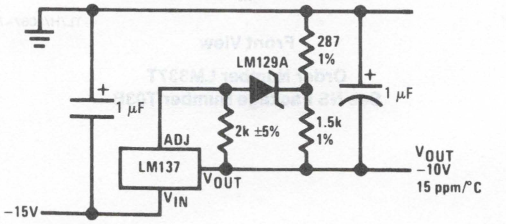

C2
10 µF
R2
6k
C_L*
≥1 µF
R1
249
D2**
1N4002
ADJ
LM137/
LM337
V_OUT
V_IN
−V_OUT
−32V
D1**
1N4002
−V_IN

TL/H/9067–13

*When $C_L$ is larger than 20 µF, D1 protects the LM137 in case the input supply is shorted

**When C2 is larger than 10 µF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

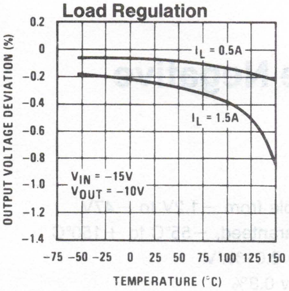
### High Stability −10V Regulator


287
1%
LM129A
1 µF
1 µF
2k ±5%
1.5k
1%
ADJ
LM137
V_OUT
V_IN
V_OUT
−10V
15 ppm/°C
−15V

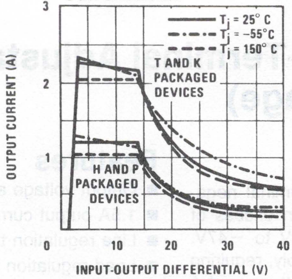
TL/H/9067–14

## Typical Performance Characteristics (K Steel and T Packages)

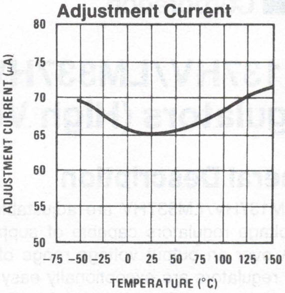
**Load Regulation**



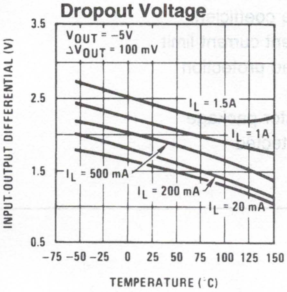
**Current Limit**



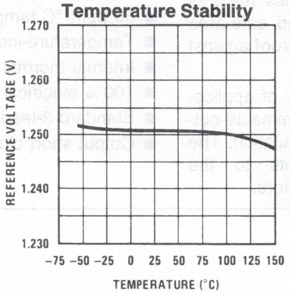
**Adjustment Current**



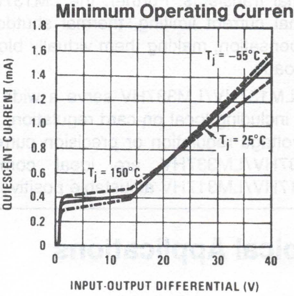
**Dropout Voltage**



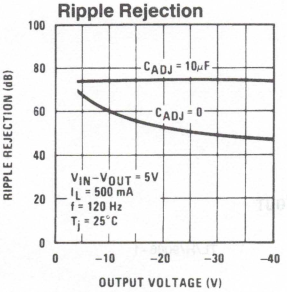
**Temperature Stability**



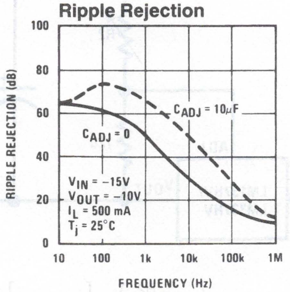
**Minimum Operating Current**



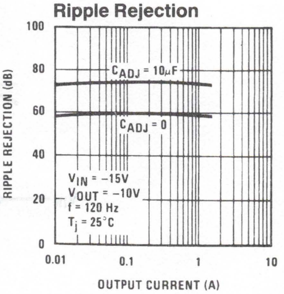
**Ripple Rejection**



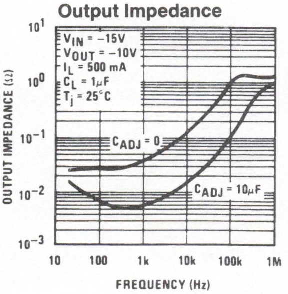
**Ripple Rejection**



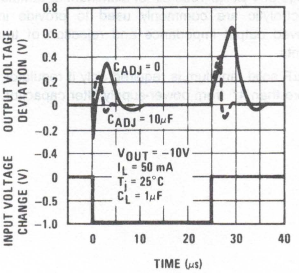
**Ripple Rejection**



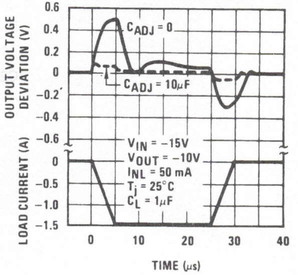
**Output Impedance**



**Line Transient Response**



**Load Transient Response**



TL/H/9067–15

National
Semiconductor
Corporation

# LM137HV/LM337HV 3-Terminal Adjustable Negative Regulators (High Voltage)

## General Description

The LM137HV/LM337HV are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −47V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137HV series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

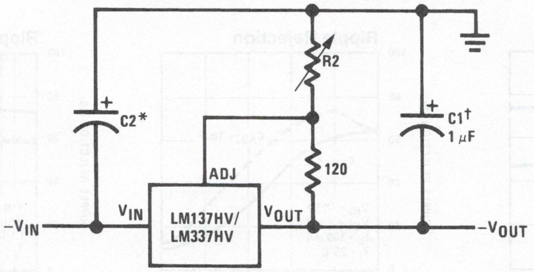
The LM137HV/LM337HV serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137HV/LM337HV are ideal complements to the LM117HV/LM317HV adjustable positive regulators.

## Features

- Output voltage adjustable from −1.2V to −47V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output short circuit protected

## Typical Applications

**Adjustable Negative Voltage Regulator**



TL/H/9066-1

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left[-I_{Adj}(R_2)\right]$$

†C1 = 1 µF solid tantalum or 10 µF aluminum electrolytic required for stability. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 µF solid tantalum is required only if regulator is more than 4″ from power-supply filter capacitor.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Power Dissipation | Internally limited |
| Input—Output Voltage Differential | 50V |
| Operating Junction Temperature Range | |
| LM137HV | −55°C to +150°C |
| LM337HV | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300° |

ESD rating is to be determined.

## Preconditioning

| | |
|---|---|
| Burn-In in Thermal Limit | 100% All Devices |

## Electrical Characteristics (Note 1)

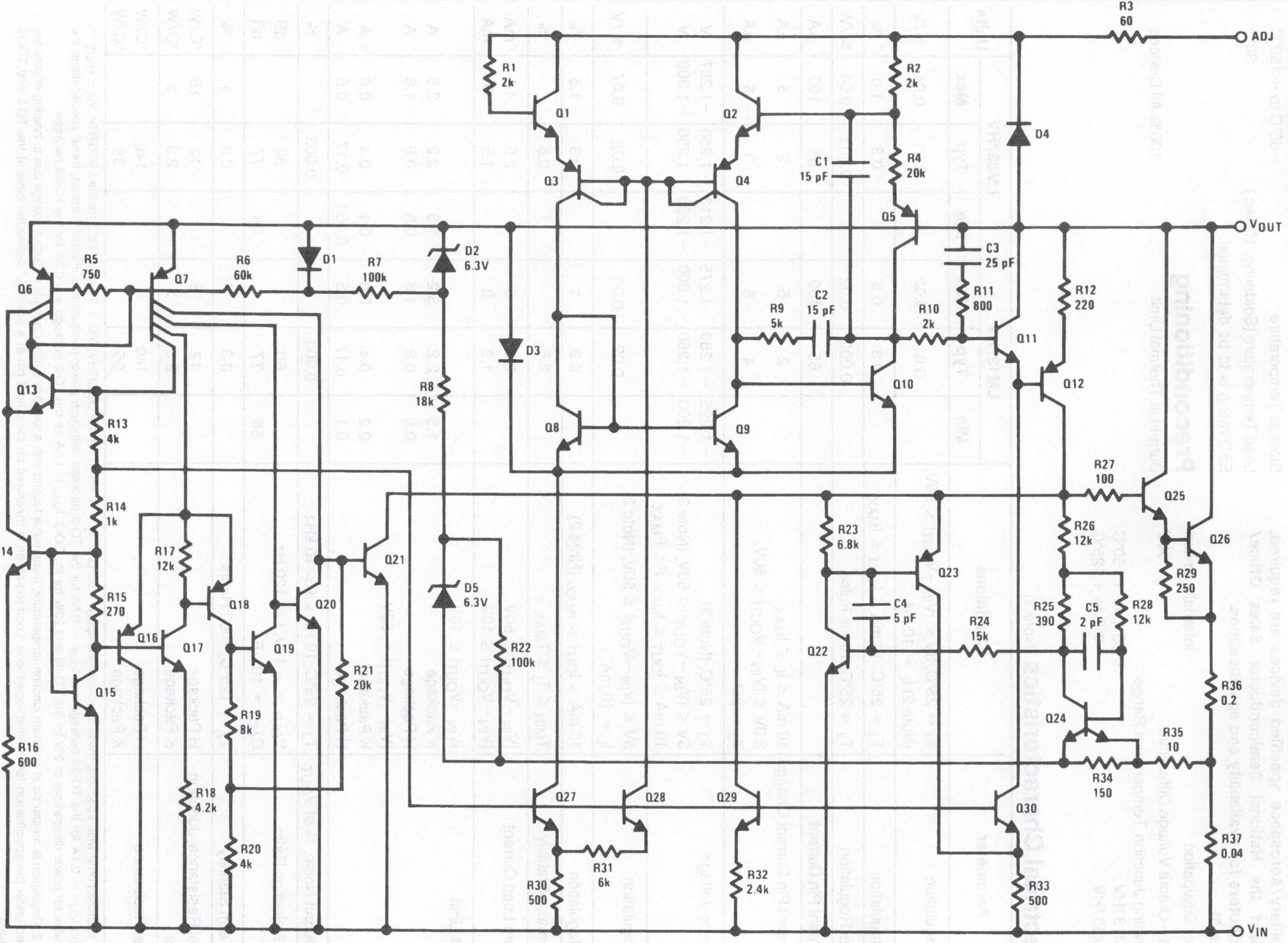
| Parameter | Conditions | LM137HV | | | LM337HV | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_J$ = 25°C, 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 50V, (Note 2) $I_L$ = 10 mA | | 0.01 | 0.02 | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_J$ = 25°C, 10 mA ≤ $I_{OUT}$ ≤ $I_{MAX}$ | | 0.3 | 0.5 | | 0.3 | 1.0 | % |
| Thermal Regulation | $T_J$ = 25°C, 10 ms Pulse | | 0.002 | 0.02 | | 0.003 | 0.04 | %/W |
| Adjustment Pin Current | | | 65 | 100 | | 65 | 100 | μA |
| Adjustment Pin Current Change | 10 mA ≤ $I_L$ ≤ $I_{MAX}$ | | 2 | 5 | | 2 | 5 | μA |
| | 3.0V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 50V, $T_J$ = 25° | | 4 | 6 | | 3 | 6 | μA |
| Reference Voltage | $T_J$ = 25°C, (Note 3) | −1.225 | −1.250 | −1.275 | −1.213 | −1.250 | −1.287 | V |
| | 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 50V, (Note 3)<br>10 mA ≤ $I_{OUT}$ ≤ $I_{MAX}$, P ≤ $P_{MAX}$ | −1.200 | −1.250 | −1.300 | −1.200 | −1.250 | −1.300 | V |
| Line Regulation | 3V ≤ $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 50V, (Note 2) $I_L$ = 10 mA | | 0.02 | 0.05 | | 0.02 | 0.07 | %/V |
| Load Regulation | 10 mA ≤ $I_{OUT}$ ≤ $I_{MAX}$, (Note 2) | | 0.3 | 1 | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN}$ ≤ $T_j$ ≤ $T_{MAX}$ | | 0.6 | | | 0.6 | | % |
| Minimum Load Current | $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 50V | | 2.5 | 5 | | 2.5 | 10 | mA |
| | $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 10V | | 1.2 | 3 | | 1.5 | 6 | mA |
| Current Limit | $\lvert V_{IN}-V_{OUT}\rvert$ ≤ 13V | | | | | | | |
| | K Package | 1.5 | 2.2 | 3.2 | 1.5 | 2.2 | 3.5 | A |
| | H Package | 0.5 | 0.8 | 1.6 | 0.5 | 0.8 | 1.8 | A |
| | $\lvert V_{IN}-V_{OUT}\rvert$ = 50V | | | | | | | |
| | K Package | 0.2 | 0.4 | 0.8 | 0.1 | 0.4 | 0.8 | A |
| | H Package | 0.1 | 0.17 | 0.5 | 0.050 | 0.17 | 0.5 | A |
| RMS Output Noise, % of $V_{OUT}$ | $T_J$ = 25°C, 10 Hz ≤ f ≤ 10 kHz | | 0.003 | | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT}$ = −10V, f = 120 Hz | | 60 | | | 60 | | dB |
| | $C_{ADJ}$ = 10 μF | 66 | 77 | | 66 | 77 | | dB |
| Long-Term Stability | $T_A$ = 125°C, 1000 Hours | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | H Package | | 12 | 15 | | 12 | 15 | °C/W |
| | K Package | | 2.3 | 3 | | 2.3 | 3 | °C/W |
| Thermal Resistance | H Package | | 140 | | | 140 | | °C/W |
| | K Package | | 35 | | | 35 | | °C/W |

**Note 1:** Unless otherwise specified, these specifications apply: −55°C ≤ $T_j$ ≤ +150°C for the LM137HV, 0°C ≤ $T_j$ ≤ +125°C for the LM337HV; $V_{IN}-V_{OUT}$ = 5V; and $I_{OUT}$ = 0.1A for the TO-39 package and $I_{OUT}$ = 0.5A for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. $I_{MAX}$ is 1.5A for the TO-3 package and 0.2A for the TO-39 package.

**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulations. Load regulation is measured on the output pin at a point ⅛″ below the base of the TO-3 and TO-39 packages.

**Note 3:** Refer to RETS237HVH drawing for LM137HVH or RETS137HVK for LM137HVK military specifications.

## Schematic Diagram

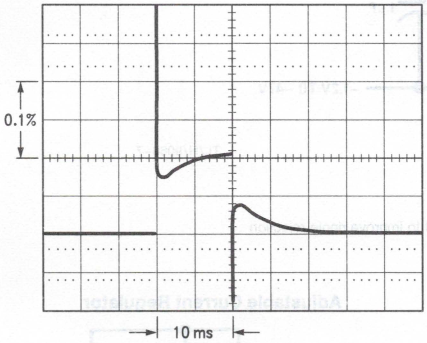

R3
60
ADJ
R1
2k
R2
2k
Q1
Q2
D4
C1
15 pF
R4
20k
Q3
Q4
Q5
VOUT
R5
750
R6
60k
D1
R7
100k
D2
6.3V
C3
25 pF
Q6
Q7
R11
800
R12
220
R9
5k
C2
15 pF
R10
2k
Q11
D3
Q13
R8
18k
Q10
Q12
R13
4k
Q8
Q9
R27
100
R14
1k
Q25
R26
12k
Q14
R17
12k
Q21
R23
6.8k
Q26
Q23
D5
6.3V
R29
250
Q18
Q20
C4
5 pF
C5
2 pF
R15
270
R25
390
R28
12k
Q16
Q17
Q19
R24
15k
R21
20k
R22
100k
Q22
R36
0.2
Q15
Q24
R19
8k
R35
10
R16
600
R34
150
R18
4.2k
Q27
Q28
Q29
Q30
R20
4k
R37
0.04
R31
6k
R32
2.4k
R30
500
R33
500
VIN

TL/H/9066-2

## Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of $V_{OUT}$, per Watt, within the first 10 ms after a step of power is applied. The LM137HV's specification is 0.02%/W, max.

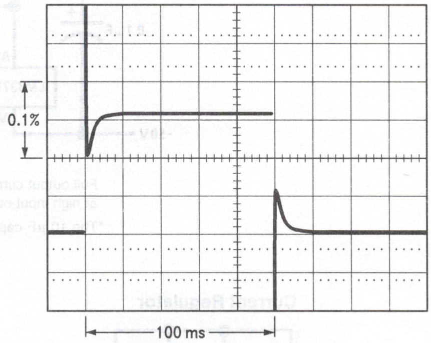
In *Figure 1,* a typical LM137HV's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137HV chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2,* when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



TL/H/9066–3

LM137HV, $V_{OUT} = -10V$
$V_{IN}-V_{OUT} = -40V$
$I_L$ = 0A → 0.25A → 0A
Vertical sensitivity, 5 mV/div

**FIGURE 1**



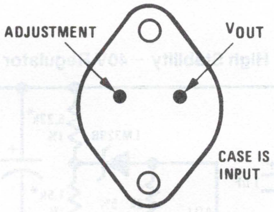
TL/H/9066–4

LM137HV, $V_{OUT} = -10V$
$V_{IN}-V_{OUT} = -40V$
$I_L$ = 0A → 0.25A → 0A
Horizontal sensitivity, 20 ms/div

**FIGURE 2**

## Connection Diagram (See Physical Dimensions section for further information)

**TO-3**
**Metal Can Package**

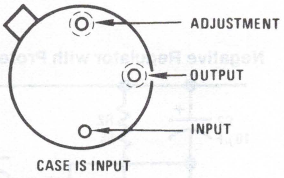


TL/H/9066–5

**Bottom View**

**Order Number LM137HVK Steel or LM337HVK Steel**
**See NS Package Number K02A**

**TO-39**
**Metal Can Package**



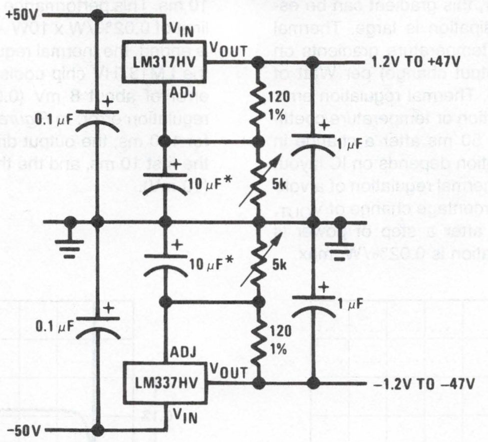
TL/H/9066–6

**Bottom View**

**Order Number LM137HVH or LML337HVH**
**See NS Package Number H03B**

## Typical Applications (Continued)

### Adjustable High Voltage Regulator

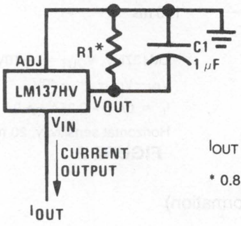

+50V
V_IN
LM317HV
V_OUT
ADJ
1.2V TO +47V
0.1 µF
120
1%
1 µF
10 µF*
5k
10 µF*
5k
1 µF
0.1 µF
120
1%
ADJ
LM337HV
V_OUT
−1.2V TO −47V
V_IN
−50V

TL/H/9066-7

Full output current not available at high input-output voltages

*The 10 µF capacitors are optional to improve ripple rejection

### Current Regulator

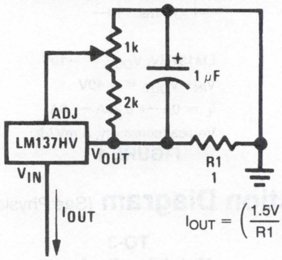

ADJ
R1*
C1
1 µF
LM137HV
V_OUT
V_IN
CURRENT
OUTPUT
I_OUT

$$I_{OUT} = \frac{V_{REF}}{R1}$$

$* \ 0.8\Omega \le R1 \le 120\Omega$

TL/H/9066-8

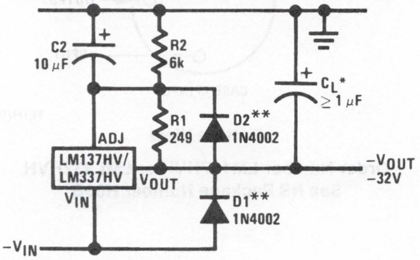
### Adjustable Current Regulator


1k
1 µF
2k
ADJ
LM137HV
V_OUT
V_IN
R1
1
I_OUT

$$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\% \text{ adjustable}$$

TL/H/9066-9

### Negative Regulator with Protection Diodes

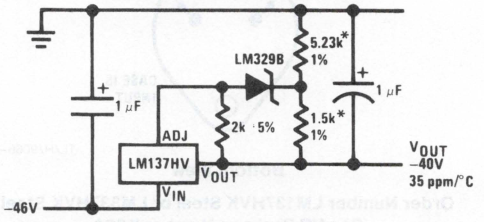

C2
10 µF
R2
6k
C_L*
≥ 1 µF
ADJ
R1
249
D2**
1N4002
LM137HV/
LM337HV
V_OUT
V_IN
−V_OUT
−32V
D1**
1N4002
−V_IN

TL/H/9066-10

*When $C_L$ is larger than 20 µF, D1 protects the LM137HV in case the input supply is shorted

**When C2 is larger than 10 µF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137HV is case the output is shorted

### High Stability −40V Regulator

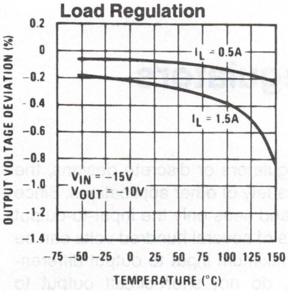

LM329B
5.23k*
1%
1 µF
1 µF
2k 5%
1.5k*
1%
ADJ
LM137HV
V_OUT
V_IN
V_OUT
−40V
35 ppm/°C
−46V

TL/H/9066-11

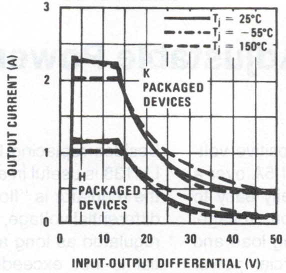
* Use resistors with good tracking TC < 25 ppm/°C

## Typical Performance Characteristics (H and K-STEEL Package)

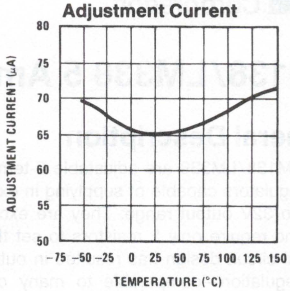
### Load Regulation



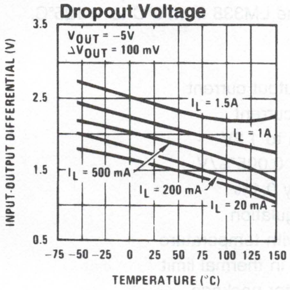
### Current Limit



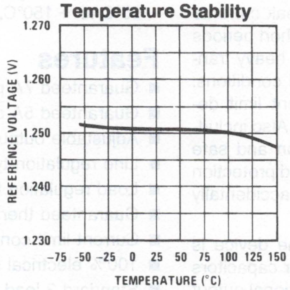
### Adjustment Current



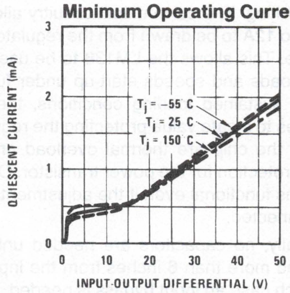
### Dropout Voltage



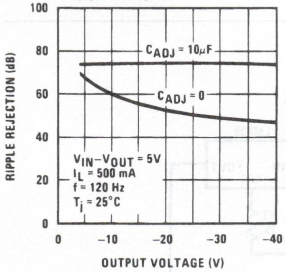
### Temperature Stability



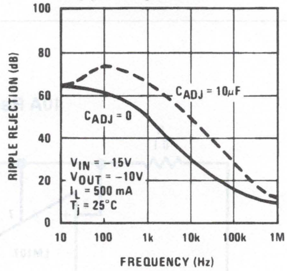
### Minimum Operating Current



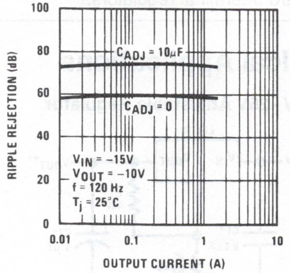
### Ripple Rejection



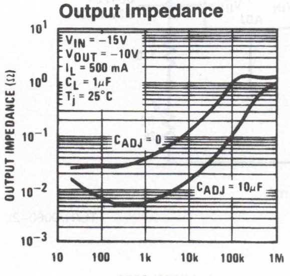
### Ripple Rejection



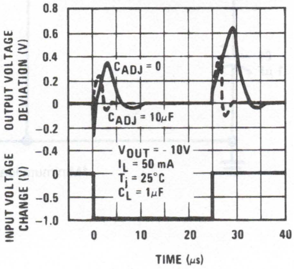
### Ripple Rejection



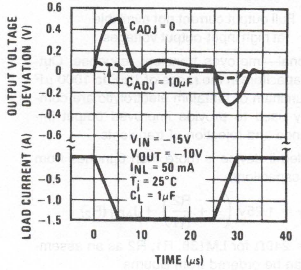
### Output Impedance



### Line Transient Response



### Load Transient Response



TL/H/9066-12

**National Semiconductor Corporation**

# LM138/LM338 5 Amp Adjustable Power Regulators

## General Description

The LM138/LM338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation—comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., do not short-circuit output to ground.

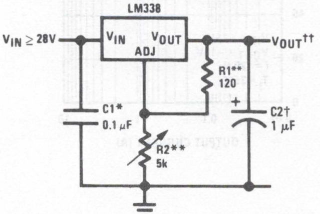
The LM138/LM338 are packaged in standard steel TO-3 transistor packages. The LM138 is rated for operation from −55°C to +150°C, and the LM338 from 0°C to +125°C.

## Features

- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- Standard 3-lead transistor package
- Output is short-circuit protected

## Typical Applications

### 1.2V–25V Adjustable Regulator



TL/H/9060-1

Full output current not available at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

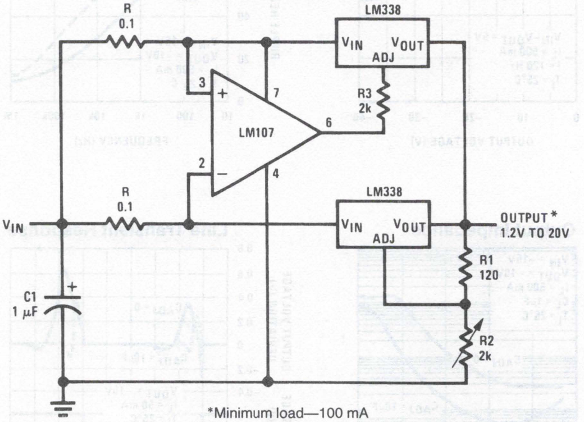
$$\dagger\dagger V_{OUT} = 1.25V\left(1+\frac{R2}{R1}\right)+I_{ADJ}(R_2)$$

**R1 = 240Ω for LM138. R1, R2 as an assembly can be ordered from Bourns:

MIL part no. 7105A-AT2-502

COMM part no. 7105A-AT7-502

### 10A Regulator



*Minimum load—100 mA

TL/H/9060-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Power Dissipation | Internally limited |
| Input—Output Voltage Differential | 35V |
| Operating Junction Temperature Range | |
| LM138 | −55°C to +150°C |
| LM338 | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## Preconditioning

| | |
|---|---|
| **Burn-In in Thermal Limit** | **All Devices 100%** |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM138 | | | LM338 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_J = 25°C$, $3V \le V_{IN} - V_{OUT} \le 35V$, (Note 2) $I_L = 10$ mA | | 0.005 | 0.01 | | 0.005 | 0.03 | %/V |
| Load Regulation | $T_J = 25°C$, $10mA \le I_{OUT} \le 5A$ | | 0.1 | 0.3 | | 0.1 | 0.5 | % |
| Thermal Regulation | Pulse = 20 ms, $T_J = 25°C$ | | 0.002 | 0.01 | | 0.002 | 0.02 | %/W |
| Adjustment Pin Current | | | 45 | 100 | | 45 | 100 | μA |
| Adjustment Pin Current Change | $10\text{ mA} \le I_L \le 5A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$ | | 0.2 | 5 | | 0.2 | 5 | μA |
| Reference Voltage | $3V \le (V_{IN} - V_{OUT}) \le 35V$, (Note 3)<br>$10\text{ mA} \le I_{OUT} \le 5A$, $P \le 50W$ | 1.19 | 1.24 | 1.29 | 1.19 | 1.24 | 1.29 | V |
| Line Regulation | $3V \le V_{IN} - V_{OUT} \le 35V$, (Note 2), $I_L = 10$ mA | | 0.02 | 0.04 | | 0.02 | 0.06 | %/V |
| Load Regulation | $10\text{ mA} \le I_{OUT} \le 5A$, (Note 2) | | 0.3 | 0.6 | | 0.3 | 1.0 | % |
| Temperature Stability | $T_{MIN} \le T_j \le T_{MAX}$ | | 1 | | | 1 | | % |
| Minimum Load Current | $V_{IN} - V_{OUT} = 35V$ | | 3.5 | 5 | | 3.5 | 10 | mA |
| Current Limit | $V_{IN} - V_{OUT} \le 10V$<br>DC<br>0.5 ms Peak<br>$V_{IN} - V_{OUT} \le 30V$ | <br>5.0<br>7<br> | <br>8<br>12<br>1 | | <br>5.0<br>7<br> | <br>8<br>12<br>1 | | <br>A<br>A<br>A |
| RMS Output Noise, % of $V_{OUT}$ | $T_J = 25°C$, $10\text{ Hz} \le f \le 10\text{ kHz}$ | | 0.003 | | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = 10V$, f = 120 Hz<br>$C_{ADJ} = 10\ \mu F$ | <br>60 | 60<br>75 | | <br>60 | 60<br>75 | | dB<br>dB |
| Long-Term Stability | $T_J = 125°C$ | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | K Package | | | 1.0 | | | 1.0 | °C/W |
| Thermal Resistance, Junction to Ambient | K Package | | 35 | | | 35 | | °C/W |

**Note 1:** Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM138, $-25°C \le T_j \le +150°C$ for the LM338, $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 2.5A$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 50W.

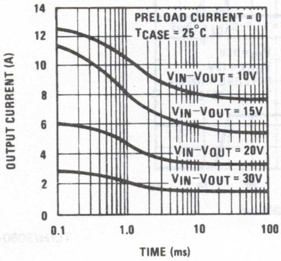
**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account separately by thermal regulation.

**Note 3:** Selected devices with tightened tolerance reference voltage available.

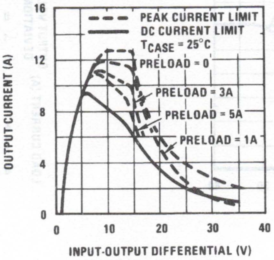
**Note 4:** Refer to RETS138K for military specification of LM138K.

## Typical Performance Characteristics

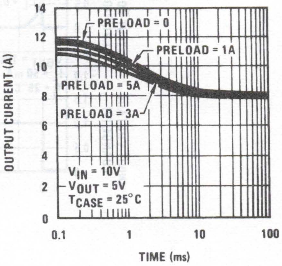
### Current Limit



### Current Limit

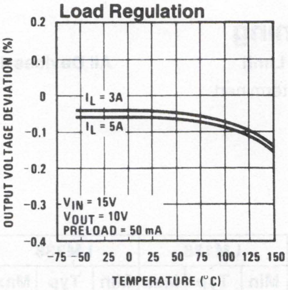


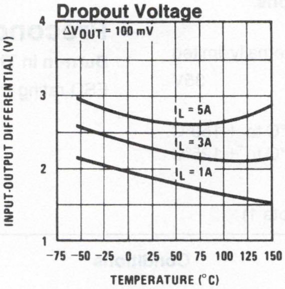
### Current Limit

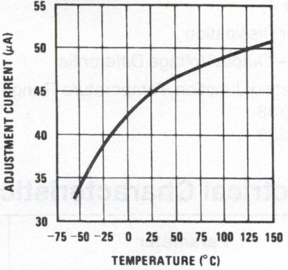


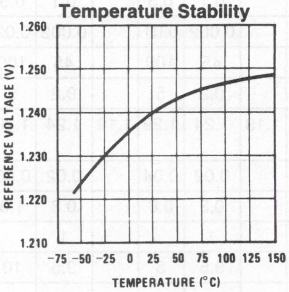
TL/H/9060–4

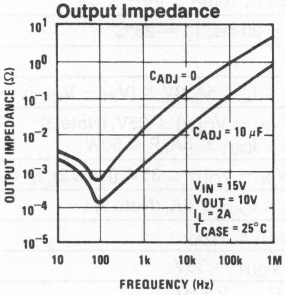
## Typical Performance Characteristics (Continued)

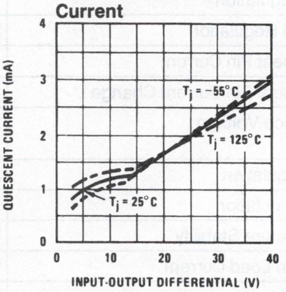

Load Regulation

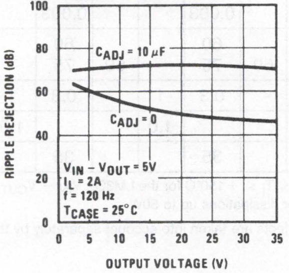

Dropout Voltage

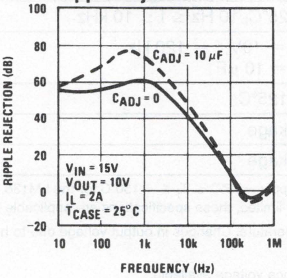

Adjustment Current

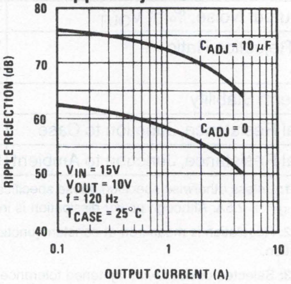

Temperature Stability

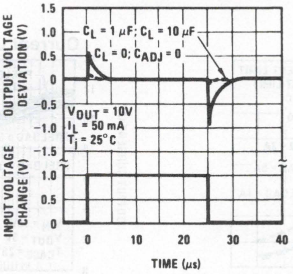

Output Impedance

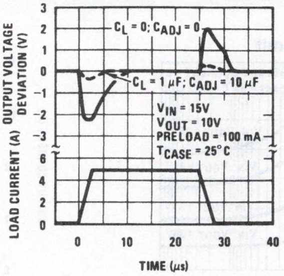

Minimum Operating Current


Ripple Rejection


Ripple Rejection


Ripple Rejection


Line Transient Response

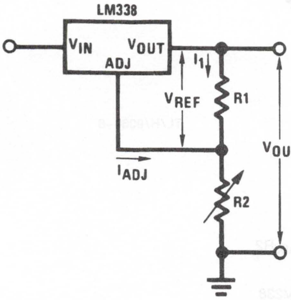

Load Transient Response

TL/H/9060–5

## Application Hints

In operation, the LM138 develops a nominal 1.25V reference voltage, $V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$



TL/H/9060-6

**FIGURE 1**

Since the 50 μA current from the adjustment terminal represents an error term, the LM138 was designed to minimize $I_{ADJ}$ and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

### External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassiing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM138 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 75 dB ripple rejection is obtainable at any output level. Increases over 20 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

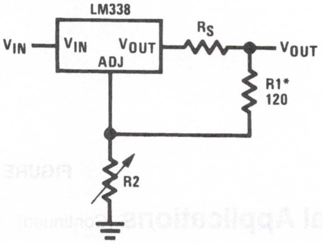
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM138 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

### Load Regulation

The LM138 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator (case) rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × $I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

*Figure 2* shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9060-7

**FIGURE 2. Regulator with Line Resistance in Output Lead**

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

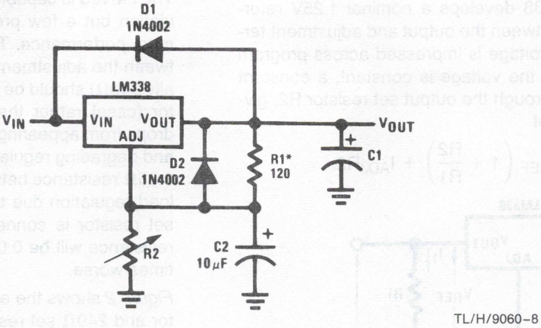
### Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{IN}$. In the LM138 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 100 μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM138 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM138 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

## Application Hints (Continued)


D1
1N4002
LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
D2
1N4002
R1*
120
$V_{OUT}$
C1
R2
C2
10 µF
TL/H/9060-8

D1 protects against C1
D2 protects against C2

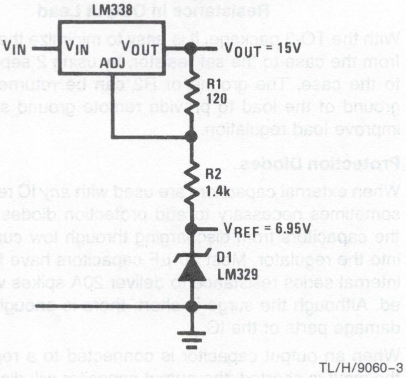
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

*R1 = 240Ω for LM138 and LM238

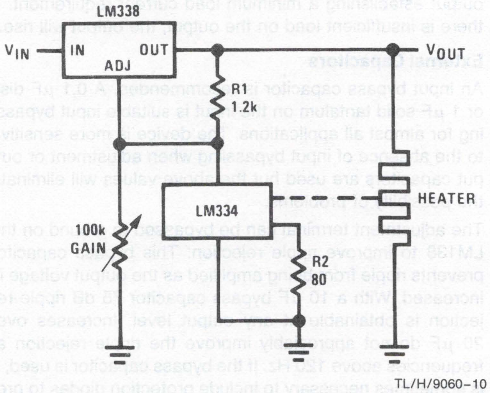
FIGURE 3. Regulator with Protection Diodes

## Typical Applications (Continued)

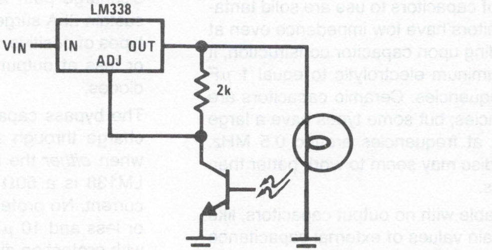
### Regulator and Voltage Reference


LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$ = 15V
R1
120
R2
1.4k
$V_{REF}$ = 6.95V
D1
LM329
TL/H/9060-3

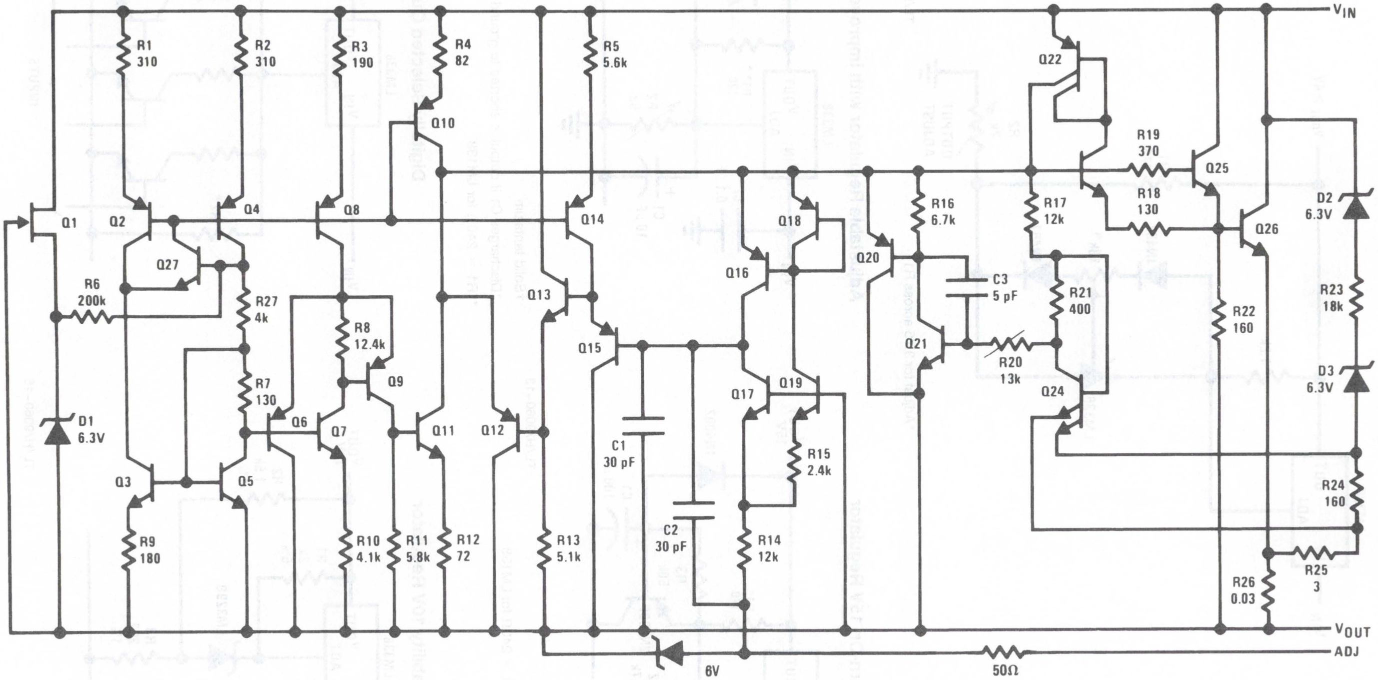
### Temperature Controller


LM338
$V_{IN}$
IN
OUT
ADJ
$V_{OUT}$
R1
1.2k
LM334
HEATER
100k
GAIN
R2
80
TL/H/9060-10

### Light Controller


LM338
$V_{IN}$
IN
OUT
ADJ
2k
TL/H/9060-11

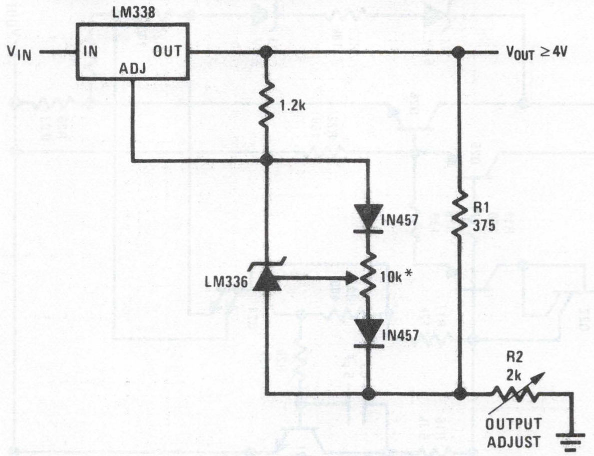
## Schematic Diagram


VIN
R1 310
R2 310
R3 190
R4 82
R5 5.6k
Q10
Q22
R19 370
Q25
R18 130
Q26
D2 6.3V
Q1
Q2
Q4
Q8
Q14
Q18
R16 6.7k
R17 12k
Q20
Q27
R6 200k
R27 4k
Q13
Q16
C3 5 pF
R21 400
R22 160
R23 18k
R8 12.4k
Q15
Q21
R20 13k
D3 6.3V
R7 130
Q9
Q17
Q19
Q24
D1 6.3V
Q6
Q7
Q11
Q12
C1 30 pF
R15 2.4k
Q3
Q5
R24 160
R9 180
R10 4.1k
R11 5.8k
R12 72
R13 5.1k
C2 30 pF
R14 12k
R25 3
R26 0.03
VOUT
ADJ
6V
50Ω

TL/H/9060–9

## Typical Applications (Continued)

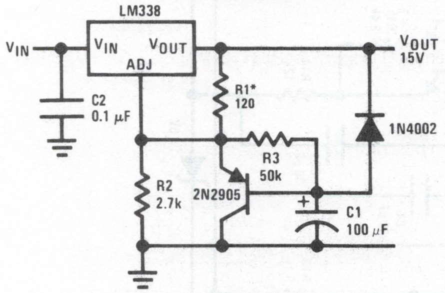
### Precision Power Regulator with Low Temperature Coefficient


LM338
VIN
IN
OUT
ADJ
VOUT ≥4V
1.2k
IN457
R1
375
LM336
10k*
IN457
R2
2k
OUTPUT
ADJUST

*Adjust for 3.75 across R1

TL/H/9060-12

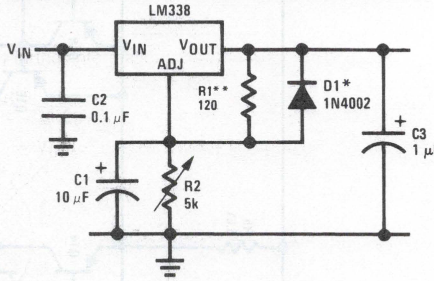
### Slow Turn-On 15V Regulator


LM338
VIN
VIN
VOUT
ADJ
VOUT
15V
C2
0.1 μF
R1*
120
1N4002
R3
50k
R2
2.7k
2N2905
C1
100 μF

TL/H/9060-13

*R1 = 240Ω for LM138

### Adjustable Regulator with Improved Ripple Rejection


LM338
VIN
VIN
VOUT
ADJ
C2
0.1 μF
R1**
120
D1*
1N4002
C3
1 μF†
C1
10 μF
R2
5k

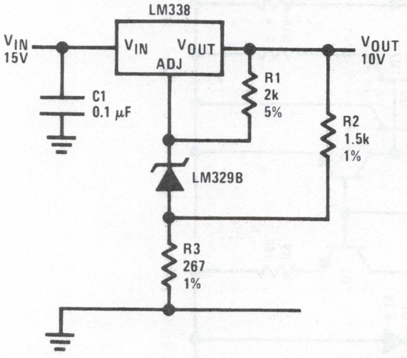
TL/H/9060-14

†Solid tantalum

*Discharges C1 if output is shorted to ground

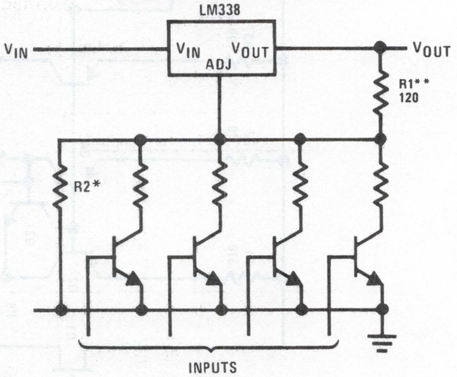
**R1 = 240Ω for LM138

### High Stability 10V Regulator


LM338
VIN
15V
VIN
VOUT
ADJ
VOUT
10V
C1
0.1 μF
R1
2k
5%
R2
1.5k
1%
LM329B
R3
267
1%

TL/H/9060-15

### Digitally Selected Outputs


LM338
VIN
VIN
VOUT
ADJ
VOUT
R1**
120
R2*
INPUTS

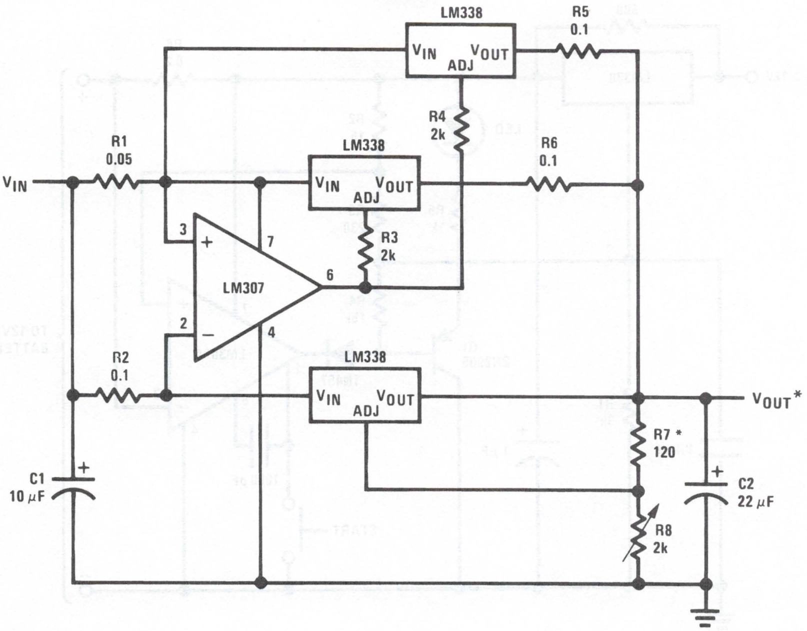
TL/H/9060-16

*Sets maximum $V_{OUT}$

**R1 = 240Ω for LM138

# Typical Applications (Continued)

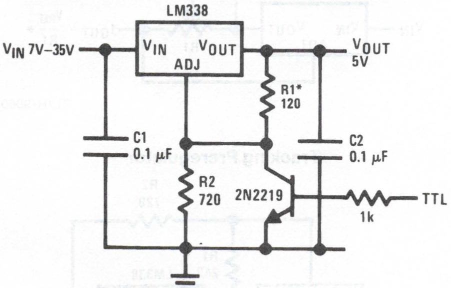
### 15A Regulator


LM338
VIN
VOUT
ADJ
R5
0.1
R4
2k
R1
0.05
LM338
R6
0.1
VIN
VIN
VOUT
ADJ
3
+
7
R3
2k
LM307
6
2
−
4
R2
0.1
LM338
VIN
VOUT
ADJ
VOUT*
R7*
120
C1
10 μF
+
C2
22 μF
+
R8
2k

TL/H/9060-17

*Minimum load—100 mA

### 5V Logic Regulator with Electronic Shutdown**

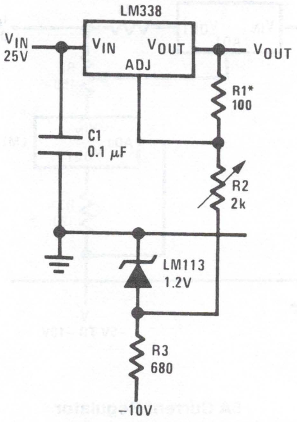

LM338
VIN 7V–35V
VIN
VOUT
ADJ
VOUT
5V
R1*
120
C1
0.1 μF
C2
0.1 μF
R2
720
2N2219
1k
TTL

TL/H/9060-18

*R1 = 240Ω for LM138

**Minimum output ≈ 1.2V

### 0 to 22V Regulator


LM338
VIN
25V
VIN
VOUT
ADJ
VOUT
R1*
100
C1
0.1 μF
R2
2k
LM113
1.2V
R3
680
−10V

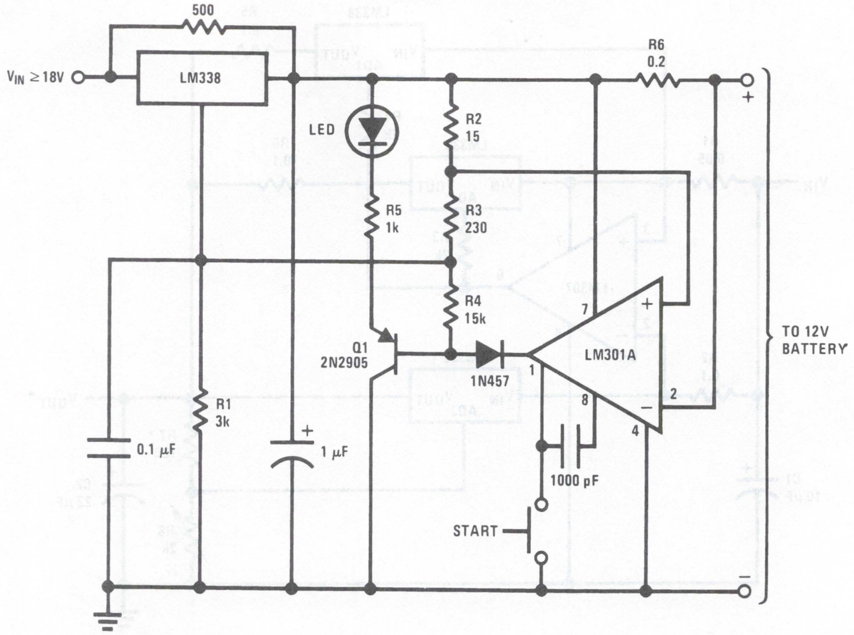
TL/H/9060-19

*R1 = 240Ω, R2 = 5k for LM138

Full output current not available at high input-output voltages

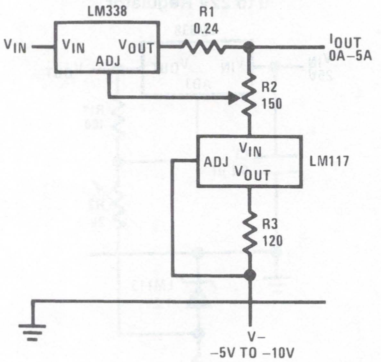
## Typical Applications (Continued)

### 12V Battery Charger


500
$V_{IN} \geq 18V$
LM338
LED
R2
15
R5
1k
R3
230
R4
15k
R6
0.2
+
Q1
2N2905
1N457
LM301A
7
1
8
2
4
+
−
TO 12V BATTERY
R1
3k
0.1 μF
+
1 μF
1000 pF
START
−

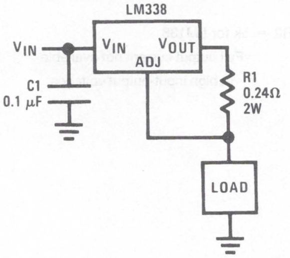
TL/H/9060-20

### Adjustable Current Regulator


LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
R1
0.24
$I_{OUT}$
0A–5A
R2
150
$V_{IN}$
ADJ
$V_{OUT}$
LM117
R3
120
V−
−5V TO −10V

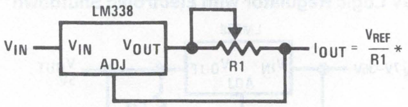
TL/H/9060-21

### 5A Current Regulator


LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
C1
0.1 μF
R1
0.24Ω
2W
LOAD

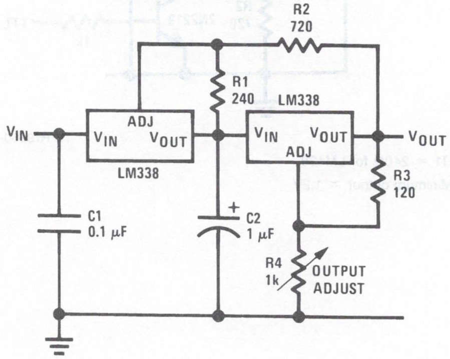
TL/H/9060-23

### Precision Current Limiter


LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
R1
$I_{OUT} = \frac{V_{REF}}{R1}$ *

TL/H/9060-22

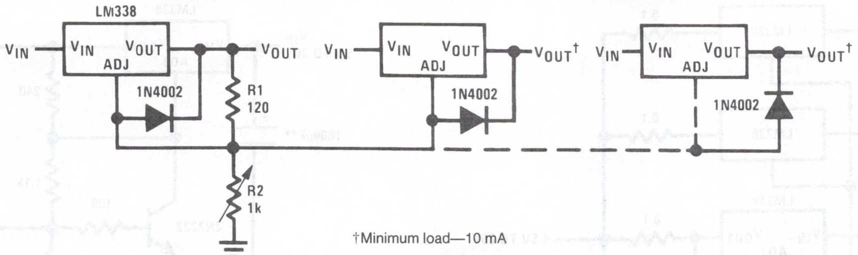
### Tracking Preregulator


R2
720
R1
240
ADJ
LM338
$V_{IN}$
$V_{IN}$
$V_{OUT}$
LM338
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R3
120
C1
0.1 μF
+
C2
1 μF
R4
1k
OUTPUT ADJUST

TL/H/9060-24

## Typical Applications (Continued)

### Adjusting Multiple On-Card Regulators with Single Control*

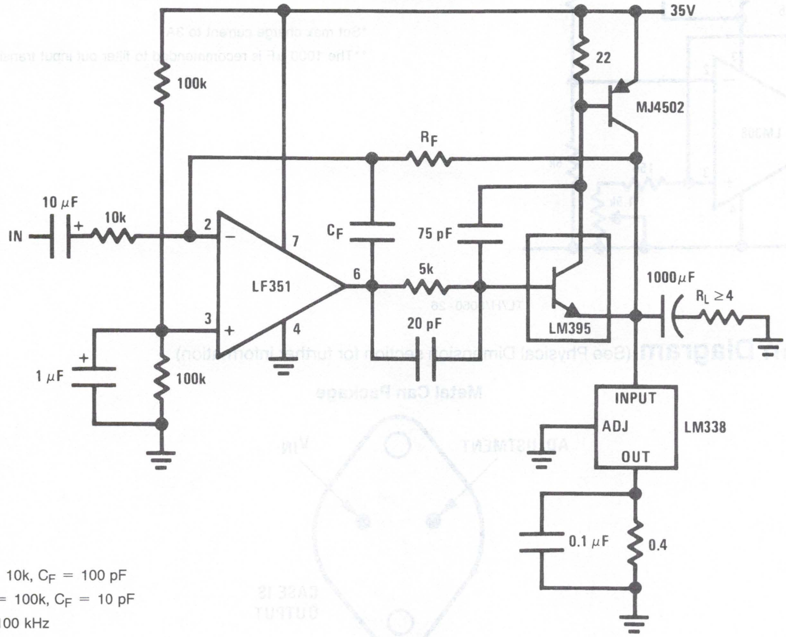

LM338
VIN
VIN
VOUT
ADJ
VOUT
1N4002
R1
120
R2
1k
VIN
VIN
VOUT
ADJ
VOUT†
1N4002
VIN
VIN
VOUT
ADJ
VOUT†
1N4002

†Minimum load—10 mA

*All outputs within ±100 mV

TL/H/9060-25

### Power Amplifier


35V
100k
22
MJ4502
RF
10 μF
10k
IN
2
7
CF
75 pF
LF351
6
5k
1000 μF
RL ≥4
3
4
20 pF
LM395
1 μF
100k
INPUT
ADJ
LM338
OUT
0.1 μF
0.4

$A_V = 1$, $R_F = 10k$, $C_F = 100$ pF

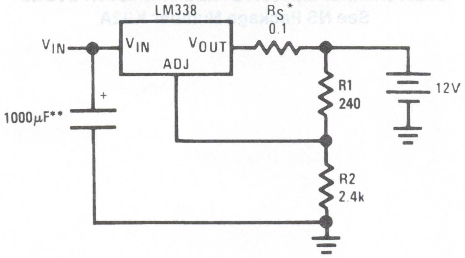
$A_V = 10$, $R_F = 100k$, $C_F = 10$ pF

Bandwidth ≥ 100 kHz

Distortion ≤ 0.1%

TL/H/9060-27

### Simple 12V Battery Charger


LM338
RS*
0.1
VIN
VIN
VOUT
ADJ
1000μF**
R1
240
12V
R2
2.4k

TL/H/9060-28

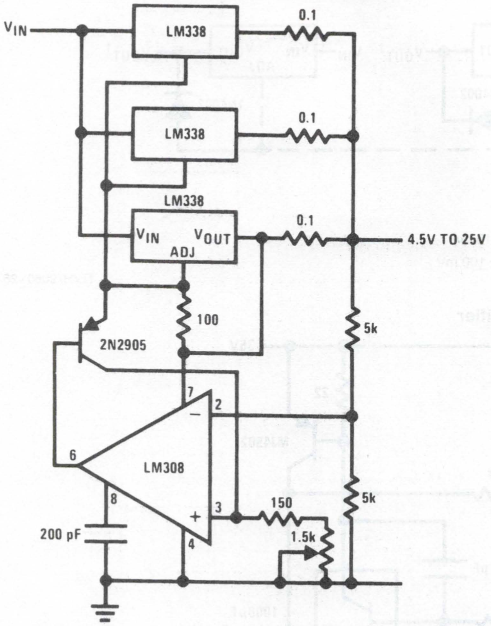
*$R_S$—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$

Use of $R_S$ allows low charging rates with fully charged battery.

**The 1000 μF is recommended to filter out input transients

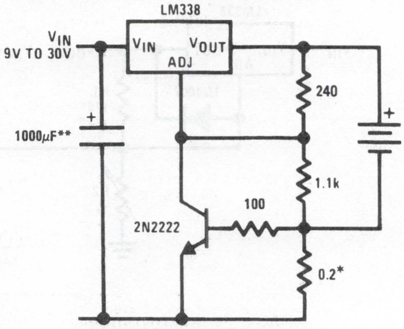
## Typical Applications (Continued)

### Adjustable 15A Regulator


VIN
LM338
0.1
LM338
0.1
LM338
VIN
VOUT
ADJ
0.1
4.5V TO 25V
100
2N2905
5k
7
2
LM308
6
8
3
4
150
5k
1.5k
200 pF

TL/H/9060–26

### Current Limited 6V Charger


LM338
VIN
9V TO 30V
VIN
VOUT
ADJ
240
1000μF**
1.1k
100
2N2222
0.2*

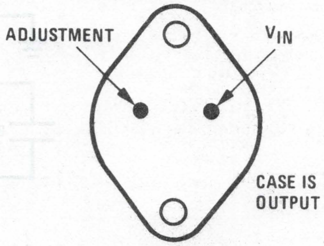
TL/H/9060–29

*Set max charge current to 3A

**The 1000 μF is recommended to filter out input transients.

## Connection Diagram (See Physical Dimension section for further information)

### Metal Can Package


ADJUSTMENT
VIN
CASE IS
OUTPUT

TL/H/9060–30

**Bottom View**

**Order Number LM138K STEEL or LM338K STEEL**

**See NS Package Number K02A**

**National Semiconductor Corporation**

# LM140A/LM140/LM340A/LM340 Series 3-Terminal Positive Regulators

## General Description

The LM140A/LM140/LM340A/LM340 series of positive 3-terminal voltage regulators are designed to provide superior performance as compared to the previously available 78XX series regulator. Computer programs were used to optimize the electrical and thermal performance of the packaged IC which results in outstanding ripple rejection, superior line and load regulation in high power applications (over 15W).

With these advances in design, the LM340 is now guaranteed to have line and load regulation that is a factor of 2 better than previously available devices. Also, all parameters are guaranteed at 1A vs 0.5A output current. The LM140A/LM340A provide tighter output voltage tolerance, ±2% along with 0.01%/V line regulation and 0.3%/A load regulation.

Current limiting is included to limit peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over limiting die temperature.

Considerable effort was expended to make the LM140-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The entire LM140A/LM140/LM340A/LM340 series of regulators is available in the metal TO-3 power package and the LM340A/LM340 series is also available in the TO-220 plastic power package.

For output voltages other than 5V, 12V, and 15V, the LM117 series provides an output voltage range from +1.2V to +57V.

## Features

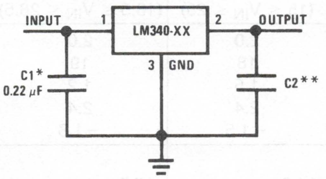
- Complete specifications at 1A load
- Output voltage tolerances of ±2% at $T_j = 25°C$ and ±4% over the temperature range (LM140A/LM340A)
- Fixed output voltages available 5, 12, and 15V
- Line regulation of 0.01% of $V_{OUT}/V \ \Delta V_{IN}$ at 1A load (LM140A/LM340A)
- Load regulation of 0.3% of $V_{OUT/A} \ \Delta I_{LOAD}$ (LM140A/LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- 100% thermal limit burn-in
- Special circuitry allows start-up even if output is pulled to negative voltage (±supplies)

**LM140 Series Package and Power Capability**

| Device | Package | Rated Power Dissipation | Design Output Current |
|---|---|---|---|
| LM140<br>LM340 | TO-3 | 20W | 1.5A |
| LM340T | TO-220 | 15W | 1.5A |

## Typical Applications

**Fixed Output Regulator**

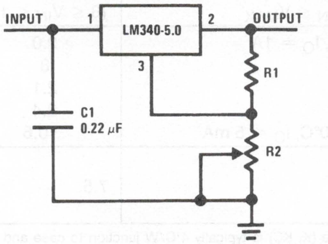


TL/H/7781–1

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

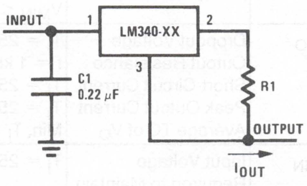
**Adjustable Output Regulator**



TL/H/7781–2

$V_{OUT} = 5V + (5V/R1 + I_Q)\ R2\ 5V/R1 > 3\ I_Q$, load regulation $(L_r) \approx [(R1 + R2)/R1]$ ($L_r$ of LM340-5).

**Current Regulator**



TL/H/7781–3

$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

$\Delta I_Q$ = 1.3 mA over line and load changes.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Input Voltage ($V_O$ = 5V, 12V, 15V) | 35V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range ($T_A$) | |
| LM140A/LM140 | −55°C to +125°C |
| LM340A/LM340 | 0°C to +70°C |
| Maximum Junction Temperature | |
| (TO-3 Package K, KC) | 150°C |
| (TO-220 Package T) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | |
| TO-3 Package K, KC | 300°C |
| TO-220 Package T | 230°C |

## Electrical Characteristics LM140A/LM340A (Note 2)

$I_{OUT}$ = 1A, $-55°C \le T_j \le +150°C$ (LM140A), or $0°C \le T_j \le +125°C$ (LM340A) unless otherwise specified

| Symbol | Output Voltage | | 5V | | | 12V | | | 15V | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Voltage (unless otherwise noted) | | 10V | | | 19V | | | 23V | | | |
| | Parameter | Conditions | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_O$ | Output Voltage | $T_j$ = 25°C | 4.9 | 5 | 5.1 | 11.75 | 12 | 12.25 | 14.7 | 15 | 15.3 | V |
| | | $P_D \le 15W$, $5 mA \le I_O \le 1A$<br>$V_{MIN} \le V_{IN} \le V_{MAX}$ | 4.8 | <br>$(7.5 \le V_{IN} \le 20)$ | 5.2 | 11.5 | <br>$(14.8 \le V_{IN} \le 27)$ | 12.5 | 14.4 | <br>$(17.9 \le V_{IN} \le 30)$ | 15.6 | V<br>V |
| $\Delta V_O$ | Line Regulation | $I_O$ = 500 mA<br>$\Delta V_{IN}$ | | <br>$(7.5 \le V_{IN} \le 20)$ | 10 | | <br>$(14.8 \le V_{IN} \le 27)$ | 18 | | <br>$(17.9 \le V_{IN} \le 30)$ | 22 | mV<br>V |
| | | $T_j$ = 25°C<br>$\Delta V_{IN}$ | | 3<br>$(7.5 \le V_{IN} \le 20)$ | 10 | | 4<br>$(14.5 \le V_{IN} \le 27)$ | 18 | | 4<br>$(17.5 \le V_{IN} \le 30)$ | 22 | mV<br>V |
| | | $T_j$ = 25°C<br>Over Temperature<br>$\Delta V_{IN}$ | | <br><br>$(8 \le V_{IN} \le 12)$ | 4<br>12 | | <br><br>$(16 \le V_{IN} \le 22)$ | 9<br>30 | | <br><br>$(20 \le V_{IN} \le 26)$ | 10<br>30 | mV<br>mV<br>V |
| $\Delta V_O$ | Load Regulation | $T_j$ = 25°C, $5 mA \le I_O \le 1.5A$<br>$250 mA \le I_O \le 750 mA$ | | 10 | 25<br>15 | | 12 | 32<br>19 | | 12 | 35<br>21 | mV<br>mV |
| | | Over Temperature,<br>$5 mA \le I_O \le 1A$ | | | 25 | | | 60 | | | 75 | mV |
| $I_Q$ | Quiescent Current | $T_j$ = 25°C<br>Over Temperature | | | 6<br>6.5 | | | 6<br>6.5 | | | 6<br>6.5 | mA<br>mA |
| $\Delta I_Q$ | Quiescent Current Change | $5 mA \le I_O \le 1A$ | | | 0.5 | | | 0.5 | | | 0.5 | mA |
| | | $T_j$ = 25°C, $I_O$ = 1A<br>$V_{MIN} \le V_{IN} \le V_{MAX}$ | | <br>$(7.5 \le V_{IN} \le 20)$ | 0.8 | | <br>$(14.8 \le V_{IN} \le 27)$ | 0.8 | | <br>$(17.9 \le V_{IN} \le 30)$ | 0.8 | mA<br>V |
| | | $I_O$ = 500 mA<br>$V_{MIN} \le V_{IN} \le V_{MAX}$ | | <br>$(8 \le V_{IN} \le 25)$ | 0.8 | | <br>$(15 \le V_{IN} \le 30)$ | 0.8 | | <br>$(17.9 \le V_{IN} \le 30)$ | 0.8 | mA<br>V |
| $V_N$ | Output Noise Voltage | $T_A$ = 25°C, $10 Hz \le f \le 100 kHz$ | | 40 | | | 75 | | | 90 | | μV |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | $T_j$ = 25°C, f = 120 Hz, $I_O$ = 1A<br>or f = 120 Hz, $I_O$ = 500 mA,<br>Over Temperature,<br>$V_{MIN} \le V_{IN} \le V_{MAX}$ | 68<br>68 | 80<br><br><br>$(8 \le V_{IN} \le 18)$ | | 61<br>61 | 72<br><br><br>$(15 \le V_{IN} \le 25)$ | | 60<br>60 | 70<br><br><br>$(18.5 \le V_{IN} \le 28.5)$ | | dB<br>dB<br><br>V |
| $R_O$ | Dropout Voltage<br>Output Resistance<br>Short-Circuit Current<br>Peak Output Current<br>Average TC of $V_O$ | $T_j$ = 25°C, $I_O$ = 1A<br>f = 1 kHz<br>$T_j$ = 25°C<br>$T_j$ = 25°C<br>Min, $T_j$ = 0°C, $I_O$ = 5 mA | | 2.0<br>8<br>2.1<br>2.4<br>−0.6 | | | 2.0<br>18<br>1.5<br>2.4<br>−1.5 | | | 2.0<br>19<br>1.2<br>2.4<br>−1.8 | | V<br>mΩ<br>A<br>A<br>mV/°C |
| $V_{IN}$ | Input Voltage Required to Maintain Line Regulation | $T_j$ = 25°C | 7.5 | | | 14.5 | | | 17.5 | | | V |

**Note 1:** Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

**Note 2:** All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle $\le 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

**Note 3:** Refer to RETS140A-12K for LM140K-12, RETS140A-15K for LM140K-15, or RETS140A-05K for LM140K-5.0 military drawing specifications.

## Electrical Characteristics LM140 (Note 2) $-55°C \le T_j \le +150°C$ unless otherwise specified

| Symbol | Output Voltage | | | 5V | | | 12V | | | 15V | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Voltage (unless otherwise noted) | | | 10V | | | 19V | | | 23V | | | |
| | Parameter | Conditions | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_O$ | Output Voltage | $T_j = 25°C$, $5\ mA \le I_O \le 1A$ | | 4.8 | 5 | 5.2 | 11.5 | 12 | 12.5 | 14.4 | 15 | 15.6 | V |
| | | $P_D \le 15W$, $5\ mA \le I_O \le 1A$ | | 4.75 | | 5.25 | 11.4 | | 12.6 | 14.25 | | 15.75 | V |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(8 \le V_{IN} \le 20)$ | | | $(15.5 \le V_{IN} \le 27)$ | | | $(18.5 \le V_{IN} \le 30)$ | | | V |
| $\Delta V_O$ | Line Regulation | $I_O = 500\ mA$ | $T_j = 25°C$ | | 3 | 50 | | 4 | 120 | | 4 | 150 | mV |
| | | | $\Delta V_{IN}$ | $(7 \le V_{IN} \le 25)$ | | | $(14.5 \le V_{IN} \le 30)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| | | | $-55°C \le T_j \le +150°C$ | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | $(8 \le V_{IN} \le 20)$ | | | $(15 \le V_{IN} \le 27)$ | | | $(18.5 \le V_{IN} \le 30)$ | | | V |
| | | $I_O \le 1A$ | $T_j = 25°C$ | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | $(7.5 \le V_{IN} \le 20)$ | | | $(14.6 \le V_{IN} \le 27)$ | | | $(17.7 \le V_{IN} \le 30)$ | | | V |
| | | | $-55°C \le T_j \le +150°C$ | | | 25 | | | 60 | | | 75 | mV |
| | | | $\Delta V_{IN}$ | $(8 \le V_{IN} \le 12)$ | | | $(16 \le V_{IN} \le 22)$ | | | $(20 \le V_{IN} \le 26)$ | | | V |
| $\Delta V_O$ | Load Regulation | $T_j = 25°C$ | $5\ mA \le I_O \le 1.5A$ | | 10 | 50 | | 12 | 120 | | 12 | 150 | mV |
| | | | $250\ mA \le I_P \le 750\ mA$ | | | 25 | | | 60 | | | 75 | mV |
| | | $-55°C \le T_j \le +150°C$, $5\ mA \le I_O \le 1A$ | | | | 50 | | | 120 | | | 150 | mV |
| $I_Q$ | Quiescent Current | $I_O \le 1A$ | $T_j = 25°C$ | | | 6 | | | 6 | | | 6 | mA |
| | | | $-55°C \le T_j \le +150°C$ | | | 7 | | | 7 | | | 7 | mA |
| $\Delta I_Q$ | Quiescent Current Change | $5\ mA \le I_O \le 1A$ | | | | 0.5 | | | 0.5 | | | 0.5 | mA |
| | | $T_j = 25°C$, $I_O \le 1A$ | | | | 0.8 | | | 0.8 | | | 0.8 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(8 \le V_{IN} \le 20)$ | | | $(15 \le V_{IN} \le 27)$ | | | $(18.5 \le V_{IN} \le 30)$ | | | V |
| | | $I_O = 500\ mA$, $-55°C \le T_j \le +150°C$ | | | | 0.8 | | | 0.8 | | | 0.8 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(8 \le V_{IN} \le 25)$ | | | $(15 \le V_{IN} \le 30)$ | | | $(18.5 \le V_{IN} \le 30)$ | | | V |
| $V_N$ | Output Noise Voltage | $T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$ | | | 40 | | | 75 | | | 90 | | μV |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | $f = 120\ Hz$ | $I_O \le 1A$, $T_j = 25°C$ or | 68 | 80 | | 61 | 72 | | 60 | 70 | | dB |
| | | | $I_O \le 500\ mA$, $-55°C \le T_j \le +150°C$ | 68 | | | 61 | | | 60 | | | dB |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(8 \le V_{IN} \le 18)$ | | | $(15 \le V_{IN} \le 25)$ | | | $(18.5 \le V_{IN} \le 28.5)$ | | | V |
| $R_O$ | Dropout Voltage | $T_j = 25°C$, $I_O = 1A$ | | | 2.0 | | | 2.0 | | | 2.0 | | V |
| | Output Resistance | $f = 1\ kHz$ | | | 8 | | | 18 | | | 19 | | mΩ |
| | Short-Circuit Current | $T_j = 25°C$ | | | 2.1 | | | 1.5 | | | 1.2 | | A |
| | Peak Output Current | $T_j = 25°C$ | | | 2.4 | | | 2.4 | | | 2.4 | | A |
| | Average TC of $V_{OUT}$ | $0°C \le T_j \le +150°C$, $I_O = 5\ mA$ | | | −0.6 | | | −1.5 | | | −1.8 | | mV/°C |
| $V_{IN}$ | Input Voltage Required to Maintain Line Regulation | $T_j = 25°C$, $I_O \le 1A$ | | 7.5 | | | 14.6 | | | 17.7 | | | V |

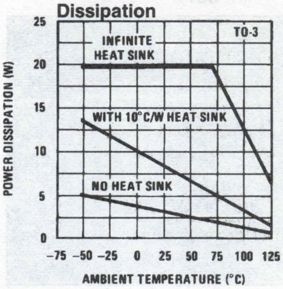
**Note 2:** All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

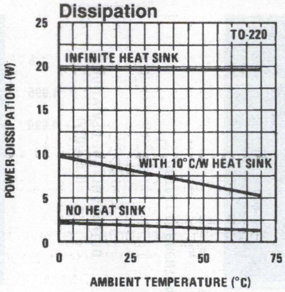
## Electrical Characteristics LM340 (Note 2) 0°C ≤ $T_j$ ≤ +125°C unless otherwise specified

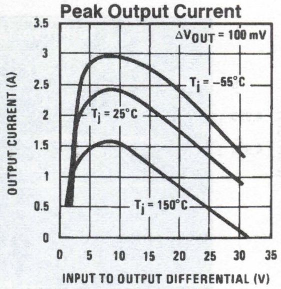
| Symbol | Output Voltage | | | 5V | | | 12V | | | 15V | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Voltage (unless otherwise noted) | | | 10V | | | 19V | | | 23V | | | |
| | Parameter | Conditions | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_O$ | Output Voltage | $T_j = 25°C$, $5\text{ mA} \le I_O \le 1\text{A}$ | | 4.8 | 5 | 5.2 | 11.5 | 12 | 12.5 | 14.4 | 15 | 15.6 | V |
| | | $P_D \le 15\text{W}$, $5\text{ mA} \le I_O \le 1\text{A}$ | | 4.75 | 5.25 | | 11.4 | | 12.6 | 14.25 | | 15.75 | V |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(7.5 \le V_{IN} \le 20)$ | | | $(14.5 \le V_{IN} \le 27)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| $\Delta V_O$ | Line Regulation | $I_O = 500\text{ mA}$ | $T_j = 25°C$ | | 3 | 50 | | 4 | 120 | | 4 | 150 | mV |
| | | | $\Delta V_{IN}$ | $(7 \le V_{IN} \le 25)$ | | | $(14.5 \le V_{IN} \le 30)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| | | | $0°C \le T_j \le +125°C$ | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | $(8 \le V_{IN} \le 20)$ | | | $(15 \le V_{IN} \le 27)$ | | | $(18.5 \le V_{IN} \le 30)$ | | | V |
| | | $I_O \le 1\text{A}$ | $T_j = 25°C$ | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | $(7.5 \le V_{IN} \le 20)$ | | | $(14.6 \le V_{IN} \le 27)$ | | | $(17.7 \le V_{IN} \le 30)$ | | | V |
| | | | $0°C \le T_j \le +125°C$ | | | 25 | | | 60 | | | 75 | mV |
| | | | $\Delta V_{IN}$ | $(8 \le V_{IN} \le 12)$ | | | $(16 \le V_{IN} \le 22)$ | | | $(20 \le V_{IN} \le 26)$ | | | V |
| $\Delta V_O$ | Load Regulation | $T_j = 25°C$ | $5\text{ mA} \le I_O \le 1.5\text{A}$ | | 10 | 50 | | 12 | 120 | | 12 | 150 | mV |
| | | | $250\text{ mA} \le I_O \le 750\text{ mA}$ | | | 25 | | | 60 | | | 75 | mV |
| | | $5\text{ mA} \le I_O \le 1\text{A}$, $0°C \le T_j \le +125°C$ | | | | 50 | | | 120 | | | 150 | mV |
| $I_Q$ | Quiescent Current | $I_O \le 1\text{A}$ | $T_j = 25°C$ | | | 8 | | | 8 | | | 8 | mA |
| | | | $0°C \le T_j \le +125°C$ | | | 8.5 | | | 8.5 | | | 8.5 | mA |
| $\Delta I_Q$ | Quiescent Current Change | $5\text{ mA} \le I_O \le 1\text{A}$ | | | | 0.5 | | | 0.5 | | | 0.5 | mA |
| | | $T_j = 25°C$, $I_O \le 1\text{A}$ | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(7.5 \le V_{IN} \le 20)$ | | | $(14.8 \le V_{IN} \le 27)$ | | | $(17.9 \le V_{IN} \le 30)$ | | | V |
| | | $I_O = 500\text{ mA}$, $0°C \le T_j \le +125°C$ | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(7 \le V_{IN} \le 25)$ | | | $(14.5 \le V_{IN} \le 30)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| $V_N$ | Output Noise Voltage | $T_A = 25°C$, $10\text{ Hz} \le f \le 100\text{ kHz}$ | | | 40 | | | 75 | | | 90 | | μV |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | $f = 120\text{ Hz}$ | $I_O \le 1\text{A}$, $T_j = 25°C$ | 62 | 80 | | 55 | 72 | | 54 | 70 | | dB |
| | | | or $I_O \le 500\text{ mA}$, $0°C \le T_j \le +125°C$ | 62 | | | 55 | | | 54 | | | dB |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | $(8 \le V_{IN} \le 18)$ | | | $(15 \le V_{IN} \le 25)$ | | | $(18.5 \le V_{IN} \le 28.5)$ | | | V |
| $R_O$ | Dropout Voltage | $T_j = 25°C$, $I_O = 1\text{A}$ | | | 2.0 | | | 2.0 | | | 2.0 | | V |
| | Output Resistance | $f = 1\text{ kHz}$ | | | 8 | | | 18 | | | 19 | | mΩ |
| | Short-Circuit Current | $T_j = 25°C$ | | | 2.1 | | | 1.5 | | | 1.2 | | A |
| | Peak Output Current | $T_j = 25°C$ | | | 2.4 | | | 2.4 | | | 2.4 | | A |
| | Average TC of $V_{OUT}$ | $0°C \le T_j \le +125°C$, $I_O = 5\text{ mA}$ | | | −0.6 | | | −1.5 | | | −1.8 | | mV/°C |
| $V_{IN}$ | Input Voltage Required to Maintain Line Regulation | $T_j = 25°C$, $I_O \le 1\text{A}$ | | 7.5 | | | 14.6 | | | 17.7 | | | V |

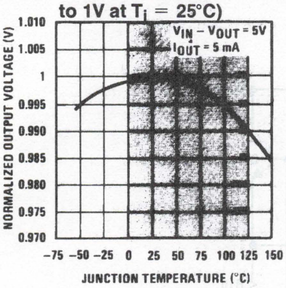
**Note 2:** All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

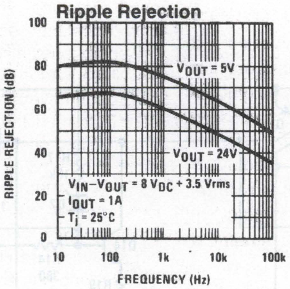
# Typical Performance Characteristics

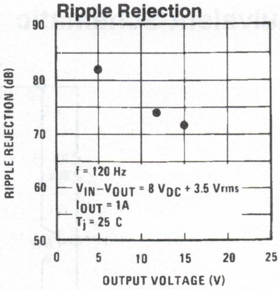

**Maximum Average Power Dissipation**


**Maximum Average Power Dissipation**

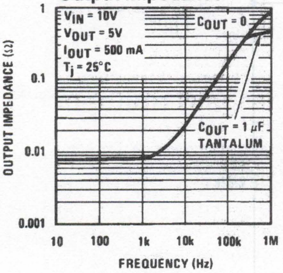

**Peak Output Current**

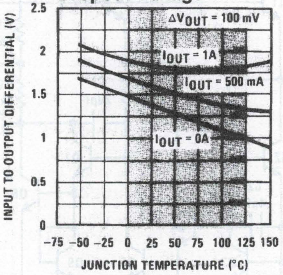

**Output Voltage (Normalized to 1V at $T_j$ = 25°C)**


**Ripple Rejection**

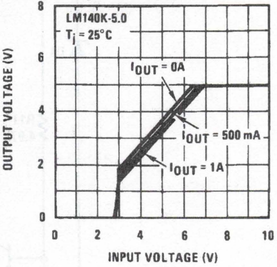

**Ripple Rejection**

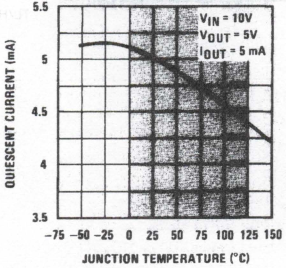
**Note:** Shaded area refers to LM340A/LM340.

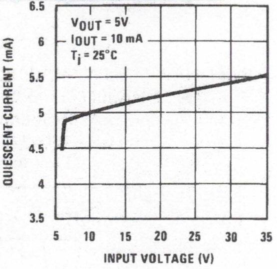

**Output Impedance**


**Dropout Voltage**

**Note:** Shaded area refers to LM340A/LM340.


**Dropout Characteristics**


**Quiescent Current**

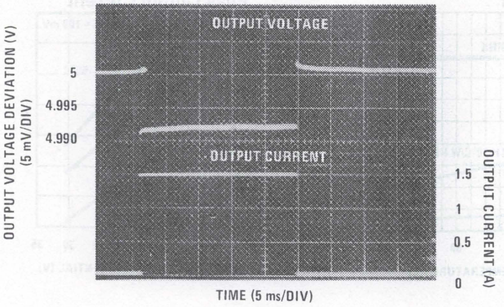

**Quiescent Current**

**Note:** Shaded area refers to LM340A/LM340.

TL/H/7781-4

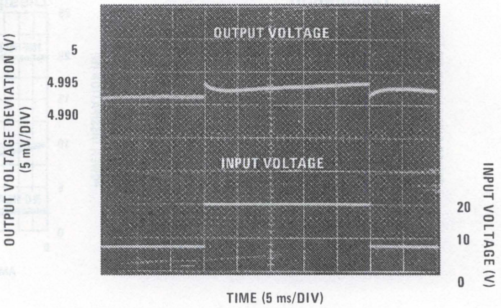
## Typical Performance Characteristics (Continued)

Load Regulation
140AK-5.0, $V_{IN} = 10V$, $T_A = 25°C$



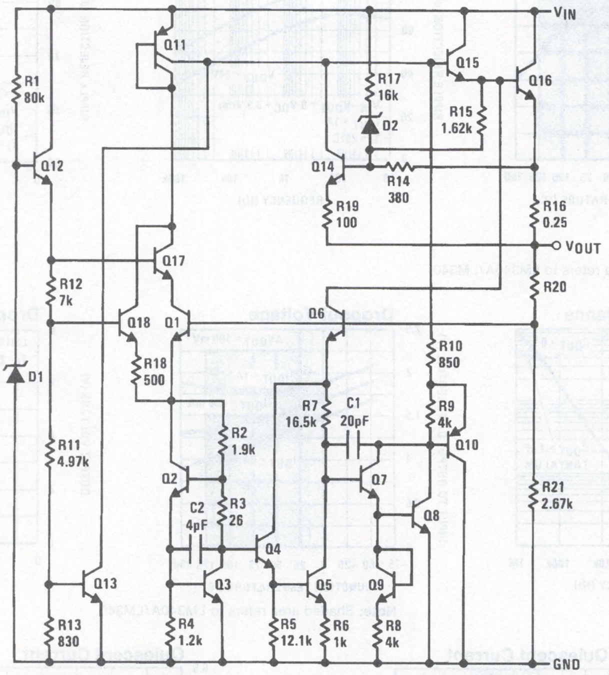
TL/H/7781–5

Line Regulation
140AK-5.0, $I_{OUT} = 1A$, $T_A = 25°C$



TL/H/7781–6

## Equivalent Schematic


VIN
VOUT
GND
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
R1 80k
R2 1.9k
R3 26
R4 1.2k
R5 12.1k
R6 1k
R7 16.5k
R8 4k
R9 4k
R10 850
R11 4.97k
R12 7k
R13 830
R14 380
R15 1.62k
R16 0.25
R17 16k
R18 500
R19 100
R20
R21 2.67k
C1 20pF
C2 4pF
D1
D2

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## Application Hints

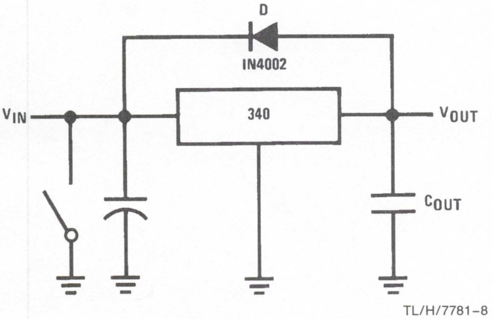
The LM340 is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

**Shorting the Regulator Input:** When using large capacitors at the output of these regulators, a protection diode connected input to output *(Figure 1)* may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial $V_{OUT}$ because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal and the regulator will be destroyed. The fast diode in *Figure 1* will shunt most of the capacitors discharge current around the regulator. Generally no protection diode is required for values of output capacitance $\leq 10\ \mu F$.

**Raising the Output Voltage above the Input Voltage:** Since the output of the LM340 does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the "Shorting the Regulator Input" section.

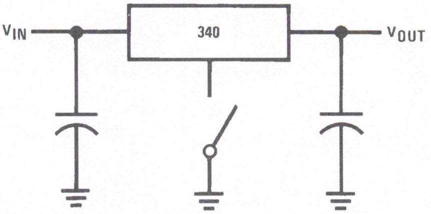
**Regulator Floating Ground***(Figure 2)*: When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to $V_{OUT}$. If ground is reconnected with power "ON", damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, thermal limit ceases operating, or ground should be connected first if power must be left on.

**Transient Voltages:** If transients exceed the maximum rated input voltage of the 340, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.



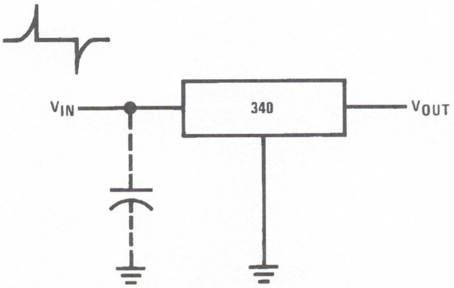
TL/H/7781–8

FIGURE 1. Input Short



TL/H/7781–9

FIGURE 2. Regulator Floating Ground

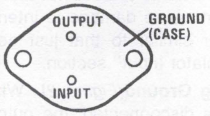


TL/H/7781–10

FIGURE 3. Transients

## Connection Diagrams

**TO-3 Metal Can Package (K and KC)**



TL/H/7781-11

**Bottom View**

**Steel Package Order Numbers:**

**LM140AK-5.0 LM140K-5.0 LM340AK-5.0 LM340K-5.0**
**LM140AK-12 LM140K-12 LM340AK-12 LM340K-12**
**LM140AK-15 LM140K-15 LM340AK-15 LM340K-15**

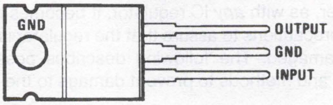
**See Package Number K02A**

**Aluminum Package Order Numbers:**

**LM340KC-5.0**
**LM340KC-12**
**LM340KC-15**

**See Package Number KC02A**

**TO-220 Power Package (T)**



TL/H/7781-12

**Top View**

**Plastic Package Order Numbers:**

**LM340AT-5.0 LM340T-5.0**
**LM340AT-12 LM340T-12**
**LM340AT-15 LM340T-15**

**See Package Number T03B**

**National Semiconductor Corporation**

# LM140L/LM340L Series 3-Terminal Positive Regulators

## General Description

The LM140L series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. The LM140LA is an improved version of the LM78LXX series with a tighter output voltage tolerance (specified over the full military temperature range), higher ripple rejection, better regulation and lower quiescent current. The LM140LA regulators have ±2% $V_{OUT}$ specification, 0.04%/V line regulation, and 0.01%/mA load regulation. When used as a zener diode/resistor combination replacement, the LM140LA usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM140LA to be used in logic systems, instrumentation, Hi-Fi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The LM140LA/LM340LA are available in the low profile metal three lead TO-39 (H) and the LM340LA are also available in the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shut-down circuit takes over, preventing the IC from overheating.

For applications requiring other voltages, see LM117L Data Sheet.

## Features

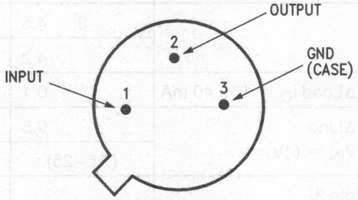
- Line regulation of 0.04%/V
- Load regulation of 0.01%/mA
- Output voltage tolerances of ±2% at $T_j = 25°C$ and ±4% over the temperature range (LM140LA) ±3% over the temperature range (LM340LA)
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in metal TO-39 low profile package (LM140LA/LM340LA) and plastic TO-92 (LM340LA)

## Output Voltage Options

| | | | |
|---|---|---|---|
| LM140LA-5.0 | 5V | LM340LA-5.0 | 5V |
| LM140LA-12 | 12V | LM340LA-12 | 12V |
| LM140LA-15 | 15V | LM340LA-15 | 15V |

## Connection Diagrams

**TO-39 Metal Can Package (H)**

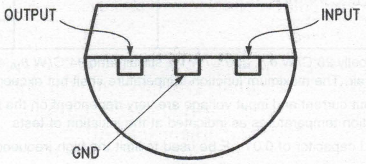


TL/H/7782-2

**Bottom View**

**Order Number LM140LAH-5.0, LM140LAH-12, LM140LAH-15, LM340LAH-5.0, LM340LAH-12 or LM340LAH-15**
**See NS Package Number H03A**

**TO-92 Plastic Package (Z)**



TL/H/7782-3

**Bottom View**

**Order Number LM340LAZ-5.0, LM340LAZ-12 or LM340LAZ-15**
**See NS Package Number Z03A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 5)**

| | |
|---|---|
| Input Voltage | |
| 5.0V, 12V, 15V Output Voltage Options | 35V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | |
| LM140LA | −55°C to +125°C |
| LM340LA | 0°C to +70°C |
| Maximum Junction Temperature | +150°C |
| Storage Temperature Range | |
| Metal Can (H package) | −65°C to +150°C |
| Molded TO-92 | −55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| Plastic TO-92 | +230°C |

## Electrical Characteristics (Note 2)

Test conditions unless otherwise specified. $T_A = -55°C$ to $+125°C$ (LM140LA), $T_A = 0°C$ to $+70°C$ (LM340LA), $I_O = 40$ mA, $C_{IN} = 0.33\ \mu F$, $C_O = 0.01\ \mu F$.

| | Output Voltage Option | | | 5.0V | | | 12V | | | 15V | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Voltage (unless otherwise noted) | | | 10V | | | 19V | | | 23V | | | Units |
| Symbol | Parameter | Conditions | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_O$ | Output Voltage | $T_j = 25°C$ | | 4.9 | 5 | 5.1 | 11.75 | 12 | 12.25 | 14.7 | 15 | 15.3 | V |
| | Output Voltage Over Temp. (Note 4) | LM140LA | $I_O = 1 - 100$ mA | 4.8 | | 5.2 | 11.5 | | 12.5 | 14.4 | | 15.6 | |
| | | | | (7.2−20) | | | (14.5−27) | | | (17.6−30) | | | |
| | | LM340LA | $I_O = 1 - 100$ mA or<br>$I_O = 1 - 40$ mA and<br>$V_{IN} = (\ )V$ | 4.85 | | 5.15 | 11.65 | | 12.35 | 14.55 | | 15.45 | |
| | | | | (7−20) | | | (14.3−27) | | | (17.5−30) | | | |
| $\Delta V_O$ | Line Regulation | $T_j = 25°C$ | $I_O = 40$ mA<br>$V_{IN} = (\ )V$ | | 18 | 30 | | 30 | 65 | | 37 | 70 | mV |
| | | | | (7−25) | | | (14.2−30) | | | (17.3−30) | | | |
| | | | $I_O = 100$ mA<br>$V_{IN} = (\ )V$ | | 18 | 30 | | 30 | 65 | | 37 | 70 | |
| | | | | (7.5−25) | | | (14.5−30) | | | (17.5−30) | | | |
| | Load Regulation | $T_j = 25°C$ | $I_O = 1 - 40$ mA | | 5 | 20 | | 10 | 40 | | 12 | 50 | |
| | | | $I_O = 1 - 100$ mA | | 20 | 40 | | 30 | 80 | | 35 | 100 | |
| | Long Term Stability | | | | 12 | | | 24 | | | 30 | | mV<br>1000 hrs |
| $I_O$ | Quiescent Current | $T_j = 25°C$ | | | 3 | 4.5 | | 3 | 4.5 | | 3.1 | 4.5 | mA |
| | | $T_j = 125°C$ | | | | 4.2 | | | 4.2 | | | 4.2 | |
| $\Delta I_Q$ | Quiescent Current Change | $T_j = 25°C$ | $\Delta$Load $I_O = 1 - 40$ mA | | | 0.1 | | | 0.1 | | | 0.1 | mA |
| | | | $\Delta$Line<br>$V_{IN} = (\ )V$ | | | 0.5 | | | 0.5 | | | 0.5 | |
| | | | | (7.5−25) | | | (14.3−30) | | | (17.5−30) | | | |
| $V_N$ | Output Noise Voltage | $T_j = 25°C$ (Note 3)<br>$f = 10$ Hz−10 kHz | | | 40 | | | 80 | | | 90 | | $\mu V$ |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | $f = 120$ Hz, $V_{IN} = (\ )V$ | | 55 | 62 | | 47 | 54 | | 45 | 52 | | dB |
| | | | | (7.5−18) | | | (14.5−25) | | | (17.5−28.5) | | | |
| | Input Voltage Required to Maintain Line Regulation | $T_j = 25°C$, $I_O = 40$ mA | | 7 | | | 14.2 | | | 17.3 | | | V |

**Note 1:** Thermal resistance of H-package is typically 26°C/W $\theta_{jC}$, 250°C/W $\theta_{jA}$ still air, and 94°C/W $\theta_{jA}$ 400 lf/min of air. For the Z-package is 60°C/W $\theta_{jC}$, 232°C/W $\theta_{jA}$ still air, and 88°C/W $\theta_{jA}$ at 400 lf/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

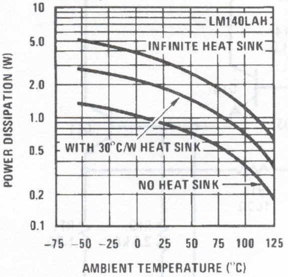
**Note 2:** The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

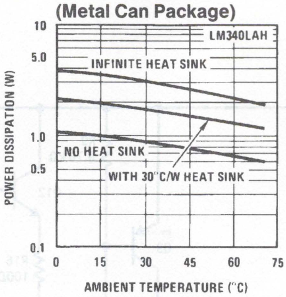
**Note 3:** It is recommended that a minimum load capacitor of 0.01 $\mu F$ be used to limit the high frequency noise bandwidth.

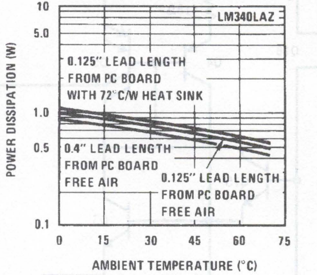
**Note 4:** The temperature coefficient of $V_{OUT}$ is typically within 0.01% $V_O$/°C.

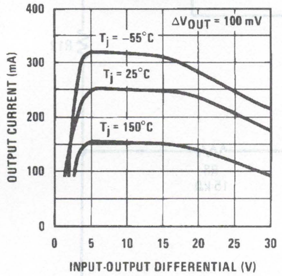
**Note 5:** Refer to RETS140-12H for LM140LAH-12, RETS140-15H for LM140LAH-15 or RETS140-15H for LM140LAH-5.0 military specification.

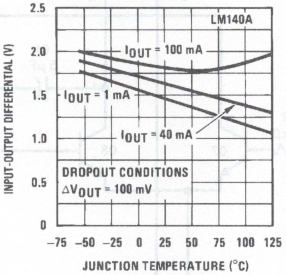
## Typical Performance Characteristics

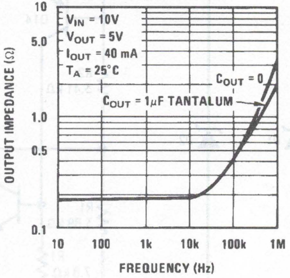

Maximum Average Power Dissipation

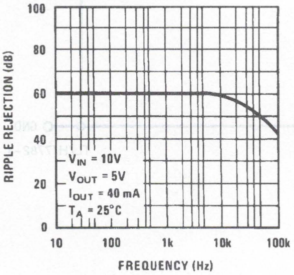

Maximum Average Power Dissipation (Metal Can Package)

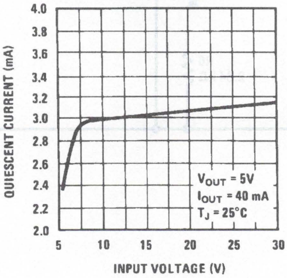

Maximum Average Power Dissipation (Plastic Package)

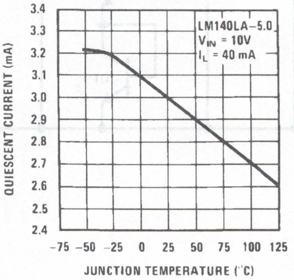

Peak Output Current


Dropout Voltage


Output Impedance


Ripple Rejection

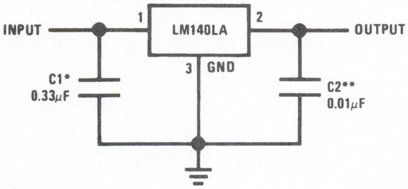

Quiescent Current


Quiescent Current

TL/H/7782-4

## Typical Applications

### Fixed Output Regulator

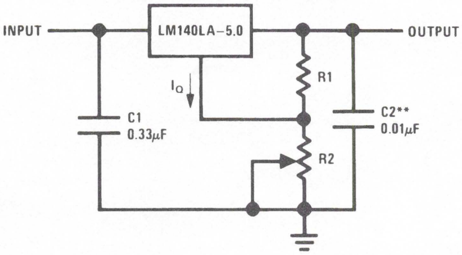

INPUT
1
LM140LA
2
OUTPUT
3
GND
C1*
0.33µF
C2**
0.01µF

TL/H/7782-5

*Required if the regulator is located far from the power supply filter.

**See note 3 in the electrical characteristics table.

### Adjustable Output Regulator

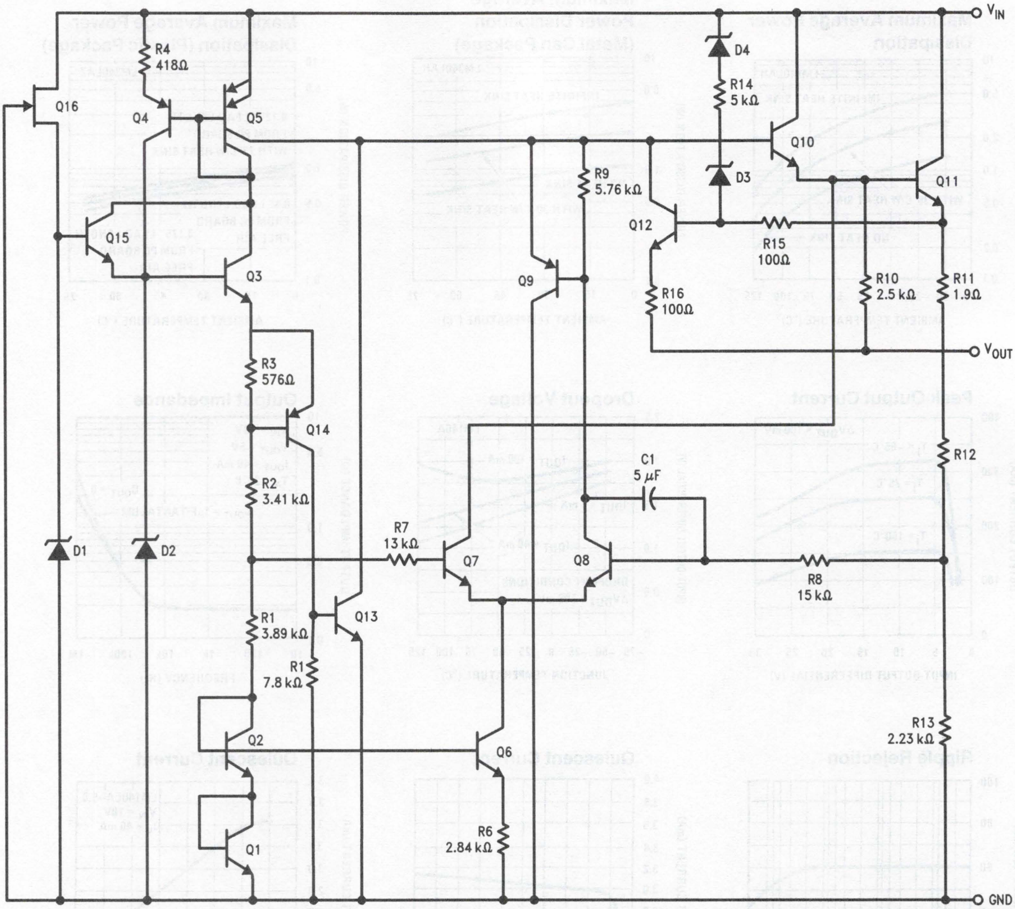

INPUT
LM140LA-5.0
OUTPUT
IO
R1
R2
C1
0.33µF
C2**
0.01µF

TL/H/7782-6

$V_{OUT} = 5V + (5V/R1 + I_O) R2$

$5V/R1 = 3 I_O$ load regulation (L,) [(R1 + R2)/R1] (L, of LM140LA-5.0)

## Equivalent Circuit


VIN
R4
418Ω
Q16
Q4
Q5
Q15
Q3
R3
576Ω
Q14
R2
3.41 kΩ
D1
D2
R1
3.89 kΩ
R1
7.8 kΩ
Q13
Q2
Q1
R7
13 kΩ
Q7
Q8
Q9
R9
5.76 kΩ
Q6
R6
2.84 kΩ
C1
5 μF
Q12
R16
100Ω
D4
R14
5 kΩ
D3
Q10
Q11
R15
100Ω
R10
2.5 kΩ
R11
1.9Ω
VOUT
R12
R8
15 kΩ
R13
2.23 kΩ
GND

TL/H/7782-1

National
Semiconductor
Corporation

# LM145/LM345 Negative Three Amp Regulator

## General Description

The LM145 is a three-terminal negative regulator with a fixed output voltage of −5V or −5.2V, and up to 3A load current capability. This device needs only one external component—a compensation capacitor at the output, making it easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM145 immune to overload conditions. The regulator has current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

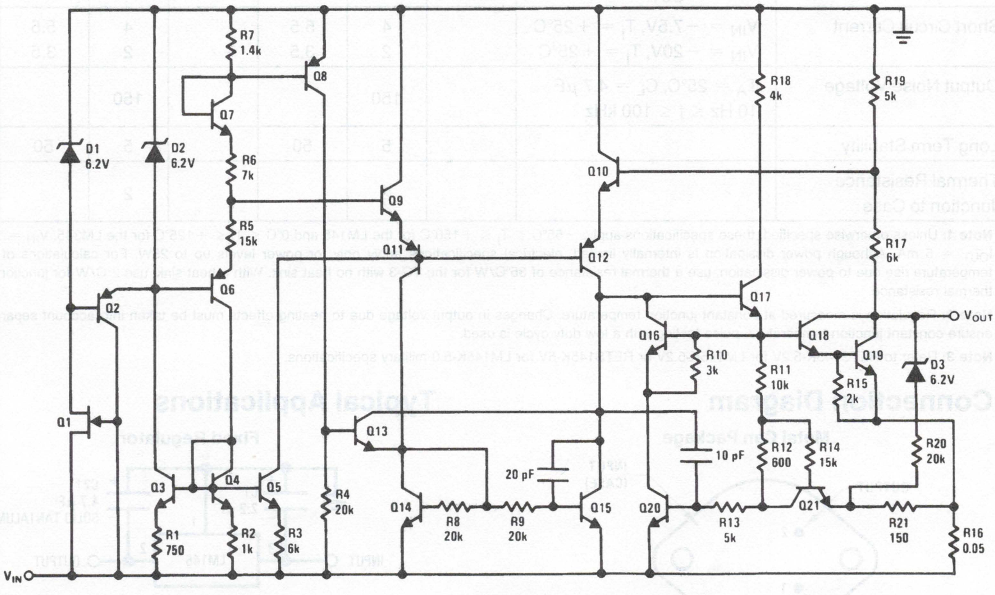
Although primarily intended for fixed output voltage applications, the LM145 may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the device allows this technique to be used with good regulation.

The LM145 comes in a hermetic TO-3 package rated at 25W. A reduced temperature range part LM345 is also available.

## Features

- Output voltage accurate to better than ±2%
- Current limit constant with temperature
- Internal thermal shutdown protection
- Operates with input-output voltage differential of 2.8V at full rated load over full temperature range
- Regulation guaranteed with 25W power dissipation
- 3A output current guaranteed
- Only one external component needed
- 100% electrical burn-in

## Schematic Diagram


R7
1.4k
Q8
Q7
D1
6.2V
D2
6.2V
R6
7k
Q9
R5
15k
Q11
Q6
Q2
Q1
Q13
Q3
Q4
Q5
R1
750
R2
1k
R3
6k
R4
20k
Q14
R8
20k
R9
20k
20 pF
VIN
R18
4k
R19
5k
Q10
Q12
R17
6k
Q17
VOUT
Q16
Q18
Q19
D3
6.2V
R10
3k
R11
10k
R15
2k
10 pF
R12
600
R14
15k
R20
20k
Q15
Q20
R13
5k
Q21
R21
150
R16
0.05

TL/H/7785–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Input Voltage | 20V |
| Input-Output Differential | 20V |
| Power Dissipation | Internally Limited |
| Operating Junction Temperature Range | |
| LM145 | −55°C to +150°C |
| LM345 | 0°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## Electrical Characteristics (−5V & −5.2V) (Note 1)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LM145 | | | LM345 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $T_j = 25°C$, $I_{OUT} = 5$ mA, | | | | | | | |
| 5.0V | $V_{IN} = -7.5$ | −5.1 | −5.0 | −4.9 | −5.2 | −5.0 | −4.8 | V |
| 5.2V | | −5.3 | −5.2 | −5.1 | −5.4 | −5.2 | −5.0 | V |
| Line Regulation (Note 2) | $T_j = 25°C$<br>$-20V \leq V_{IN} \leq -7.5V$ | | 5 | 15 | | 5 | 25 | mV |
| Load Regulation (Note 2) | $T_j = 25°C$, $V_{IN} = -7.5V$<br>$5\text{ mA} \leq I_{OUT} \leq 3A$ | | 30 | 75 | | 30 | 100 | mV |
| Output Voltage | $-20V \leq V_{IN} \leq -7.8V$ | | | | | | | |
| 5.0V | $5\text{ mA} \leq I_{OUT} \leq 3A$ | −5.20 | | −4.80 | −5.25 | | −4.75 | V |
| 5.2V | $P \leq 25W$ | −5.40 | | −5.00 | −5.45 | | −4.95 | V |
| | $T_{MIN} \leq T_j \leq T_{MAX}$ | | | | | | | |
| Quiescent Current | $-20V \leq V_{IN} \leq -7.5V$<br>$5\text{ mA} \leq I_{OUT} \leq 3A$ | | 1.0 | 3.0 | | 1.0 | 3.0 | mA |
| Short Circuit Current | $V_{IN} = -7.5V$, $T_j = +25°C$ | | 4 | 5.5 | | 4 | 5.5 | A |
| | $V_{IN} = -20V$, $T_j = +25°C$ | | 2 | 3.5 | | 2 | 3.5 | A |
| Output Noise Voltage | $T_A = 25°C$, $C_L = 4.7\ \mu F$<br>$10\text{ Hz} \leq f \leq 100\text{ kHz}$ | | 150 | | | 150 | | µV |
| Long Term Stability | | | 5 | 50 | | 5 | 50 | mV |
| Thermal Resistance Junction to Case | | | 2 | | | 2 | | °C/W |

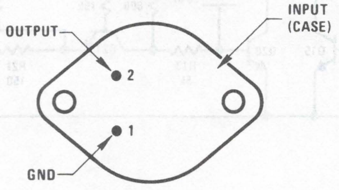
**Note 1:** Unless otherwise specified, these specifications apply: $-55°C \leq T_j \leq +150°C$ for the LM145 and $0°C \leq T_j \leq +125°C$ for the LM345. $V_{IN} = 7.5V$ and $I_{OUT} = 5$ mA. Although power dissipation is internally limited, electrical specifications apply only for power levels up to 25W. For calculations of junction temperature rise due to power dissipation, use a thermal resistance of 35°C/W for the TO-3 with no heat sink. With a heat sink, use 2°C/W for junction to case thermal resistance.

**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

**Note 3:** Refer to RETS145K-5.2V for LM145K-5.2V or RETS145K-5V for LM145K-5.0 military specifications.

## Connection Diagram

### Metal Can Package

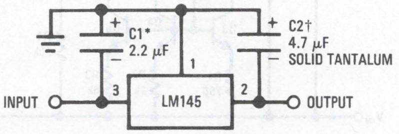


TL/H/7785–2

**Bottom View**
**Order Number LM145K-5.0, LM345K-5.0, LM145K-5.2, or LM345K-5.2**
**See NS Package Number K02A**

## Typical Applications

### Fixed Regulator

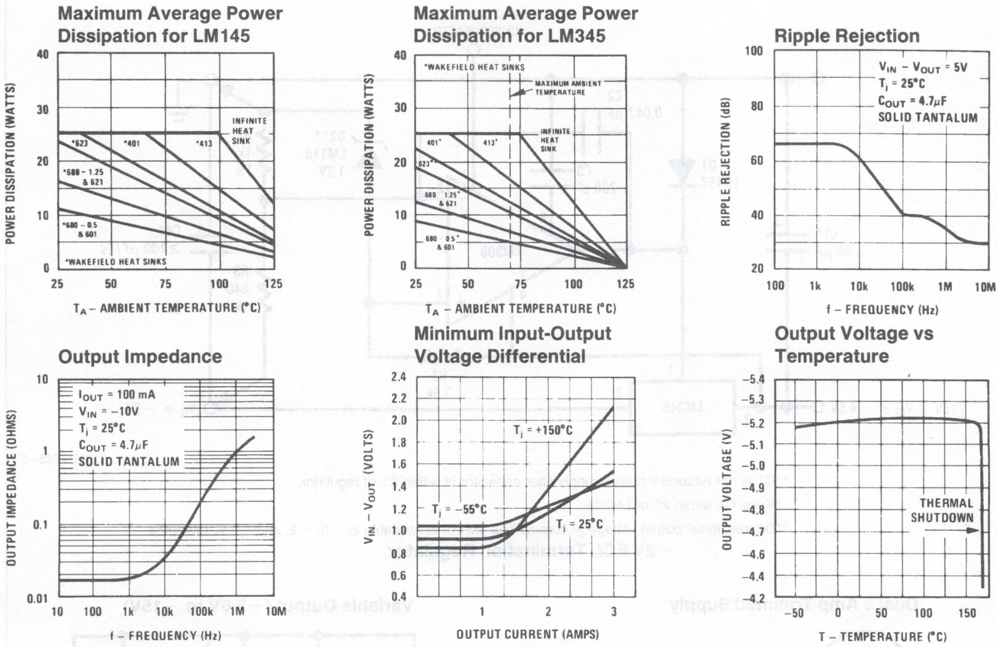


TL/H/7785–3

†Required for stability. For value given, capacitor must be solid tantalum. 50 µF aluminum electrolytic may be substituted. Values given may be increased without limit.

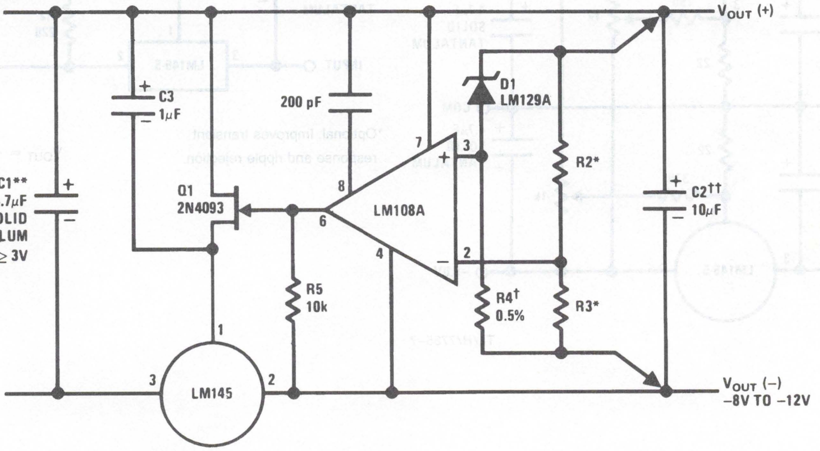
*Required if regulator is separated from filter capacitor. For value given, capacitor must be solid tantulum. 50 µF aluminum electrolytic may be substituted.

## Typical Performance Characteristics



TL/H/7785–4

## Typical Applications (Continued)


VOUT (+)
C1**
4.7μF
SOLID
TANTALUM
VIN – VOUT ≥ 3V
C3
1μF
200 pF
Q1
2N4093
R5
10k
LM145
1
2
3
LM108A
7
3
8
6
4
2
D1
LM129A
R2*
R4†
0.5%
R3*
C2††
10μF
VOUT (–)
–8V TO –12V

TL/H/7785–5

*Select resistors to set output voltage. 1 ppm/C tracking suggested.

**C1 is not needed if power supply filter capacitor is within 3″ of regulator.

†Determines zener current. May be adjusted to minimize temperature drift.

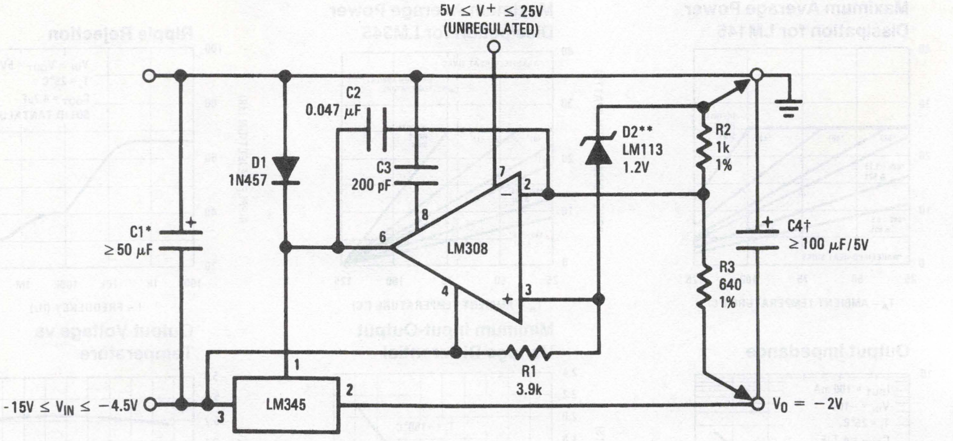
††Solid tantalum.

Load and line regulation < 0.01%

Temperature drift < 0.001%/C

## Typical Applications (Continued)

### High Stability Regulator


5V ≤ V+ ≤ 25V
(UNREGULATED)
C2
0.047 µF
D1
1N457
C3
200 pF
C1*
≥50 µF
7
8
6
2
3
4
LM308
D2**
LM113
1.2V
R2
1k
1%
C4†
≥100 µF/5V
R3
640
1%
R1
3.9k
1
2
3
LM345
−15V ≤ V_IN ≤ −4.5V
V_O = −2V

TL/H/7785-6

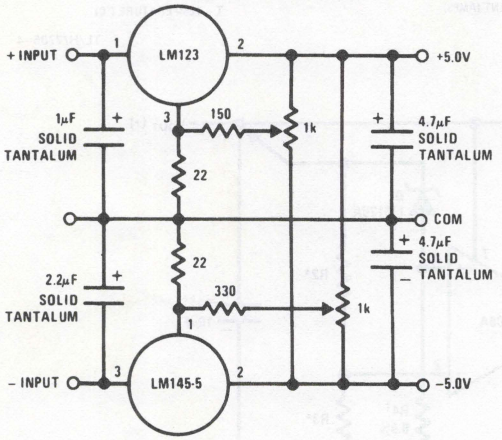
**C1 is not needed if power supply filter capacitor is within 3″ of regulator.

†Keep C4 within 2″ of LM345.

**D2 sets initial output voltage accuracy. The LM113 is available in −5, −2, and −1% tolerance.

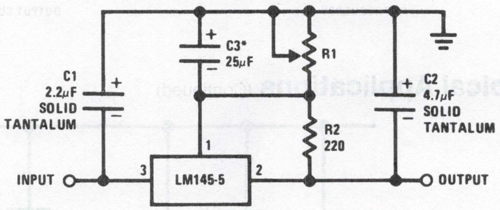
### −2V ECL Termination Regulator

### Dual 3 Amp Trimmed Supply


+INPUT
1
LM123
2
+5.0V
1µF
SOLID
TANTALUM
3
150
1k
4.7µF
SOLID
TANTALUM
22
COM
22
4.7µF
SOLID
TANTALUM
2.2µF
SOLID
TANTALUM
330
1k
1
−INPUT
3
LM145-5
2
−5.0V

TL/H/7785-7

### Variable Output (−5.0V to −15V)


C3*
25µF
R1
C1
2.2µF
SOLID
TANTALUM
C2
4.7µF
SOLID
TANTALUM
R2
220
1
INPUT
3
LM145-5
2
OUTPUT

TL/H/7785-8

*Optional. Improves transient response and ripple rejection.

$$V_{OUT} = -5V\left(\frac{R1 + R2}{R2}\right)$$

**National Semiconductor Corporation**

# LM150/LM350 3 Amp Adjustable Power Regulators

## General Description

The LM150/LM350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

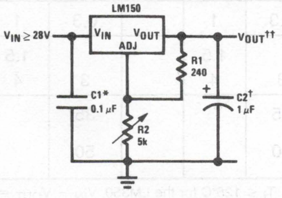
The LM150K/LM350K are packaged in standard steel TO-3 transistor packages. The LM350T is packaged in a TO-220 plastic package. The LM150 is rated for operation from −55°C to +150°C, and the LM350 from 0°C to +125°C.

## Features

- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Output is short circuit protected
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 86 dB ripple rejection

## Typical Applications

**1.2V—25V Adjustable Regulator**



TL/H/9061-1

Full output current not available at high input-output voltages.

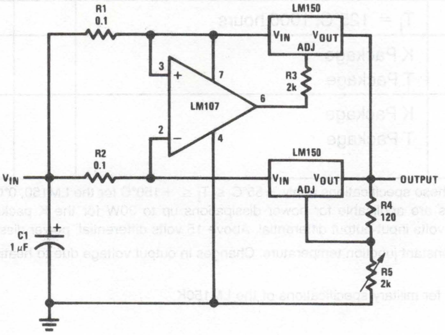
†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R2)$$

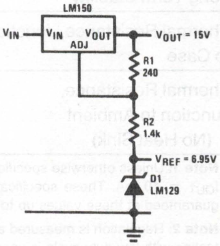
**Note:** Usually R1 = 240Ω for LM150 and R1 = 120Ω for LM350.

**6A Regulator**



TL/H/9061-2

**Regulator and Voltage Reference**



TL/H/9061-3

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Power Dissipation | Internally limited |
| Input−Output Voltage Differential | 35V |
| Operating Junction Temperature Range | |
| LM150 | −55°C to +150°C |
| LM350 | 0°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |
| Plastic Package (Soldering, 4 seconds) | 260°C |

## Preconditioning

| | |
|---|---|
| Burn-In in Thermal Limit | All Devices 100% |

ESD Rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM150 | | | LM350 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $T_A = 25°C$, $3V \leq (V_{IN} - V_{OUT}) \leq 35V$, $I_L = 0.010A$ (Note 2) | | 0.005 | 0.01 | | 0.005 | 0.03 | %/V |
| Load Regulation | $T_A = 25°C$, $10mA \leq I_{OUT} \leq 3A$ | | 0.1 | 0.3 | | 0.1 | 0.5 | % |
| Thermal Regulation | Pulse = 20 ms, $T_j = 25°C$ | | 0.002 | 0.01 | | 0.002 | 0.03 | %/W |
| Adjustment Pin Current | | | 50 | 100 | | 50 | 100 | μA |
| Adjustment Pin Current Change | $10\ mA \leq I_L \leq 3A$<br>$3V \leq (V_{IN} - V_{OUT}) \leq 35V$ | | 0.2 | 5 | | 0.2 | 5 | μA |
| Reference Voltage | $3V \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 3)<br>$10\ mA \leq I_{OUT} \leq 3A$, $P \leq 30W$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation | $3V \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 2)<br>$I_L = 0.010A$ | | 0.02 | 0.05 | | 0.02 | 0.07 | %/V |
| Load Regulation | $10\ mA \leq I_{OUT} \leq 3A$, (Note 2) | | 0.3 | 1 | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \leq T_j \leq T_{MAX}$ | | 1 | | | 1 | | % |
| Minimum Load Current | $V_{IN} - V_{OUT} = 35V$ | | 3.5 | 5 | | 3.5 | 10 | mA |
| Current Limit | $(V_{IN} - V_{OUT}) \leq 10V$<br>$(V_{IN} - V_{OUT}) = 30V$, $T_j = +25°C$ | 3.0<br>0.3 | 4.5<br>1 | | 3.0<br>0.25 | 4.5<br>1 | | A<br>A |
| RMS Output Noise, % of $V_{OUT}$ | $T_j = 25°C$, $10\ Hz \leq f \leq 10\ kHz$ | | 0.001 | | | 0.001 | | % |
| Ripple Rejection Ratio | $V_{OUT} = 10V$, $f = 120\ Hz$<br>$C_{ADJ} = 10\ \mu F$ | <br>66 | 65<br>86 | | <br>66 | 65<br>86 | | dB<br>dB |
| Long Term Stability | $T_j = 125°C$, 1000 hours | | 0.3 | 1 | | 0.3 | 1 | % |
| Thermal Resistance, Junction to Case | K Package<br>T Package | | <br>3 | 1.5<br>4 | | <br>3 | 1.5<br>4 | °C/W<br>°C/W |
| Thermal Resistance, Junction to Ambient (No Heat Sink) | K Package<br>T Package | | 35<br>50 | | | 35<br>50 | | °C/W<br>°C/W |

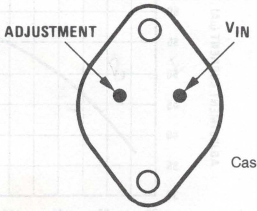
**Note 1:** Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM150, $0°C \leq T_j \leq 125°C$ for the LM350. $V_{IN} - V_{OUT} = 5V$, and $I_{OUT} = 10$ mA. These specifications are applicable for power dissipations up to 30W for the K package and 25W for the T package. Power dissipation is guaranteed at these values up to 15 volts input-output differential. Above 15 volts differential, power dissipation will be limited by internal protection circuitry.

**Note 2:** Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**Note 3:** Refer to RETS150K drawing for military specifications of the LM150K.

## Connection Diagrams (See Physical Dimensions section for further information)

**(TO-3 STEEL)**
**Metal Can Package**

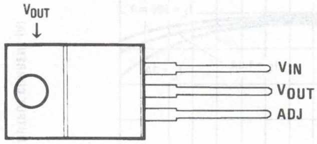

ADJUSTMENT
$V_{IN}$
Case is Output

TL/H/9061–4

**Bottom View**

**Order Number LM150K STEEL or LM350K STEEL**
**See NS Package Number K02A**

**(TO-220)**
**Plastic Package**

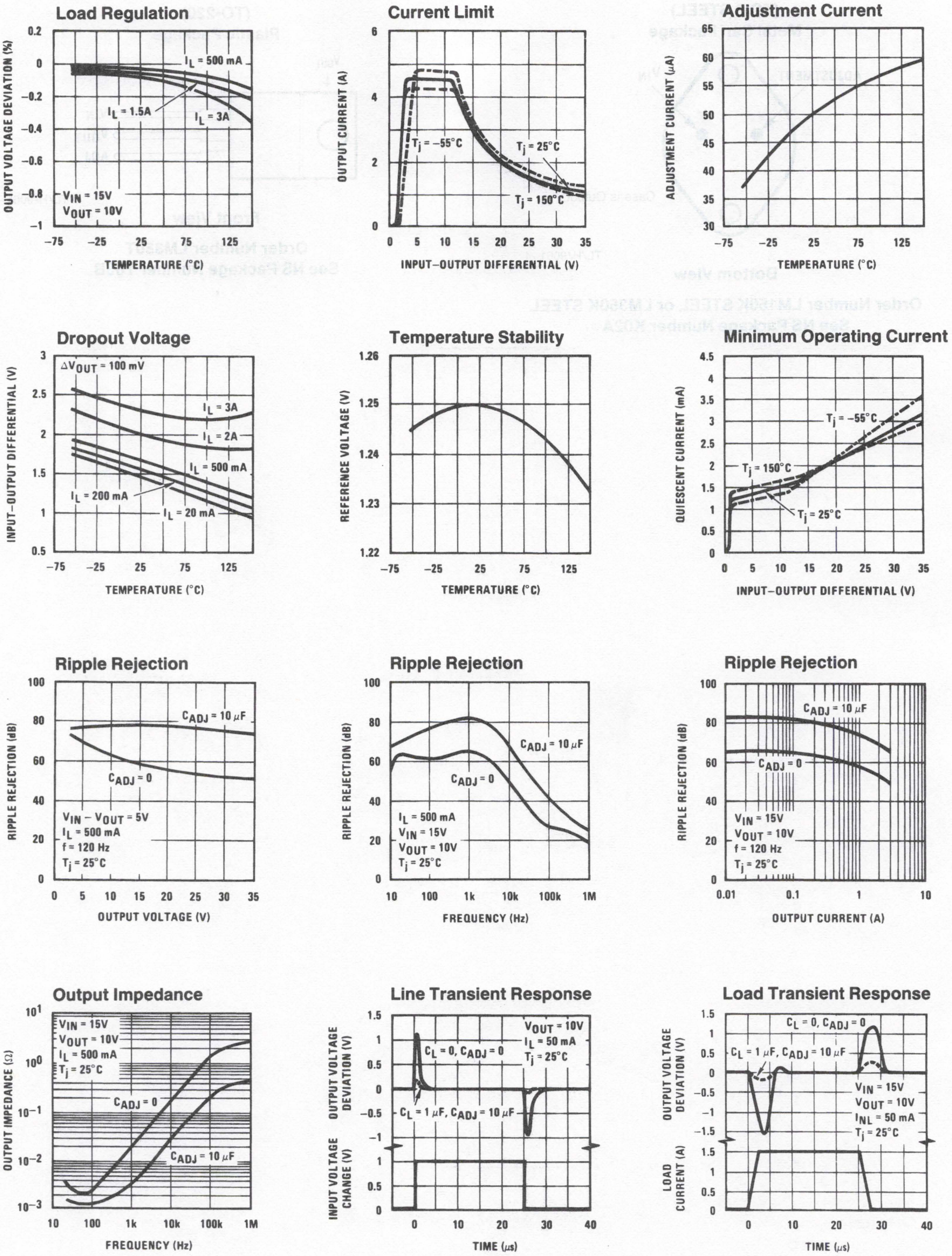

$V_{OUT}$
$V_{IN}$
$V_{OUT}$
ADJ

TL/H/9061–5

**Front View**

**Order Number LM350T**
**See NS Package Number T03B**

## Typical Performance Characteristics

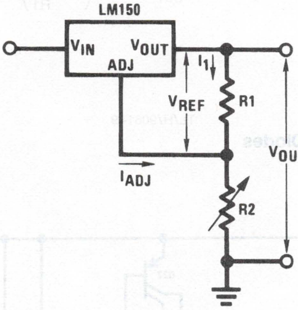


TL/H/9061–6

## Application Hints

In operation, the LM150 develops a nominal 1.25V reference voltage, $V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2.$$



TL/H/9061-7

**FIGURE 1**

Since the 50 $\mu$A current from the adjustment terminal represents an error term, the LM150 was designed to minimize $I_{ADJ}$ and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

### EXTERNAL CAPACITORS

An input bypass capacitor is recommended. A 0.1 $\mu$F disc or 1 $\mu$F solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 $\mu$F bypass capacitor 86 dB ripple rejection is obtainable at any output level. Increases over 10 $\mu$F do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

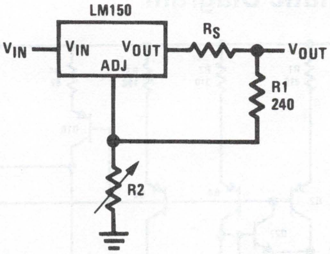
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 $\mu$F in aluminum electrolytic to equal 1 $\mu$F solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 $\mu$F disc may seem to work better than a 0.1 $\mu$F disc as a bypass.

Although the LM150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 $\mu$F solid tantalum (or 25 $\mu$F aluminum electrolytic) on the output swamps this effect and insures stability.

### LOAD REGULATION

The LM150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × $I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

*Figure 2* shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9061-8

**FIGURE 2. Regulator with Line Resistance in Output Lead**

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

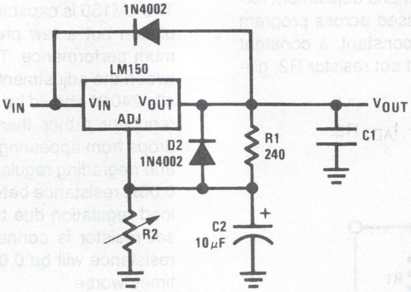
### PROTECTION DIODES

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 $\mu$F capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{IN}$. In the LM150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 $\mu$F or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 $\mu$F capacitance. *Figure 3* shows an LM150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

## Application Hints (Continued)


D1
1N4002
LM150
VIN
VIN
VOUT
ADJ
D2
1N4002
R1
240
C1
VOUT
R2
C2
10μF
+

D1 protects against C1

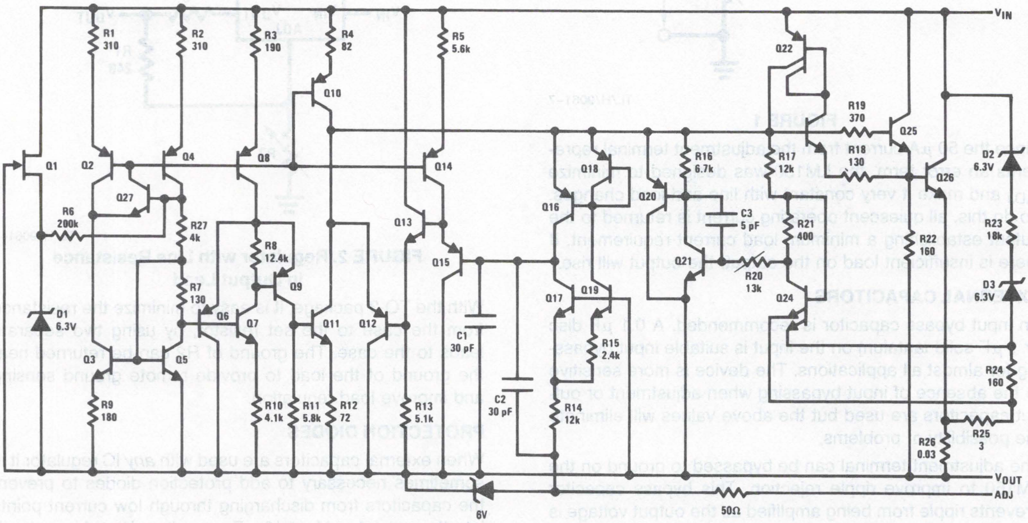
D2 protects against C2

$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

TL/H/9061-9

**FIGURE 3. Regulator with Protection Diodes**

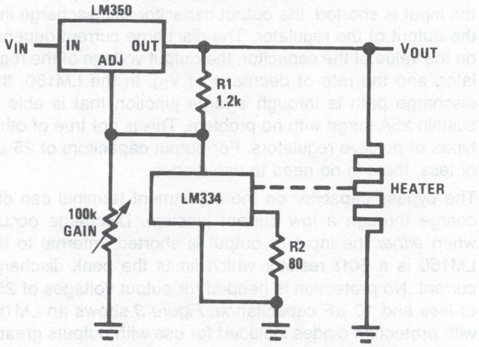
## Schematic Diagram


R1
310
R2
310
R3
190
R4
82
R5
5.6k
Q10
Q1
Q2
Q4
Q8
Q14
Q27
R6
200k
R27
4k
R8
12.4k
Q13
Q15
Q9
R7
130
Q6
Q7
Q11
Q12
C1
30 pF
C2
30 pF
D1
6.3V
Q3
Q5
R9
180
R10
4.1k
R11
5.8k
R12
72
R13
5.1k
6V
VIN
Q22
R19
370
R18
130
Q25
R16
6.7k
R17
12k
Q18
Q20
Q16
C3
5 pF
R21
400
Q21
R20
13k
Q17
Q19
R15
2.4k
R14
12k
Q24
D2
6.3V
Q26
R23
18k
R22
160
D3
6.3V
R24
160
R25
3
R26
0.03
VOUT
ADJ
50Ω

TL/H/9061-10

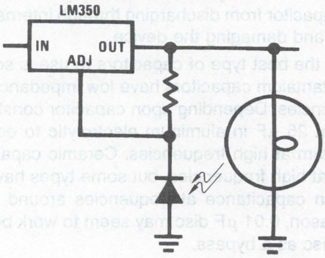
## Typical Applications (Continued)

### Temperature Controller


LM350
VIN
IN
OUT
ADJ
VOUT
R1
1.2k
LM334
HEATER
100k
GAIN
R2
80

TL/H/9061-11

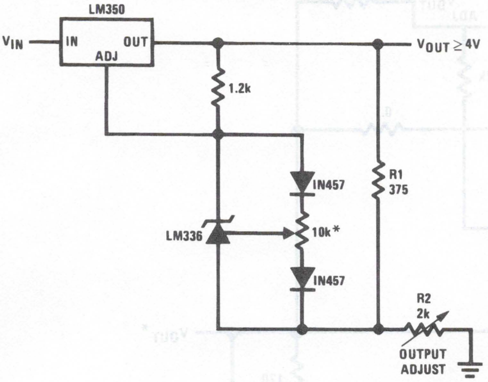
### Light Controller


LM350
IN
OUT
ADJ

TL/H/9061-12

## Typical Applications (Continued)

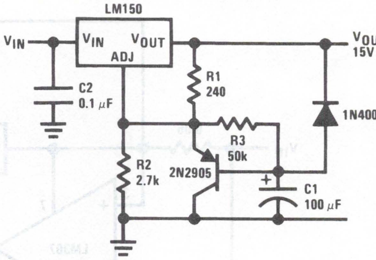
### Precision Power Regulator with Low Temperature Coefficient


LM350
VIN
IN
OUT
ADJ
VOUT ≥ 4V
1.2k
IN457
LM336
10k*
IN457
R1
375
R2
2k
OUTPUT ADJUST

*Adjust for 3.75V across R1

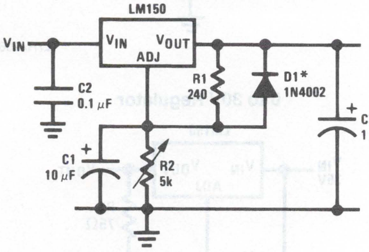
TL/H/9061–13

### Slow Turn-ON 15V Regulator


LM150
VIN
VIN
VOUT
ADJ
VOUT
15V
C2
0.1 μF
R1
240
1N4002
R3
50k
R2
2.7k
2N2905
C1
100 μF

TL/H/9061–14

### Adjustable Regulator with Improved Ripple Rejection

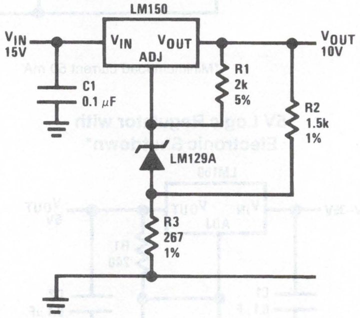

LM150
VIN
VIN
VOUT
ADJ
C2
0.1 μF
R1
240
D1*
1N4002
C3
1 μF†
C1
10 μF
R2
5k

†Solid tantalum

*Discharges C1 if output is shorted to ground

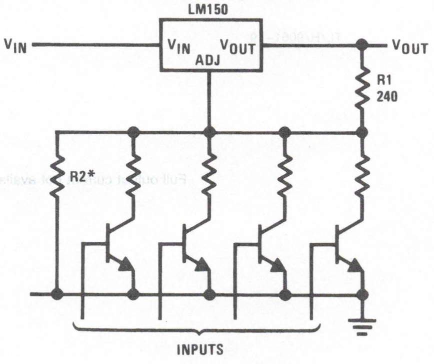
TL/H/9061–15

### High Stability 10V Regulator


LM150
VIN
15V
VIN
VOUT
ADJ
VOUT
10V
C1
0.1 μF
R1
2k
5%
R2
1.5k
1%
LM129A
R3
267
1%

TL/H/9061–16

### Digitally Selected Outputs

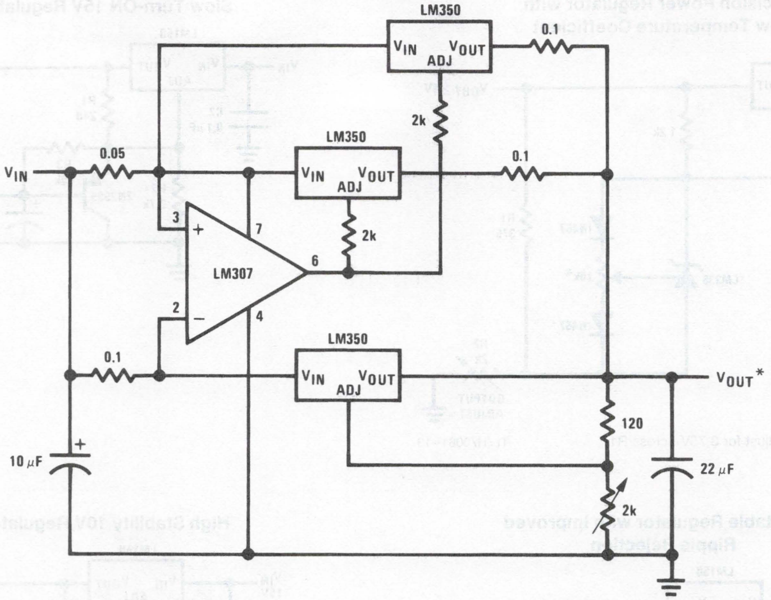

LM150
VIN
VIN
VOUT
ADJ
VOUT
R1
240
R2*
INPUTS

TL/H/9061–17

*Sets maximum $V_{OUT}$

## Typical Applications (Continued)

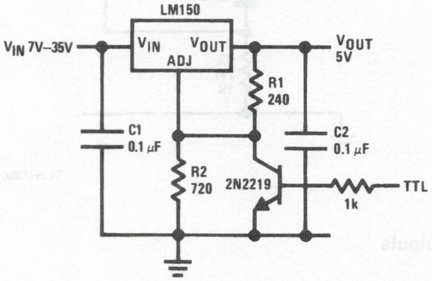
### 10A Regulator


LM350
V_IN
V_OUT
ADJ
0.1
2k
V_IN
0.05
LM350
0.1
3
+
7
2k
6
LM307
2
−
4
LM350
0.1
V_OUT*
120
10 μF
+
22 μF
2k

*Minimum load current 50 mA

TL/H/9061–18

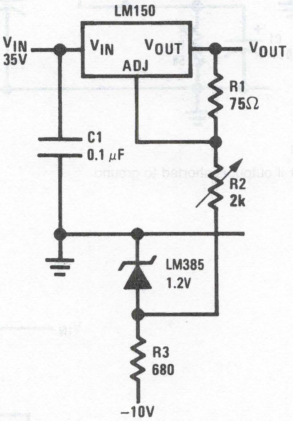
### 5V Logic Regulator with Electronic Shutdown*


LM150
V_IN 7V–35V
V_IN
V_OUT
ADJ
V_OUT
5V
R1
240
C1
0.1 μF
C2
0.1 μF
R2
720
2N2219
1k
TTL

TL/H/9061–19

*Min output ≈ 1.2V

### 0 to 30V Regulator

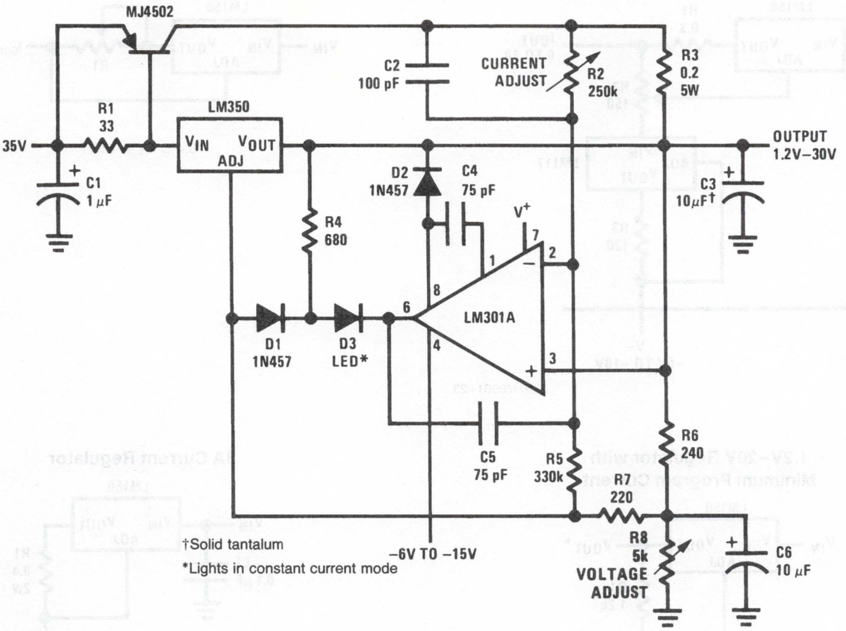

LM150
V_IN
35V
V_IN
V_OUT
ADJ
V_OUT
R1
75Ω
C1
0.1 μF
R2
2k
LM385
1.2V
R3
680
−10V

TL/H/9061–20

Full output current not available at high input-output voltages

## Typical Applications (Continued)

### 5A Constant Voltage/Constant Current Regulator

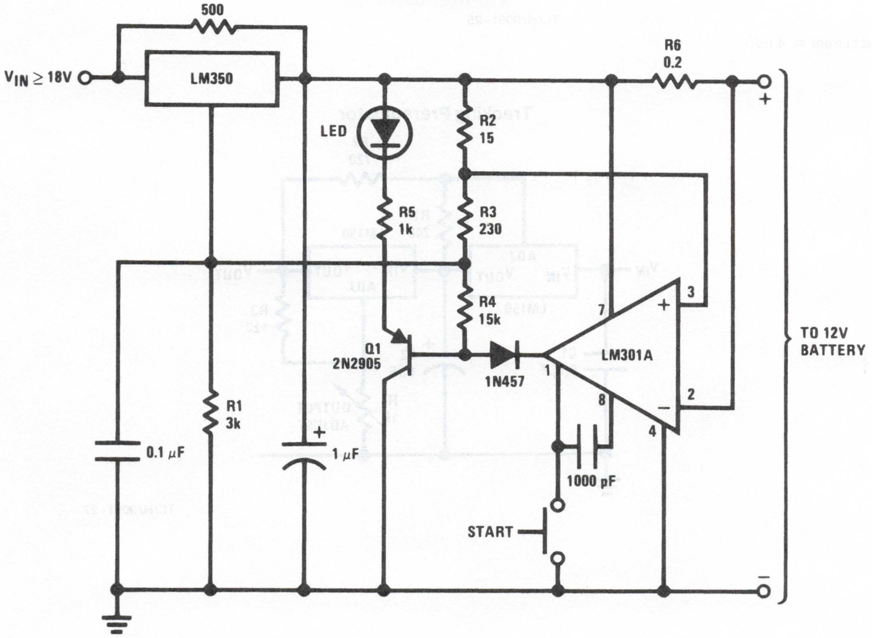

MJ4502
C2
100 pF
CURRENT
ADJUST
R2
250k
R3
0.2
5W
R1
33
LM350
$V_{IN}$
$V_{OUT}$
ADJ
35V
+
C1
1 μF
D2
1N457
C4
75 pF
$V^+$
7
2
1
8
6
LM301A
4
3
−
+
R4
680
D1
1N457
D3
LED*
OUTPUT
1.2V–30V
C3
10μF†
R6
240
C5
75 pF
R5
330k
R7
220
R8
5k
VOLTAGE
ADJUST
−6V TO −15V
C6
10 μF

†Solid tantalum

*Lights in constant current mode

TL/H/9061–21

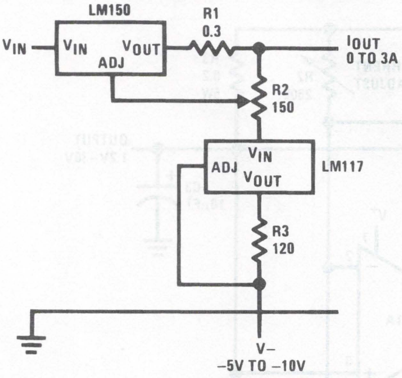
### 12V Battery Charger


500
$V_{IN} \geq 18V$
LM350
LED
R2
15
R5
1k
R3
230
R4
15k
Q1
2N2905
1N457
LM301A
7
3
+
1
8
2
−
4
R1
3k
0.1 μF
1 μF
1000 pF
START
R6
0.2
TO 12V
BATTERY
+
−

TL/H/9061–22

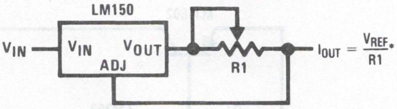
## Typical Applications (Continued)

### Adjustable Current Regulator


LM150
R1
0.3
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$I_{OUT}$
0 TO 3A
R2
150
$V_{IN}$
ADJ
$V_{OUT}$
LM117
R3
120
V−
−5V TO −10V

TL/H/9061-23

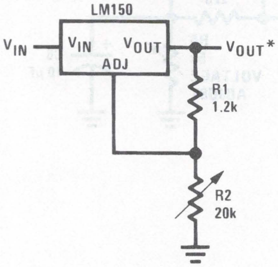
### Precision Current Limiter


LM150
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
R1
$I_{OUT} = \frac{V_{REF}}{R1}$*

$^*0.4 \le R_1 \le 120\Omega$

TL/H/9061-24

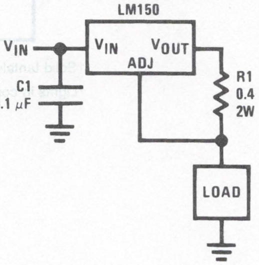
### 1.2V–20V Regulator with Minimum Program Current


LM150
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$*
R1
1.2k
R2
20k

TL/H/9061-25

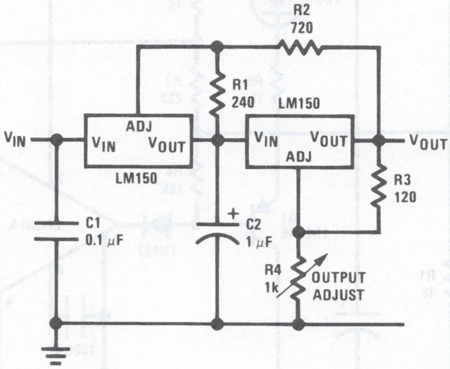
*Minimum load current ≈ 4 mA

### 3A Current Regulator


LM150
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
C1
0.1 µF
R1
0.4
2W
LOAD

TL/H/9061-26

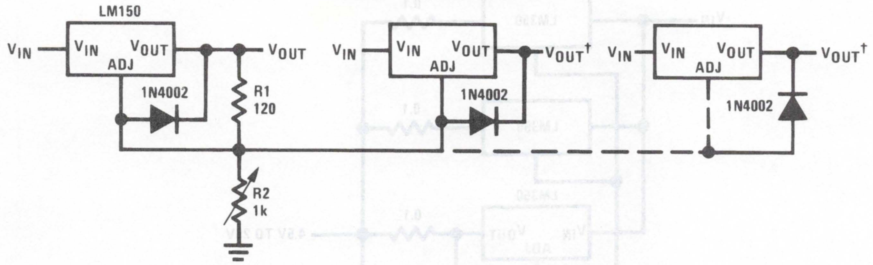
### Tracking Preregulator


R2
720
R1
240
LM150
ADJ
$V_{IN}$
$V_{IN}$
$V_{OUT}$
LM150
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
R3
120
C1
0.1 µF
+
C2
1 µF
R4
1k
OUTPUT
ADJUST

TL/H/9061-27

## Typical Applications (Continued)

### Adjusting Multiple On-Card Regulators with Single Control*

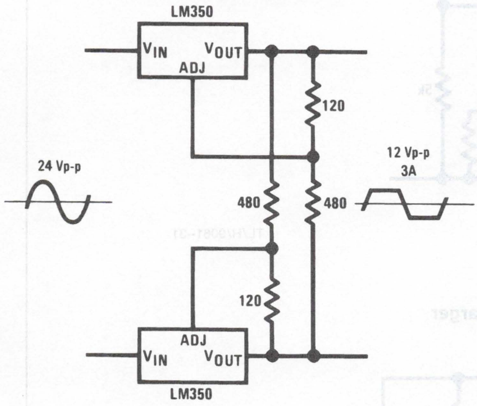

LM150
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
1N4002
R1
120
R2
1k
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†
1N4002
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$†
1N4002

TL/H/9061-28

†Minimum load—10 mA

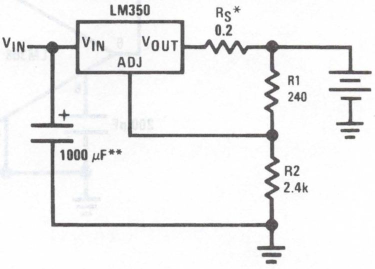
*All outputs within ±100 mV

### AC Voltage Regulator


LM350
$V_{IN}$
$V_{OUT}$
ADJ
120
24 Vp-p
480
480
12 Vp-p
3A
120
ADJ
$V_{IN}$
$V_{OUT}$
LM350

TL/H/9061-29

### Simple 12V Battery Charger


LM350
$R_S$*
0.2
$V_{IN}$
$V_{IN}$
$V_{OUT}$
ADJ
R1
240
+
1000 μF**
R2
2.4k

TL/H/9061-30

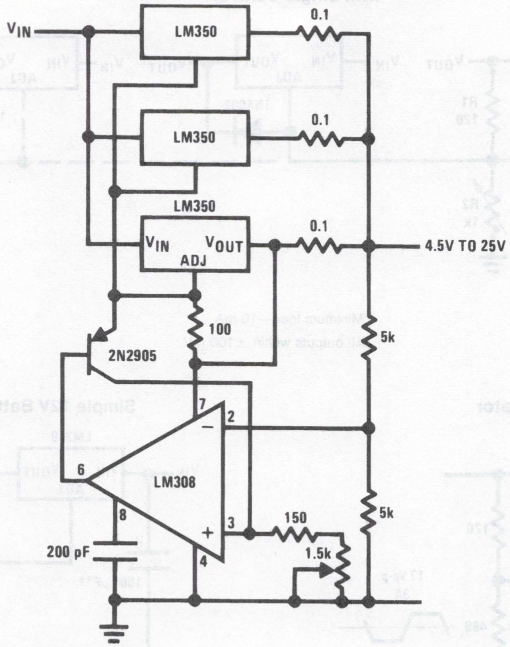
*$R_S$—sets output impedance of charger: $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$

Use of $R_S$ allows low charging rates with fully charged battery.

**1000 μF is recommended to filter out any input transients

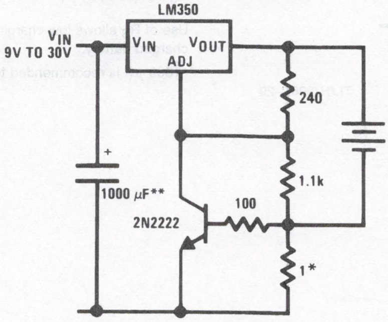
## Typical Applications (Continued)

### Adjustable 10A Regulator


VIN
LM350
0.1
LM350
0.1
LM350
VIN
VOUT
ADJ
0.1
4.5V TO 25V
100
2N2905
5k
7
2
6
LM308
8
200 pF
3
4
150
1.5k
5k

TL/H/9061-31

### Current Limited 6V Charger


LM350
VIN
9V TO 30V
VIN
VOUT
ADJ
240
1000 μF**
1.1k
2N2222
100
1*

TL/H/9061-32

*Sets peak current (2A for 0.3Ω)

**1000 μF is recommended to filter out any input transients.

**National Semiconductor Corporation**

**PRELIMINARY**

# LM196/LM396 10 Amp Adjustable Voltage Regulator

## General Description

The LM196 is a 10 amp regulator, adjustable from 1.25V to 15V, which uses a revolutionary new IC fabrication structure to combine high power discrete transistor technology with modern monolithic linear IC processing. This combination yields a high-performance single-chip regulator capable of supplying in excess of 10 amps and operating at power levels up to 70 watts. The regulators feature on-chip trimming of reference voltage to ±0.8% and simultaneous trimming of reference temperature drift to 30 ppm/°C typical. Thermal interaction between control circuitry and the pass transistor which affects the output voltage has been reduced to extremely low levels by strict attention to isothermal layout. This interaction, called thermal regulation, is 100% tested.

These new regulators have all the protection features of popular lower power adjustable regulators such as LM117 and LM138, including current limiting and thermal limiting. The combination of these features makes the LM196 immune to blowout from output overloads or shorts, even if the adjustment pin is accidentally disconnected. All devices are "burned-in" in thermal shutdown to guarantee proper operation of these protective features under actual overload conditions.

Output voltage is continuously adjustable from 1.25V to 15V. Higher output voltages are possible if the maximum input-output voltage differential specification is not exceeded. Full load current of 10A is available at all output voltages, subject only to the maximum power limit of 70W and of course, maximum junction temperature.

The LM196 is exceptionally easy to use. Only two external resistors are used to to set output voltage. On-chip adjustment of the reference voltage allows a much tighter specification of output voltage, eliminating any need for trimming in most cases. The regulator will tolerate an extremely wide range of reactive loads, and does not depend on external capacitors for frequency stabilization. Heat sink requirements are much less stringent, because overload situations do not have to be accounted for—only worst-case full load conditions.

The LM196 is in a TO-3 package with oversized (0.060″) leads to provide best possible load regulation. Operating junction temperature range is −55°C to +150°C. The LM396 is specified for a 0°C to +125°C junction temperature range.

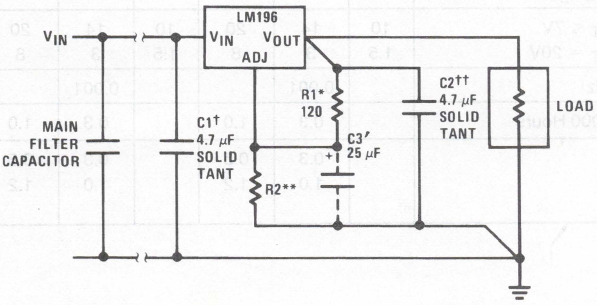
## Features

### Common

- Output pre-trimmed to ±0.8%
- 10A guaranteed output current
- 100% burn-in in thermal limit
- 70W maximum power dissipation
- Adjustable output—1.25V to 15V
- Internal current and power limiting
- Guaranteed thermal resistance
- Output voltage guaranteed under worst-case conditions
- Output is short circuit protected

## Typical Applications

$$V_{OUT} = (1.25V)\left(\frac{R1 + R2}{R1}\right) + I_{ADJ}\,(R2)$$



*For best TC of $V_{OUT}$, R1 should be wirewound or metal film, 1% or better.

**R2 should be same type as R1, with TC tracking of 30 ppm/°C or better.

†C1 is necessary only if main filter capacitor is more than 6″ away, assuming #18 or larger leads.

††C2 is not absolutely necessary, but is suggested to lower high frequency output impedance. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

′C3 improves ripple rejection, output impedance, and noise. C2 should be 1 μF or larger close to the regulator if C3 is used.

TL/H/9059–1

**FIGURE 1. Basic 1.25V to 15V Regulator**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input-Output Voltage Differential | 20V |
| Operating Junction Temperature Range | |
| LM196 Control Section | −55°C to +150°C |
| Power Transistor | −55°C to +200°C |
| LM396 Control Section | 0°C to +125°C |
| Power Transistor | 0°C to +175°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

ESD rating to be determined

## Pre-Conditioning

**100% Burn-In in Thermal Limit**

## Electrical Characteristics (Note 1)

| Parameter | Conditions | LM196 | | | LM396 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reference Voltage | $I_{OUT} = 10$ mA | 1.24 | 1.25 | 1.26 | 1.23 | 1.25 | 1.27 | V |
| Reference Voltage (Note 2) | $V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$<br>10 mA $\le I_{OUT}$ 10A, $P \le P_{MAX}$<br>Full Temperature Range | 1.22 | 1.25 | 1.28 | 1.21 | 1.25 | 1.29 | V |
| Line Regulation | $V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$ | | 0.005 | 0.01 | | 0.005 | 0.02 | %/V |
| (Note 3) | Full Temperature Range | | | 0.05 | | | 0.05 | %/V |
| Load Regulation<br>LM196/LM396 | 10 mA $\le I_{OUT} \le$ 10A<br>$V_{MIN} \le V_{IN} - V_{OUT} \le 10V$, $P \le P_{MAX}$ | | | 0.1 | | | 0.1 | %/V |
| (Note 4) | Full Temperature Range | | | 0.15 | | | 0.15 | %/A |
| Ripple Rejection | $C_{ADJ} = 25\ \mu F$, f = 120 Hz | 60 | 74 | | 66 | 74 | | dB |
| (Note 5) | Full Temperature Range | 54 | | | 54 | | | dB |
| Thermal Regulation (Note 6) | $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 10A$ | | 0.003 | 0.005 | | 0.003 | 0.015 | %/W |
| Average Output Voltage Temperature Coefficient | $T_{jMIN} \le T_j \le T_{jMAX}$<br>(See Curves for Limits) | | 0.003 | | | 0.003 | | %/°C |
| Adjustment Pin Current | | | 50 | 100 | | 50 | 100 | µA |
| Adjustment Pin Current Change (Note 7) | 10 mA $\le I_{OUT} \le$ 10A<br>$3V \le V_{IN} - V_{OUT} \le 20V$<br>$P \le P_{MAX}$, Full Temperature Range | | | 3 | | | 3 | µA |
| Minimum Load Current (Note 9) | $2.5V \le (V_{IN} - V_{OUT}) \le 20V$<br>Full Temperature Range | | | 10 | | | 10 | mA |
| Current Limit | $2.5 \le (V_{IN} - V_{OUT} \le 7V$ | 10 | 14 | 20 | 10 | 14 | 20 | A |
| (Note 8) | $V_{IN} - V_{OUT} = 20V$ | 1.5 | 3 | 8 | 1.5 | 3 | 8 | A |
| Rms Output Noise | 10 Hz $\le$ f $\le$ 10 kHz | | 0.001 | | | 0.001 | | $\%V_{OUT}$ |
| Long Term Stability | $T_j = 125°C$, t = 1000 Hours | | 0.3 | 1.0 | | 0.3 | 1.0 | % |
| Thermal Resistance Junction to Case | Control Circuitry | | 0.3 | 0.5 | | 0.3 | 0.5 | °C/W |
| (Note 10) | Power Transistor | | 1.0 | 1.2 | | 1.0 | 1.2 | °C/W |

## Electrical Characteristics (Note 1) (Continued)

| Parameter | Conditions | LM196 |  |  | LM396 |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Power Dissipation ($P_{MAX}$) (Note 11) | $7.0V \le V_{IN} - V_{OUT} \le 12V$ | 70 | 100 |  | 70 | 100 |  | W |
|  | $V_{IN} - V_{OUT} = 15V$ | 50 |  |  | 50 |  |  | W |
|  | $V_{IN} - V_{OUT} = 18V$ | 36 |  |  | 36 |  |  | W |
| Drop-Out Voltage LM196/LM396 | $I_{OUT} = 10A$, | | 2.1 | 2.5 | | 2.1 | 2.5 | V |
|  | Full Temperature Range |  |  | 2.75 |  |  | 2.75 |  |

**Note 1:** Unless otherwise stated, these specifications apply for $T_j = 25°C$, $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 10$ mA to 10A.

**Note 2:** This is a worst-case specification which includes all effects due to input voltage, output current, temperature, and power dissipation. Maximum power ($P_{MAX}$) is specified under Electrical Characteristics.

**Note 3:** Line regulation is measured on a short-pulse, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Line Regulation under Application Hints.

**Note 4:** Load regulation on the 2-pin package is determined primarily by the voltage drop along the output pin. Specifications apply for an external Kelvin sense connnection at a point on the output pin ¼″ from the bottom of the package. Testing is done on a short-pulse-width, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Load Regulation under Application Hints.

**Note 5:** Ripple rejection is measured with the adjustment pin bypassed with 25 μF capacitor, and is therefore independent of output voltage. With no load or bypass capacitor, ripple rejection is determined by line regulation and may be calculated from; $RR = 20 \log_{10} [100/(K \times V_{OUT})]$ where K is line regulation expressed in %/V. At frequencies below 100 Hz, ripple rejection may be limited by thermal effects, if load current is above 1A.

**Note 6:** Thermal regulation is defined as the change in output voltage during the time period of 0.2 ms to 20 ms after a change in power dissipation in the regulator, due to either a change in input voltage or output current. See graphs and discussion of thermal effects under Application Hints.

**Note 7:** Adjustment pin current change is specified for the worst-case combination of input voltage, output current, and power dissipation. Changes due to temperature must be taken into account separately. See graph of adjustment pin current vs temperature.

**Note 8:** Current limit is measured 10 ms after a short is applied to the output. DC measurements may differ slightly due to the rapidly changing junction temperature, tending to drop slightly as temperature increases. A minimum available load current of 10A is guaranteed over the full temperature range as long as power dissipation does not exceed 70W, and $V_{IN} - V_{OUT}$ is less than 7.0V.

**Note 9:** Minimum load current of 10 mA is normally satisfied by the resistor divider which sets up output voltage.

**Note 10:** Total thermal resistance, junction-to-ambient, will include junction-to-case thermal resistance plus interface resistance and heat sink resistance. See discussion of Heat Sinking under Application Hints.

**Note 11:** Although power dissipation is internally limited, electrical specifications apply only for power dissipation up to the limits shown. Derating with temperature is a function of both power transistor temperature and control area temperature, which are specified differently. See discussion of Heat Sinking under Application Hints. For $V_{IN} - V_{OUT}$ less than 7V, power dissipation is limited by current limit of 10A.

**Note 12:** Dropout voltage is input-output voltage differential measured at a forced reference voltage of 1.15V, with a 10A load, and is a measurement of the minimum input/output differential at full load.

## Application Hints

Further improvements in efficiency can be obtained by using Schottky diodes or high efficiency diodes with lower forward voltage, combined with larger filter capacitors to reduce ripple. However, this reduces the voltage difference between input and drive pins and may not allow sufficient voltage to fully saturate the pass transistor. Special transformers are available from Signal Transformer that have a 1V tap on the output winding to provide the extra voltage for the drive pin. The transformers are available as standard items for 5V applications at 5A, 10A and 20A. Other voltages are available on special request.

### Heat Sinking

Because of its extremely high power dissipation capability, the *major limitation* in the load driving capability of the LM196 is *heat sinking*. Previous regulators such as LM109, LM340, LM117, etc., had internal power limiting circuitry which limited power dissipation to about 30W. The LM196 is guaranteed to dissipate up to 70W continuously, as long as the maximum junction temperature limit is not exceeded. This requires careful attention to all sources of thermal resistance from junction-to-ambient, including junction-to-case resistance, case-to-heat sink interface resistance (0.1–1.0°C/W), and heat sink resistance itself. A good thermal joint compound such as Wakefield type 120 or Thermalloy Thermocote must be used when mounting the LM196, especially if an electrical insulator is used to isolate the regulator from the heat sink. Interface resistance without this compound will be no better than 0.5°C/W, and probably much worse. With the compound, and no insulator, interface resistance will be 0.2°C/W or less, assuming 0.005″ or less combined flatness run-out of TO-3 and heat sink. Proper torquing of the mounting bolts is important to achieve minimum thermal resistance. Four to six inch pounds is recommended. Keep in mind that good electrical, as well as thermal, contact must be made to the case.

## Application Hints (Continued)

The actual heat sink chosen for the LM196 will be determined by the worst-case continuous full load current, input voltage and maximum ambient temperature. Overload or short circuit output conditions do not normally have to be considered when selecting a heat sink because the thermal shutdown built into the LM196 will protect it under these conditions. An exception to this is in situations where the regulator must recover very quickly from overload. The LM196 may take some time to recover to within specified output tolerance following an extended overload, if the regulator is cooling from thermal shutdown temperature (approximately 175°) to specified operating temperature (125°C or 150°C). The procedure for heat sink selection is as follows:

> Calculate worst-case *continuous* average power dissipation in the regulator from $P = (V_{IN} - V_{OUT}) \times (I_{OUT})$. To do this, you must know the raw power supply voltage/current characteristics fairly accurately. For example, consider a 10V output with 15V nominal input voltage. At full load of 10A, the regulator will dissipate $P = (15 - 10) \times (10) = 50W$. If input voltage rises by 10%, power dissipation will increase to $(16.5 - 10) \times (10) = 65W$, a *30% increase.* It is strongly suggested that a raw supply be assembled and tested to determine its average DC output voltage *under full load with maximum line voltage.* Do not over-design by using unloaded voltage as a worst-case, since the regulator will not be dissipating any power under no load conditions. Worst-case regulator dissipation normally occurs under full load conditions except when the effective DC resistance of the raw supply ($\Delta V/\Delta I$) is larger than $(V_{IN}^* - V_{OUT})/2I_{fL}$, where $V_{IN}^*$ is the lightly-loaded raw supply voltage and $I_{fL}$ is full load current. For $(V_{IN}^* - V_{OUT}) = 5V - 8V$, and $I_{fL} = 5A–10A$, this gives a resistance of 0.25Ω to 0.8Ω. If raw supply resistance is higher than this, the regulator power dissipation may be *less* at full load current, then at some intermediate current, due to the large drop in input voltage. Fortunately, most well designed raw supplies have low enough output resistance that regulator dissipation does maximize at full load current, or very close to it, so tedious testing is not usually required to find worst-case power dissipation.

A very important consideration is the size of the filter capacitor in the raw supply. At these high current levels, capacitor size is usually dictated by ripple current ratings rather than just obtaining a certain ripple voltage. Capacitor ripple current (rms) is 2–3 times the DC output current of the filter. If the capacitor has just 0.05Ω DC resistance, this can cause 30W internal power dissipation at 10A output current. Capacitor life is very senesitive to operating temperature, decreasing by a factor of two for each 15°C rise in internal temperature. Since capacitor life is not all that great to start with, it is obvious that a small capacitor with a large internal temperature rise is inviting very short mean-time-to-failure. A second consideration is the loss of usable input voltage to the regulator. If the capacitor is small, the large dips in the input voltage may cause the LM196 to drop out of regulation. 2000 μF per ampere of load current is the *minimum* recommended value, yielding about 2 Vp-p ripple of 120 Hz. Larger values will have longer life and the reduced ripple will allow lower DC input voltage to the regulator, with subsequent cost savings in the transformer and heat sink. Sometimes several capacitors in parallel are better to decrease series resistance and increase heat dissipating area.

After the raw supply characteristics have been determined, and worst-case power dissipation in the LM196 is known, the heat sink thermal resistance can be found from the graphs titled Maximum Heat Sink Thermal Resistance. These curves indicate the minimim size heat sink required as a function of ambient temperature. They are derived from a case-to-control area thermal resistance of 0.5°C/W and a case-to-power transistor thermal resistance of 1.2°C/W. 0.2°C/W is assumed for interface resistance. A maximum control area temperature of 150°C is used for the LM196 and 125°C for the LM396. Maximum power transistor temperature is 200°C for the LM196 and 175°C for the LM396. For conservative designs, it is suggested that when using these curves, you assume an ambient temperature 25°C–50°C higher than is actually anticipated, to avoid running the regulator right at its design limits of operating temperature. A quick look at the curves show that heat sink resistance ($\theta_{SA}$) will normally fall into the range of 0.2°C/W–1.5°C/W. These are *not* small heat sinks. A model 441, for instance, which is sold by several manufacturers, has a $\theta_{SA}$ of 0.6°C/W with natural convection and is about five inches on a side. Smaller sinks are more volumetrically efficient, and larger sinks, less so. A rough formula for estimating the volume of heat sink required is: $V = 50/\theta_{SA}^{1.5}$ CU. IN. This holds for natural convection only. If the heat sink is inside a small sealed enclosure, $\theta_{SA}$ will increase substantially because the air is not free to form natural convection currents. Fan-forced convection can reduce $\theta_{SA}$ by a factor of two at 200 FPM air velocity, and by four at 1000 FPM.

### Ripple Rejection

Ripple rejection at the normal ripple frequency of 120 Hz is a function of both electrical and thermal effects in the LM196. If the adjustment pin is not bypassed with a capacitor, it is also dependent on output voltage. A 25 μF capacitor from the adjustment pin to ground will make ripple rejection independent of output voltage for frequencies above 100 Hz. If lower ripple frequencies are encountered, the capacitor should be increased proportionally.

To keep in mind that the bypass capacitor on the adjustment pin will limit the turn-on time of the regulator. A 25 μF capacitor, combined with the output divider resistance, will give an extended output voltage settling time following the application of input power.

### Load Regulation (LM196/LM396)

Because the LM196 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the output pin and the wire connecting the regulator to the load. For the data sheet specification, regulation is measured 1/4″ from the bottom of the package on the output pin. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load.

## Application Hints (Continued)

Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the output pin, *not to the load*. This is illustrated in *Figure 2*. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$(\text{Rw}) \times \left(\frac{R2 + R1}{R1}\right)$$

Rw = Line Resistance

Connected as shown, Rw is not multiplied by the divider ratio. Rw is about 0.004Ω per foot using 16 gauge wire. This translates to 40 mV/ft at 10A load current, so it is important to keep the positive lead between regulator and load as short as possible.

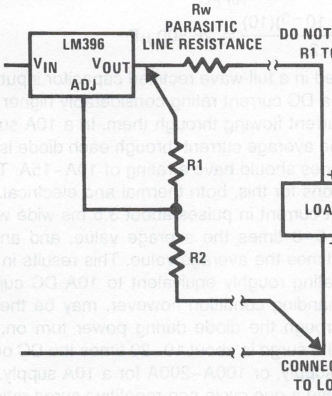


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**FIGURE 2. Proper Divider Connection**

The input resistance of the sense pin is typically 6 kΩ, modeled as a resistor between the sense pin and the output pin. Load regulation will start to degrade if a resistance higher than 10Ω is inserted in series with the sense. This assumes a worst-case condition of 0.5V between output and sense pins. Lower differential voltage will allow higher sense series resistance.

### Thermal Load Regulation

Thermal, as well as electrical, load regulation must be considered with IC regulators. Electrical load regulation occurs in microseconds, thermal regulation due to die thermal gradients occurs in the 0.2 ms-20 ms time frame, and regulation due to overall temperature changes in the die occurs over a 20 ms to 20 minute period, depending on the time constant of the heat sink used. Gradient induced load regulation is calculated from

$$\Delta V_{OUT} = (V_{IN}\ V_{OUT}) \times (\Delta I_{OUT}) \times (\beta)$$

$\beta$ = Thermal regulation specified on data sheet.

For $V_{IN}$ = 9V, $V_{OUT}$ = 5V, $\Delta I_{OUT}$ = 10A, and $\beta$ = 0.005%/W, this yields a 0.2% change in output voltage. Changes in output voltage due to overall temperature rise are calculated from

$$V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (TC) \times (\theta_{jA})$$

TC = Temperature coefficient of output voltage.

$\theta_{jA}$ = Thermal resistance from junction to ambient. $\theta_{jA}$ is approximately 0.5°C/W + $\theta$ of heat sink.

For the same conditions as before, with TC = 0.003%/°C, and $\theta_{jA}$ = 1.5°C/W, the change in output voltage will be 0.18%. Because these two thermal terms can have either polarity, they may subtract from, or add to, electrical load regulation. For worst-case analysis, they must be assumed to add. If the output of the regulator is trimmed under load, only that portion of the load that changes need be used in the previous calculations, significantly improving output accuracy.

### Line Regulation

Electrical line regulation is very good on the LM196—typically less than 0.005% change in output voltage for a 1V change in input. This level of regulation is achieved only for very low load currents, however, because of thermal effects. Even with a thermal regulation of 0.002%.W, and a temperature coefficient of 0.003%/°C, DC line regulation will be dominated by thermal effects as shown by the following example:

Assume $V_{OUT}$ = 5V, $V_{IN}$ = 9V, $I_{OUT}$ = 8A

Following a 10% change in input voltage (0.9), the output will change quickly (≤100 μs), due to electrical effects, by (0.005%V) × (0.9V) = 0.0045%. In the next 20 ms, the output will change an additional (0.002%/W) × (8A) × (0.9V) = 0.0144% due to thermal gradients across the die. After a much longer time, determined by the time constant of the heat sink, the output will change an additional (0.003%/°C) × (8A) × (0.9V) × (2°C/W) = 0.043% due to the temperature coefficient of output voltage and the thermal resistance from die to ambient. (2°C/W was chosen for this calculation). The sign of these last two terms varies from part to part, so no assumptions can be made about any cancelling effects. All three terms must be added for a proper analysis. This yields 0.0045 + 0.0144 + 0.043 = 0.062% using *typical* values for thermal regulation and temperature coefficient. For worst-case analysis, the maximum data sheet specifications for thermal regulation and temperature coefficient should be used, along with the *actual* thermal resistance of the heat sink being used.

### Paralleling Regulators

Direct paralleling of regulators is not normally recommended because they do not share currents equally. The regulator with the highest reference voltage will supply all the current to the load until it current limits. With an 18A load, for instance, one regulator might be operating in current limit at 16A while the second device is only carrying 2A. Power dissipation in the high current regulator is extremely high with attendant high junction temperatures. Long term reliability cannot be guaranteed under these conditions.

Quasi-paralleling may be accomplished if load regulation is not critical. The connection shown in *Figure 5a* will typically share to within 1A, with a worst-case of about 3A. Load regulation is degraded by 150 mV at 20A loads. An external op amp may be used as in *Figure 5b* to improve load regulation and provide remote sensing.

## Application Hints (Continued)

### Input and Output Capacitors

The LM196 will tolerate a wide range of input and output capacitance, but long wire runs or small values of output capacitance can sometimes cause problems. If an output capacitor is used, it should be 1 $\mu$F or larger. We suggest 10 $\mu$F solid tantalum if significant improvements in high frequency output impedance are needed (see output impedance graph). This capacitor should be as close to the regulator as possible, with short leads, to reduce the effects of lead inductance. No input capacitor is needed if the regulator is within 6 inches of the power supply filter capacitor, using 18 gauge stranded wire. For longer wire runs, the LM196 input should be bypassed locally with a 4.7 $\mu$F (or larger) solid tantalum capacitor, or a 100 $\mu$F (or larger) aluminum electrolytic capacitor.

### Correcting for Output Wire Losses (LM196/LM396)

Three-terminal regulators can only provide partial Kelvin load sensing (see Load Regulation). Full remote sensing can be added by using an external op amp to cancel the effect of voltage drops in the unsensed positive output lead. In *Figure 7*, the LM301A op amp forces the voltage loss across the unsensed output lead to appear across R3. The current through R3 then flows out the $V^-$ pin of the op amp through R4. The voltage drop across R4 will raise the output voltage by an amount equal to the line loss, just cancelling the line loss itself. A small ($\cong$ 40 mV) initial output voltage error is created by the quiescent current of the op amp. Cancellation range is limited by the maximum output current of the op amp, about 300 mV as shown. This can be raised by increasing R3 or R4 at the expense of more initial output error.

### Transformers and Diodes

Proper transformer ratings are very important in a high current supply because of the conflicting requirements of efficiency and tolerance to low-line conditions. A transformer with a high secondary voltage will waste power and cause unnecessary heating in the regulator. Too low a secondary voltage will cause loss of regulation under low-line conditions. The following formulas may be used to calculate the required secondary voltage and current ratings using a full-wave center tap:

$$V_{rms} = \left(\frac{V_{OUT} + V_{REG} + V_{RECT} + V_{RIPPLE}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right)(1.1)^*$$

$$I_{rms} = (I_{OUT})\,(1.2) \qquad \text{(Full-wave center tap)}$$

where:

$V_{OUT}$ = DC regulated output voltage

$V_{REG}$ = Minimum input-output voltage of regulator

$V_{RECT}$ = Rectifier forward voltage drop at three times DC output current

$V_{RIPPLE}$ = 1/2 peak-to-peak capacitor ripple voltage $= \dfrac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$

$V_{NOM}$ = Nominal line voltage AC rms

$V_{LOW}$ = Low line voltage AC rms

$I_{OUT}$ = DC output current

Example: $I_{OUT} = 10A$, $V_{OUT} = 5V$

Assume: $V_{REG} = 2.2V$, $V_{RECT} = 1.2V$
$V_{RIPPLE} = 2$ Vp-p, $V_{NOM} = 115V$,
$V_{LOW} = 105V$

$$V_{rms} = \left(\frac{5 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{115}{105}\right)1.1$$

$$= 8.01\ V_{rms}$$

$$\text{Capacitor C} = \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2 \times V_{RIPPLE}}$$

$$= \frac{(5.3 \times 10^{-3})(10)}{2} = 26{,}500\ \mu F$$

The diodes used in a full-wave rectified capacitor input supply must have a DC current rating considerably higher than the average current flowing through them. In a 10A supply, for instance, the average current through each diode is only 5A, but the diodes should have a rating of 10A–15A. There are many reasons for this, both thermal and electrical. The diodes conduct current in pulses about 3.5 ms wide with a peak value of 5–8 times the average value, and an rms value 1.5–2.0 times the average value. This results in long term diode heating roughly equivalent to 10A DC current. The most demanding condition however, may be the one cycle surge through the diode during power turn on. The peak value of the surge is about 10–20 times the DC output current of the supply, or 100A–200A for a 10A supply. The diodes must have a one cycle non-repetitive surge rating of 200A or more, and this is usually not found in a diode with less than 10A average current rating. Keep in mind that even though the LM196 may be used at current levels below 10A, the diodes may still have to survive shorted output conditions where average current could rise to 12A–15A. Smaller transformers and filter capacitors used in lower current supplies will reduce surge currents, but unless specific information is available on worst-case surges, it is best not to economize on diodes. Stud-mounted devices in a DO-4 package are recommended. Cathode-to-case types may be bolted directly to the same heat sink as the LM196 because the case of the regulator is its power input. Part numbers to consider are the 1N1200 series rated at 12A average current in a DO-4 stud package. Additional types include common cathode duals in a TO-3 package, both standard and Schottky, and various duals in plastic filled assemblies. Schottky diodes will improve efficiency, especially in low voltage applications. In a 5V supply for instance, Schottky diodes will decrease wasted power by up to 6W, or alternatively provide an additional 5% "drop out" margin for low-line conditions. Several manufacturers are producing "high efficiency" diodes with a forward voltage drop nearly as good as Schottkys at high current levels. These devices do not have the low breakdown voltages of Schottkys, so are much less prone to reverse breakdown induced failures.

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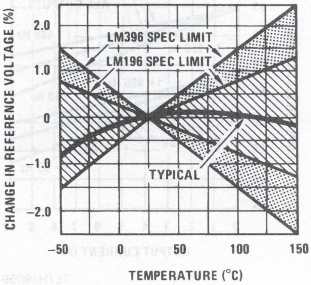
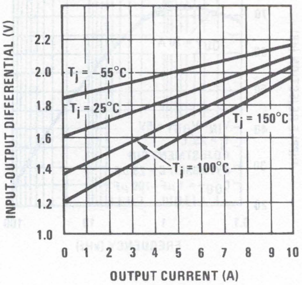
*The factor of 1.1 is only an approximate factor accounting for load regulation of the transformer.

## Typical Performance Characteristics

### Reference Drift

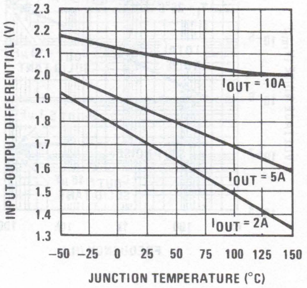


### Minimum Input-Output Differential*



*$V_{IN}$ is reduced until output drops 2%

### Minimum Input-Output Differential*



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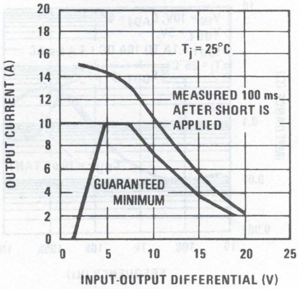
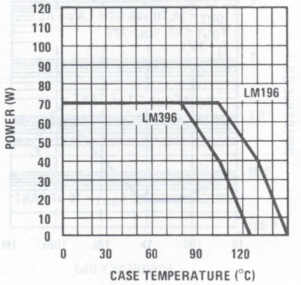
*$V_{IN}$ is reduced until output drops 2%

### Current Limit

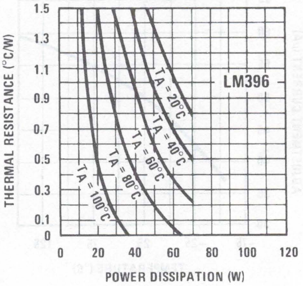


### Maximum Power Dissipation*



*As limited by maximum junction temperature.

### Maximum Heat Sink Thermal Resistance*



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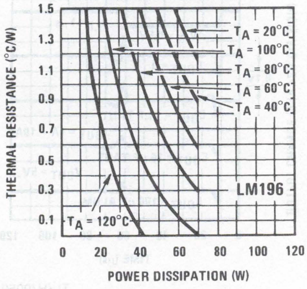
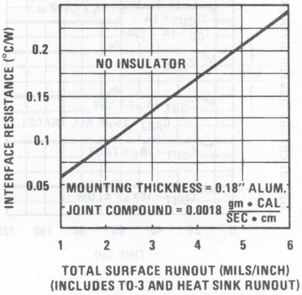
*See "Heat Sinking" under Applications Hints.

### Maximum Heat Sink Thermal Resistance*

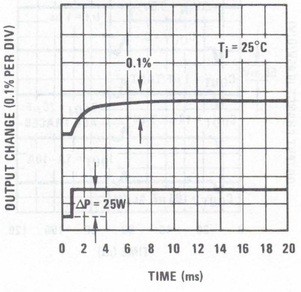


*See "Heat Sinking" under Application Hints.

### TO-3 Interface Thermal Resistance Using Thermal Joint Compound



### Thermal Regulation



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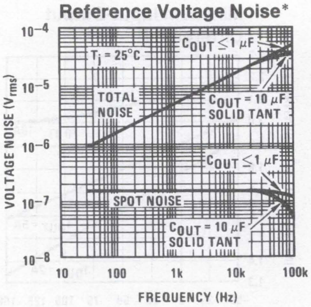
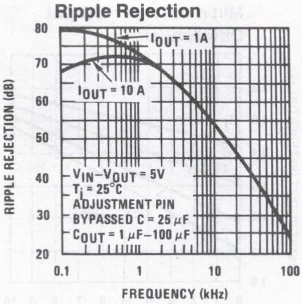
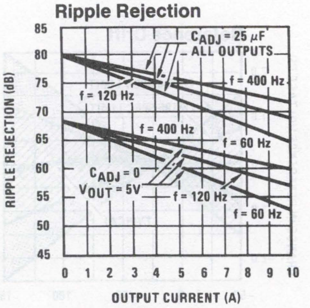
## Typical Performance Characteristics (Continued)


**Reference Voltage Noise***

*To obtain output noise, multiply by $V_{OUT}/1.25$ if adjustment pinis not bypassed.


**Ripple Rejection**


**Ripple Rejection**

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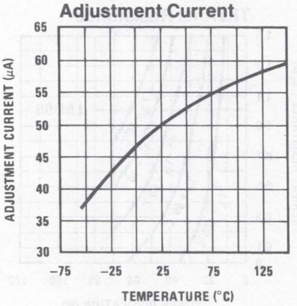
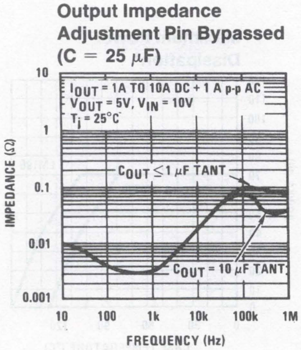
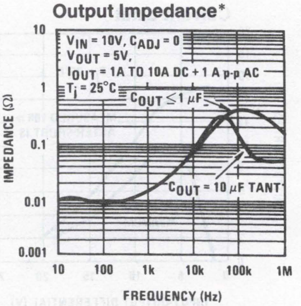

**Adjustment Current**


**Output Impedance Adjustment Pin Bypassed (C = 25 μF)**


**Output Impedance***

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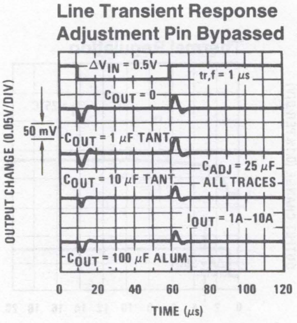
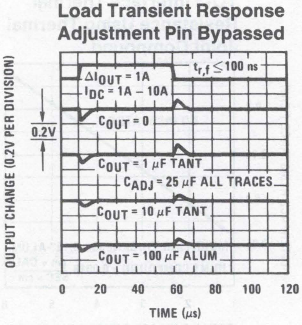
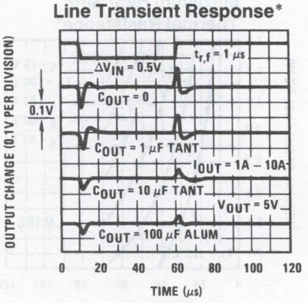
*For output voltages other than 5V, multiply vertical scale readings by $V_{OUT}/5$.


**Line Transient Response Adjustment Pin Bypassed**


**Load Transient Response Adjustment Pin Bypassed**

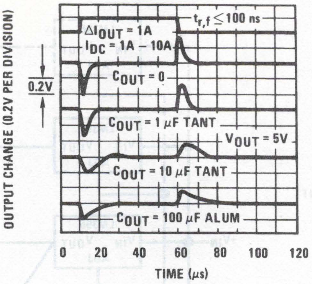

**Line Transient Response***

TL/H/9059-8

*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

## Typical Performance Characteristics (Continued)

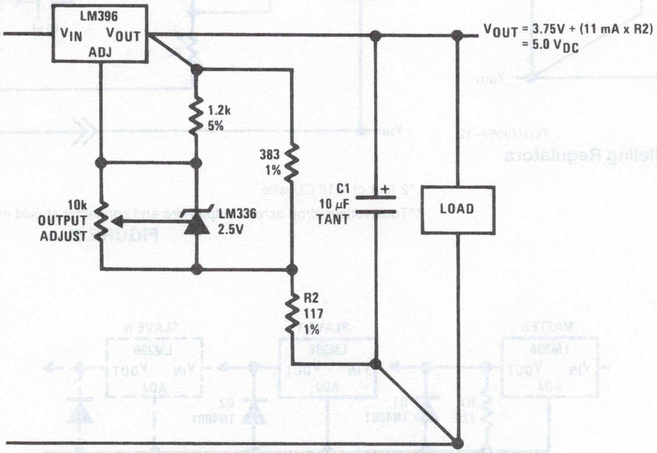
**Load Transient Response***



TL/H/9059–9

*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

## Typical Applications (Continued)



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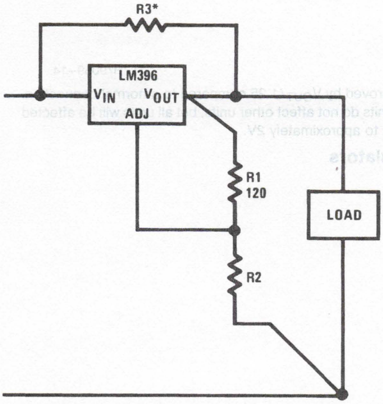
*Regulation can be improved by adding an LM336 reference diode to increase the effective reference voltage to 3.75V. Load and line regulation are improved by 3:1, including thermal effects.

**FIGURE 3. Improving Regulation***



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*R3 is selected to supply partial load current. Therefore, a minimum load must always be maintained to prevent the regulated output from rising uncontrolled. R3 must be greater than $(V_{MAX} - V_{OUT})/I_{MIN}$, where $V_{MAX}$ is worst-case high input voltage, and $I_{MIN}$ is the minimum load current. R3 must be rated for at least $(V_{IN} - V_{OUT})^2/R3$ watts. Regulator power dissipation will be reduced by a factor of 2–3 in a typical situation where minimum load current is 1/2 full load current. Regulator dissipation will peak at:

$$V_{IN} = \frac{(R3)(I_{OUT})}{2} + V_{OUT}$$

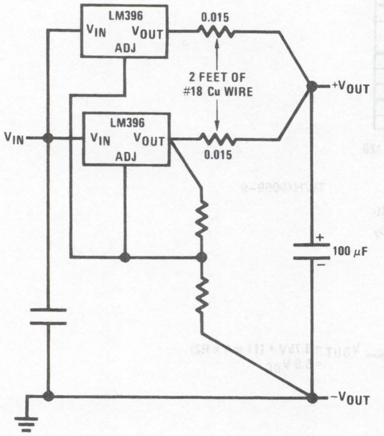
and will be equal to:

$$P_{MAX} = \frac{(R3)(I_{OUT})^2}{4} \text{ Assuming: } (R3)(I_{OUT}) \le V_{MAX} - V_{OUT}$$

A few words of caution; (1) R3 power rating must be increased to $(V_{MAX})^2/R3$ if continuous output shorts are possible. (2) Under normal load conditions, system power dissipation is not changed, but under short circuit conditions *system* power dissipation increases by $(V_{IN})^2/R3$ watts over the already high power of a shorted regulator. The LM196 will not be harmed and neither will R3 if it is rated properly, but the raw supply components must be able to withstand the overload also. Thermal shutdown of the LM196 will probably occur for sustained shorts, somewhat alleviating the problem.

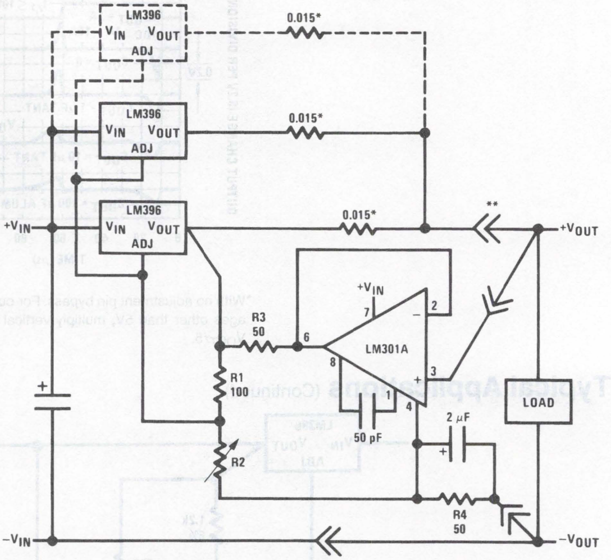
**FIGURE 4. Reducing Regulator Power Dissipation**

## Typical Applications (Continued)


LM396
VIN VOUT
ADJ
0.015
2 FEET OF
#18 Cu WIRE
+VOUT
LM396
VIN VOUT
ADJ
0.015
VIN
+
100 µF
−
−VOUT

TL/H/9059–12

**FIGURE 5a. Paralleling Regulators**

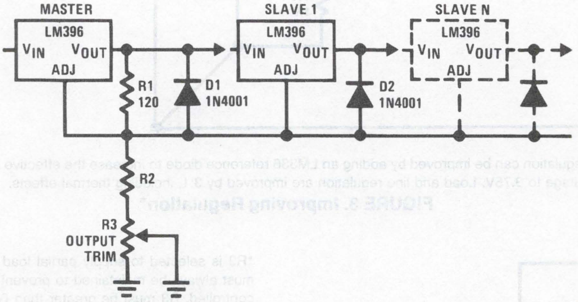

LM396
VIN VOUT
ADJ
0.015*
LM396
VIN VOUT
ADJ
0.015*
LM396
VIN VOUT
ADJ
+VIN
0.015*
**
+VOUT
+VIN
7
2
R3
50
6
LM301A
8
3
R1
100
1
4
50 pF
2 µF
+
LOAD
R2
R4
50
−VIN
−VOUT

TL/H/9059–13

*2 feet of #18 CU wire

**Total voltage drop across output wire and connector should not exceed 0.3V

**FIGURE 5b**

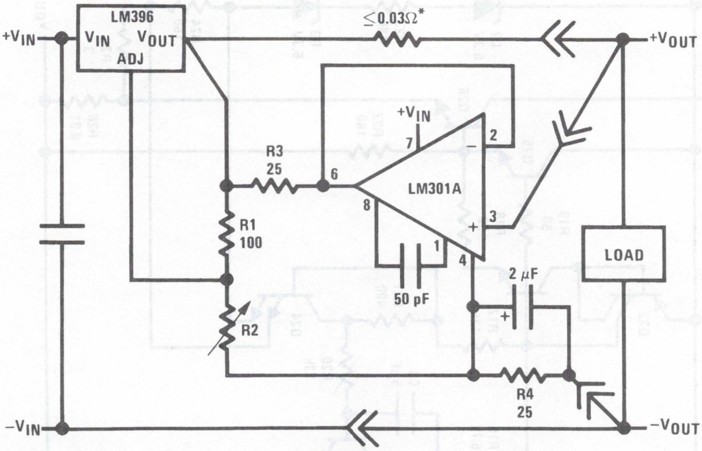

MASTER
LM396
VIN VOUT
ADJ
SLAVE 1
LM396
VIN VOUT
ADJ
SLAVE N
LM396
VIN VOUT
ADJ
R1
120
D1
1N4001
D2
1N4001
R2
R3
OUTPUT
TRIM

TL/H/9059–14

Output will be within ±20 mV at 25°C, no load. Regulation of tracking units is improved by $V_{OUT}/1.25$ compared to a normal connection. Regulation of master unit is unchanged. Load or input voltage changes on slave units do not affect other units, but all units will be affected by changes on master. A short on any output will cause all other outputs to drop to approximately 2V.

**FIGURE 6. Tracking Regulators**

## Typical Applications (Continued)

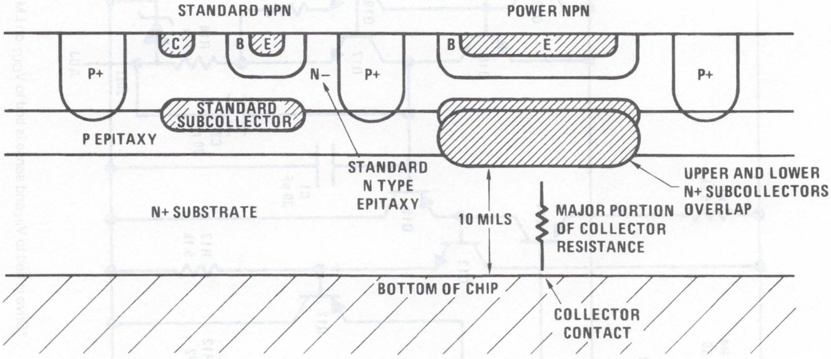


LM396
VIN
VOUT
ADJ
+VIN
−VIN
≤0.03Ω*
+VOUT
−VOUT
+VIN
7
2
R3
25
6
LM301A
8
3
R1
100
1
4
50 pF
2 µF
+
R2
R4
25
LOAD

TL/H/9059–15

*Parasatic line resistance created by wiring connectors, or parallel ballasting.

**FIGURE 7. Correcting for Line Losses**



STANDARD NPN
POWER NPN
C
B
E
B
E
P+
N−
P+
P+
STANDARD SUBCOLLECTOR
P EPITAXY
STANDARD N TYPE EPITAXY
UPPER AND LOWER N+ SUBCOLLECTORS OVERLAP
N+ SUBSTRATE
10 MILS
MAJOR PORTION OF COLLECTOR RESISTANCE
BOTTOM OF CHIP
COLLECTOR CONTACT

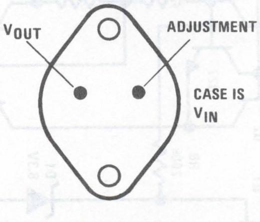
TL/H/9059–16

Power NPS have low collecter resistance, and do not require collector bond wires. Collectors are all common to substrate. Standard NPNs are still isolated.

**FIGURE 8. Process Technology**

## Connection Diagram

**Metal Can Package**



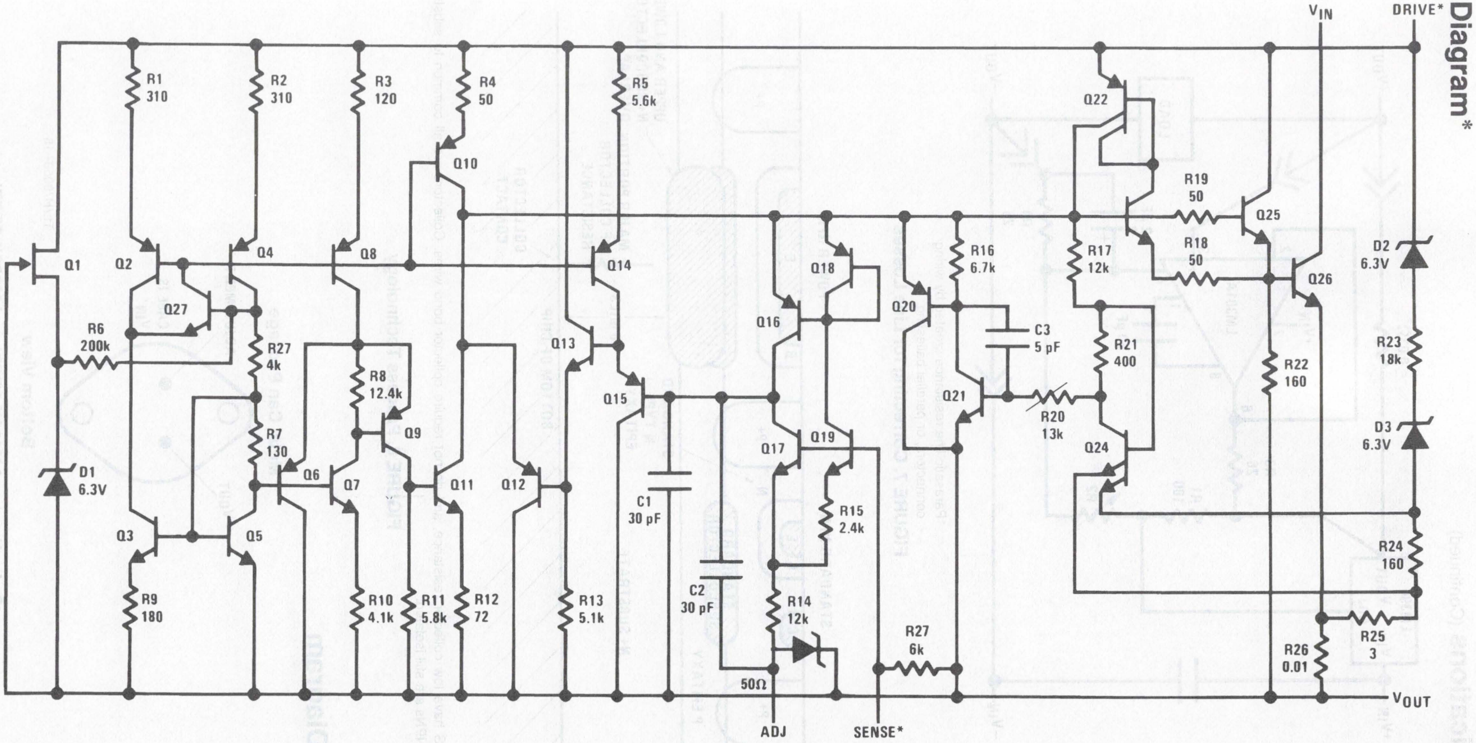
VOUT
ADJUSTMENT
CASE IS VIN

TL/H/9059–18

**Bottom View**

**Order Number LM196K STEEL or LM396K STEEL**
**See NS Package Number K02B**

## Schematic Diagram*


V_IN
DRIVE*
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q24
Q25
Q26
Q27
R1 310
R2 310
R3 120
R4 50
R5 5.6k
R6 200k
R7 130
R8 12.4k
R9 180
R10 4.1k
R11 5.8k
R12 72
R13 5.1k
R14 12k
R15 2.4k
R16 6.7k
R17 12k
R18 50
R19 50
R20 13k
R21 400
R22 160
R23 18k
R24 160
R25 3
R26 0.01
R27 4k
R27 6k
C1 30 pF
C2 30 pF
C3 5 pF
D1 6.3V
D2 6.3V
D3 6.3V
50Ω
ADJ
SENSE*
V_OUT

TL/H/9059–17

*Drive is tied to $V_{IN}$ and sense is tied to $V_{OUT}$ on LM196 and LM396.

**National Semiconductor Corporation**

# LM317L 3-Terminal Adjustable Regulator

## General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is available packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

## Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

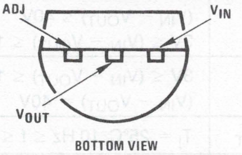
Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

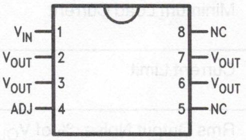
The LM317L is available in a standard TO-92 transistor package and the SO-8 package. The LM317L is rated for operation over a −25°C to 125°C range.

## Connection Diagram



TL/H/9064-4

**Order Number LM317LZ**
**See NS Package**
**Number Z03A**

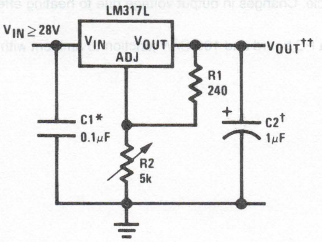


TL/H/9064-5

**Order Number LM317LM**
**See NS Package**
**Number M08A**

## Typical Applications

### 1.2V–25V Adjustable Regulator



TL/H/9064-1

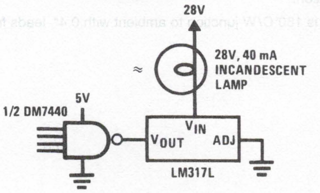
Full output current not available at high input-output voltages

†Optional—improves transient response

*Needed if device is more than 6 inches from filter capacitors

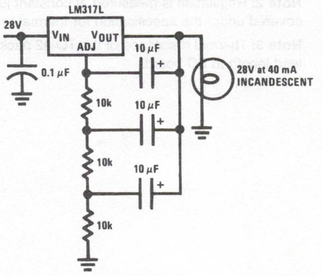
$$††V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

### Fully Protected (Bulletproof) Lamp Driver



TL/H/9064-2

### Lamp Flasher



TL/H/9064-3

Output rate—4 flashes per second at 10% duty cycle

1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input-Output Voltage Differential | 40V |
| Operating Junction Temperature Range | −40°C to +125°C |
| Storage Temperature | −55°C to +150°C |
| Lead Temperature (Soldering, 4 seconds) | 260°C |

Output is Short Circuit Protected

ESD rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Line Regulation | $T_j = 25°C$, $3V \leq (V_{IN} - V_{OUT}) \leq 40V$, $I_L \leq 20$ mA (Note 2) | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_j = 25°C$, $5 \text{ mA} \leq I_{OUT} \leq I_{MAX}$, (Note 2) | | 0.1 | 0.5 | % |
| Thermal Regulation | $T_j = 25°C$, 10 ms Pulse | | 0.04 | 0.2 | %/W |
| Adjustment Pin Current | | | 50 | 100 | μA |
| Adjustment Pin Current Change | $5 \text{ mA} \leq I_L \leq 100$ mA<br>$3V \leq (V_{IN} - V_{OUT}) \leq 40V$, $P \leq 625$ mW | | 0.2 | 5 | μA |
| Reference Voltage | $3V \leq (V_{IN} - V_{OUT}) \leq 40V$, (Note 3)<br>$5 \text{ mA} \leq I_{OUT} \leq 100$ mA, $P \leq 625$ mW | 1.20 | 1.25 | 1.30 | V |
| Line Regulation | $3V \leq (V_{IN} - V_{OUT}) \leq 40V$, $I_L \leq 20$ mA (Note 2) | | 0.02 | 0.07 | %/V |
| Load Regulation | $5 \text{ mA} \leq I_{OUT} \leq 100$ mA, (Note 2) | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \leq T_j \leq T_{Max}$ | | 0.65 | | % |
| Minimum Load Current | $(V_{IN} - V_{OUT}) \leq 40V$<br>$3V \leq (V_{IN} - V_{OUT}) \leq 15V$ | | 3.5<br>1.5 | 5<br>2.5 | mA |
| Current Limit | $3V \leq (V_{IN} - V_{OUT}) \leq 13V$<br>$(V_{IN} - V_{OUT}) = 40V$ | 100<br>25 | 200<br>50 | 300<br>150 | mA<br>mA |
| Rms Output Noise, % of $V_{OUT}$ | $T_j = 25°C$, $10 \text{ Hz} \leq f \leq 10$ kHz | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = 10V$, $f = 120$ Hz, $C_{ADJ} = 0$<br>$C_{ADJ} = 10$ μF | <br>66 | 65<br>80 | | dB<br>dB |
| Long-Term Stability | $T_j = 125°C$, 1000 Hours | | 0.3 | 1 | % |
| Thermal Resistance Junction to Ambient | Z Package 0.4″ Leads<br>Z Package 0.125 Leads<br>SO-8 Package | | 180<br>160<br>165 | | °C/W<br>°C/W<br>°C/W |
| Thermal Rating of SO Package | | | 165 | | °C/W |

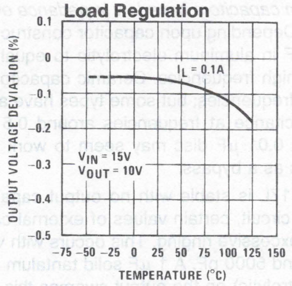
**Note 1:** Unless otherwise noted, these specifications apply: $-25°C \leq T_j \leq 125°C$ for the LM317L; $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 40$ mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. $I_{MAX}$ is 100 mA.

**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

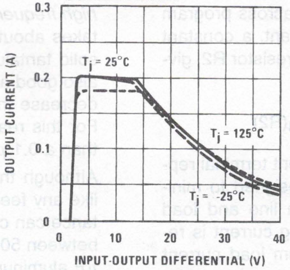
**Note 3:** Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to PC board.

# Typical Performance Characteristics (Output capacitor = 0 μF unless otherwise noted.)

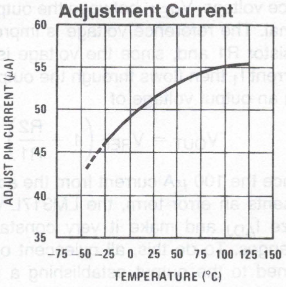
### Load Regulation



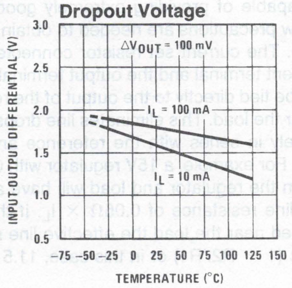
### Current Limit



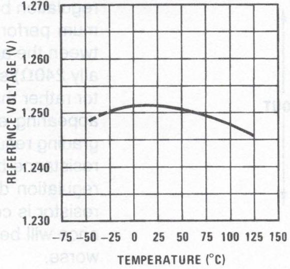
### Adjustment Current



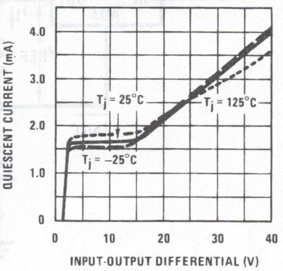
### Dropout Voltage



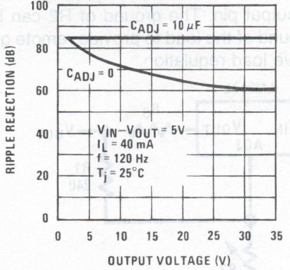
### Reference Voltage Temperature Stability



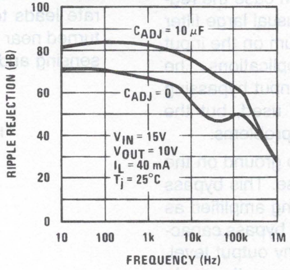
### Minimum Operating Current



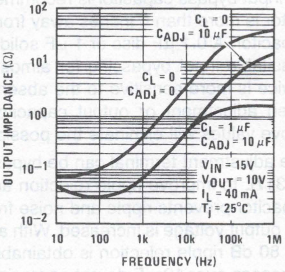
### Ripple Rejection



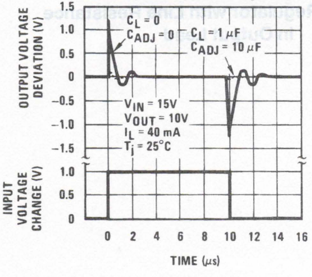
### Ripple Rejection



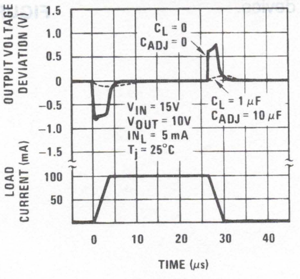
### Output Impedance



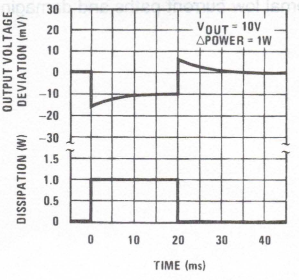
### Line Transient Response



### Load Transient Response



### Thermal Regulation



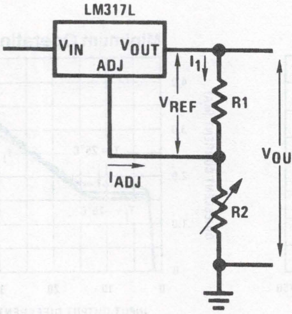
TL/H/9064-6

## Application Hints

In operation, the LM317L develops a nominal 1.25V reference voltage, $V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R2)$$

Since the 100 μA current from the adjustment terminal represents an error term, the LM317L was designed to minimize $I_{ADJ}$ and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.



TL/H/9064-7

**FIGURE 1**

### External Capacitors

An input bypass capacitor is recommended in case the regulator is more than 6 inches away from the usual large filter capacitor. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM317L to improve ripple rejection and noise. This bypass capacitor prevents ripple and noise from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. *Solid tantalum capacitors have low impedance even at high frequencies.* Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, a 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

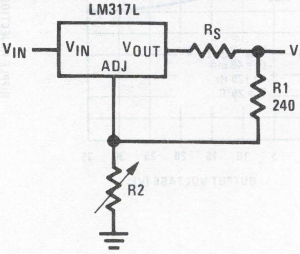
Although the LM317L is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

### Load Regulation

The LM317L is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × $I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

*Figure 2* shows the effect of resistance between the regulator and 240Ω set resistor.

With the TO-92 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the output pin. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.



TL/H/9064-8

**FIGURE 2. Regulator with Line Resistance in Output Lead**

## Application Hints (Continued)

### Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of $V_{OUT}$, per watt, within the first 10 ms after a step of power is applied. The LM317L specification is 0.2%/W, maximum.

In the Thermal Regulation curve at the bottom of the Typical Performance Characteristics page, a typical LM317L's output changes only 7 mV (or 0.07% of $V_{OUT} = -10V$) when a 1W pulse is applied for 10 ms. This performance is thus well inside the specification limit of $0.2\%/W \times 1W = 0.2\%$ maximum. When the 1W pulse is ended, the thermal regulation again shows a 7 mV change as the gradients across the LM317L chip die out. Note that the load regulation error of about 14 mV (0.14%) is additional to the thermal regulation error.

### Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 µF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{IN}$. In the LM317L, this discharge path is through a large junction that is able to sustain a 2A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 µF or less, the LM317L's ballast resistors and output structure limit the peak current to a low enough level so that there is no need to use a protection diode.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM317L is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 µF capacitance. *Figure 3* shows an LM317L with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

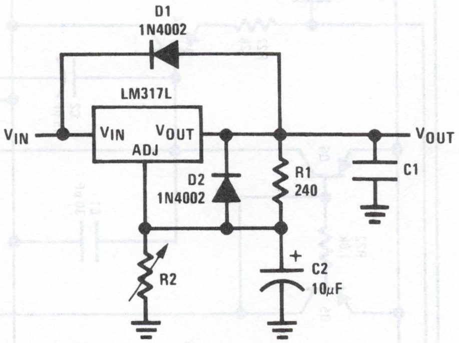


FIGURE 3. Regulator with Protection Diodes

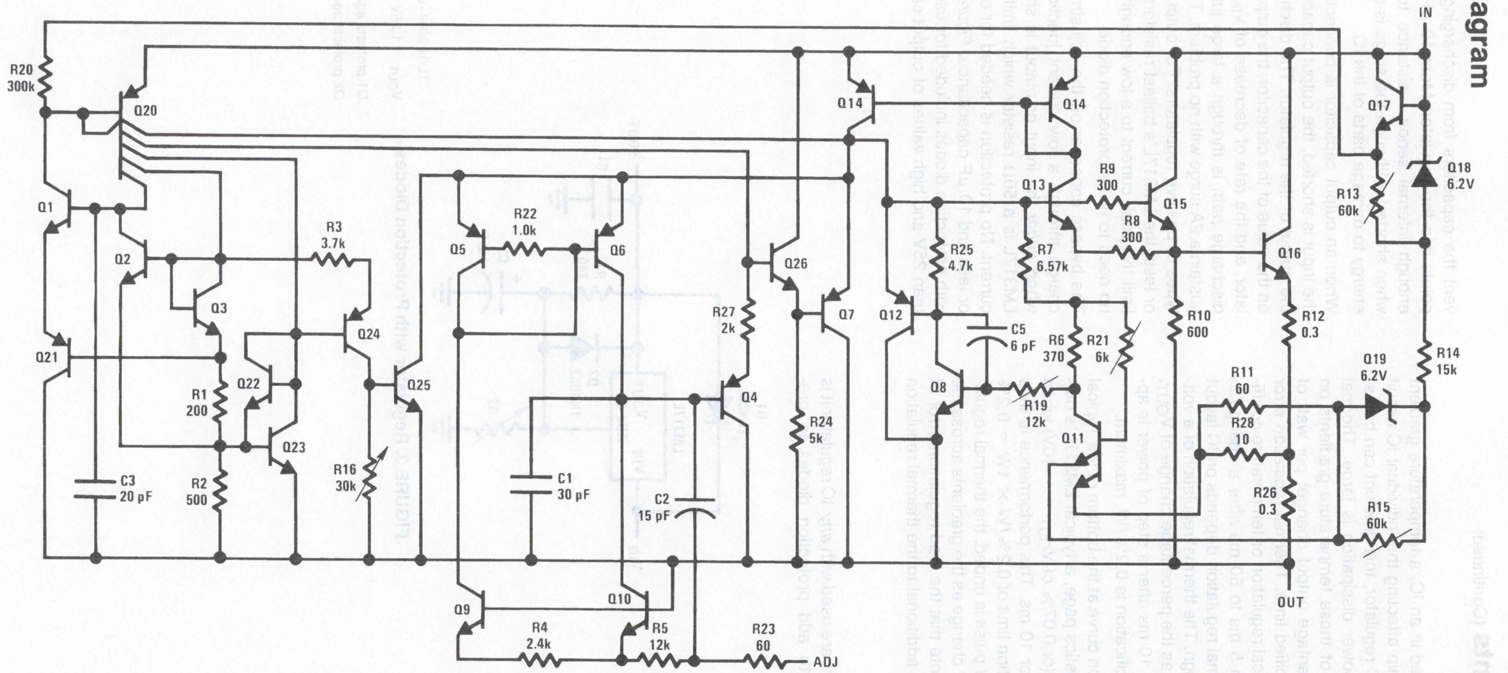
TL/H/9064–9

$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) I_{ADJ} R2$

D1 protects against C1

D2 protects against C2

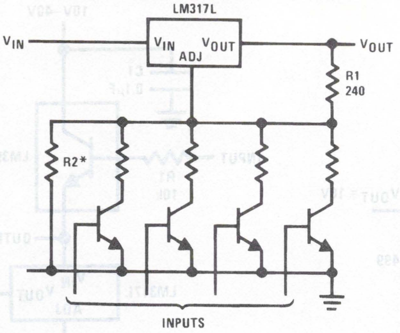
## Schematic Diagram


IN
Q17
Q18 6.2V
R13 60k
Q14
Q14
Q13
R9 300
Q15
R8 300
Q16
R10 600
R12 0.3
R14 15k
Q19 6.2V
R11 60
R28 10
R26 0.3
R15 60k
OUT
R25 4.7k
R7 6.57k
Q12
C5 6 pF
R6 370
R21 6k
Q8
R19 12k
Q11
Q7
Q26
R27 2k
Q4
R24 5k
C2 15 pF
Q5
R22 1.0k
Q6
C1 30 pF
Q9
R4 2.4k
Q10
R5 12k
R23 60
ADJ
R20 300k
Q20
Q1
Q2
Q3
R3 3.7k
Q24
Q21
Q22
R1 200
Q23
R2 500
C3 20 pF
Q25
R16 30k

TL/H/9064–10

## Typical Applications (Continued)

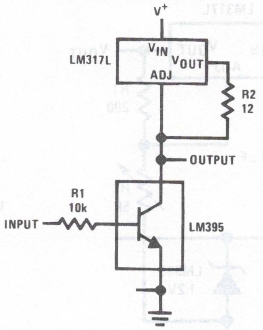
### Digitally Selected Outputs


LM317L
VIN
VIN
VOUT
ADJ
VOUT
R1
240
R2*
INPUTS

TL/H/9064–11

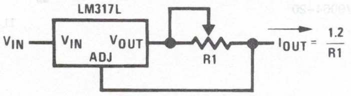
*Sets maximum $V_{OUT}$

### High Gain Amplifier


V+
LM317L
VIN
VOUT
ADJ
R2
12
OUTPUT
R1
10k
INPUT
LM395

TL/H/9064–12

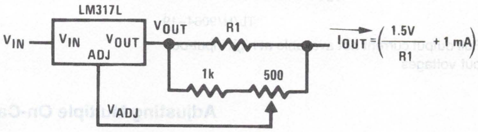
### Adjustable Current Limiter


LM317L
VIN
VIN
VOUT
ADJ
R1
IOUT = 1.2/R1

TL/H/9064–13

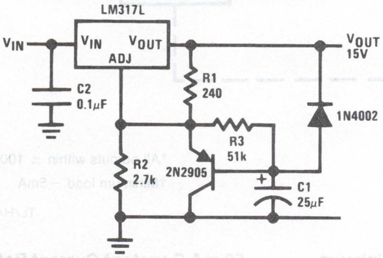
12 ≤ R1 ≤ 240

### Precision Current Limiter


LM317L
VIN
VIN
VOUT
ADJ
VOUT
R1
IOUT = (1.5V/R1 + 1 mA)
1k
500
VADJ

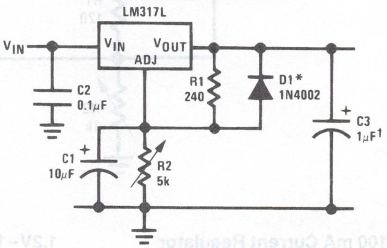
TL/H/9064–14

### Slow Turn-On 15V Regulator


LM317L
VIN
VIN
VOUT
ADJ
VOUT
15V
C2
0.1μF
R1
240
1N4002
R3
51k
R2
2.7k
2N2905
C1
25μF

TL/H/9064–15

### Adjustable Regulator with Improved Ripple Rejection

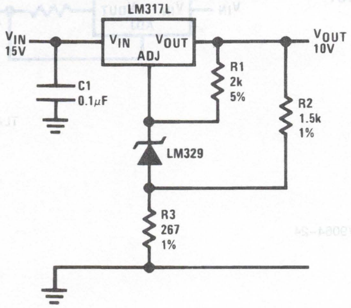

LM317L
VIN
VIN
VOUT
ADJ
R1
240
D1*
1N4002
C3
1μF†
C2
0.1μF
C1
10μF
R2
5k

TL/H/9064–16

†Solid tantalum

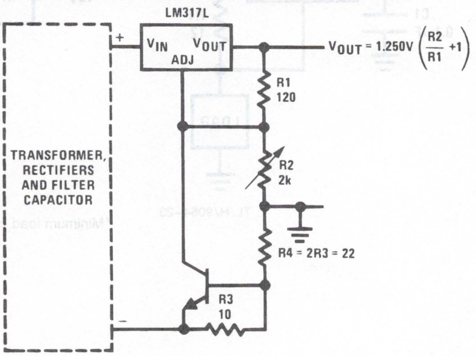
*Discharges C1 if output is shorted to ground

### High Stability 10V Regulator


LM317L
VIN
15V
VIN
VOUT
ADJ
VOUT
10V
C1
0.1μF
R1
2k
5%
R2
1.5k
1%
LM329
R3
267
1%

TL/H/9064–17

### Adjustable Regulator with Current Limiter


LM317L
+
VIN
VOUT
ADJ
VOUT = 1.250V (R2/R1 + 1)
R1
120
R2
2k
TRANSFORMER, RECTIFIERS AND FILTER CAPACITOR
R4 = 2R3 = 22
R3
10
−

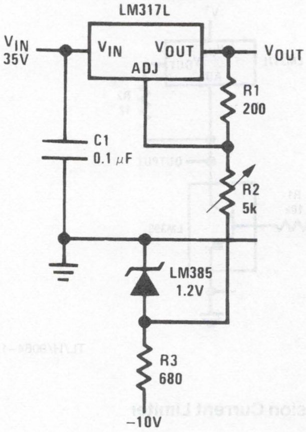
TL/H/9064–18

Short circuit current is approximately 600 mV/R3, or 60 mA (compared to LM317LZ's 200 mA current limit).

At 25 mA output only 3/4V of drop occurs in R3 and R4.

## Typical Applications (Continued)

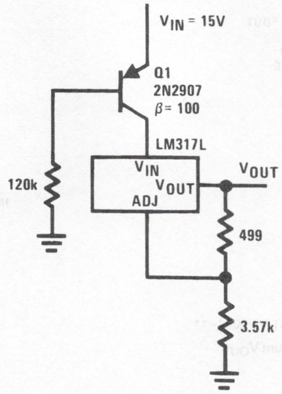
### 0V–30V Regulator


LM317L
VIN 35V
VIN
VOUT
ADJ
VOUT
R1 200
C1 0.1 μF
R2 5k
LM385 1.2V
R3 680
−10V

TL/H/9064–19

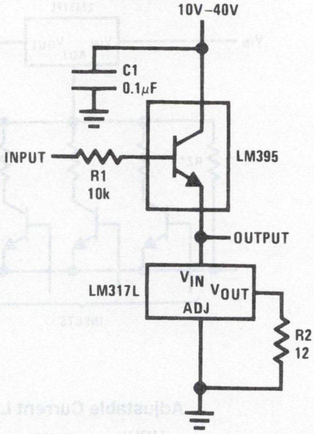
Full output current not available at high input-output voltages

### Regulator With 15 mA Short Circuit Current


VIN = 15V
Q1 2N2907 β = 100
LM317L
120k
VIN
VOUT
ADJ
VOUT = 10V
499
3.57k

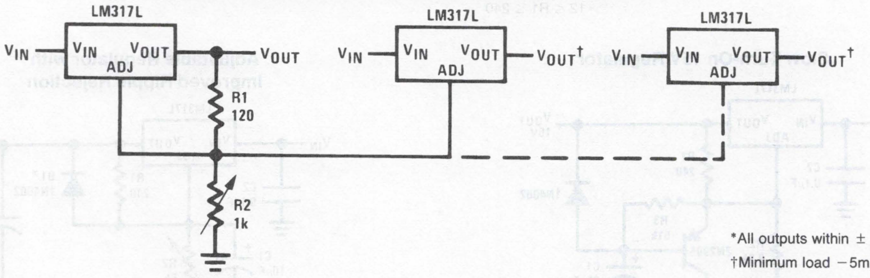
TL/H/9064–20

### Power Follower


10V–40V
C1 0.1μF
INPUT
R1 10k
LM395
OUTPUT
LM317L
VIN
VOUT
ADJ
R2 12

TL/H/9064–21

### Adjusting Multiple On-Card Regulators with Single Control*

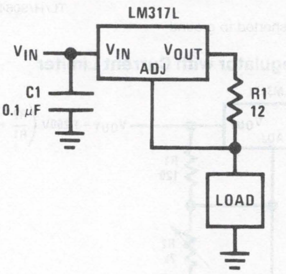

LM317L
VIN
VIN
VOUT
ADJ
VOUT
R1 120
R2 1k
LM317L
VIN
VIN
VOUT
ADJ
VOUT†
LM317L
VIN
VIN
VOUT
ADJ
VOUT†

*All outputs within ± 100 mV

†Minimum load −5mA

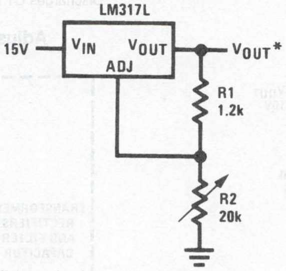
TL/H/9064–22

### 100 mA Current Regulator


LM317L
VIN
VIN
VOUT
ADJ
C1 0.1 μF
R1 12
LOAD

TL/H/9064–23

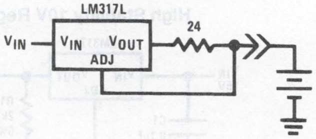
### 1.2V–12V Regulator with Minimum Program Current


LM317L
15V
VIN
VOUT
ADJ
VOUT*
R1 1.2k
R2 20k

*Minimum load current ≈ 2 mA

TL/H/9064–24

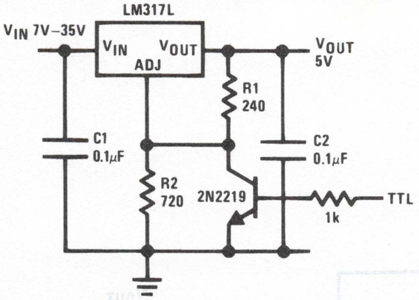
### 50 mA Constant Current Battery Charger for Nickel-Cadmium Batteries


LM317L
VIN
VIN
VOUT
ADJ
24

TL/H/9064–25

## Typical Applications (Continued)

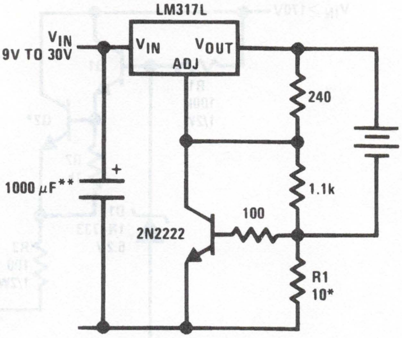
### 5V Logic Regulator with Electronic Shutdown*


LM317L
$V_{IN}$ 7V–35V
$V_{IN}$
$V_{OUT}$
ADJ
$V_{OUT}$
5V
R1
240
C1
0.1μF
C2
0.1μF
R2
720
2N2219
1k
TTL

TL/H/9064-26

*Minimum output ≈ 1.2V

### Current Limited 6V Charger

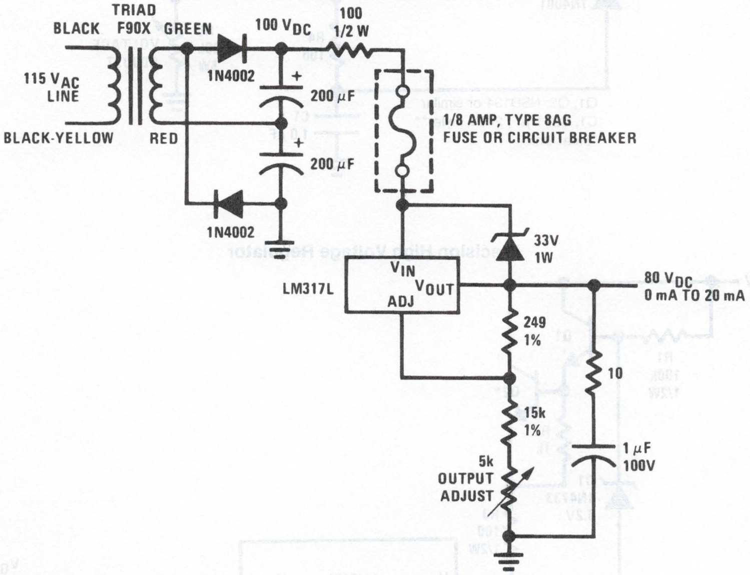

LM317L
$V_{IN}$
9V TO 30V
$V_{IN}$
$V_{OUT}$
ADJ
240
+
1000 μF**
1.1k
100
2N2222
R1
10*

TL/H/9064-27

*Sets peak current, $I_{PEAK}$ = 0.6V/R1

**1000 μF is recommended to filter out any input transients.

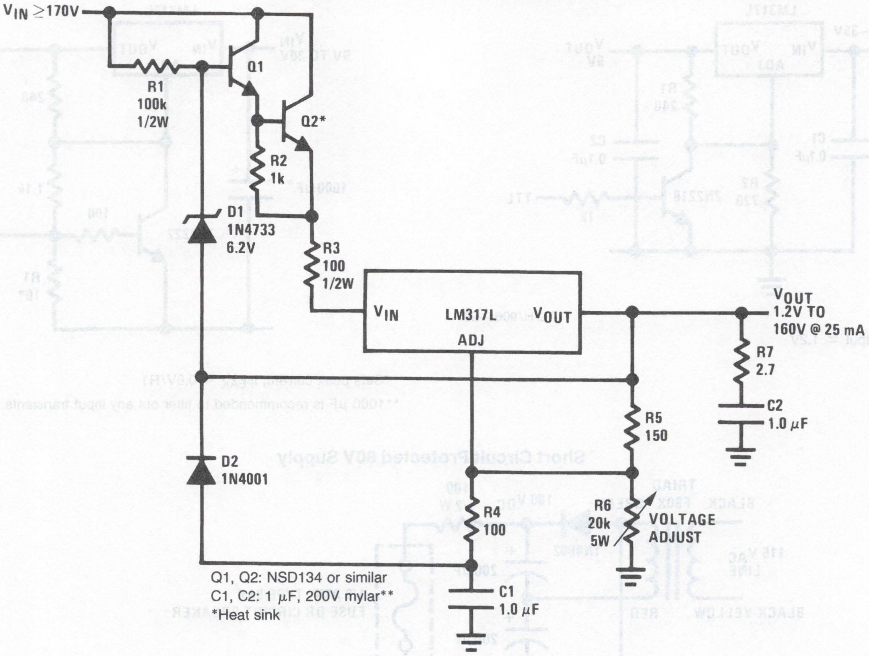
### Short Circuit Protected 80V Supply


TRIAD
BLACK
F90X
GREEN
100 $V_{DC}$
100
1/2 W
115 $V_{AC}$
LINE
1N4002
+
200 μF
1/8 AMP, TYPE 8AG
FUSE OR CIRCUIT BREAKER
BLACK-YELLOW
RED
+
200 μF
1N4002
33V
1W
LM317L
$V_{IN}$
$V_{OUT}$
ADJ
80 $V_{DC}$
0 mA TO 20 mA
249
1%
10
15k
1%
1 μF
100V
5k
OUTPUT
ADJUST

TL/H/9064-28

## Typical Applications (Continued)

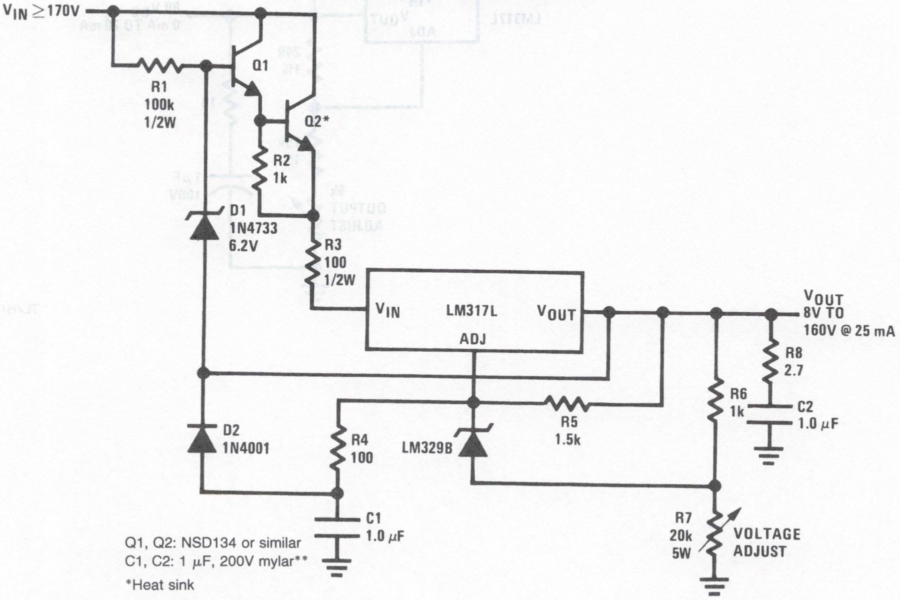
### Basic High Voltage Regulator


$V_{IN} \geq 170V$
R1
100k
1/2W
Q1
Q2*
R2
1k
D1
1N4733
6.2V
R3
100
1/2W
$V_{IN}$
LM317L
$V_{OUT}$
ADJ
$V_{OUT}$
1.2V TO
160V @ 25 mA
R7
2.7
C2
1.0 μF
R5
150
D2
1N4001
R4
100
R6
20k
5W
VOLTAGE
ADJUST
C1
1.0 μF

Q1, Q2: NSD134 or similar
C1, C2: 1 μF, 200V mylar**
*Heat sink

TL/H/9064–29

### Precision High Voltage Regulator


$V_{IN} \geq 170V$
R1
100k
1/2W
Q1
Q2*
R2
1k
D1
1N4733
6.2V
R3
100
1/2W
$V_{IN}$
LM317L
$V_{OUT}$
ADJ
$V_{OUT}$
8V TO
160V @ 25 mA
R8
2.7
R6
1k
C2
1.0 μF
D2
1N4001
R4
100
LM329B
R5
1.5k
C1
1.0 μF
R7
20k
5W
VOLTAGE
ADJUST

Q1, Q2: NSD134 or similar
C1, C2: 1 μF, 200V mylar**

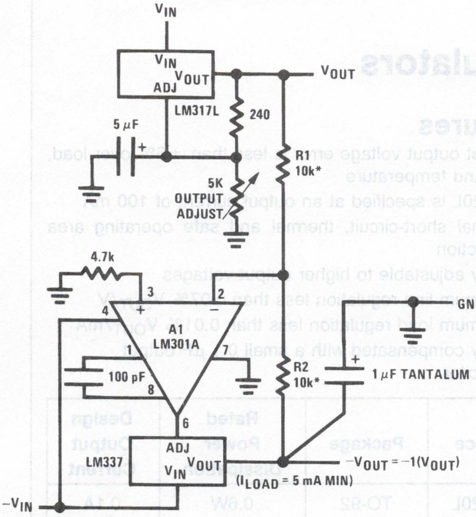
*Heat sink

**Mylar is a registered trademark of DuPont Co.

TL/H/9064–30

## Typical Applications (Continued)

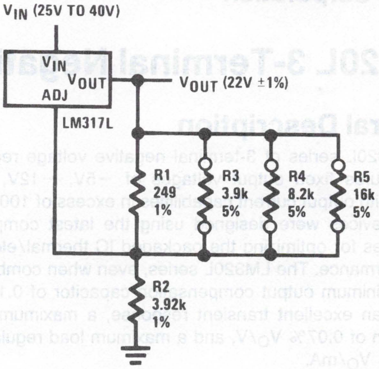
### Tracking Regulator



TL/H/9064–31

A1 = LM301A, LM307, or LF13741 only
R1, R2 = matched resistors with good TC tracking

### Regulator With Trimmable Output Voltage


$V_{IN}$ (25V TO 40V)
$V_{IN}$
$V_{OUT}$
ADJ
LM317L
$V_{OUT}$ (22V ±1%)
R1 249 1%
R3 3.9k 5%
R4 8.2k 5%
R5 16k 5%
R2 3.92k 1%

TL/H/9064–32

**Trim Procedure:**

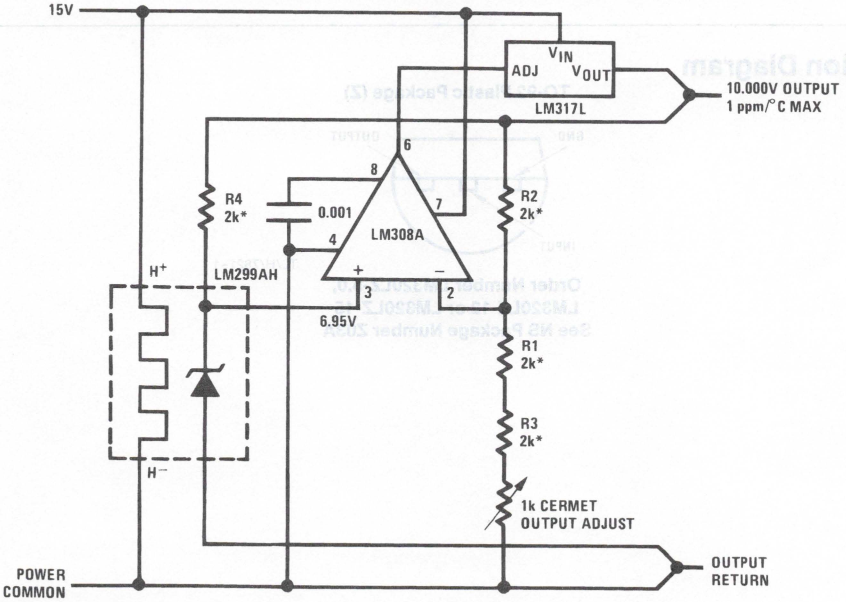
— If $V_{OUT}$ is 23.08V or higher, cut out R3 (if lower, don't cut it out).

— Then if $V_{OUT}$ is 22.47V or higher, cut out R4 (if lower, don't).

— Then if $V_{OUT}$ is 22.16V or higher, cut out R5 (if lower, don't).

This will trim the output to well within ±1% of 22.00 $V_{DC}$, without any of the expense or uncertainty of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

### Precision Reference with Short-Circuit Proof Output


15V
$V_{IN}$
ADJ
$V_{OUT}$
LM317L
10.000V OUTPUT
1 ppm/°C MAX
6
8
7
4
3
2
R4 2k*
0.001
LM308A
R2 2k*
$H^+$
LM299AH
+
−
6.95V
R1 2k*
R3 2k*
$H^-$
1k CERMET OUTPUT ADJUST
POWER COMMON
OUTPUT RETURN

TL/H/9064–33

*R1–R4 from thin-film network, Beckman 694-3-R2K-D or similar

**National Semiconductor Corporation**

# LM320L 3-Terminal Negative Regulators

## General Description

The LM320L series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V, with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM320L series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% $V_O$/V, and a maximum load regulation of 0.01% $V_O$/mA.

The LM320L series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM320L series is available in the 3-lead TO-92 package.

For output voltages other than −5V, −12V and −15V, the LM137 series provides an output voltage range from −1.2V to −47V.

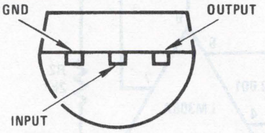
## Features

- Preset output voltage error is less than ±5% over load, line and temperature
- LM320L is specified at an output current of 100 mA
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% $V_{OUT}$/V
- Maximum load regulation less than 0.01% $V_{OUT}$/mA
- Easily compensated with a small 0.1 μF output capacitor

| Device | Package | Rated Power Dissipation | Design Output Current |
|---|---|---|---|
| LM320L | TO-92 | 0.6W | 0.1A |

## Connection Diagram

**TO-92 Plastic Package (Z)**



TL/H/7821-1

**Order Number LM320LZ-5.0, LM320LZ-12 or LM320LZ-15**
**See NS Package Number Z03A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| $V_{OUT}$ = −5V 12V and 15V | −35V |
| Internal Power Dissipation (Notes 1 and 3) | Internally Limited |
| Operating Temperature Range | 0°C to +70°C |
| Maximum Junction Temperature | +125°C |
| Storage Temperature Range | |
| Molded TO-92 | −55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## Electrical Characteristics (Note 2) $T_A$ = 0°C to +70°C unless otherwise noted.

| **Output Voltage** | | | | **−5V** | | | **−12V** | | | **−15V** | | **Units** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input Voltage (unless otherwise noted)** | | | | **−10V** | | | **−17V** | | | **−20V** | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $V_O$ | Output Voltage | $T_j$ = 25°C, $I_O$ = 100 mA | −5.2 | −5 | −4.8 | −12.5 | −12 | −11.5 | −15.6 | −15 | −14.4 | V |
| | | 1 mA ≤ $I_O$ ≤ 100 mA<br>$V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | −5.25 | (−20 ≤ $V_{IN}$ ≤ −7.5) | −4.75 | −12.6 | (−27 ≤ $V_{IN}$ ≤ −14.8) | −11.4 | −15.75 | (−30 ≤ $V_{IN}$ ≤ −18) | −14.25 | |
| | | 1 mA ≤ $I_O$ ≤ 40 mA<br>$V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | −5.25 | (−20 ≤ $V_{IN}$ ≤ −7) | −4.75 | −12.6 | (−27 ≤ $V_{IN}$ ≤ −14.5) | −11.4 | −15.75 | (−30 ≤ $V_{IN}$ ≤ −17.5) | −14.25 | |
| $\Delta V_O$ | Line Regulation | $T_j$ = 25°C, $I_O$ = 100 mA<br>$V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | (−20 ≤ $V_{IN}$ ≤ −7.3) | 60 | | (−27 ≤ $V_{IN}$ ≤ −14.6) | 45 | | (−30 ≤ $V_{IN}$ ≤ −17.7) | 45 | mV<br>V |
| | | $T_j$ = 25°C, $I_O$ = 40 mA<br>$V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | (−20 ≤ $V_{IN}$ ≤ −7) | 60 | | (−27 ≤ $V_{IN}$ ≤ −14.5) | 45 | | (−30 ≤ $V_{IN}$ ≤ −17.5) | 45 | mV<br>V |
| $\Delta V_O$ | Load Regulation | $T_j$ = 25°C<br>1 mA ≤ $I_O$ ≤ 100 mA | | | 50 | | | 100 | | | 125 | mV |
| $\Delta V_O$ | Long Term Stability | $I_O$ = 100 mA | | 20 | | | 48 | | | 60 | | mV/khr |
| $I_Q$ | Quiescent Current | $I_O$ = 100 mA | | 2 | 6 | | 2 | 6 | | 2 | 6 | mA |
| $\Delta I_Q$ | Quiescent Current Change | 1 mA ≤ $I_O$ ≤ 100 mA | | | 0.3 | | | 0.3 | | | 0.3 | mA |
| | | 1 mA ≤ $I_O$ ≤ 40 mA | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | $I_O$ = 100 mA<br>$V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | (−20 ≤ $V_{IN}$ ≤ −7.5) | 0.25 | | (−27 ≤ $V_{IN}$ ≤ −14.8) | 0.25 | | (−30 ≤ $V_{IN}$ ≤ −18) | 0.25 | mA<br>V |
| $V_n$ | Output Noise Voltage | $T_j$ = 25°C, $I_O$ = 100 mA<br>f = 10 Hz–10 kHz | | 40 | | | 96 | | | 120 | | µV |
| $\frac{\Delta V_{IN}}{\Delta V_O}$ | Ripple Rejection | $T_j$ = 25°C, $I_O$ = 100 mA<br>f = 120 Hz | 50 | | | 52 | | | 50 | | | dB |
| | Input Voltage Required to Maintain Line Regulation | $T_j$ = 25°C<br>$I_O$ = 100 mA | | | −7.3 | | | −14.6 | | | −17.7 | V |
| | | $I_O$ = 40 mA | | | −7.0 | | | −14.5 | | | −17.5 | |

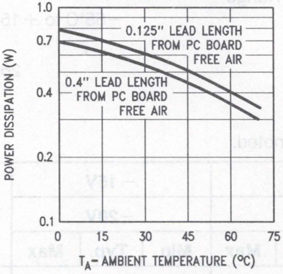
---

**Note 1:** Thermal resistance of Z package is typically 60°C/W $\theta_{JC}$, 232°C/W $\theta_{jA}$ at still air, and 88°C/W at 400 ft/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

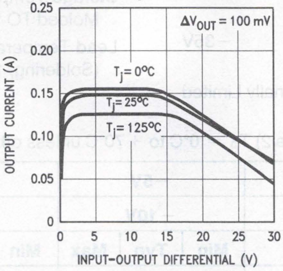
**Note 2:** To ensure constant junction temperature pulse testing is used.

## Typical Performance Characteristics

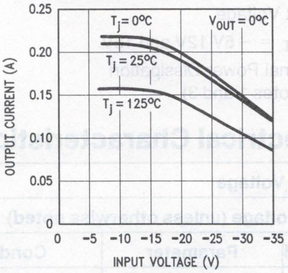
### Maximum Average Power Dissipation (TO-92)



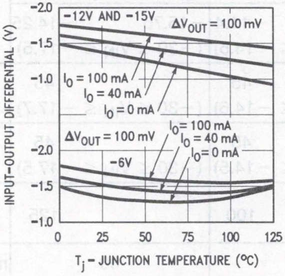
### Peak Output Current



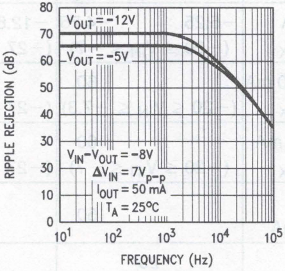
### Short Circuit Output Current



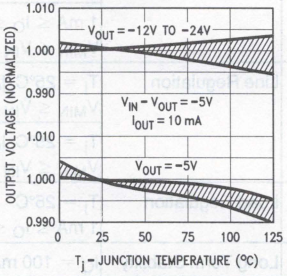
### Dropout Voltage



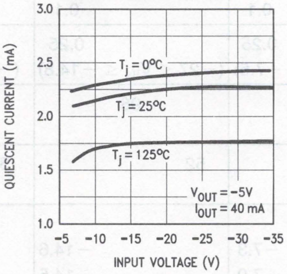
### Ripple Rejection



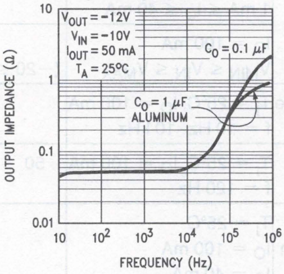
### Output Voltage vs Temperature (Normalized to 1V @ 25°C)



### Quiescent Current



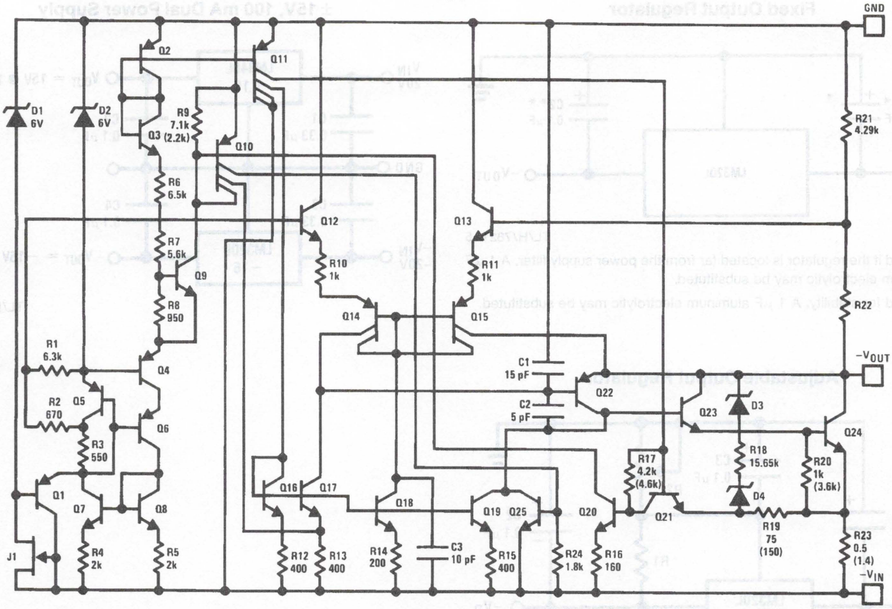
### Output Impedance



TL/H/7821-2

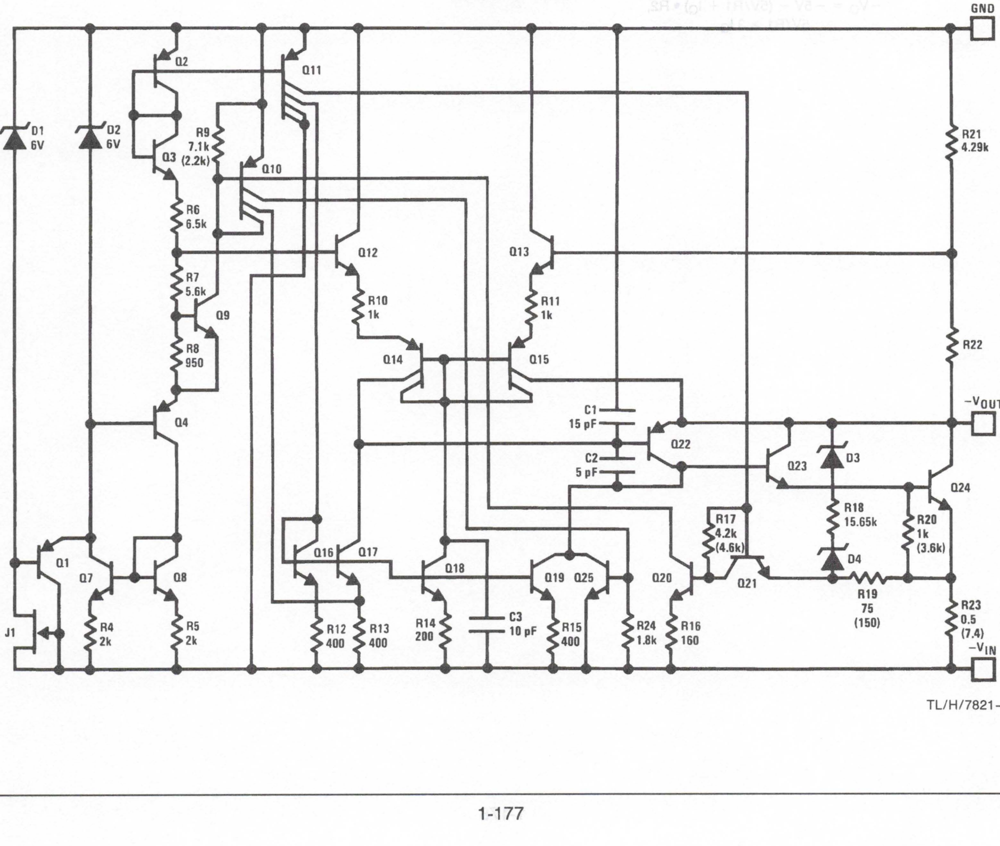
## Schematic Diagrams

−5V


GND
Q2
Q11
D1
6V
D2
6V
R9
7.1k
(2.2k)
Q3
Q10
R6
6.5k
Q12
Q13
R21
4.29k
R7
5.6k
Q9
R10
1k
R11
1k
R8
950
Q14
Q15
R22
R1
6.3k
Q4
C1
15 pF
−VOUT
Q22
D3
R2
670
Q5
C2
5 pF
Q23
Q6
Q24
R3
550
R17
4.2k
(4.6k)
R18
15.65k
R20
1k
(3.6k)
Q1
Q16
Q17
Q18
D4
Q7
Q8
Q19
Q25
Q20
Q21
R19
75
(150)
J1
R4
2k
R5
2k
R12
400
R13
400
R14
200
C3
10 pF
R15
400
R24
1.8k
R16
160
R23
0.5
(1.4)
−VIN

TL/H/7821–3

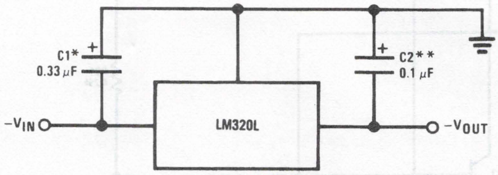
−12V and −15V


GND
Q2
Q11
D1
6V
D2
6V
R9
7.1k
(2.2k)
Q3
Q10
R21
4.29k
R6
6.5k
Q12
Q13
R7
5.6k
Q9
R10
1k
R11
1k
R8
950
Q14
Q15
R22
Q4
C1
15 pF
−VOUT
Q22
D3
C2
5 pF
Q23
Q24
R17
4.2k
(4.6k)
R18
15.65k
R20
1k
(3.6k)
Q16
Q17
Q1
Q18
D4
Q7
Q8
Q19
Q25
Q20
Q21
R19
75
(150)
J1
R4
2k
R5
2k
R12
400
R13
400
R14
200
C3
10 pF
R15
400
R24
1.8k
R16
160
R23
0.5
(7.4)
−VIN

TL/H/7821–4

# Typical Applications

## Fixed Output Regulator

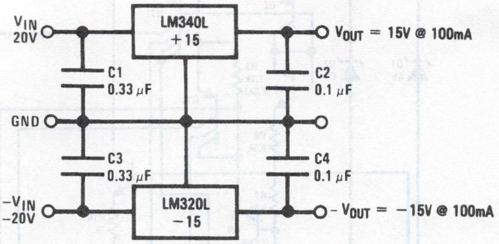

C1*
0.33 μF
C2**
0.1 μF
$-V_{IN}$
LM320L
$-V_{OUT}$

TL/H/7821-5

*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

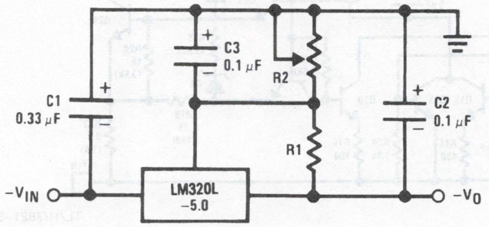
**Required for stability. A 1 μF aluminum electrolytic may be substituted.

## ±15V, 100 mA Dual Power Supply


$V_{IN}$ 20V
LM340L +15
$V_{OUT}$ = 15V @ 100mA
C1 0.33 μF
C2 0.1 μF
GND
C3 0.33 μF
C4 0.1 μF
$-V_{IN}$ −20V
LM320L −15
$-V_{OUT}$ = −15V @ 100mA

TL/H/7821-7

## Adjustable Output Regulator


C3 0.1 μF
R2
C1 0.33 μF
C2 0.1 μF
R1
$-V_{IN}$
LM320L −5.0
$-V_O$

TL/H/7821-6

$$-V_O = -5V - (5V/R1 + I_Q) \bullet R2,$$
$$5V/R1 > 3\,I_Q$$

National Semiconductor Corporation

# LM330 3-Terminal Positive Regulator

## General Description

The LM330 5V 3-terminal positive voltage regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

The low dropout voltage makes the LM330 useful for certain battery applications since this feature allows a longer battery discharge before the output falls out of regulation. For example, a battery supplying the regulator input voltage may discharge to 5.6V and still properly regulate the system and load voltage. Supporting this feature, the LM330 protects both itself and regulated systems from negative voltage inputs resulting from reverse installations of batteries.

Other protection features include line transient protection up to 26V, when the output actually shuts down to avoid damaging internal and external circuits. Also, the LM330 regulator cannot be harmed by a temporary mirror-image insertion.

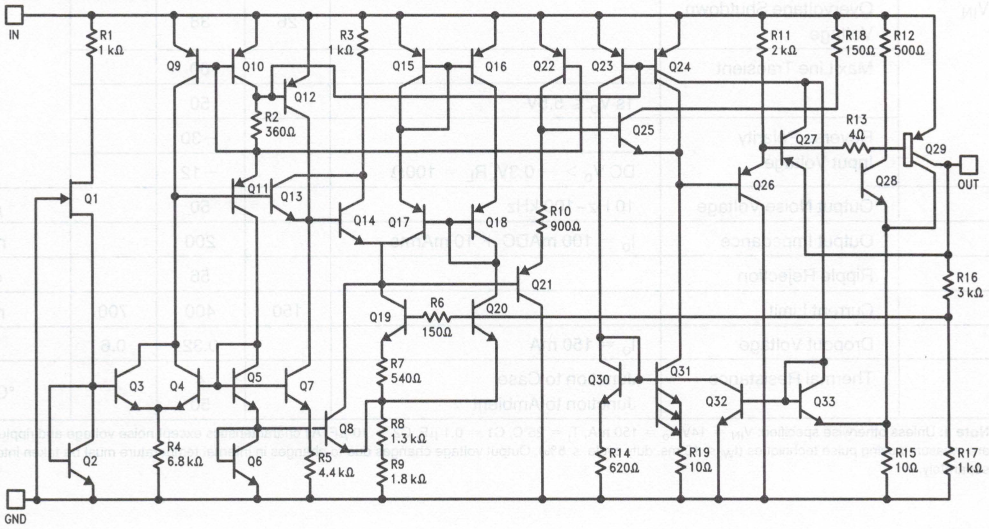
## Features

- Input-output differential less than 0.6V
- Output current of 150 mA
- Reverse battery protection
- Line transient protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in the thermal limit

## Voltage Range

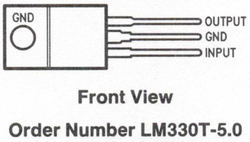
| | |
|---|---|
| LM33QT-5.0 | 5V |

## Schematic and Connection Diagrams


IN
R1 1 kΩ
Q9
Q10
Q12
R2 360Ω
R3 1 kΩ
Q15
Q16
Q22
Q23
Q24
Q25
R11 2 kΩ
R18 150Ω
R12 500Ω
R13 4Ω
Q27
Q29
OUT
Q26
Q28
Q1
Q11
Q13
Q14
Q17
Q18
R10 900Ω
Q21
R16 3 kΩ
R6 150Ω
Q19
Q20
R7 540Ω
Q3
Q4
Q5
Q7
Q30
Q31
Q32
Q33
Q8
R8 1.3 kΩ
R9 1.8 kΩ
R4 6.8 kΩ
Q2
Q6
R5 4.4 kΩ
R14 620Ω
R19 10Ω
R15 10Ω
R17 1 kΩ
GND

TL/H/9306-1

**(TO-220)**
**Plastic Package**


GND
OUTPUT
GND
INPUT

TL/H/9306-2

**Front View**

**Order Number LM330T-5.0**
**See NS Package Number T03B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

Input Voltage
  Operating Range 26V
  Line Transient Protection (1000 ms) 40V

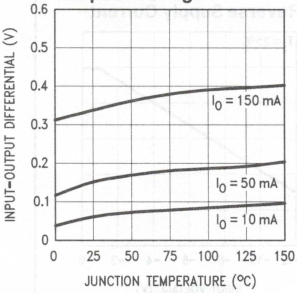
Internal Power Dissipation Internally Limited
Operating Temperature Range 0°C to +70°C
Maximum Junction Temperature +125°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) +300°C

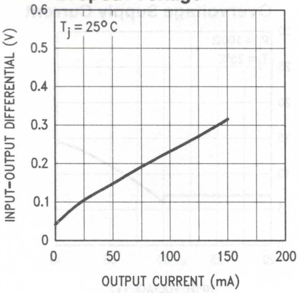
## Electrical Characteristics (Note 1)

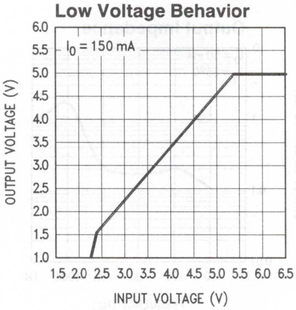
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_O$ | Output Voltage | $T_j = 25°C$ | 4.8 | 5 | 5.2 | V |
| | Output Voltage Over Temp | $5 < I_O < 150$ mA<br>$6 < V_{IN} < 26V$; $0°C \leq T_j \leq 100°C$ | 4.75 | | 5.25 | |
| $\Delta V_O$ | Line Regulation | $9 < V_{IN} < 16V$, $I_O = 5$ mA<br>$6 < V_{IN} < 26V$, $I_O = 5$ mA | | 7<br>30 | 25<br>60 | mV |
| | Load Regulation | $5 < I_O < 150$ mA | | 14 | 50 | |
| | Long Term Stability | | | 20 | | mV/1000 hrs |
| $I_Q$ | Quiescent Current | $I_O = 10$ mA<br>$I_O = 50$ mA<br>$I_O = 150$ mA | | 3.5<br>5<br>18 | 7<br>11<br>40 | mA |
| | Line Transient<br>Reverse Polarity | $V_{IN} = 40V$, $R_L = 100\Omega$, 1s<br>$V_{IN} = -6V$, $R_L = 100\Omega$ | | 14<br>−80 | | |
| $\Delta I_Q$ | Quiescent Current Change | $6 < V_{IN} < 26V$ | | 10 | | % |
| $V_{IN}$ | Overvoltage Shutdown Voltage | | 26 | 38 | | V |
| | Max Line Transient | | | 60 | | |
| | | 1s $V_O \leq 5.5V$ | | 50 | | |
| | Reverse Polarity Input Voltage | | | −30 | | |
| | | DC $V_O > -0.3V$, $R_L = 100\Omega$ | | −12 | | |
| | Output Noise Voltage | 10 Hz–100 kHz | | 50 | | μV |
| | Output Impedance | $I_O = 100$ mADC + 10 mArms | | 200 | | mΩ |
| | Ripple Rejection | | | 56 | | dB |
| | Current Limit | | 150 | 400 | 700 | mA |
| | Dropout Voltage | $I_O = 150$ mA | | 0.32 | 0.6 | V |
| | Thermal Resistance | Junction to Case<br>Junction to Ambient | | 4<br>50 | | °C/W |

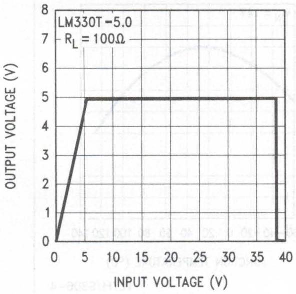
**Note 1:** Unless otherwise specified: $V_{IN} = 14V$, $I_o = 150$ mA, $T_j = 25°C$, C1 = 0.1 μF, C2 = 10 μF. All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

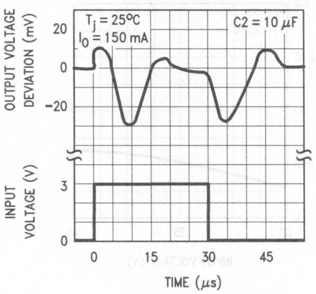
## Typical Performance Characteristics

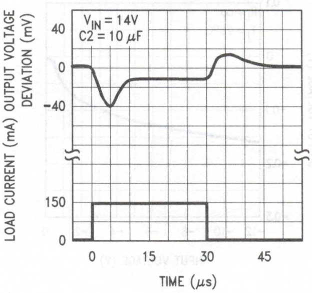

**Dropout Voltage**

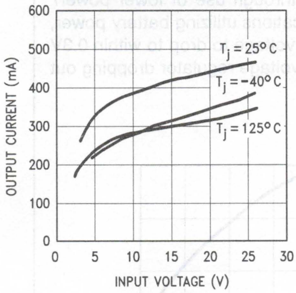

**Dropout Voltage**

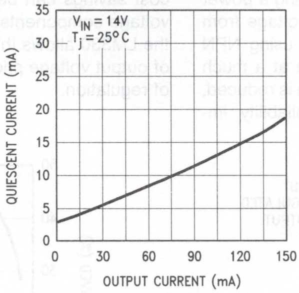

**Low Voltage Behavior**

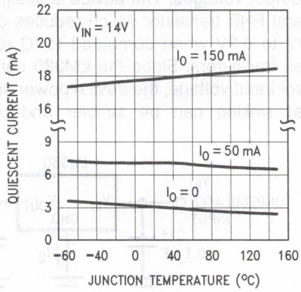

**High Voltage Behavior**

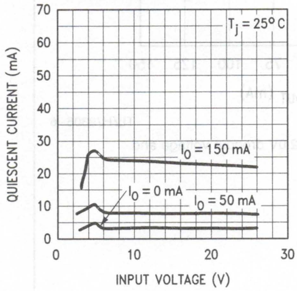

**Line Transient Response**

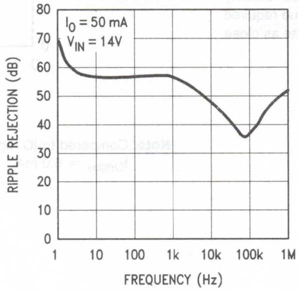

**Load Transient Response**

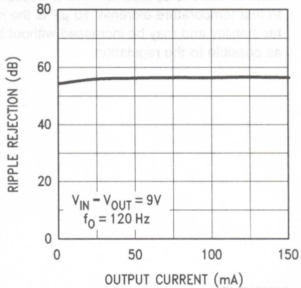

**Peak Output Current**


**Quiescent Current**


**Quiescent Current**


**Quiescent Current**

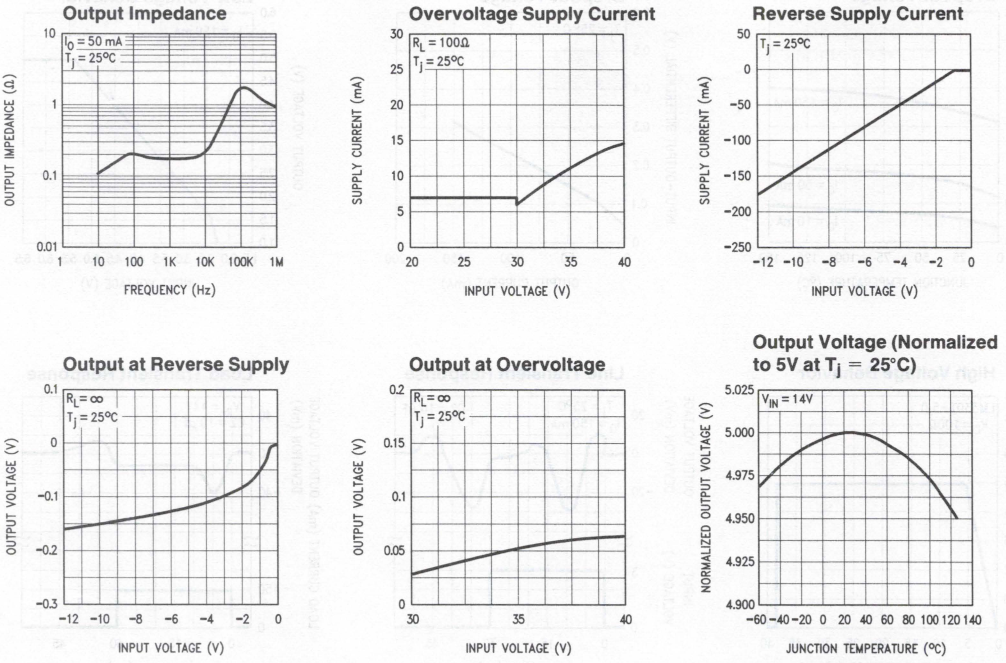

**Ripple Rejection**


**Ripple Rejection**

TL/H/9306-3

1

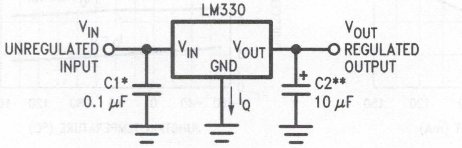
## Typical Performance Characteristics (Continued)



TL/H/9306-4

## Typical Applications

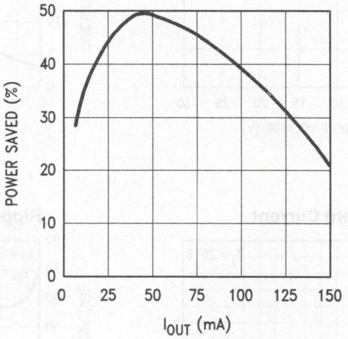
The LM330 is designed specifically to operate at lower input to output voltages. The device is designed utilizing a power lateral PNP transistor which reduces dropout voltage from 2.0V to 0.3V when compared to IC regulators using NPN pass transistors. Since the LM330 can operate at a much lower input voltage, the device power dissipation is reduced, heat sinking can be simpler and device reliability improved through lower chip operating temperature. Also, a cost savings can be utilized through use of lower power/voltage components. In applications utilizing battery power, the LM330 allows the battery voltage to drop to within 0.3V of output voltage prior to the voltage regulator dropping out of regulation.



TL/H/9306-5

* Required if regulator is located far from power supply filter.

** C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 10 μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulation.



TL/H/9306-6

**Note:** Compared to IC regulator with 2.0V dropout voltage and $I_{Qmax}$, = 6.0 mA.

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

**National Semiconductor Corporation**

**PRELIMINARY**

# LM337L 3-Terminal Adjustable Regulator

## General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, only a single 1 µF solid tantalum output capacitor is needed unless the device is situated more than 6 inches from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

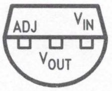
The LM337L is available in a standard TO-92 transistor package and a SO-8 surface mount package. The LM337L is rated for operation over a −25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

## Features

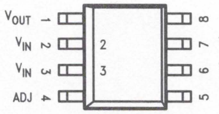
- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

## Connection Diagram



TL/H/9134-1

**Bottom View**



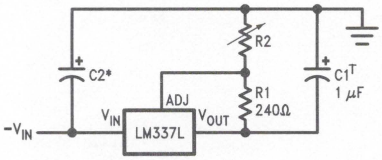
TL/H/9134-2

**Top View**

**Order Number LM337LM or LM337LZ**
**See NS Package Number M08A or Z03A**

## Typical Applications

### 1.2V–25V Adjustable Regulator



TL/H/9134-3

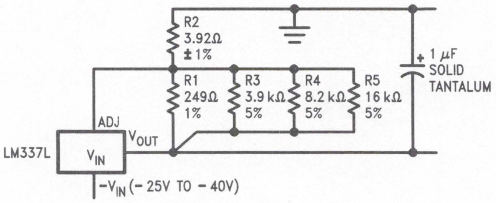
Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1+\frac{R2}{240\Omega}\right)$$

†C1 = 1 µF solid tantalum or 10 µF aluminum electrolytic required for stability

*C2 = 1 µF solid tantalum is required only if regulator is more than 4″ from power supply filter capacitor

### Regulator with Trimmable Output Voltage



TL/H/9134-4

Trim Procedure:

—If $V_{OUT}$ is −23.08V or bigger, cut out R3 (if smaller, don't cut it out).

—Then if $V_{OUT}$ is −22.47V or bigger, cut out R4 (if smaller, don't).

—Then if $V_{OUT}$ is −22.16V or bigger, cut out R5 (if smaller, don't).

This will trim the output to well within 1% of −22.00 $V_{DC}$, without any of the expense or trouble of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Power Dissipation | Internally Limited |
| Input–Output Voltage Differential | 40V |
| Operating Junction Temperature Range | −25°C to +125°C |
| Storage Temperature | −55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| Plastic Package (Soldering 4 sec.) | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Line Regulation | $T_A = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2) | | 0.01 | 0.04 | %/V |
| Load Regulation | $T_A = 25°C$, $5\ mA \le I_{OUT} \le I_{MAX}$, (Note 2) | | 0.1 | 0.5 | % |
| Thermal Regulation | $T_A = 25°C$, 10 ms Pulse | | 0.04 | 0.2 | %/W |
| Adjustment Pin Current | | | 50 | 100 | μA |
| Adjustment Pin Current Change | $5\ mA \le I_L \le 100\ mA$<br>$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ | | 0.2 | 5 | μA |
| Reference Voltage | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3)<br>$10\ mA \le I_{OUT} \le 100\ mA$, $P \le 625\ mW$ | 1.20 | 1.25 | 1.30 | V |
| Line Regulation | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2) | | 0.02 | 0.07 | %/V |
| Load Regulation | $5\ mA \le I_{OUT} \le 100\ mA$, (Note 2) | | 0.3 | 1.5 | % |
| Temperature Stability | $T_{MIN} \le T_j \le T_{MAX}$ | | 0.65 | | % |
| Minimum Load Current | $\lvert V_{IN} - V_{OUT} \rvert \le 40V$<br>$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 15V$ | | 3.5<br>2.2 | 5<br>3.5 | mA<br>mA |
| Current Limit | $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 13V$<br>$\lvert V_{IN} - V_{OUT} \rvert = 40V$ | 100<br>25 | 200<br>50 | 320<br>120 | mA<br>mA |
| Rms Output Noise, % of $V_{OUT}$ | $T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$ | | 0.003 | | % |
| Ripple Rejection Ratio | $V_{OUT} = -10V$, $F = 120\ Hz$, $C_{ADJ} = 0$<br>$C_{ADJ} = 10\ \mu F$ | <br>66 | 65<br>80 | | dB<br>dB |
| Long-Term Stability | $T_A = 125°C$ | | 0.3 | 1 | % |

**Note 1:** Unless otherwise specified, these specifications apply $-25°C \le T_j \le +125°C$ for the LM337L; $\lvert V_{IN} - V_{OUT} \rvert = 5V$ and $I_{OUT} = 40\ mA$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. $I_{MAX}$ is 100 mA.

**Note 2:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

**Note 3:** Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to PC board.

**National Semiconductor Corporation**

# LM723/LM723C Voltage Regulator

## General Description

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

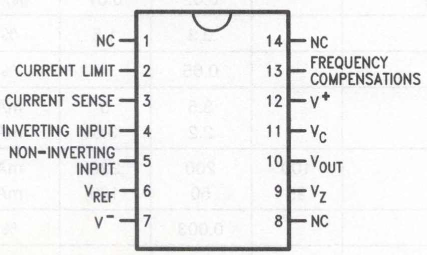
The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

## Features

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

## Connection Diagrams

**Dual-In-Line Package**

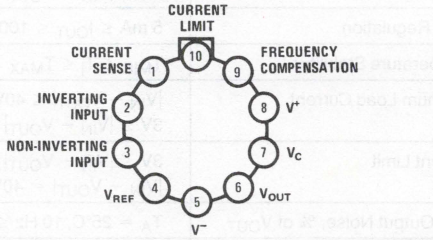

NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
VREF 6
V− 7
14 NC
13 FREQUENCY COMPENSATIONS
12 V+
11 VC
10 VOUT
9 VZ
8 NC

TL/H/8563-2

**Top View**

**Order Number LM723J, LM723CJ, LM723CM or LM723CN**
**See NS Package J14A, M14A or N14A**

**Metal Can Package**


CURRENT LIMIT
10
CURRENT SENSE
1
FREQUENCY COMPENSATION
9
INVERTING INPUT
2
8
V+
NON-INVERTING INPUT
3
7
VC
VREF
4
5
6
VOUT
V−

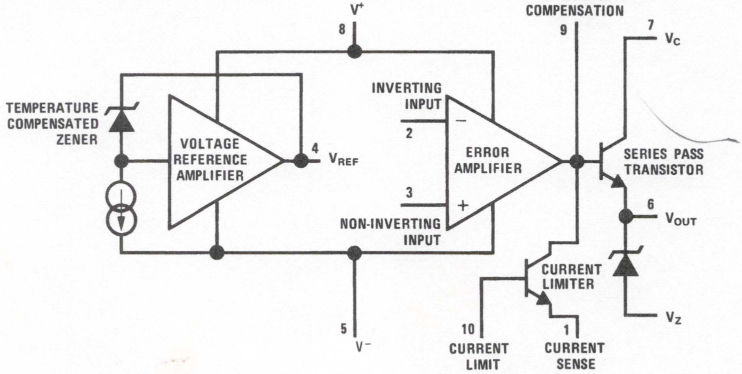
TL/H/8563-3

**Note:** Pin 5 connected to case.

**Top View**

**Order Number LM723H or LM723CH**
**See NS Package H10C**

## Equivalent Circuit*


V+
8
FREQUENCY COMPENSATION
9
7
VC
TEMPERATURE COMPENSATED ZENER
VOLTAGE REFERENCE AMPLIFIER
4
VREF
INVERTING INPUT
2
−
ERROR AMPLIFIER
3
+
NON-INVERTING INPUT
SERIES PASS TRANSISTOR
6
VOUT
CURRENT LIMITER
VZ
5
V−
10
CURRENT LIMIT
1
CURRENT SENSE

TL/H/8563-4

*Pin numbers refer to metal can package.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 9)**

| | |
|---|---|
| Pulse Voltage from $V^+$ to $V^-$ (50 ms) | 50V |
| Continuous Voltage from $V^+$ to $V^-$ | 40V |
| Input-Output Voltage Differential | 40V |
| Maximum Amplifier Input Voltage (Either Input) | 8.5V |
| Maximum Amplifier Input Voltage (Differential) | 5V |
| Current from $V_Z$ | 25 mA |
| Current from $V_{REF}$ | 15 mA |

| | |
|---|---|
| Internal Power Dissipation Metal Can (Note 1) | 800 mW |
| Cavity DIP (Note 1) | 900 mW |
| Molded DIP (Note 1) | 660 mW |
| Operating Temperature Range LM723 | −55°C to +150°C |
| LM723C | 0°C to +70°C |
| Storage Temperature Range Metal Can | −65°C to +150°C |
| Molded DIP | −55°C to +150°C |
| Lead Temperature (Soldering, 4 sec. max.) | |
| Hermetic Package | 300°C |
| Plastic Package | 260°C |

## Electrical Characteristics (Note 2)

| Parameter | Conditions | LM723 | | | LM723C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation | $V_{IN} = 12V$ to $V_{IN} = 15V$ | | 0.01 | 0.1 | | 0.01 | 0.1 | % $V_{OUT}$ |
| | $-55°C \leq T_A \leq +125°C$ | | | 0.3 | | | | % $V_{OUT}$ |
| | $0°C \leq T_A \leq +70°C$ | | | | | | 0.3 | % $V_{OUT}$ |
| | $V_{IN} = 12V$ to $V_{IN} = 40V$ | | 0.02 | 0.2 | | 0.1 | 0.5 | % $V_{OUT}$ |
| Load Regulation | $I_L = 1$ mA to $I_L = 50$ mA | | 0.03 | 0.15 | | 0.03 | 0.2 | % $V_{OUT}$ |
| | $-55°C \leq T_A \leq +125°C$ | | | 0.6 | | | | % $V_{OUT}$ |
| | $0°C \leq T_A \leq +70°C$ | | | | | | 0.6 | % $V_{OUT}$ |
| Ripple Rejection | f = 50 Hz to 10 kHz, $C_{REF} = 0$ | | 74 | | | 74 | | dB |
| | f = 50 Hz to 10 kHz, $C_{REF} = 5\ \mu F$ | | 86 | | | 86 | | dB |
| Average Temperature Coefficient of Output Voltage (Note 8) | $-55°C \leq T_A \leq +125°C$ | | 0.002 | 0.015 | | | | %/°C |
| | $0°C \leq T_A \leq +70°C$ | | | | | 0.003 | 0.015 | %/°C |
| Short Circuit Current Limit | $R_{SC} = 10\Omega$, $V_{OUT} = 0$ | | 65 | | | 65 | | mA |
| Reference Voltage | | 6.95 | 7.15 | 7.35 | 6.80 | 7.15 | 7.50 | V |
| Output Noise Voltage | BW = 100 Hz to 10 kHz, $C_{REF} = 0$ | | 86 | | | 86 | | μVrms |
| | BW = 100 Hz to 10 kHz, $C_{REF} = 5\ \mu F$ | | 2.5 | | | 2.5 | | μVrms |
| Long Term Stability | | | 0.05 | | | 0.05 | | %/1000 hrs |
| Standby Current Drain | $I_L = 0$, $V_{IN} = 30V$ | | 1.7 | 3.5 | | 1.7 | 4.0 | mA |
| Input Voltage Range | | 9.5 | | 40 | 9.5 | | 40 | V |
| Output Voltage Range | | 2.0 | | 37 | 2.0 | | 37 | V |
| Input-Output Voltage Differential | | 3.0 | | 38 | 3.0 | | 38 | V |
| $\theta_{JA}$ | Molded DIP | | 105 | | | 105 | | °C/W |
| $\theta_{JA}$ | Cavity DIP | | 150 | | | 150 | | °C/W |
| $\theta_{JA}$ | TO-5 Board Mount in Still Air | | 225 | | | 225 | | °C/W |
| $\theta_{JA}$ | TO-5 Board Mount in 400 LF/Min Air Flow | | 90 | | | 90 | | °C/W |
| $\theta_{JA}$ | SO | | | | | 125 | | °C/W |
| $\theta_{JC}$ | | | 25 | | | 25 | | °C/W |

**Note 1:** See derating curves for maximum power rating above 25°C.

**Note 2:** Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12V$, $V^- = 0$, $V_{OUT} = 5V$, $I_L = 1$ mA, $R_{SC} = 0$, $C_1 = 100$ pF, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in *Figure 1*. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

**Note 3:** $L_1$ is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

**Note 4:** Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

**Note 5:** Replace R1/R2 in figures with divider shown in *Figure 13*.

**Note 6:** $V^+$ must be connected to a +3V or greater supply.

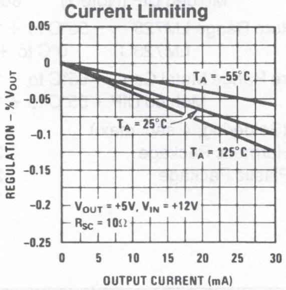
**Note 7:** For metal can applications where $V_Z$ is required, an external 6.2V zener diode should be connected in series with $V_{OUT}$.

**Note 8:** Guaranteed by correlation to other tests.

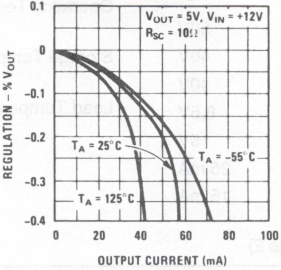
**Note 9:** Refer to RETS723X military specifications for the LM723.

# Typical Performance Characteristics

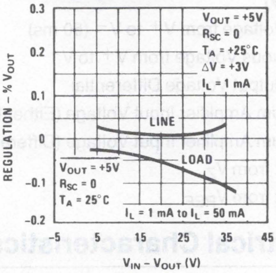
### Load Regulation Characteristics with Current Limiting



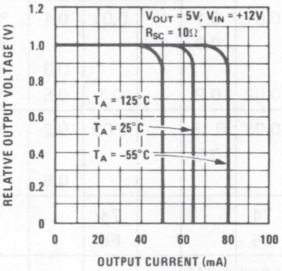
### Load Regulation Characteristics with Current Limiting



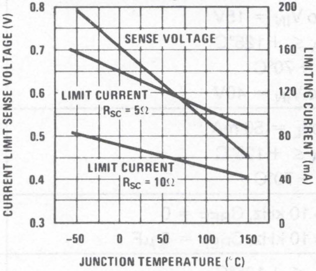
### Load & Line Regulation vs Input-Output Voltage Differential



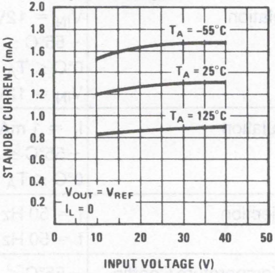
### Current Limiting Characteristics



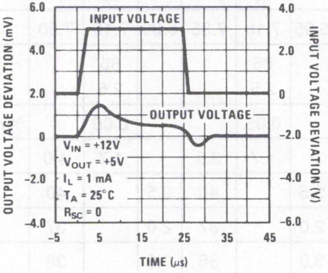
### Current Limiting Characteristics vs Junction Temperature



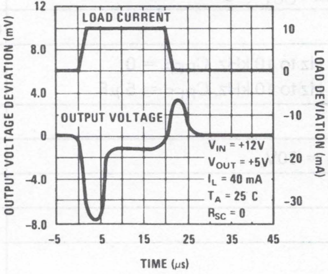
### Standby Current Drain vs Input Voltage



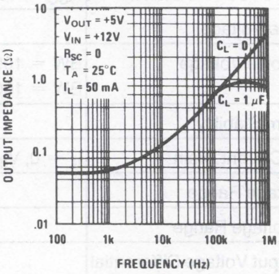
### Line Transient Response



### Load Transient Response



### Output Impedence vs Frequency



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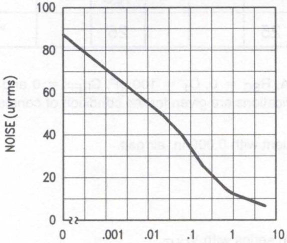
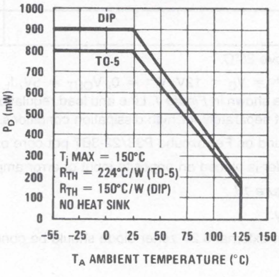
### Noise vs Filter Capacitor (CREF in Circuit of *Figure 1*) (Bandwidth 100 Hz to 10 kHz)



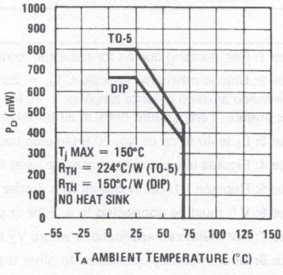
TL/H/8563–7

## Maximum Power Ratings

### LM723 Power Dissipation vs Ambient Temperature



### LM723C Power Dissipation vs Ambient Temperature



TL/H/8563–5

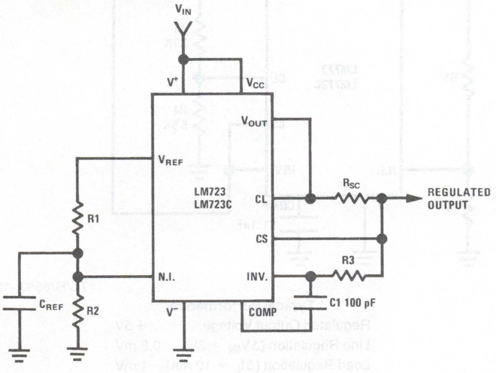
### TABLE I. Resistor Values (kΩ) for Standard Output Voltage

| Positive Output Voltage | Applicable Figures | Fixed Output ±5% | | Output Adjustable ±10% (Note 5) | | | Negative Output Voltage | Applicable Figures | Fixed Output ±5% | | 5% Output Adjustable ±10% | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | (Note 4) | R1 | R2 | R1 | P1 | R2 | | | R1 | R2 | R1 | P1 | R2 |
| +3.0 | 1, 5, 6, 9, 12 (4) | 4.12 | 3.01 | 1.8 | 0.5 | 1.2 | +100 | 7 | 3.57 | 102 | 2.2 | 10 | 91 |
| +3.6 | 1, 5, 6, 9, 12 (4) | 3.57 | 3.65 | 1.5 | 0.5 | 1.5 | +250 | 7 | 3.57 | 255 | 2.2 | 10 | 240 |
| +5.0 | 1, 5, 6, 9, 12 (4) | 2.15 | 4.99 | 0.75 | 0.5 | 2.2 | −6 (Note 6) | 3, (10) | 3.57 | 2.43 | 1.2 | 0.5 | 0.75 |
| +6.0 | 1, 5, 6, 9, 12 (4) | 1.15 | 6.04 | 0.5 | 0.5 | 2.7 | −9 | 3, 10 | 3.48 | 5.36 | 1.2 | 0.5 | 2.0 |
| +9.0 | 2, 4, (5, 6, 9, 12) | 1.87 | 7.15 | 0.75 | 1.0 | 2.7 | −12 | 3, 10 | 3.57 | 8.45 | 1.2 | 0.5 | 3.3 |
| +12 | 2, 4, (5, 6, 9, 12) | 4.87 | 7.15 | 2.0 | 1.0 | 3.0 | −15 | 3, 10 | 3.65 | 11.5 | 1.2 | 0.5 | 4.3 |
| +15 | 2, 4, (5, 6, 9, 12) | 7.87 | 7.15 | 3.3 | 1.0 | 3.0 | −28 | 3, 10 | 3.57 | 24.3 | 1.2 | 0.5 | 10 |
| +28 | 2, 4, (5, 6, 9, 12) | 21.0 | 7.15 | 5.6 | 1.0 | 2.0 | −45 | 8 | 3.57 | 41.2 | 2.2 | 10 | 33 |
| +45 | 7 | 3.57 | 48.7 | 2.2 | 10 | 39 | −100 | 8 | 3.57 | 97.6 | 2.2 | 10 | 91 |
| +75 | 7 | 3.57 | 78.7 | 2.2 | 10 | 68 | −250 | 8 | 3.57 | 249 | 2.2 | 10 | 240 |

### TABLE II. Formulae for Intermediate Output Voltages

| | | |
|---|---|---|
| **Outputs from +2 to +7 volts**<br>(*Figures 1, 5, 6, 9, 12, [4]*)<br>$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$ | **Outputs from +4 to +250 volts**<br>(*Figure 7*)<br>$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right)$; R3 = R4 | **Current Limiting**<br>$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$ |
| **Outputs from +7 to +37 volts**<br>(*Figures 2, 4, [5, 6, 9, 12]*)<br>$V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$ | **Outputs from −6 to −250 volts**<br>(*Figures 3, 8, 10*)<br>$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right)$; R3 = R4 | **Foldback Current Limiting**<br>$I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$<br>$I_{SHORT\,CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$ |

## Typical Applications

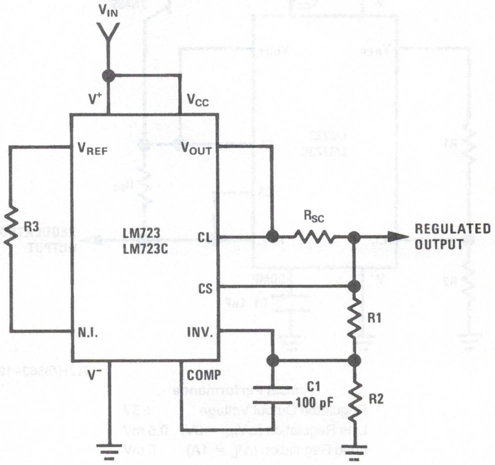


TL/H/8563-8

Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

| Typical Performance | |
|---|---|
| Regulated Output Voltage | 5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 1.5 mV |

**FIGURE 1. Basic Low Voltage Regulator ($V_{OUT}$ = 2 to 7 Volts)**



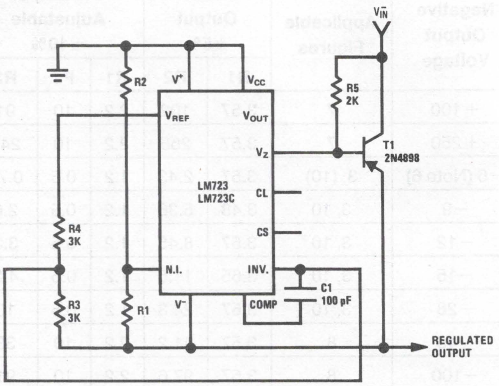
TL/H/8563-9

Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift. R3 may be eliminated for minimum component count.

| Typical Performance | |
|---|---|
| Regulated Output Voltage | 15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1.5 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 4.5 mV |

**FIGURE 2. Basic High Voltage Regulator ($V_{OUT}$ = 7 to 37 Volts)**

## Typical Applications (Continued)

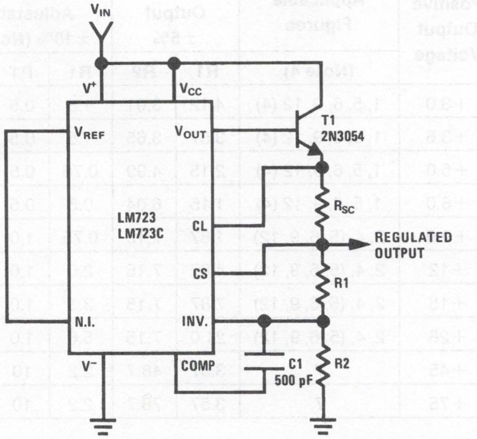

VIN
R2
V+
VCC
VREF
VOUT
VZ
R5
2K
T1
2N4898
LM723
LM723C
CL
CS
R4
3K
N.I.
INV.
C1
100 pF
R3
3K
R1
V−
COMP
REGULATED
OUTPUT

TL/H/8563-10

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | −15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1 mV |
| Load Regulation ($\Delta I_L$ = 100 mA) | 2 mV |

**FIGURE 3. Negative Voltage Regulator**

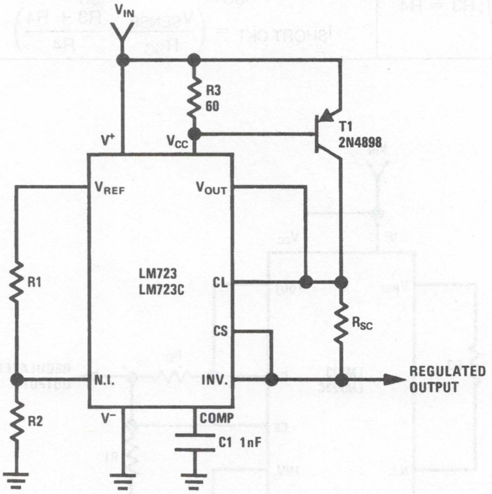

VIN
V+
VCC
VREF
VOUT
T1
2N3054
RSC
LM723
LM723C
CL
REGULATED
OUTPUT
CS
R1
N.I.
INV.
V−
COMP
C1
500 pF
R2

TL/H/8563-11

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +15V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 1.5 mV |
| Load Regulation ($\Delta I_L$ = 1A) | 15 mV |

**FIGURE 4. Positive Voltage Regulator (External NPN Pass Transistor)**

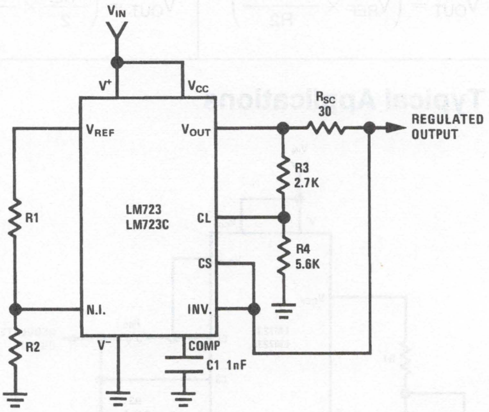

VIN
R3
60
T1
2N4898
V+
VCC
VREF
VOUT
R1
LM723
LM723C
CL
RSC
CS
N.I.
INV.
REGULATED
OUTPUT
R2
V−
COMP
C1 1nF

TL/H/8563-12

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 1A) | 5 mV |

**FIGURE 5. Positive Voltage Regulator (External PNP Pass Transistor)**


VIN
V+
VCC
RSC
30
REGULATED
OUTPUT
VREF
VOUT
R3
2.7K
R1
LM723
LM723C
CL
R4
5.6K
CS
N.I.
INV.
R2
V−
COMP
C1 1nF

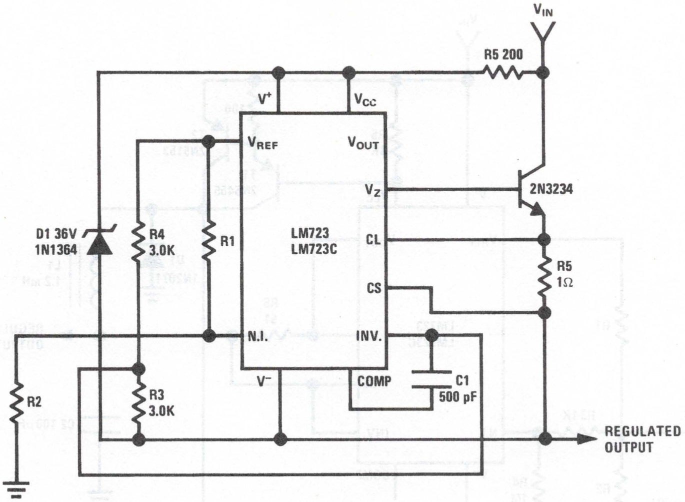
TL/H/8563-13

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 3V) | 0.5 mV |
| Load Regulation ($\Delta I_L$ = 10 mA) | 1 mV |
| Short Circuit Current | 20 mA |

**FIGURE 6. Foldback Current Limiting**

## Typical Applications (Continued)

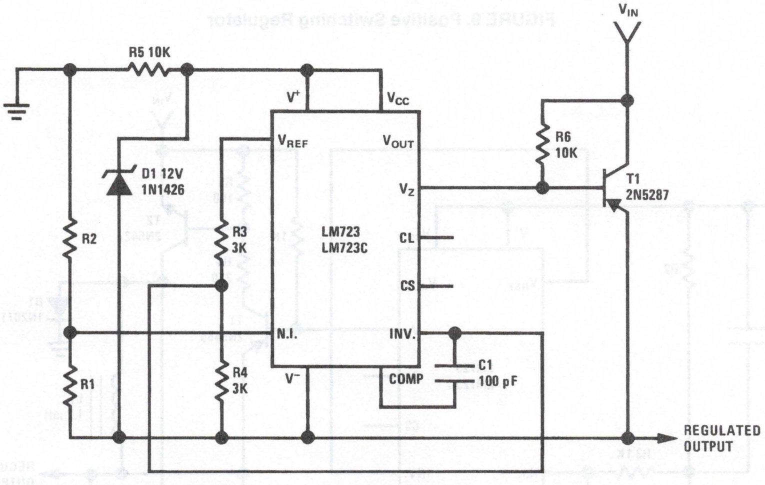

V_IN
R5 200
V+
V_CC
V_REF
V_OUT
V_Z
2N3234
D1 36V
1N1364
R4
3.0K
R1
LM723
LM723C
CL
R5
1Ω
CS
N.I.
INV.
R2
R3
3.0K
V−
COMP
C1
500 pF
REGULATED
OUTPUT

TL/H/8563-14

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +50V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 15 mV |
| Load Regulation ($\Delta I_L$ = 50 mA) | 20 mV |

**FIGURE 7. Positive Floating Regulator**


V_IN
R5 10K
V+
V_CC
V_REF
V_OUT
R6
10K
V_Z
T1
2N5287
D1 12V
1N1426
R2
R3
3K
LM723
LM723C
CL
CS
N.I.
INV.
R1
R4
3K
V−
COMP
C1
100 pF
REGULATED
OUTPUT

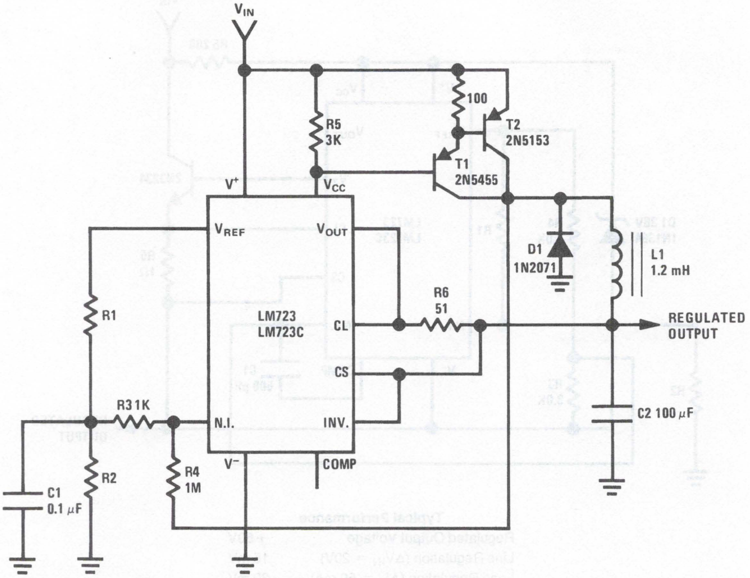
TL/H/8563-15

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | −100V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 30 mV |
| Load Regulation ($\Delta I_L$ = 100 mA) | 20 mV |

**FIGURE 8. Negative Floating Regulator**

## Typical Applications (Continued)

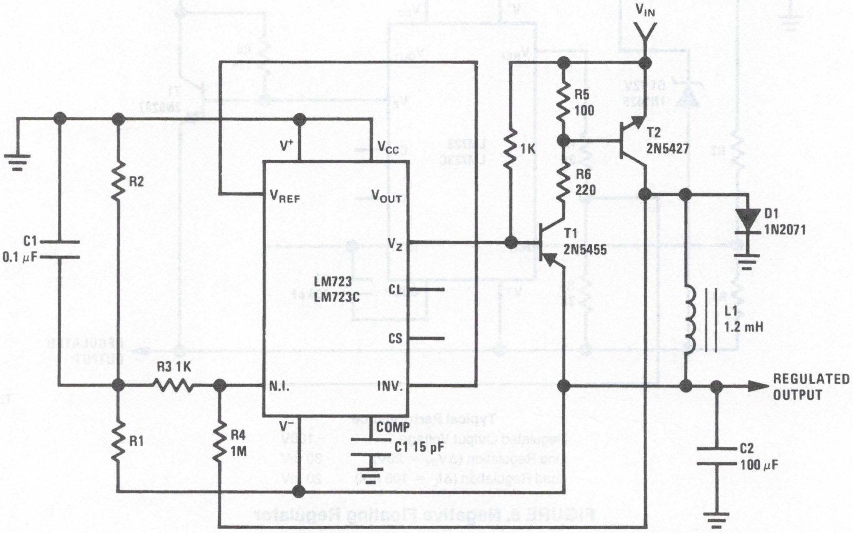

V_IN
100
T2
2N5153
R5
3K
T1
2N5455
V+
V_CC
V_REF
V_OUT
D1
1N2071
L1
1.2 mH
R1
LM723
LM723C
R6
51
CL
REGULATED OUTPUT
CS
R3 1K
N.I.
INV.
C2 100 μF
V−
COMP
R2
R4
1M
C1
0.1 μF

TL/H/8563-16

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN}$ = 30V) | 10 mV |
| Load Regulation ($\Delta I_L$ = 2A) | 80 mV |

**FIGURE 9. Positive Switching Regulator**


V_IN
R5
100
T2
2N5427
V+
V_CC
R2
1K
R6
220
V_REF
V_OUT
D1
1N2071
C1
0.1 μF
V_Z
T1
2N5455
LM723
LM723C
CL
L1
1.2 mH
CS
R3 1K
N.I.
INV.
REGULATED OUTPUT
R1
R4
1M
V−
COMP
C1 15 pF
C2
100 μF

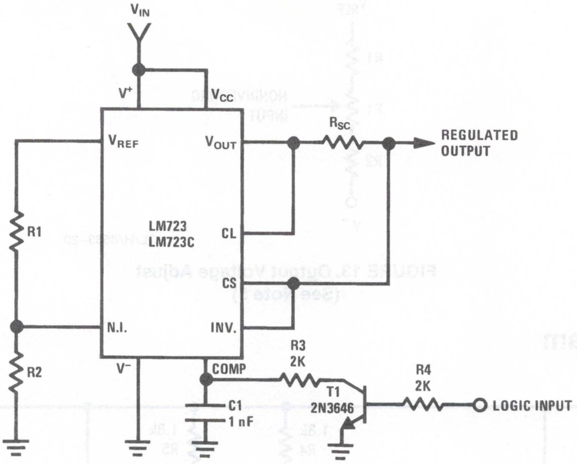
TL/H/8563-17

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | −15V |
| Line Regulation ($\Delta V_{IN}$ = 20V) | 8 mV |
| Load Regulation ($\Delta I_L$ = 2A) | 6 mV |

**FIGURE 10. Negative Switching Regulator**

## Typical Applications (Continued)


V_IN
V+
V_CC
V_REF
V_OUT
R_SC
REGULATED OUTPUT
R1
LM723
LM723C
CL
CS
N.I.
INV.
R2
V−
COMP
R3
2K
R4
2K
T1
2N3646
C1
1 nF
LOGIC INPUT

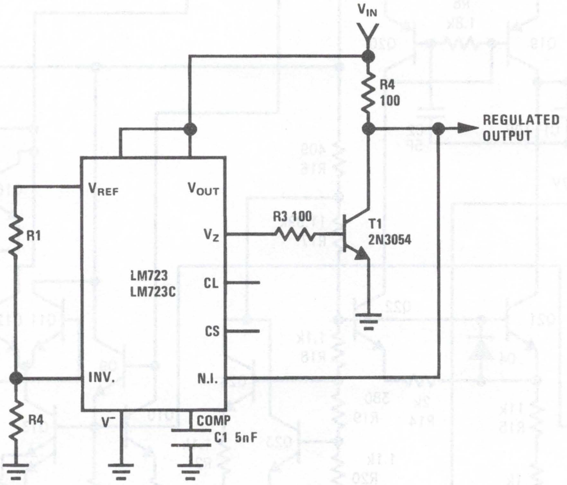
TL/H/8563-18

**Note:** Current limit transistor may be used for shutdown if current limiting is not required.

**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN} = 3V$) | 0.5 mV |
| Load Regulation ($\Delta I_L = 50$ mA) | 1.5 mV |

FIGURE 11. Remote Shutdown Regulator with Current Limiting


V_IN
R4
100
REGULATED OUTPUT
V_REF
V_OUT
R3 100
T1
2N3054
V_Z
R1
LM723
LM723C
CL
CS
INV.
N.I.
R4
V−
COMP
C1 5nF

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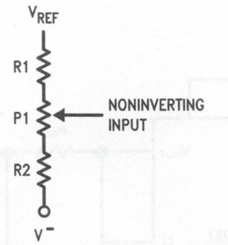
**Typical Performance**

| | |
|---|---|
| Regulated Output Voltage | +5V |
| Line Regulation ($\Delta V_{IN} = 10V$) | 0.5 mV |
| Load Regulation ($\Delta I_L = 100$ mA) | 1.5 mV |

FIGURE 12. Shunt Regulator

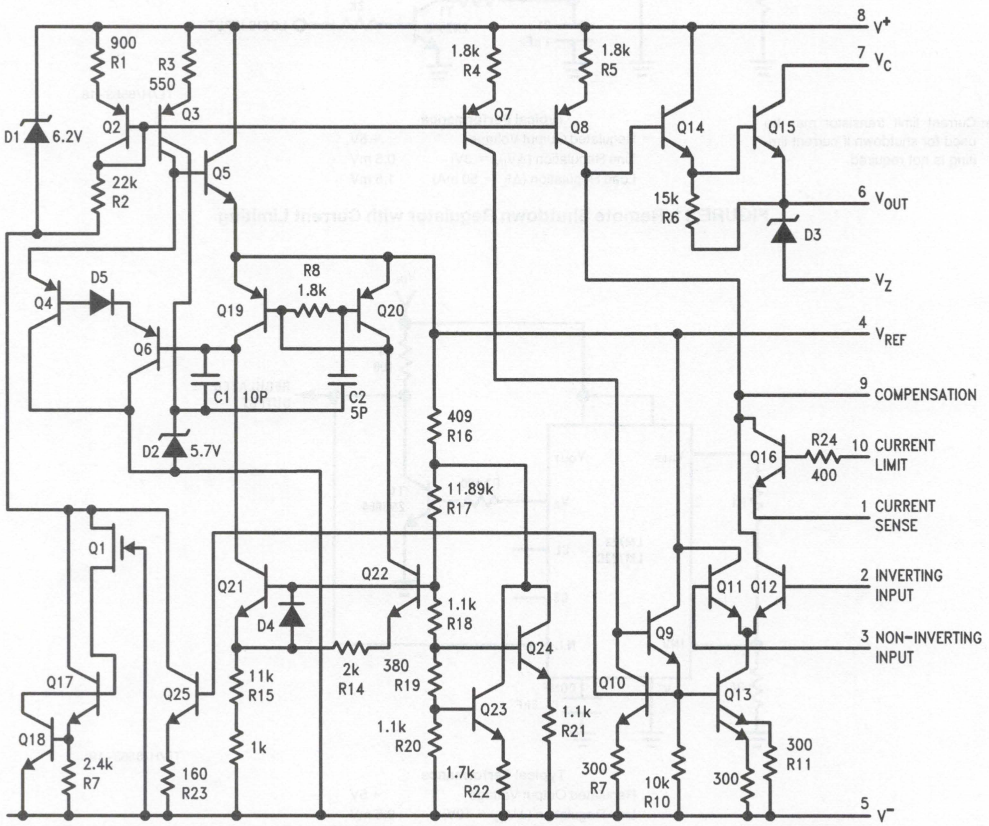
## Typical Applications (Continued)


V_REF
R1
P1
NONINVERTING INPUT
R2
V⁻

TL/H/8563-20

**FIGURE 13. Output Voltage Adjust (See Note 5)**

## Schematic Diagram


8 V⁺
7 V_C
6 V_OUT
V_Z
4 V_REF
9 COMPENSATION
10 CURRENT LIMIT
1 CURRENT SENSE
2 INVERTING INPUT
3 NON-INVERTING INPUT
5 V⁻
900 R1
R3 550
22k R2
D1 6.2V
Q1
Q2
Q3
Q4
Q5
Q6
D5
R8 1.8k
Q19
Q20
C1 10P
C2 5P
D2 5.7V
1.8k R4
1.8k R5
Q7
Q8
Q14
Q15
15k R6
D3
409 R16
11.89k R17
R24 400
Q16
Q11 Q12
Q9
Q10
Q13
Q21
Q22
D4
1.1k R18
2k R14
380 R19
1.1k R20
Q24
Q23
1.1k R21
1.7k R22
300 R7
10k R10
300
300 R11
Q17
Q18
2.4k R7
Q25
160 R23
11k R15
1k

TL/H/8563-1

**National Semiconductor Corporation**

**PRELIMINARY**

# LM1578/LM2578/LM3578 Switching Regulator

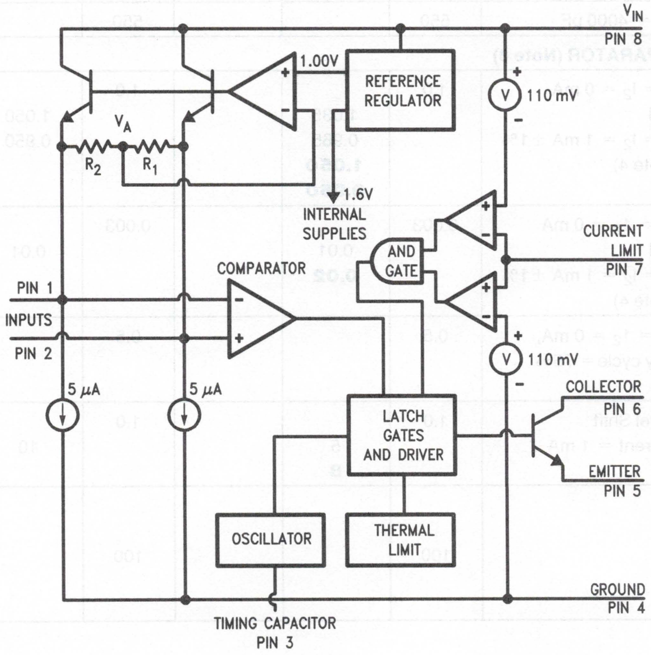
## General Description

The LM1578 is a flexible 8-pin switching regulator which can easily be set up for such dc-to-dc voltage conversion circuits as the buck, boost, and inverting configurations. The LM1578 features a unique comparator input stage which not only has separate pin-outs for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. The current limit terminal may be referenced to either the ground or the $V_{in}$ terminal, depending upon the application. In addition, the LM1578 has an on-board oscillator, which is set by a single external capacitor.

## Features

- Inverting and non-inverting inputs
- 1.0V reference at inputs
- Operates from supply voltages of 2V to 40V
- Output current up to 750 mA, saturation less than 1V
- Oscillator frequency adjustable to 100 kHz
- Current limit and thermal shut down
- Duty cycle up to 90%
- Design flexibility including buck, boost, inverting, and transformer configurations

## Functional Diagram


V_IN
PIN 8
1.00V
REFERENCE REGULATOR
V
110 mV
V_A
R_2
R_1
1.6V
INTERNAL SUPPLIES
CURRENT LIMIT
PIN 7
AND GATE
COMPARATOR
PIN 1
INPUTS
PIN 2
V
110 mV
5 μA
5 μA
COLLECTOR
PIN 6
LATCH GATES AND DRIVER
EMITTER
PIN 5
OSCILLATOR
THERMAL LIMIT
GROUND
PIN 4
TIMING CAPACITOR
PIN 3

TL/H/8711–1

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Total Supply Voltage | 40V |
| Collector Output to Ground | −0.3V to +40V |
| Emitter Output to Ground | −1V to +40V |
| Power Dissipation (Note 2) | internally limited |
| Output Current | 750 mA |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (soldering, 10 seconds) | 300°C |
| Operating Temperature Range | |
| LM1578 | −55°C to +125°C |
| LM2578 | −40°C to +85°C |
| LM3578 | 0°C to +70°C |
| Maximum Junction Temperature | 150°C |

ESD rating is to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM1578 Typ | LM1578 Tested (Note 5) | LM1578 Design (Note 6) | LM2578/LM3578 Typ | LM2578/LM3578 Tested (Note 5) | LM2578/LM3578 Design (Note 6) | Units/ Limit |
|---|---|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | | | |
| Frequency | $C_T$ = 4000 pF | 20 | 22.4<br>17.6 | | 20 | 25<br>15 | | kHz<br>kHz max<br>kHz min |
| Frequency Drift with Temperature | $C_T$ = 4000 pF | −0.13 | | **−0.25** | −0.13 | | **−0.30** | %/°C<br>%/°C max |
| Amplitude | $C_T$ = 4000 pF | 550 | | | 550 | | | mVpk-pk |
| **REFERENCE/COMPARATOR (Note 8)** | | | | | | | | |
| Input Reference Voltage | $I_1 = I_2 = 0$ mA and $I_1 = I_2 = 1$ mA ±1% (Note 4) | 1.0 | 1.035<br>0.965<br>**1.050**<br>**0.950** | | 1.0 | 1.050<br>0.950 | **1.070**<br>**0.930** | V<br>V max<br>V min<br>V max<br>V min |
| Input Reference Voltage Line Regulation | $I_1 = I_2 = 0$ mA and $I_1 = I_2 = 1$ mA ±1% (Note 4) | 0.003 | 0.01<br>**0.02** | | 0.003 | 0.01 | **0.02** | %/V<br>%/V max<br>%/V max |
| Inverting Input Current | $I_1 = I_2 = 0$ mA, duty cycle = 75% | 0.5 | | | 0.5 | | | μA |
| Level Shift Accuracy | Level Shift Current = 1 mA | 1.0 | 5<br>**8** | | 1.0 | 10 | **13** | %<br>% max<br>% max |
| Input Reference Voltage Long Term Stability | | 100 | | | 100 | | | ppm/kHr |

## Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM1578 Typ | LM1578 Tested (Note 5) | LM1578 Design (Note 6) | LM2578/LM3578 Typ | LM2578/LM3578 Tested (Note 5) | LM2578/LM3578 Design (Note 6) | Units/Limit |
|---|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | | |
| Collector Saturation Voltage | $I_c$ = 750 mA, Emitter Grounded | 0.7 | | | 0.7 | | | V |
| | | | 0.85 | | | 0.90 | | V max |
| | | | **1.2** | | | | **1.2** | V max |
| Emitter Saturation Voltage | $I_e$ = 80 mA, Collector at $V_{in}$ = 40V | 1.4 | | | 1.4 | | | V |
| | | | 1.6 | | | 1.7 | | V max |
| | | | **2.1** | | | | **2.0** | V max |
| Collector Leakage Current | Collector to Emitter = 40V, Emitter Grounded, Output off | 0.1 | | | 0.1 | | | μA |
| | | | 50 | | | 200 | | μA max |
| | | | **100** | | | | **250** | μA max |
| Collector-Emitter Sustaining Voltage | | 40 | | | 40 | | | V |
| | | | | 34 | | | 34 | V min |
| **CURRENT LIMIT** | | | | | | | | |
| Sense Voltage for Shutdown | Referred to $V_{in}$ or Ground (Note 7) | 110 | | | 110 | | | mV |
| | | | 95 | | | 80 | | mV min |
| | | | **140** | | | 160 | | mV max |
| Sense Voltage Temperature Drift | | 0.3 | | | 0.3 | | | %/°C |
| Sense Current | Referred to $V_{in}$ | 40 | | | 40 | | | μA |
| | Referred to Ground | 0.4 | | | 0.4 | | | μA |
| **DEVICE POWER CONSUMPTION** | | | | | | | | |
| Supply Current | Output Off | 2.0 | | | 2.0 | | | mA |
| | | | 3.0 | | | 3.5 | | mA max |
| | | | **3.3** | | | | **4.0** | mA max |
| | Output On, $I_c$ = 750 mA | 14 | | | 14 | | | mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions.

**Note 2:** At elevated temperatures, devices must be derated based on package thermal resistance. The device in a TO-5 package must be derated at 150°C/W, junction to ambient or 45°C/W, junction to case. The thermal resistance for the 8-pin N package is 130°C/W, junction to ambient.

**Note 3:** Unless otherwise specified, these specifications apply for $V_{in} = 2V$ (2.2V, $< -25°C$) and $V_{in} = 40V$. Timing Capacitor = 4000 pF with 25% and 75% duty cycle. Normal typeface indicates $T_j = 25°C$ limits. **Boldface type indicates limits for full temperature range.** This is $T_j = -55°C$ to $+150°C$ for the LM1578, $T_j = -40°C$ to $+125°C$ for the LM2578, and $T_j = 0°C$ to $+125°C$ for the LM3578.

**Note 4:** $I_1$ and $I_2$ are the external sink currents at the inputs.

**Note 5:** Guaranteed and 100% production tested.

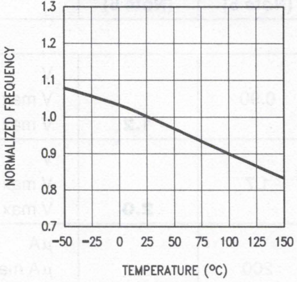
**Note 6:** Guaranteed (but not 100% production tested) over the operating temperature ranges. These limits are not to be used to calculate outgoing quality levels.

**Note 7:** Connection of a 10 kΩ resistor from pin 1 to pin 4 establishes the duty cycle at its maximum of 90% with a maximum voltage swing on the output collector of 40V. Applying the minimum current sense voltage will not reduce the duty cycle to less than 50%. Applying the maximum current limit sense voltage is certain to reduce the duty cycle below 50%. An additional 15 mV above the sense voltage may be required to reduce the duty cycle to 0% (see current limit of the typical performance characteristics).

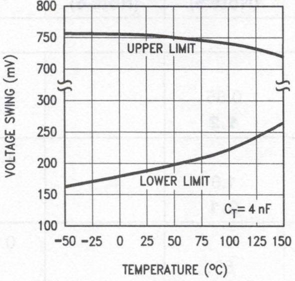
**Note 8:** Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage is applied, excessive current will flow and should be limited to less than 5 mA.

## Typical Performance Characteristics

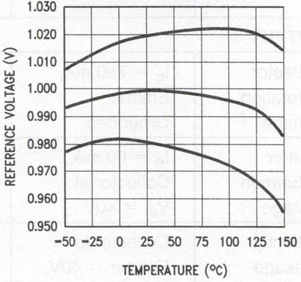
**Oscillator Frequency Change With Temperature**



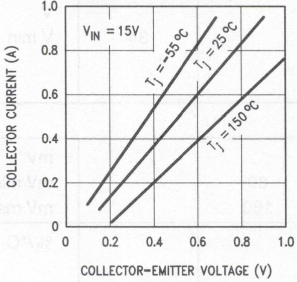
**Oscillator Voltage Swing**



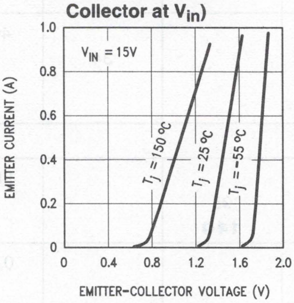
**Input Reference Voltage Drift with Temperature**



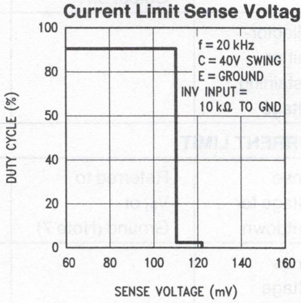
**Collector Saturation Voltage (Sinking Current, Emitter Grounded)**



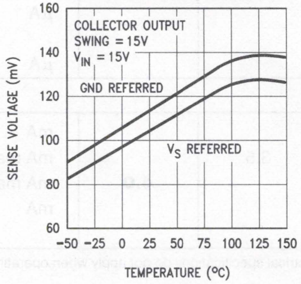
**Emitter Saturation Voltage (Sourcing Current, Collector at $V_{in}$)**



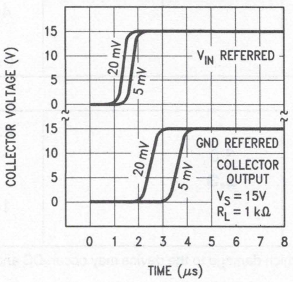
**Ground Referred Current Limit Sense Voltage**



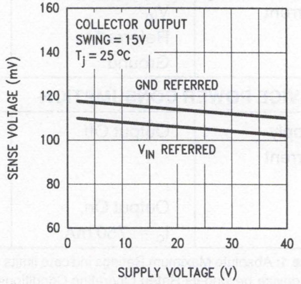
**Current Limit Sense Voltage Drift with Temperature**



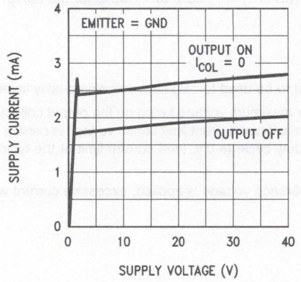
**Current Limit Response Time For Various Over Drives**



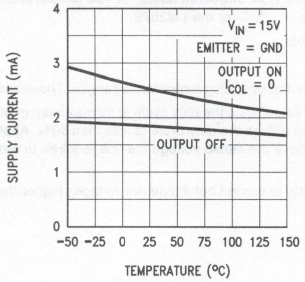
**Current Limit Sense Voltage vs. Supply Voltage**



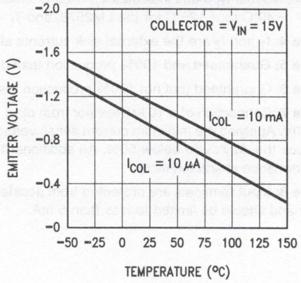
**Supply Current**



**Supply Current**



**Collector Current With Emitter Output Below Ground**



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## Test Circuit*

Parameter tests can be made using the test circuit shown. Select the desired $V_{in}$, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference Voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = $(T_{P3}(V)/1V) \times 100\%$; S1 at $I_1 = I_2 = 1$ mA

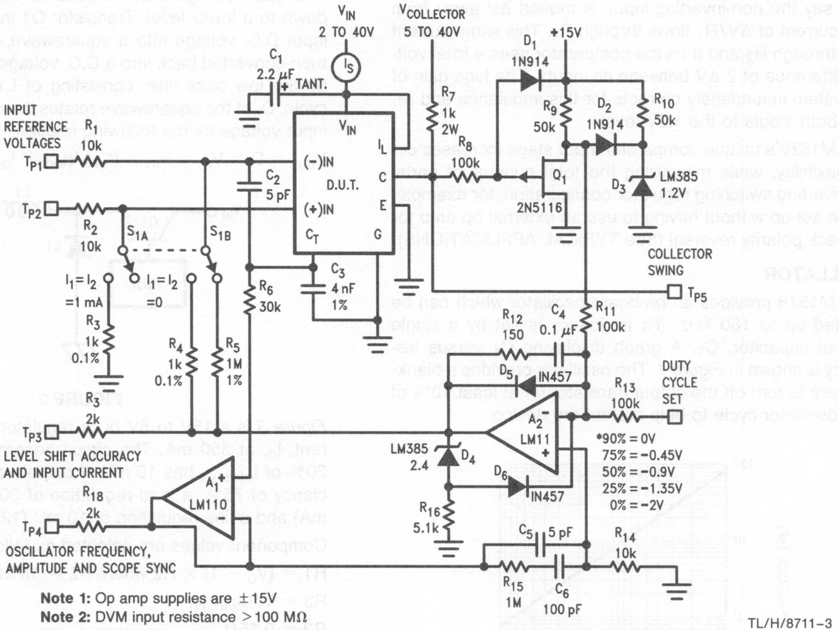
Input Current (mA) = $(1V - T_{P3}(V))/1$ MΩ: S1 at $I_1 = I_2 = 0$ mA.

Oscillator $T_{P4}$ can be measured using a frequency counter or an oscilloscope.

The current limit sense voltage is measured by connecting an adjustable 0 to 1V floating power supply in series with the current limit terminal and referring it to either the ground or the $V_{in}$ terminal. Set the duty cycle to 90% and monitor test point $T_{P5}$ while adjusting the floating power supply voltage until the LM1578's duty cycle just reaches 0%. This voltage is the current limit sense voltage.

The supply current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

*LM1578 specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.


V_IN
2 TO 40V
V_COLLECTOR
5 TO 40V
+15V
C1
2.2 µF
+ TANT.
I_S
D1
1N914
R7
1k
2W
R9
50k
D2
1N914
R10
50k
INPUT
REFERENCE
VOLTAGES
R1
10k
T_P1
V_IN
I_L
R8
100k
(−)IN
C
Q
LM385
1.2V
D3
C2
5 pF
D.U.T.
E
2N5116
T_P2
(+)IN
R2
10k
S1A
S1B
C_T
G
COLLECTOR
SWING
T_P5
I1 = I2
=1 mA
I1 = I2
=0
C3
4 nF
1%
R6
30k
R11
100k
R12
150
C4
0.1 µF
R3
1k
0.1%
R4
1k
0.1%
R5
1M
1%
D5
IN457
DUTY
CYCLE
SET
R13
100k
R3
2k
T_P3
A2
LM11
*90% = 0V
75% = −0.45V
50% = −0.9V
25% = −1.35V
0% = −2V
LM385
2.4
D4
D6
IN457
LEVEL SHIFT ACCURACY
AND INPUT CURRENT
A1
LM110
R18
2k
T_P4
R16
5.1k
C5
5 pF
R14
10k
OSCILLATOR FREQUENCY,
AMPLITUDE AND SCOPE SYNC
R15
1M
C6
100 pF

**Note 1:** Op amp supplies are ±15V

**Note 2:** DVM input resistance >100 MΩ

**Note 3:** *LM1578 max duty cycle is 90%

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## Definition of Terms

**Input Reference Voltage:** The reference voltage referred to ground, applied to either the inverting or non-inverting inputs, which will cause the output to switch on or off.

**Input Reference Current:** The current applied to either the inverting or the non-inverting input which will cause the output to switch on or off.

**Input Level Shift Accuracy:** For two equal resistors sinking current from the inverting and non-inverting input terminals, the input level shift accuracy is the ratio of the voltage across the resistors to produce a given duty cycle at the output.

**Collector Saturation Voltage:** With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's emitter connected to ground, the collector saturation voltage is the collector-to-emitter voltage for a given collector current.

**Emitter Saturation Voltage:** With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's collector connected to $V_{in}$, the emitter saturation voltage is the collector-to-emitter voltage for a given emitter current.

**Current Limit Sense Voltage:** The voltage referred to either the supply or the ground terminal which will cause the output transistor to turn off and resets cycle-by-cycle at the oscillator frequency.

**Current Limit Sense Current:** The bias current for the current limit terminal at sense voltage.

**Supply Current:** The IC power supply current, excluding the output transistor's collector current, with the oscillator operating.

## Functional Description

The LM1578 is a very simple device. A control signal is fedback to the LM1578's comparator section for output error detection. The comparator and oscillator feed their respective signals to a logic network for determining when the output transistor is to be turned on and off. The following is a brief description of the various stages of the LM1578.

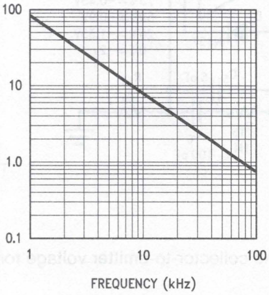
### COMPARATOR INPUT STAGE

The LM1578 has a unique comparator input stage-not only are both the inverting and non-inverting inputs available to the user, but both are referenced to a 1.0V reference This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both inputs are floating, no current flows through either $R_1$ or $R_2$, and thus, both inputs to the comparator are at the same potential as $V_a$, i.e. 1.0V. When one input, say the non-inverting input, is moved $\Delta V$ away from $V_a$, a current of $\Delta V/R_1$ flows through $R_1$. This same current flows through $R_2$ and thus the comparator sees a total voltage difference of 2 $\Delta V$ between its inputs. The high gain of the system immediately corrects for this imbalance and returns both inputs to the 1.0V level

The LM1578's unique comparator input stage increases circuit flexibility, while minimizing the total number of parts. The inverting switching regulator configuration, for example, can be set-up without having to use an external op amp for feedback polarity reversal (See TYPICAL APPLICATIONS).

### OSCILLATOR

The LM1578 provides an on-board oscillator which can be adjusted up to 100 kHz. It's frequency is set by a single external capacitor, $C_1$. A graph displaying $C_1$ versus frequency is shown in *Figure 1*. The oscillator provides a blanking pulse to turn off the output transistor for at least 10% of each oscillator cycle to help protect the device.



TL/H/8711–4

**FIGURE 1**

### OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 750 mA of current with a saturation voltage of less than 1.2V. The collector and emitter are both available as shown in the functional diagram.

### CURRENT LIMIT

The LM1578's current limit is novel in that it may be referenced to either the ground or the $V_{in}$ terminal, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage, V, 110 mV below $V_{in}$, the other with its inverting input referenced 110 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 110 mV away from either $V_{in}$ or ground.

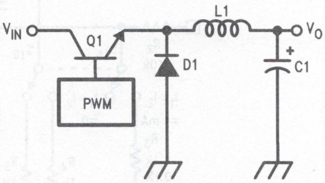
## Typical Applications

The LM1578 may be operated in either the continuous or the discontinuous conduction mode. The following applications (except for the Buck-Boost Regulator) are designed for continous conduction operation. That is, the inductor current is not allowed to fall to zero. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

### BUCK REGULATOR

The buck configuration is used to step an input voltage down to a lower level. Transistor Q1 in *Figure 2* chops the input D.C. voltage into a squarewave. This squarewave is then converted back into a D.C. voltage of lower magnitude by the low pass filter consisting of L1 and C1. The duty cycle, D, of the squarewave relates the output voltage to the input voltage by the following relation:

$V_{out} = D \times V_{in} = V_{in} \times (t_{on})/(t_{on} + t_{off})$.



TL/H/8711–5

**FIGURE 2**

*Figure 3* is a 15V to 5V buck regulator with an output current, $I_o$, of 350 mA. The circuit becomes discontinuous at 20% of $I_{o(max)}$, has 10 mV of output voltage ripple, an efficiency of 75%, a load regulation of 30 mV (70 mA to 350 mA) and a line regulation of 10 mV ($12 \leq V_{in} \leq 18V$).

Component values are selected as follows:

$R1 = (V_o - 1) \times R2$ where $R2 = 10\ k\Omega$

$R3 = V/I_{sw(max)}$

$R3 = 0.15\Omega$

where:

V is the current limit sense voltage, 0.11V

$I_{sw(max)}$ is the maximum allowable current thru the output transistor.

L1 is the inductor and may be found from the inductance calculation chart, as follows.

Given $V_{in} = 15V$ $\quad V_o = 5V$

$I_{o(max)} = 350$ mA $\quad f_{osc} = 50$ kHz

Discontinuous at 20% of $I_{o(max)}$.

Note that since the circuit will become discontinuous at 20% of $I_{o(max)}$, the load current must not be allowed to fall below 70 mA.

**Step 1:** Calculate the maximum D.C. current through the inductor, $I_{IND(max)}$. The necessary equations are indicated at the top of the chart and show that $I_{IND(max)} = I_{o(max)}$ for the buck configuration. Thus, $I_{IND(max)} = 350$ mA.

## Typical Applications (Continued)

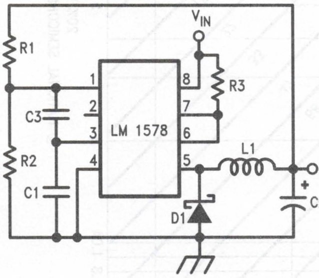
**Step 2:** Calculate the inductor Volts-sec product, $E\text{-}T_{op}$, according to the equations given from the chart. For the Buck;

$E\text{-}T_{op} = (V_{in} - V_o)\,(V_o/V_{in})\,(1000/f_{osc})$

$= (15 - 5)\,(5/15)\,(1000/50)$

$= 100V - \mu s.$

with the oscillator frequency, $f_{osc}$, expressed in kHz.



$V_{in} = 15V$
$V_o = 5V$
$V_{ripple} = 50\ mV$
$I_o = 350\ mA$
$f_{osc} = 50\ kHz$
$R1 = 40\ k\Omega$
$R2 = 10\ k\Omega$
$R3 = 0.15\Omega$
$C1 = 1820\ pF$
$C2 = 220\ \mu F$
$C3 = 20\ pF$
$L1 = 470\ \mu H$
$D1 = 1N5818$

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**FIGURE 3. Buck or Step-Down Regulator**

**Step 3:** Using the graph with axis labeled "Discontinuous At % $I_o$" and "$I_{IND(max,\ DC)}$" find the point where the desired maximum inductor current, $I_{IND(max,\ DC)}$ intercepts the desired discontinuity percentage.

In this example, the point of interest is where the 0.35A line intersects with the 20% line. This is nearly the midpoint of the horizontal axis.

**Step 4:** This last step is merely the translation of the point found in Step 3 to the graph directly below it. This is accomplished by moving straight down the page to the point which intercepts the desired $E\text{-}T_{op}$. For this example, $E\text{-}T_{op}$ is 66V-µs and the desired inductor value is 470 µH. Since this example was for 20% discontinuity, the bottom chart could have been used directly, as noted in step 3 of the chart instructions.

For a full line of standard inductor values, contact Pulse Engineering (San Diego, Calif.) regarding their PE526XX series, or A. I. E. Magnetics (Nashville, Tenn.).

A more precise inductance value may be calculated for the Buck, Boost and Inverting Regulators as follows:

**BUCK**

$L = V_o\,(V_{in} - V_o)/(\Delta I_o\ V_{in}\ f_{osc})$

**BOOST**

$L = V_{in}^2\,(V_o - V_{in})/(\Delta I_o\ f_{osc}\ V_o^2)$

**INVERT**

$L = V_{in}^2\,|V_o|/[\Delta I_o(V_{in} + |V_o|)^2 f_{osc}]$

where:

$\Delta I_o = 2I_o \times$ (Discontinuity Factor). The Discontinuity Factor is the percent discontinuity of $I_o$ expressed as a decimal (i.e.; for 10% discontinuity, the discontinuity factor is 0.1).

C1 is the frequency selection capacitor found in *Figure 1.*

$C2 \geq V_o\,(V_{in} - V_o)/(8f_{osc}{}^2V_{in}V_{ripple}L1)$

where $V_{ripple}$ is the peak-to-peak output voltage ripple.

C3 is necessary for continuous operation and is generally in the 10 to 30 pF range.

D1 should be a Schottky type diode, such as the 1N5818 or 1N5819.

**BUCK WITH BOOSTED OUTPUT CURRENT**

For applications requiring a large output current, an external transistor may be used as shown in *Figure 4.* This circuit steps a 15V supply down to 5V with 1.5A of output current. The output ripple is 50 mV, with an efficiency of 80%, a load regulation of 40 mV (150 mA to 1.5A), and a line regulation of 20 mV ($12V \leq V_{in} \leq 18V$).

Component values are selected as outlined for the buck regulator with a discontinuity factor of 10%, with the addition of R4 and R5:

$R4 = 10V_{BE1}B_f/I_p$

$R5 = (V_{in} - V - V_{BE1} - V_{sat})\ B_f/(I_{IND(max,\ DC)} + I_{R4})$

where:

$V_{BE1}$ is the $V_{BE}$ of transistor Q1.

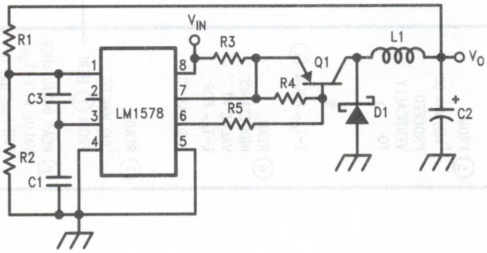
$V_{sat}$ is the saturation voltage of the LM1578 output transistor.

V is the current limit sense voltage.

$B_f$ is the forced current gain of transistor Q1 ($B_f = 30$ for *Figure 4*).

$I_{R4} = V_{BE1}/R4$

$I_p = I_{IND(max,\ DC)} + 0.5\Delta I_o$



$V_{in} = 15V$
$V_o = 5V$
$V_{ripple} = 50\ mV$
$I_o = 1.5A$
$f_{osc} = 50\ kHz$
$R1 = 40\ k\Omega$
$R2 = 10\ k\Omega$
$R3 = 0.05\Omega$

$R4 = 200\Omega$
$R5 = 330\Omega$
$C1 = 1820\ pF$
$C2 = 330\ \mu F$
$C3 = 20\ pF$
$L1 = 220\ \mu H$
$D1 = 1N5819$
$Q1 = D45$

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**FIGURE 4. Buck Converter with Boosted Output Current**

## Typical Applications (Continued)

**DC/DC CONVERTER INDUCTANCE CALCULATOR**

HOW TO USE THIS CHART

① CALCULATE $I_{IND, MAX DC}$ HERE →

② CALCULATE $E\text{-}T_{OP}$ HERE →

③ ENTER REQUIRED % DISCONTINUITY HERE → IF "20%" PROCEED TO ⑦

④ PROCEED → HORIZONTALLY TO $I_{IND, MAX DC}$ FROM ①

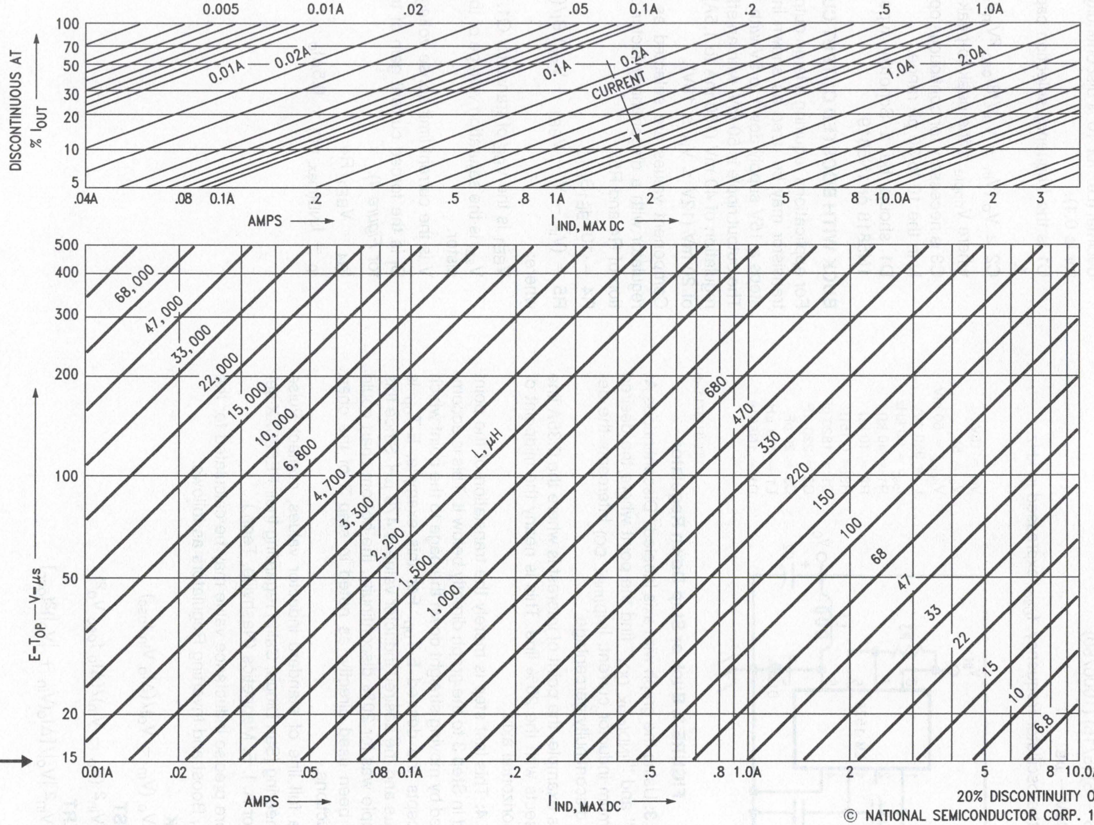
⑤ FROM $I_{IND, MAX DC}$ PROCEED VERTICALLY TO ↓ $E\text{-}T_{OP}$ FROM ②

⑥ READ INDUCTANCE VALUE AT $E\text{-}T_{OP}$ FOR $I_{IND, MAX DC}$

⑦ READ $I_{IND, MAX DC}$ FROM ① HERE →

⑧ READ INDUCTANCE VALUE AT $E\text{-}T_{OP}$ FOR $I_{IND, MAX DC}$

| BUCK | BOOST | INVERT | |
|---|---|---|---|
| $I_{IND} = I_{LOAD}$ | $I_{IND} = I_{LOAD} \cdot \frac{V_O}{V_{IN}}$ | $I_{IND} = I_{LOAD} \cdot \frac{V_{IN} + \lvert V_O \rvert}{V_{IN}}$ | $I_{IND}$ |
| $(V_{IN} - V_O) \cdot \frac{V_O}{V_{IN}} \cdot \frac{1000}{F, kHz}$ | $(V_O - V_{IN}) \cdot \frac{V_{IN}}{V_O} \cdot \frac{1000}{F, kHz}$ | $V_{IN} \cdot \frac{\lvert V_O \rvert}{V_{IN} + \lvert V_O \rvert} \cdot \frac{1000}{F, kHz}$ | $E\text{-}T_{OP}$ |



20% DISCONTINUITY ONLY

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## Typical Applications (Continued)

### BOOST REGULATOR

The boost regulator converts a low input voltage into a higher output voltage. The basic configuration is shown in *Figure 5.* Energy is stored in the inductor while the transistor is on and then transferred with the input voltage to the output capacitor for filtering when the transistor is off. Thus, $V_o = V_{in} + V_{in}(t_{on}/t_{off})$.

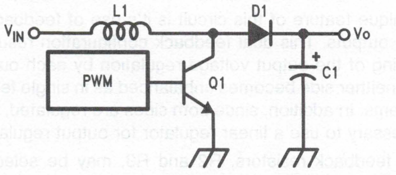

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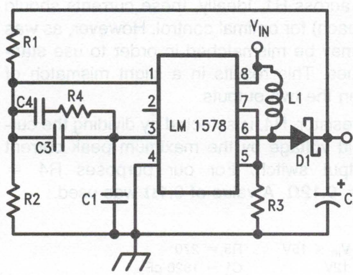
**FIGURE 5**

The circuit of *Figure 6* converts a 5V supply into a 15V supply with 150 mA of output current, a load regulation of 14 mV (30 mA to 150 mA), and a line regulation of 35 mV (4.5V ≤ $V_{in}$ ≤ 8.5V).



$V_{in} = 5V$
$V_o = 15V$
$V_{ripple} = 10\ mV$
$I_o = 150\ mA$
$f_{osc} = 50\ kHz$
R1 = 140 kΩ
R2 = 10 kΩ
R3 = 0.1 Ω
R4 = 220 kΩ
C1 = 1820 pF
C2 = 470 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 330 μH
D1 = 1N5818

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**FIGURE 6. Boost or Step-Up Regulator**

$R1 = (V_o - 1)\ R2$ where R2 = 10 kΩ.

$R3 = V/(I_{IND(max,\ DC)} + 0.5\ \Delta I_o)$

where:

$\Delta I_o$ is defined in the "Buck Regulator" section.

R4, C3 and C4 are necessary for continuous operation and are typically 220 kΩ, 20 pF, and 0.0022 μF respectively.

C1 is the oscillator frequency selection capacitor found in *Figure 1*.

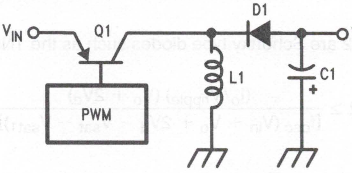
$C2 \geq I_o\ (V_o - V_{in})/(f_{osc}\ V_o\ V_{ripple})$.

D1 is a Schottky type diode such as a IN5818 or IN5819.

L1 is found as described in the buck converter section.

### INVERTING REGULATOR

*Figure 7* shows the basic configuration for an inverting regulator. The input voltage is of a positive polarity, but the output is negative. The output may be less than, equal to, or greater in magnitude than the input. The relationship between the magnitude of the input voltage and the output voltage is $V_o = V_{in} \times (t_{on}/t_{off})$.



TL/H/8711-10

**FIGURE 7.**

*Figure 8* shows an LM1578 configured as a 5V to −15V polarity inverter with an output current of 300 mA, a load regulation of 44 mV (60 mA to 300 mA) and a line regulation of 50 mV (4.5V ≤ $V_{in}$ ≤ 8.5V).

$$R1 = (|V_o| + 1)\ R2 \text{ where } R2 = 10\ k\Omega.$$

$$R3 = V/(I_{IND(max,\ DC)} + 0.5\ \Delta I_o).$$

$$R4 = 10 V_{BE1} B_f/(I_{IND\ (max,\ DC)} + 0.5\ \Delta I_o)$$

where:

V, $V_{BE1}$, $V_{sat}$, and $B_f$ are defined in the "Buck Converter with Boosted Output Current" section.

$\Delta I_o$ is defined in the "Buck Regulator" section.

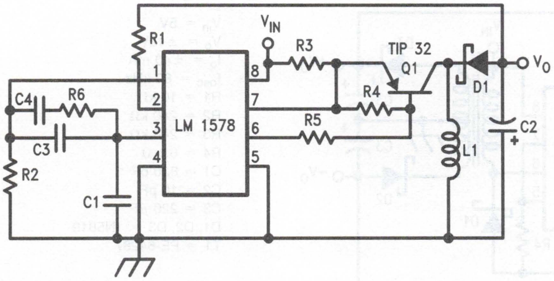
R5 is defined in the "Buck with Boosted Output Current" section.

R6 serves the same purpose as R4 in the Boost Regulator circuit and is typically 220 kΩ.

C1, C3 and C4 are defined in the "Boost Regulator" section.

$$C2 \geq I_o\ |V_o|/[f_{osc}(|V_o| + V_{in})\ V_{ripple}]$$

L1 is found as outlined in the section on buck converters, using the inductance chart for the invert configuration and 20% discontinuity.



$V_{in} = 5V$
$V_o = -15V$
$V_{ripple} = 5\ mV$
$I_o = 300\ mA$, $I_{min} = 60\ mA$
$f_{osc} = 50\ kHz$
R1 = 160 kΩ R2 = 10 kΩ
R3 = 0.01 Ω R4 = 190Ω
R5 = 82Ω R6 = 220 kΩ
C1 = 1820 pF
C2 = 1000 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 150 μH
D1 = 1N5818

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**FIGURE 8. Inverting Regulator**

## Typical Applications (Continued)

### BUCK-BOOST REGULATOR

The Buck-Boost Regulator, shown in *Figure 9*, may step a voltage up or down, depending upon whether or not the desired output voltage is greater or less than the input voltage. In this case, the output voltage is 12V with an input voltage from 9V to 15V. The circuit exhibits an efficiency of 75%, with a load regulation of 60 mV (10 mA to 100 mA) and a line regulation of 52 mV.

$R1 = (V_o - 1)\, R2$ where $R2 = 10\ k\Omega$

$R3 = V/0.75A$

R4, C1, C3 and C4 are defined in the "Boost Regulator" section.

D1 and D2 are Schottky type diodes such as the 1N5818 or 1N5819.

$$C2 \geq \frac{(I_o/V_{ripple})\,(V_o + 2V_d)}{[f_{osc}\,(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})]}$$

where:

$V_d$ is the forward voltage drop of the diodes.

$V_{sat}$ is the saturation voltage of the LM1578 output transistor.

$V_{sat1}$ is the saturation voltage of transistor Q1.

$$L1 \geq (V_{in} - V_{sat} - V_{sat1})\,(t_{on}/I_p)$$

where:

$$t_{on} = \frac{(1/f_{osc})\,(V_o + 2V_d)}{(V_o + V_{in} + 2V_d - V_{sat} - V_{sat1})}$$

$$I_P = \frac{2I_o\,(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})}{(V_{in} - V_{sat} - V_{sat1})}$$

### RS-232 LINE DRIVER POWER SUPPLY

The power supply, shown in *Figure 10*, operates from an input voltage as low as 4.2V (5V nominal), and delivers an output of ±12V at ±40 mA with better than 70% efficiency. The circuit provides a load regulation of ±150 mV (from 10% to 100% of full load) and a line regulation of ±10 mV. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this circuit is it's use of feedback from both outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that neither side becomes unbalanced as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

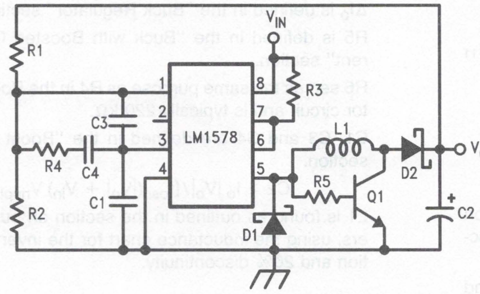
The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_O - 1V)/45.8\ \mu A = 240\ k\Omega$

$R3 = (|V_O| + 1V)/54.2\ \mu A = 240\ k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 μA to 60 μA, as long as their sum is equal to the 100 μA necessary to establish the 1V threshold across R1. Ideally, these currents should be equal (50 μA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage by the maximum peak current level in the output switch. For our purposes R4 = 90 mV/750 mA = 0.12Ω. A value of 0.1Ω was used.



$9V \leq V_{in} \leq 15V$
$V_o = 12V$
$I_o = 100\ mA$
$V_{ripple} = 50\ mV$
$f_{osc} = 50\ kHz$
R1 = 110 k
R2 = 10 k
R3 = 0.1
R4 = 220 k
R5 = 270
C1 = 1820 pF
C2 = 220 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 220 μH
D1, D2 = 1N5819
Q1 = D44

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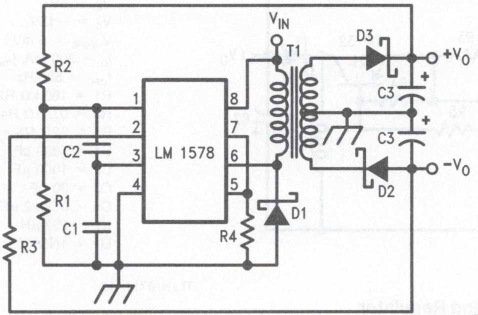
**FIGURE 9. Buck-Boost Regulator**



$V_{in} = 5V$
$V_o = \pm 12V$
$I_o = \pm 40\ mA$
$f_{osc} = 80\ kHz$
R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1 Ω
C1 = 820 pF
C2 = 10 pF
C3 = 220 μF
D1, D2, D3 = 1N5819
T1 = PE-64287

TL/H/8711–14

**FIGURE 10. RS-232 Line Driver Power Supply**

## Typical Applications (Continued)

Capacitor C1 sets the oscillator frequency and is selected from *Figure 1*.

Capacitor C2 serves as a compensation capacitor for synchronous operation and a value of 10 to 50 pF should be sufficient for most applications.

A minimum value for an ideal output capacitor C3, could be calculated as $C = I \times t/\Delta V$ where I is the load current, t is the transistor on time (typically $0.4/f_{OSC}$), and $\Delta V$ is the peak-to-peak output voltage ripple. A larger output capacitor than this theoretical value should be used since electrolytics have poor high frequency performance. Experience has shown that a value from 5 to 10 times the calculated value should be used.

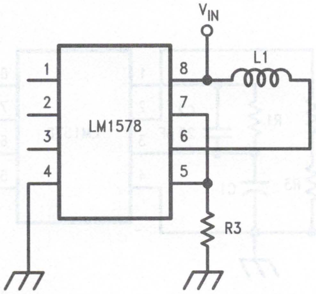
For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Transformer selection should be picked for an output transistor "on" time of $0.4/f_{OSC}$, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in *Figure 10* was a Pulse Engineering PE-64287.

### CURRENT LIMIT

As mentioned in the functional description, the current limit terminal may be referenced to either the $V_{in}$ or the ground terminal. Resistor, R3 converts the current to be sensed into a voltage for current limit detection.

**Current Limit Ground Referred**



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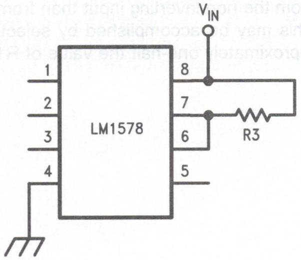
**Current Limit $V_{in}$ Referred**



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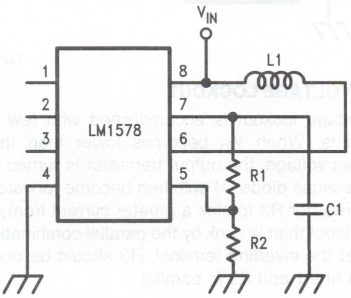
### CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, R1 and C1 act together as a low pass filter to control the current limit circuitry's response time.

Because the sense current of the current limit terminal varies according to where it is referenced, R1 should be less than 2 kΩ when referenced to ground, and less than 100 Ω when referenced to $V_{in}$.

**Current Limit Transient Suppressor Ground Referred**



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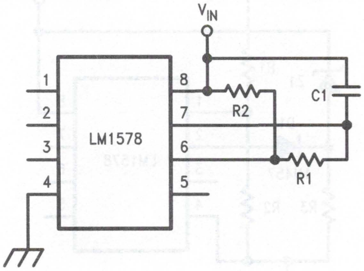
**Current Limit Transient Suppressor $V_{in}$ Referred**



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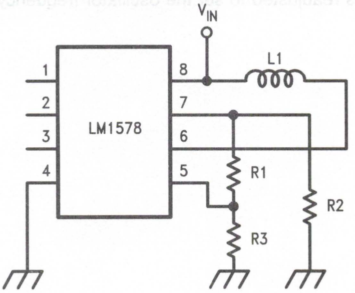
### C. L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, the voltage divider network, consisting of R1 and R2, may be used. This effectively multiplies the sense voltage by $(1 + R1/R2)$. Also, $R_1$ can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode $V_f$ + 110 mV).

**Current Limit Sense Voltage Multiplication Ground Referred**



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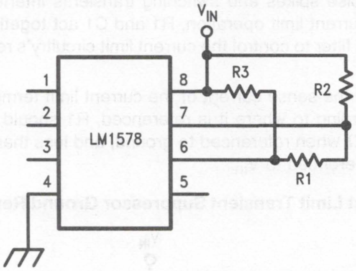
## Typical Applications (Continued)

### Current Limit Sense Voltage Multiplication $V_{in}$ Referred



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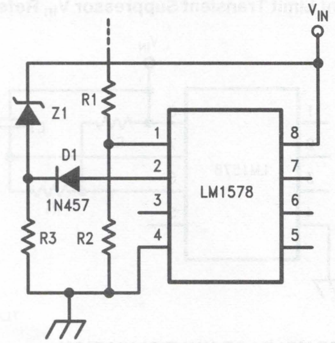
### UNDER-VOLTAGE LOCKOUT

Under-voltage lockout is accomplished with few external components. When $V_{in}$ becomes lower than the zener breakdown voltage, the output transistor is turned off. This occurs because diode D1 will then become forward biased, allowing resistor R3 to sink a greater current from the non-inverting input than is sunk by the parallel combination of R1 and R2 at the inverting terminal. R3 should be one-fifth of the value of R1 and R2 in parallel.

### Under Voltage Lockout



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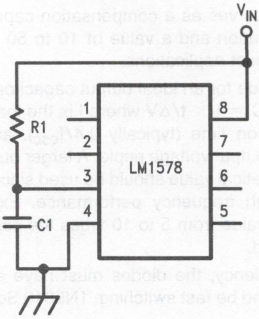
### MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge to discharge ratio of the oscillator capacitor with a single external resistor. Typical values are 50 $\mu$A for the charge current, 450 $\mu$A for the discharge current, and a voltage swing from 200 mV to 750 mV. Therefore, R1 is selected for the desired charging and discharging slopes and C1 is readjusted to set the oscillator frequency.

### Maximum Duty Cycle Limiting



TL/H/8711-21

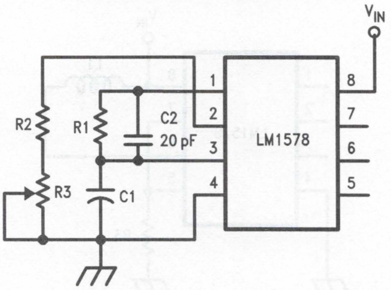
### DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the circuit shown below may be used. The output will turn on with the beginning of each oscillator cycle and turn off when the current sunk by R2 and R3 from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

R1 should be less than 500 kΩ but greater than 100 kΩ to prevent loading of the oscillator. R2 should be approximately 100 kΩ. R3 is used to adjust the duty cycle.

When the sum of R2 and R3 is twice the value of R1, the duty cycle will be about 50%. Capacitor C1 may be electrolytic to lower the oscillator frequency below 1 Hz.

### Duty Cycle Adjustment



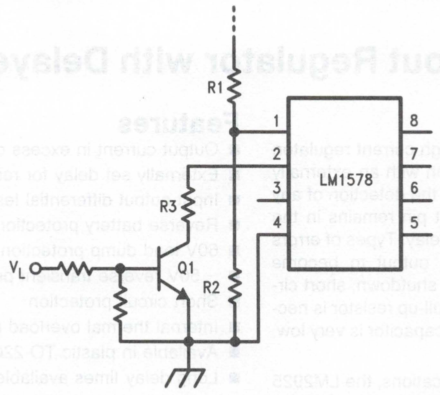
TL/H/8711-23

### REMOTE SHUTDOWN

The LM1578 may be remotely shutdown by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R3 to be approximately one-half the value of R1 and R2 in parallel.

## Typical Applications (Continued)

**Remote Shutdown—Shutdown Occurs When $V_L$ is High**


R1
R3
Q1
R2
$V_L$
LM1578
1
2
3
4
5
6
7
8

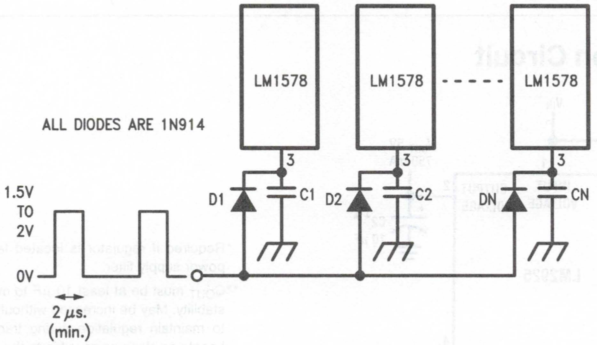
TL/H/8711–24

**SYNCHRONIZING DEVICES**

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal. This drive signal should be a pulse waveform with a minimum pulse width of 2 μsec. and an amplitude from 1.5V to 2.0V. The signal source must be capable of 1.) driving capacitive loads and 2.) delivering up to 500 μA for each LM1578.

Capacitors C1 thru CN are to be selected for a 20% slower frequency than the synchronization frequency.

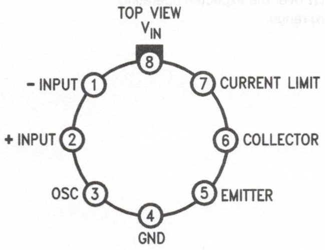
**Synchronizing Devices**


LM1578
LM1578
LM1578
ALL DIODES ARE 1N914
3
3
3
D1
C1
D2
C2
DN
CN
1.5V TO 2V
0V
2 μs. (min.)

TL/H/8711–25

## Connection Diagram

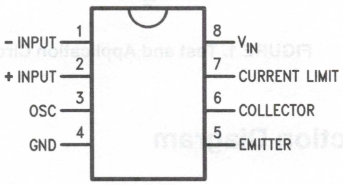
**Metal Can**


TOP VIEW
$V_{IN}$
8
- INPUT 1
7 CURRENT LIMIT
+ INPUT 2
6 COLLECTOR
OSC 3
5 EMITTER
4
GND

TL/H/8711–26

**Order Number LM1578H, LM2578H, or LM3578H**
**See NS Package Number H08C**

**Dual-In-Line Package**


- INPUT 1
+ INPUT 2
OSC 3
GND 4
8 $V_{IN}$
7 CURRENT LIMIT
6 COLLECTOR
5 EMITTER

TL/H/8711–27

**Order Number LM2578N, LM3578N**
**See NS Package Number N08E**

**National Semiconductor Corporation**

**PRELIMINARY**

# LM2925 Low Dropout Regulator with Delayed Reset

## General Description

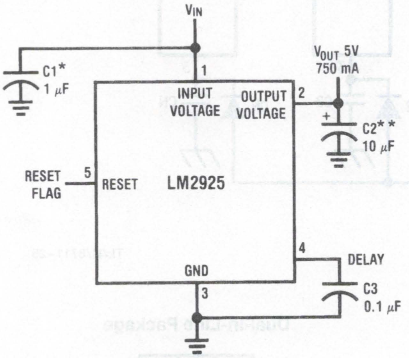
The LM2925 features a low dropout, high current regulator. Also included on-chip is a reset function with an externally set delay time. Upon power up, or after the detection of any error in the regulated output, the reset pin remains in the active low state for the duration of the delay. Types of errors detected include any that cause the output to become unregulated: low input voltage, thermal shutdown, short circuit, input transients, etc. No external pull-up resistor is necessary. The current charging the delay capacitor is very low, allowing long delay times.

Designed primarily for automotive applications, the LM2925 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load. The LM2925 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

## Features

- Output current in excess of 750 mA
- Externally set delay for reset
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- Long delay times available
- 100% electrical burn-in in thermal limit

## Typical Application Circuit



*Required if regulator is located far from power supply filter.

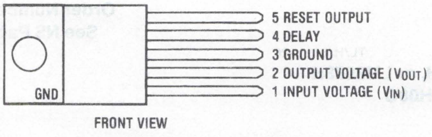
**$C_{OUT}$ must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

TL/H/5268–1

**FIGURE 1. Test and Application Circuit**

## Connection Diagram

**TO-220 5-Lead**



TL/H/5268–2

**Order Number LM2925T**
**See NS Package Number T05A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Operating Range | 26V |
| Overvoltage Protection | 60V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | −40°C to + 125°C |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | −65°C to + 150°C |
| Lead Temperature (Soldering, 10 seconds) | 230°C |

## Electrical Characteristics for $V_{OUT}$

$V_{IN}$ = 14V, C2 = 10 µf, $I_O$ = 500 mA, $T_J$ = 25°C (Note 3) (unless otherwise specified)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | | Note 2 | | | |
| Output Voltage | 6V≤ $V_{IN}$ ≤26V, $I_O$ ≤ 500 mA, −40°C≤ $T_J$ ≤ +125°C | 4.75 | 5.00 | 5.25 | V |
| Line Regulation | 9V ≤ $V_{IN}$ ≤ 16V, $I_O$ = 5 mA<br>6V ≤ $V_{IN}$ ≤ 26V, $I_O$ = 5 mA | | 4<br>10 | 25<br>50 | mV<br>mV |
| Load Regulation | 5 mA ≤ $I_O$ ≤ 500 mA | | 10 | 50 | mV |
| Output Impedance | 500 $mA_{DC}$ and 10 mArms, 100 Hz-10 kHz | | 200 | | mΩ |
| Quiescent Current | $I_O$ ≤ 10 mA<br>$I_O$ = 500 mA<br>$I_O$ = 750 mA | | 3<br>40<br>90 | <br>100<br> | mA<br>mA<br>mA |
| Output Noise Voltage | 10 Hz-100 kHz | | 100 | | µVrms |
| Long Term Stability | | | 20 | | mV/1000 hr |
| Ripple Rejection | $f_o$ = 120 Hz | | 66 | | dB |
| Dropout Voltage | $I_O$= 500 mA<br>$I_O$ = 750 mA | | 0.45<br>0.82 | 0.6<br> | V<br>V |
| Current Limit | | 0.75 | 1.2 | | A |
| Maximum Operational Input Voltage | | 26 | 31 | | V |
| Maximum Line Transient | $V_O$ ≤ 5.5V | 60 | 70 | | V |
| Reverse Polarity Input Voltage, DC | $V_O$ ≥ − 0.6V, 10Ω Load | −15 | −30 | | V |
| Reverse Polarity Input Voltage, Transient | 1% Duty Cycle, -TA ≤ 100 ms, 10Ω Load | −50 | −80 | | V |

## Electrical Characteristics for Reset Output

$V_{IN}$ = 14V, C3 = 0.1 µF, $T_A$ = 25°C (Note 3) (unless otherwise specified)

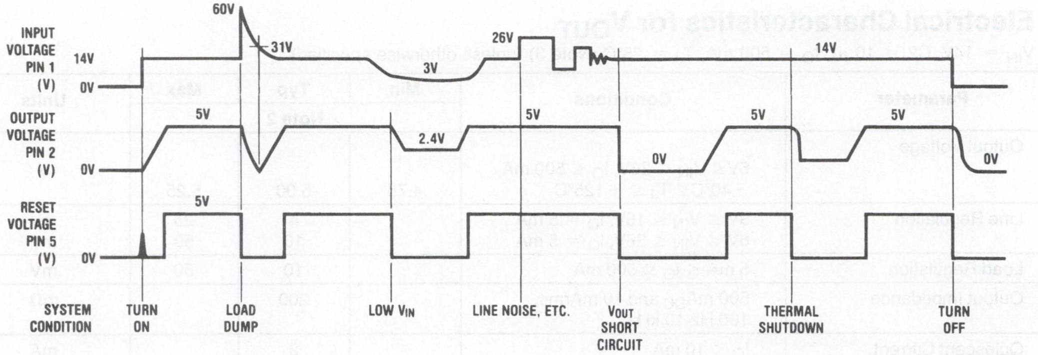
| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | | Note 2 | | | |
| Reset Voltage<br>Output Low<br>Output High | <br>$I_{SINK}$ = 1.6 mA<br>$I_{SOURCE}$ = 0 | <br><br>4.5 | <br>0.3<br>5.0 | <br>0.6<br>5.5 | <br>V<br>V |
| Reset Internal Pull-up Resistor | | | 30 | | kΩ |
| Reset Output Current Limit | $V_{RESET}$ = 1.2 V | | 5 | | mA |
| $V_{OUT}$ Threshold | | | 4.5 | | V |
| Delay Time | $C_3$ = .005 µF<br>$C_3$ = 0.1 µF<br>$C_3$ = 4.7 µF tantalum | <br>150<br> | 12<br>250<br>12 | <br>300<br> | ms<br>ms<br>s |
| Delay Current | Pin 4 | 1.2 | 1.6 | 2.0 | µA |

**Note 1:** Thermal resistance without a heat sink for junction to case temperature is 3°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

**Note 2:** These parameters are guaranteed and 100% production tested.

**Note 3:** To ensure constant junction temperature, low duty cycle pulse testing is used.

## Typical Circuit Waveforms

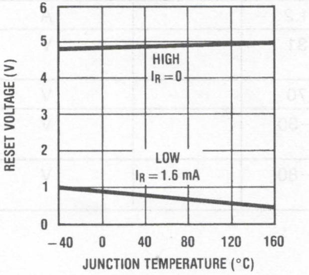


TL/H/5268-3

**FIGURE 2**

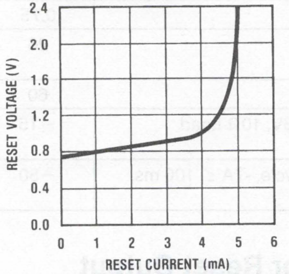
## Typical Performance Characteristics

**Reset Voltage**



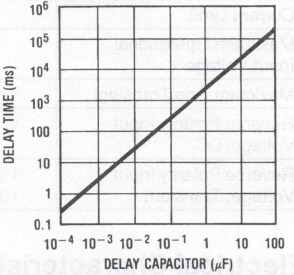
TL/H/5268-4

**Reset Voltage**



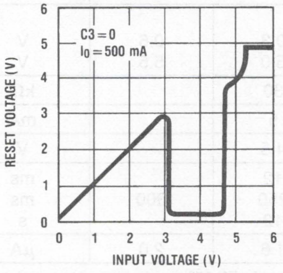
TL/H/5268-5

**Delay Time**



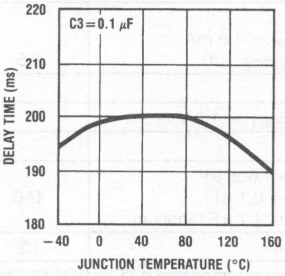
TL/H/5268-6

**Reset Voltage on Power-up**



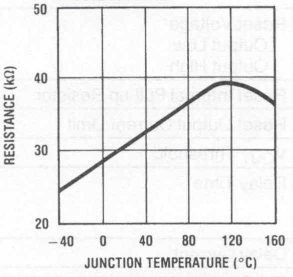
TL/H/5268-7

**Delay Time**



TL/H/5268-8

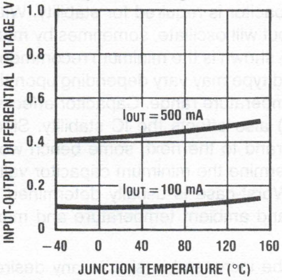
**Reset Pull-up Resistor R10**



TL/H/5268-9

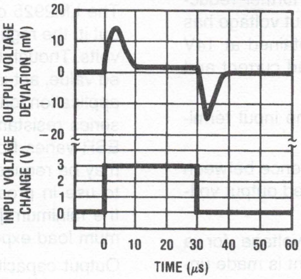
## Typical Performance Characteristics (Continued)

**Dropout Voltage**



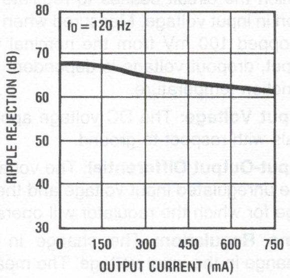
TL/H/5268-10

**Line Transient Response**



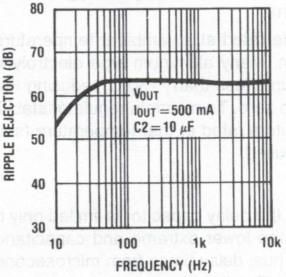
TL/H/5268-11

**Ripple Rejection**



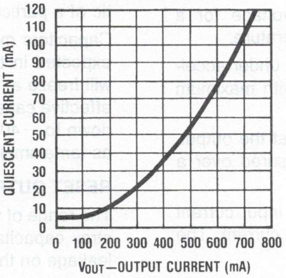
TL/H/5268-12

**Ripple Rejection**



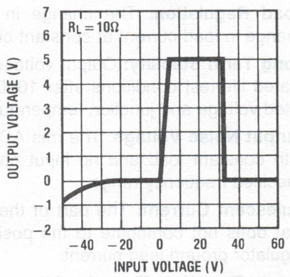
TL/H/5268-13

**Quiescent Current**



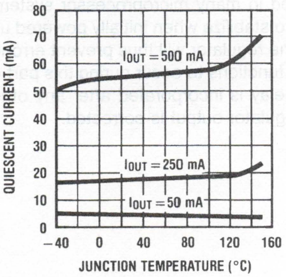
TL/H/5268-14

**Output Voltage**



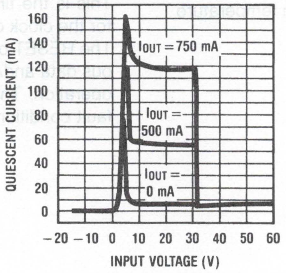
TL/H/5268-15

**Quiescent Current**



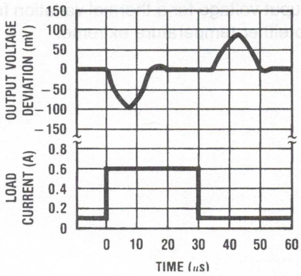
TL/H/5268-19

**Quiescent Current**



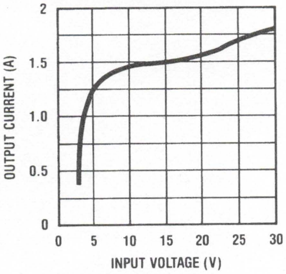
TL/H/5268-17

**Load Transient Response**



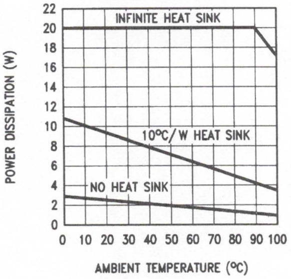
TL/H/5268-18

**Peak Output Current**



TL/H/5268-20

**Maximum Power Dissipation (TO-220)**



TL/H/5268-21

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentage change in ouput voltage for a thermal variation from room temperature to either temperature extreme.

## Application Hints

### EXTERNAL CAPACITORS

The LM2925 output capacitor is required for stability. Without it, the regulator output will oscillate, sometimes by many volts. Though the 10 $\mu$F shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also effects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum junction and ambient temperature and maximum load expected.

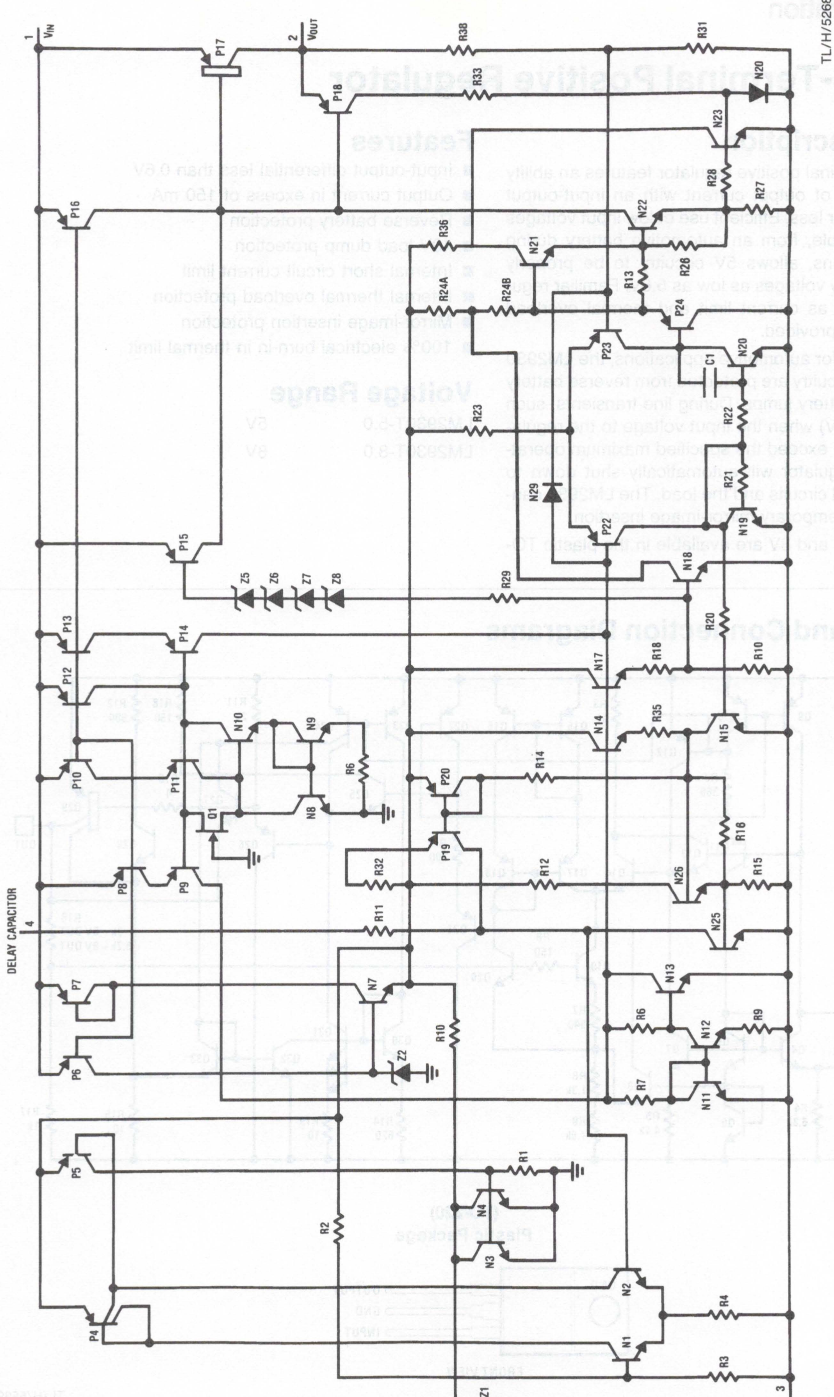
Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

### RESET OUTPUT

The range of values for the delay capacitor is limited only by stray capacitances on the lower extreme and capacitance leakage on the other. Thus, delay times from microseconds to seconds are possible. The low charging current, typically 2.0 microamps, allows the use of small, inexpensive disc capacitors for the nominal range of 100 to 500 milliseconds. This is the time required in many microprocessor systems for the clock oscillator to stabilize when initially powered up. The RESET output of the regulator will thus prevent erroneous data and/or timing functions to occur during this part of operation. The same delay is incorporated after any other fault condition in the regulator output is corrected.

## Circuit Schematic


1
VIN
2
VOUT
3
GND
4
DELAY CAPACITOR
5
RESET
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P22
P23
P24
Q1
N1
N2
N3
N4
N7
N8
N9
N10
N11
N12
N13
N14
N15
N17
N18
N19
N20
N21
N22
N23
N25
N26
N29
N20
Z1
Z2
Z5
Z6
Z7
Z8
R1
R2
R3
R4
R6
R6
R7
R9
R10
R10
R11
R12
R13
R14
R15
R16
R18
R20
R21
R22
R23
R24A
R24B
R26
R27
R28
R29
R31
R32
R33
R35
R36
R38
C1

TL/H/5268–22

FIGURE 3

**National Semiconductor Corporation**

# LM2930 3-Terminal Positive Regulator

## General Description

The LM2930 3-terminal positive regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Efficient use of low input voltages obtained, for example, from an automotive battery during cold crank conditions, allows 5V circuitry to be properly powered with supply voltages as low as 5.6V. Familiar regulator features such as current limit and thermal overload protection are also provided.

Designed originally for automotive applications, the LM2930 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (40V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2930 cannot be harmed by temporary mirror-image insertion.

Fixed outputs of 5V and 8V are available in the plastic TO-220 power package.

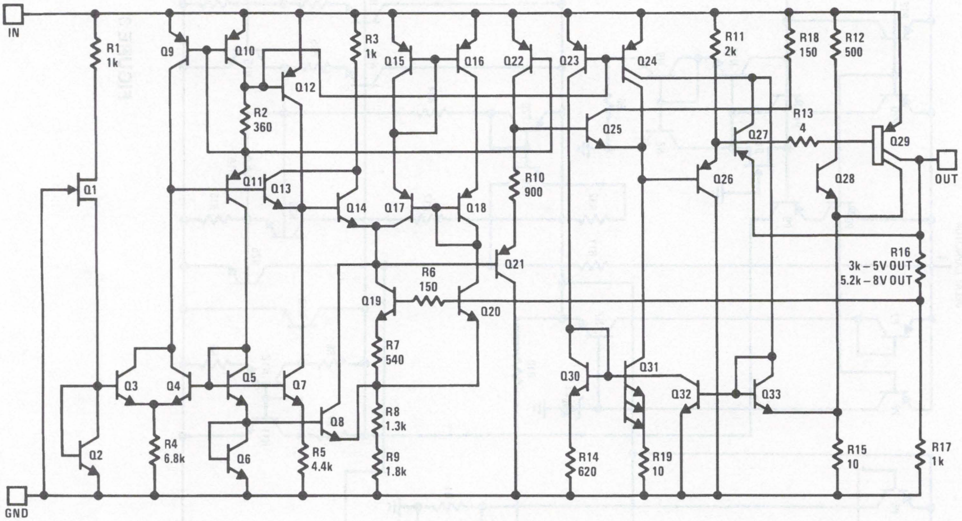
## Features

- Input-output differential less than 0.6V
- Output current in excess of 150 mA
- Reverse battery protection
- 40V load dump protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in thermal limit

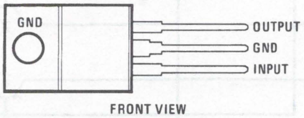
## Voltage Range

| | |
|---|---|
| LM2930T-5.0 | 5V |
| LM2930T-8.0 | 8V |

## Schematic and Connection Diagrams


IN
R1 1k
Q9
Q10
R3 1k
Q15
Q16
Q22
Q23
Q24
R11 2k
R18 150
R12 500
Q12
R2 360
Q25
R13 4
Q27
Q29
OUT
Q1
Q11
Q13
Q14
Q17
Q18
R10 900
Q26
Q28
R16 3k – 5V OUT 5.2k – 8V OUT
Q21
R6 150
Q19
Q20
R7 540
Q3
Q4
Q5
Q7
Q30
Q31
Q32
Q33
Q8
R8 1.3k
R4 6.8k
Q2
Q6
R5 4.4k
R9 1.8k
R14 620
R19 10
R15 10
R17 1k
GND

**(TO-220)**
**Plastic Package**


GND
OUTPUT
GND
INPUT
FRONT VIEW

TL/H/5539–1

**Order Number LM2930T-5.0 or LM2930T-8.0**
**See NS Package T03B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Operating Range | 26V |
| Overvoltage Protection | 40V |
| Reverse Voltage (100 ms) | −12V |
| Reverse Voltage (DC) | −6V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | −40°C to +85°C |
| Maximum Junction Temperature | 125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 230°C |

## Electrical Characteristics (Note 2)

LM2930T-5.0 $V_{IN}=14V$, $I_O=150$ mA, $T_j=25°C$ (Note 5), C2 = 10 μF, unless otherwise specified

| Parameter | Conditions | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | Unit |
|---|---|---|---|---|---|
| Output Voltage | | 5 | 5.3<br>4.7 | | $V_{MAX}$<br>$V_{MIN}$ |
| | $6V \le V_{IN} \le 26V$, $5\text{ mA} \le I_O \le 150\text{ mA}$<br>$-40°C \le T_J \le 125°C$ | | | 5.5<br>4.5 | $V_{MAX}$<br>$V_{MIN}$ |
| Line Regulation | $9V \le V_{IN} \le 16V$, $I_O=5$ mA<br>$6V \le V_{IN} \le 26V$, $I_O=5$ mA | 7<br>30 | 25<br>80 | | $mV_{MAX}$<br>$mV_{MAX}$ |
| Load Regulation | $5\text{ mA} \le I_O \le 150\text{ mA}$ | 14 | 50 | | $mV_{MAX}$ |
| Output Impedance | 100 $mA_{DC}$ & 10 $mA_{rms}$, 100 Hz − 10 kHz | 200 | | | mΩ |
| Quiescent Current | $I_O=10$ mA<br>$I_O=150$ mA | 4<br>18 | 7<br>40 | | $mA_{MAX}$<br>$mA_{MAX}$ |
| Output Noise Voltage | 10 Hz − 100 kHz | 140 | | | $\mu V_{rms}$ |
| Long Term Stability | | 20 | | | mV/1000 hr |
| Ripple Rejection | $f_O=120$ Hz | 56 | | | dB |
| Current Limit | | 400 | 700<br>150 | | $mA_{MAX}$<br>$mA_{MIN}$ |
| Dropout Voltage | $I_O=150$ mA | 0.32 | 0.6 | | $V_{MAX}$ |
| Output Voltage Under Transient Conditions | $-12V \le V_{IN} \le 40V$, $R_L=100\Omega$ | | 5.5<br>−0.3 | | $V_{MAX}$<br>$V_{MIN}$ |

## Electrical Characteristics (Note 2)

LM2930T-8.0 ($V_{IN}=14V$, $I_O=150$ mA, $T_j=25°C$ (Note 5), C2 = 10 μF, unless otherwise specified)

| Parameter | Conditions | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | Unit |
|---|---|---|---|---|---|
| Output Voltage | | 8 | 8.5<br>7.5 | | $V_{MAX}$<br>$V_{MIN}$ |
| | $9.4V \le V_{IN} \le 26V$, $5\text{ mA} \le I_O \le 150\text{ mA}$,<br>$-40°C \le T_J \le 125°C$ | | | 8.8<br>7.2 | $V_{MAX}$<br>$V_{MIN}$ |
| Line Regulation | $9.4V \le V_{IN} \le 16V$, $I_O=5$ mA<br>$9.4V \le V_{IN} \le 26V$, $I_O=5$ mA | 12<br>50 | 50<br>100 | | $mV_{MAX}$<br>$mV_{MAX}$ |
| Load Regulation | $5\text{ mA} \le I_O \le 150\text{ mA}$ | 25 | 50 | | $mV_{MAX}$ |
| Output Impedance | 100 $mA_{DC}$ & 10 $mA_{rms}$, 100 Hz − 10 kHz | 300 | | | mΩ |
| Quiescent Current | $I_O=10$ mA<br>$I_O=150$ mA | 4<br>18 | 7<br>40 | | $mA_{MAX}$<br>$mA_{MAX}$ |
| Output Noise Voltage | 10 Hz − 100 kHz | 170 | | | $\mu V_{rms}$ |
| Long Term Stability | | 30 | | | mV/1000 hr |
| Ripple Rejection | $f_O=120$ Hz | 52 | | | dB |
| Current Limit | | 400 | 700<br>150 | | $mA_{MAX}$<br>$mA_{MIN}$ |
| Dropout Voltage | $I_O=150$ mA | 0.32 | 0.6 | | $V_{MAX}$ |
| Output Voltage Under Transient Conditions | $-12V \le V_{IN} \le 40V$, $R_L=100\Omega$ | | 8.8<br>−0.3 | | $V_{MAX}$<br>$V_{MIN}$ |

**Note 1:** Thermal resistance without a heat sink for junction to case temperature is 3°C/W and for case to ambient temperature is 50°C/W.

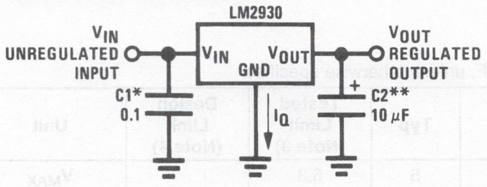
**Note 2:** All characteristics are measured with a capacitor across the input of 0.1 μF and a capacitor across the output of 10 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

**Note 3:** Guaranteed and 100% production tested.

**Note 4:** Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

**Note 5:** To ensure constant junction temperature, low duty cycle pulse testing is used.

## Typical Application



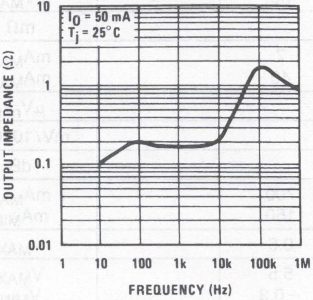
TL/H/5539-5

*Required if regulator is located far from power supply filter.

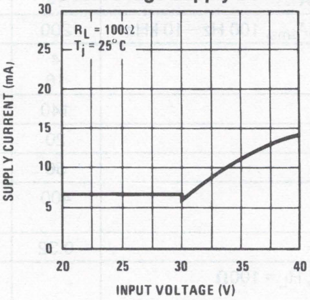
**$C_{OUT}$ must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

## Typical Performance Characteristics

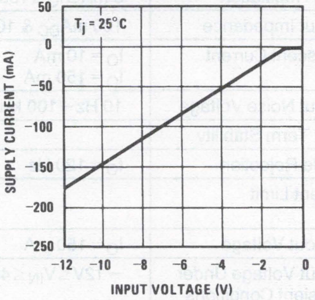
**Output Impedance**



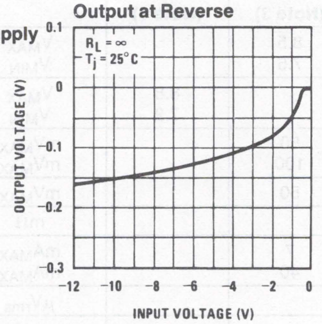
**Overvoltage Supply Current**



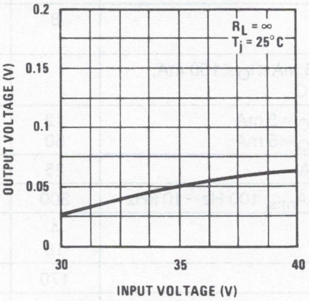
**Reverse Supply Current**



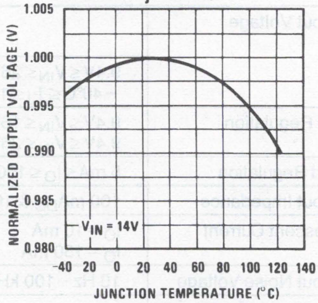
**Output at Reverse Supply**



**Output at Overvoltage**

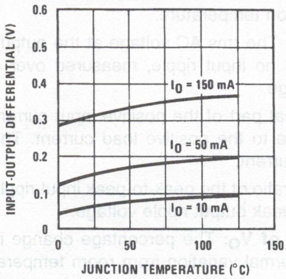


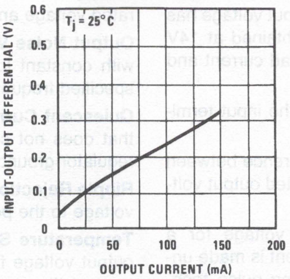
**Output Voltage (Normalized to 1V at $T_j = 25°C$)**

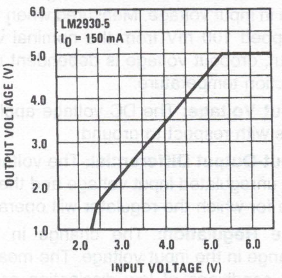


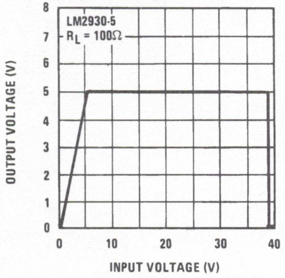
TL/H/5539-4

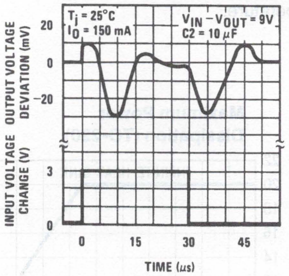
## Typical Performance Characteristics (Continued)

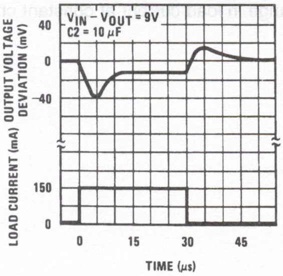

**Dropout Voltage**

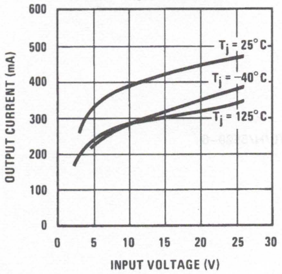

**Dropout Voltage**

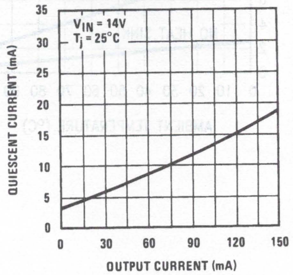

**Low Voltage Behavior**

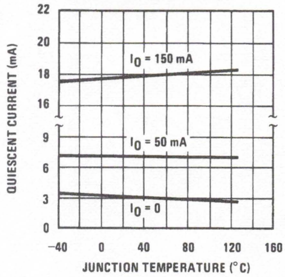

**High Voltage Behavior**

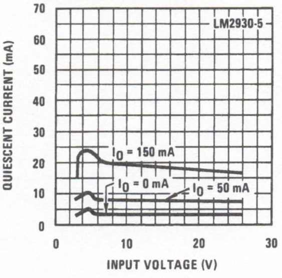

**Line Transient Response**

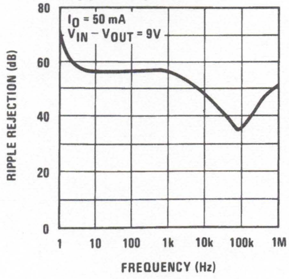

**Load Transient Response**

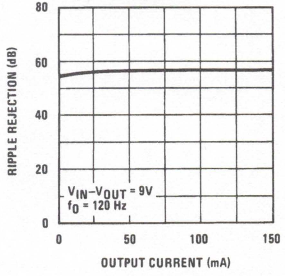

**Peak Output Current**


**Quiescent Current**


**Quiescent Current**


**Quiescent Current**


**Ripple Rejection**


**Ripple Rejection**

TL/H/5539–2

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

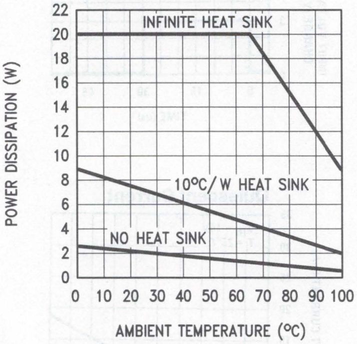
**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

**Maximum Power Dissipation (TO-220)**



TL/H/5539-6

**National Semiconductor Corporation**

# LM2931 Series Low Dropout Regulators

## General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1 mA or less when supplying 10 mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10 mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 100 mA of output current.

Designed originally for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed output of 5V is available in the plastic TO-220 power package or the popular TO-92 package. An adjustable output version, with on/off switch, is available in a 5-lead TO-220 package.

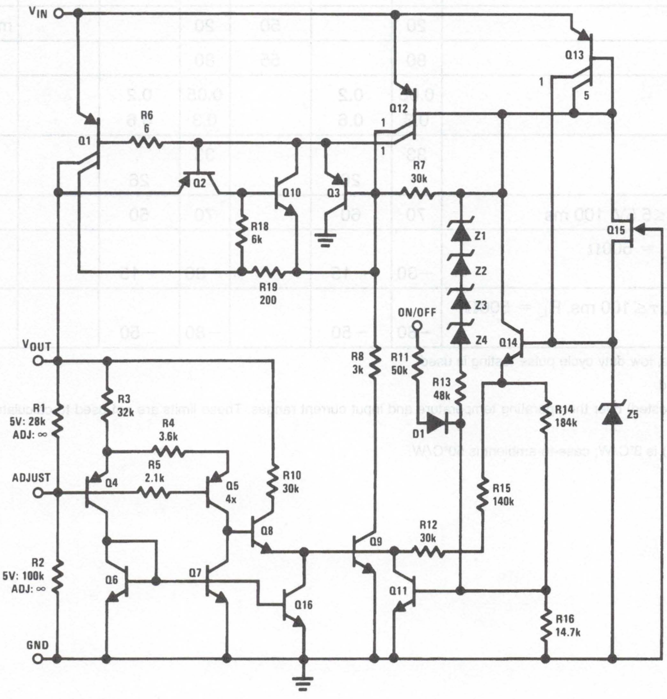
## Features

- Very low quiescent current
- Output current in excess of 100 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in plastic TO-220 or TO-92
- Available as adjustable with TTL compatible switch
- 100% electrical burn-in in thermal limit

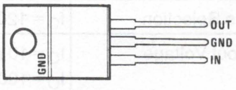
## Output Voltage Options

| | | | |
|---|---|---|---|
| LM2931T-5.0 | 5V | LM2931AT-5.0 | 5V |
| LM2931Z-5.0 | 5V | LM2931AZ-5.0 | 5V |
| LM2931CT | Adjustable | | |

## Schematic and Connection Diagrams


VIN
Q1
R6 6
Q2
Q10
Q3
R18 6k
R19 200
Q12
1
1
R7 30k
Q13
1
5
Z1
Z2
Z3
Z4
Q15
Q14
Z5
ON/OFF
R8 3k
R11 50k
R13 48k
D1
R14 184k
R15 140k
R12 30k
R16 14.7k
VOUT
R1 5V: 28k ADJ: ∞
R3 32k
R4 3.6k
R5 2.1k
ADJUST
Q4
Q5 4x
R10 30k
Q8
Q9
Q11
Q16
Q6
Q7
R2 5V: 100k ADJ: ∞
GND

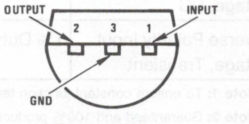
**TO-220 3-Lead**


OUT
GND
IN
GND

**Front View**

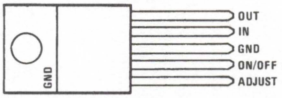
**Order Number LM2931**
**See NS Package T03B, Z03A, T05A**

**TO-92**


OUTPUT
INPUT
2
3
GND

**Bottom View**

**TO-220 5-Lead**


OUT
IN
GND
ON/OFF
ADJUST
GND

**Front View**

TL/H/5254–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Operating Range | 26V |
| Overvoltage Protection | |
| LM2931A, LM2931CT Adjustable | 60V |
| LM2931 | 50V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | −40°C to +85°C |
| Maximum Junction Temperature | 125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 230°C |

## Electrical Characteristics

$V_{IN} = 14V$, $I_O = 10$ mA, $T_J = 25°C$ (Note 1), C2 = 100 $\mu$F (unless otherwise specified)

| Parameter | Conditions | LM2931A-5.0 | | | LM2931-5.0 | | | |
|---|---|---|---|---|---|---|---|---|
| | | Typ | Test Limit (Note 2) | Design Limit (Note 3) | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | Units Limit |
| Output Voltage | | 5 | 5.19<br>4.81 | | | 5.25<br>4.75 | | $V_{MAX}$<br>$V_{MIN}$ |
| | $6.0V \leq V_{IN} \leq 26V$, $I_O$ 100 mA<br>$-40°C \leq T_j \leq 125°C$ | | | 5.25<br>4.75 | | | 5.5<br>4.5 | $V_{MAX}$<br>$V_{MIN}$ |
| Line Regulation | $9V \leq V_{IN} \leq 16V$<br>$6V \leq V_{IN} \leq 26V$ | 2<br>4 | 10<br>30 | | 2<br>4 | 10<br>30 | | $mV_{MAX}$<br>$mV_{MAX}$ |
| Load Regulation | $5 mA \leq I_O \leq 100$ mA | 14 | 50 | | 14 | 50 | | $mV_{MAX}$ |
| Output Impedance | 100 $mA_{DC}$ and 10 $mA_{rms}$, 100 Hz–10 kHz | 200 | | 600 | 200 | | | $m\Omega_{MAX}$ |
| Quiescent Current | $I_O \leq 10$ mA, $6V \leq V_{IN} \leq 26V$<br>$-40°C \leq T_j \leq 125°C$ | 0.4 | 1.0 | 1.0 | 0.4 | 1.0 | 1.0 | $mA_{MAX}$<br>$mA_{MIN}$ |
| | $I_O = 100$ mA, $V_{IN} = 14V$, $T_j = 25°C$ | 15 | | 30<br>5 | 15 | | | $mA_{MAX}$<br>$mA_{MIN}$ |
| Output Noise Voltage | 10 Hz–100 kHz, $C_{OUT}$ = 100 $\mu$F | 500 | | 1000 | 500 | | | $\mu V_{rms_{MAX}}$ |
| Long Term Stability | | 20 | | 50 | 20 | | | mV/1000 hr |
| Ripple Rejection | $f_O = 120$ Hz | 80 | | 55 | 80 | | | $dB_{MIN}$ |
| Dropout Voltage | $I_O = 10$ mA<br>$I_O = 100$ mA | 0.05<br>0.3 | 0.2<br>0.6 | | 0.05<br>0.3 | 0.2<br>0.6 | | $V_{MAX}$<br>$V_{MAX}$ |
| Maximum Operational Input Voltage | | 33 | 26 | | 33 | 26 | | $V_{MAX}$<br>$V_{MIN}$ |
| Maximum Line Transient | $R_L = 500\Omega$, $V_O \leq 5.5V$, 100 ms | 70 | 60 | | 70 | 50 | | $V_{MIN}$ |
| Reverse Polarity Input Voltage, DC | $V_O \geq -0.3V$, $R_L$ = 500$\Omega$ | −30 | −15 | | −30 | −15 | | $V_{MIN}$ |
| Reverse Polarity Input Voltage, Transient | 1% Duty Cycle, $\tau \leq 100$ ms, $R_L$ = 500$\Omega$ | −80 | −50 | | −80 | −50 | | $V_{MIN}$ |

**Note 1:** To ensure constant junction temperature, low duty cycle pulse testing is used.

**Note 2:** Guaranteed and 100% production tested.

**Note 3:** Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

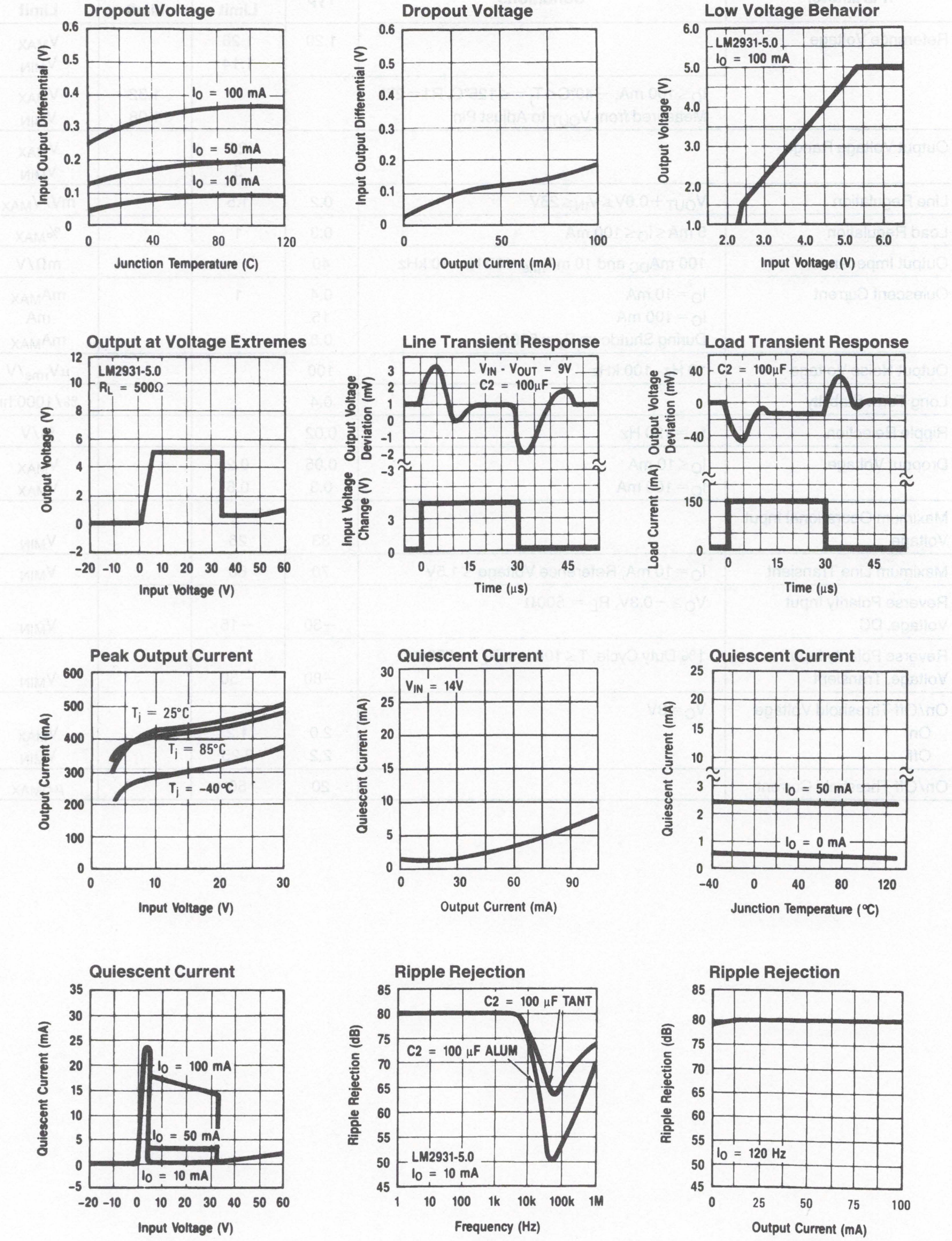
**Note 4:** Thermal resistance junction-to-case ($\theta_{jc}$) is 3°C/W; case-to-ambient is 50°C/W.

## Electrical Characteristics for Adjustable LM2931CT

$V_{IN}=14V$, $V_{OUT}=3V$, $I_O=10$ mA, $T_J=25°C$ (Note 1), R1 = 27k, C2 = 100 µF (unless otherwise specified)

| Parameter | Conditions | Typ | Tested Limit | Design Limit | Units Limit |
|---|---|---|---|---|---|
| Reference Voltage | | 1.20 | 1.26<br>1.14 | | $V_{MAX}$<br>$V_{MIN}$ |
| | $I_O \le 100$ mA, $-40°C \le T_j = \le 125°C$, R1 = 27k<br>Measured from $V_{OUT}$ to Adjust Pin | | | 1.32<br>1.08 | $V_{MAX}$<br>$V_{MIN}$ |
| Output Voltage Range | | | 24<br>3 | | $V_{MAX}$<br>$V_{MIN}$ |
| Line Regulation | $V_{OUT}+0.6V \le V_{IN} \le 26V$ | 0.2 | 1.5 | | $mV/V_{MAX}$ |
| Load Regulation | $5\ mA \le I_O \le 100\ mA$ | 0.3 | 1 | | $\%_{MAX}$ |
| Output Impedance | 100 $mA_{DC}$ and 10 $mA_{rms}$, 100 Hz–10 kHz | 40 | | | mΩ/V |
| Quiescent Current | $I_O=10$ mA<br>$I_O=100$ mA<br>During Shutdown $R_L=500\Omega$ | 0.4<br>15<br>0.8 | 1<br><br>1 | | $mA_{MAX}$<br>mA<br>$mA_{MAX}$ |
| Output Noise Voltage | 10 Hz–100 kHz | 100 | | | $\mu V_{rms}/V$ |
| Long Term Stability | | 0.4 | | | %/1000 hr |
| Ripple Rejection | $f_O=120$ Hz | 0.02 | | | %/V |
| Dropout Voltage | $I_O \le 10$ mA<br>$I_O=100$ mA | 0.05<br>0.3 | 0.2<br>0.6 | | $V_{MAX}$<br>$V_{MAX}$ |
| Maximum Operational Input Voltage | | 33 | 26 | | $V_{MIN}$ |
| Maximum Line Transient | $I_O=10$ mA, Reference Voltage $\le 1.5V$ | 70 | 60 | | $V_{MIN}$ |
| Reverse Polarity Input Voltage, DC | $V_O \ge -0.3V$, $R_L = 500\Omega$ | −30 | −15 | | $V_{MIN}$ |
| Reverse Polarity Input Voltage, Transient | 1% Duty Cycle, $T \le 100$ ms, $R_L = 500\Omega$ | −80 | −50 | | $V_{MIN}$ |
| On/Off Threshold Voltage<br>On<br>Off | $V_O=3V$ | <br>2.0<br>2.2 | <br>1.2<br>3.25 | | <br>$V_{MAX}$<br>$V_{MIN}$ |
| On/Off Threshold Current | | 20 | 50 | | $\mu A_{MAX}$ |

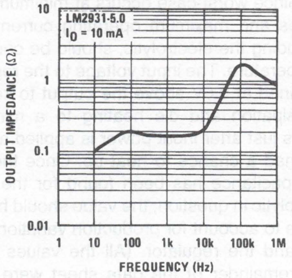
## Typical Performance Characteristics



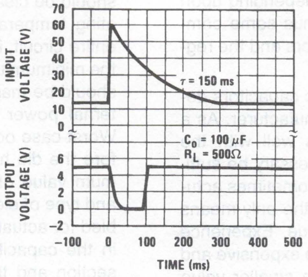
TL/H/5254-2

## Typical Performance Characteristics (Continued)

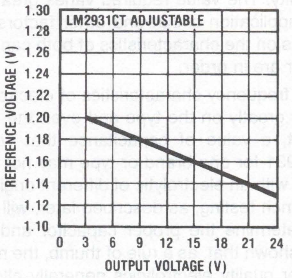
### Output Impedance



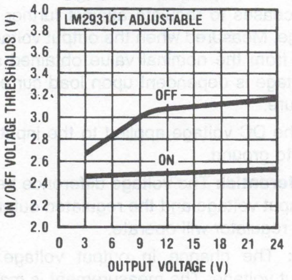
### Operation During Load Dump



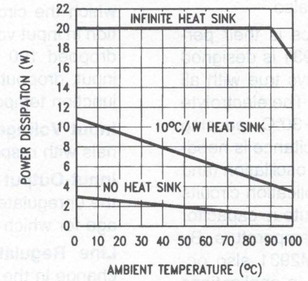
### Reference Voltage



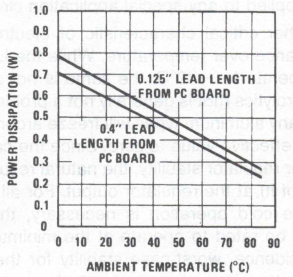
### On/Off Threshold



### Maximum Power Dissipation (TO-220)

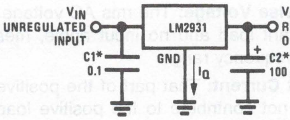


### Maximum Power Dissipation (TO-92)

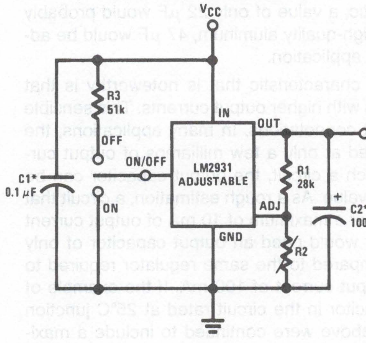


TL/H/5254-3

## Typical Applications


$V_{IN}$
UNREGULATED INPUT
C1*
0.1
LM2931
GND
$I_Q$
$V_{OUT}$
REGULATED OUTPUT
C2**
100 µF

### LM2931 Adjustable


$V_{CC}$
R3
51k
OFF
ON/OFF
ON
C1*
0.1 µF
IN
OUT
LM2931
ADJUSTABLE
ADJ
GND
$V_{OUT}$
R1
28k
C2**
100 µF
R2

TL/H/5254-4

$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

**Note:** Using 28k for R1 will automatically compensate for errors in $V_{OUT}$ due to the input bias current of the ADJ pin (approximately 1 µA).

*Required if regulator is located far from power supply filter.

**$C_{OUT}$ must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

## Application Hints

One of the distinguishing factors of the LM2931 series regulators is the requirement of an output capacitor for device stability. The value required varies greatly depending upon the application circuit and other factors. Thus some comments on the characteristics of both capacitors and the regulator are in order.

High frequency characteristics of electrolytic capacitors depend greatly on the type and even the manufacturer. As a result, a value of capacitance that works well with the LM2931 for one brand or type may not necessary be sufficient with an electrolytic of different origin. Sometimes actual bench testing, as described later, will be the only means to determine the proper capacitor and value. Experience has shown that, as a rule of thumb, the more expensive and higher quality electrolytics generally allow a smaller value for regulator stability. As an example, while a high-quality 100 μF aluminum electrolytic covers all general application circuits, similar stability can be obtained with a tantalum electrolytic of only 47 μF. This factor of two can generally be applied to any special application circuit also.

Another critical characteristic of electrolytics is their performance over temperature. While the LM2931 is designed to operate to −40°C, the same is not always true with all electrolytics (hot is generally not a problem). The electrolyte in many aluminum types will freeze around −30°C, reducing their effective value to zero. Since the capacitance is needed for regulator stability, the natural result is oscillation (and lots of it) at the regulator output. For all application circuits where cold operation is necessary, the output capacitor must be rated to operate at the minimum temperature. By coincidence, worst-case stability for the LM2931 also occurs at minimum temperatures. As a result, in applications where the regulator junction temperature will never be less than 25°C, the output capacitor can be reduced approximately by a factor of two over the value needed for the entire temperature range. To continue our example with the tantalum electrolytic, a value of only 22 μF would probably thus suffice. For high-quality aluminum, 47 μF would be adequate in such an application.

Another regulator characteristic that is noteworthy is that stability decreases with higher output currents. This sensible fact has important connotations. In many applications, the LM2931 is operated at only a few milliamps of output current or less. In such a circuit, the output capacitor can be further reduced in value. As a rough estimation, a circuit that is required to deliver a maximum of 10 mA of output current from the regulator would need an output capacitor of only half the value compared to the same regulator required to deliver the full output current of 100 mA. If the example of the tantalum capacitor in the circuit rated at 25°C junction temperature and above were continued to include a maximum of 10 mA of output current, then the 22 μF output capacitor could be reduced to only 10 μF.

In the case of the LM2931CT adjustable regulator, the minimum value of output capacitance is a function of the output voltage. As a general rule, the value decreases with higher output voltages, since internal loop gain is reduced.

At this point, the procedure for bench testing the minimum value of an output capacitor in a special application circuit should be clear. Since worst-case occurs at minimum operating temperatures and maximum operating currents, the entire circuit, including the electrolytic, should be cooled to the minimum temperature. The input voltage to the regulator should be maintained at 0.6V above the output to keep internal power dissipation and die heating to a minimum. Worst-case occurs just after input power is applied and before the die has had a chance to heat up. Once the minimum value of capacitance has been found for the brand and type of electrolytic in question, the value should be doubled for actual use to account for production variations both in the capacitor and the regulator. (All the values in this section and the remainder of the data sheet were determined in this fashion.)

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

**National Semiconductor Corporation**

# LM2935 Low Dropout Dual Regulator

## General Description

The LM2935 positive voltage regulator features a low quiescent current of 3 mA or less when supplying 10 mA loads from the standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include processor power supplies demanding as much as 750 mA of output current.

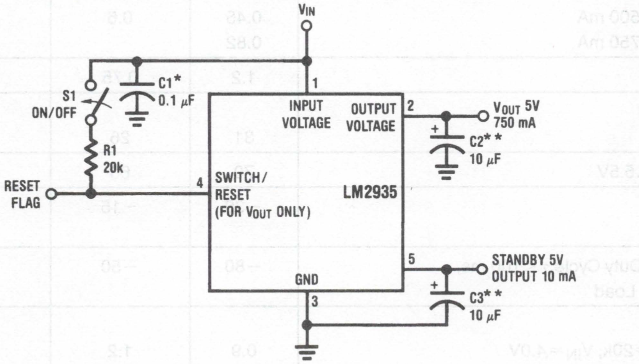
Designed originally for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed outputs of 5V are available in the plastic TO-220 power package.

## Features

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- ON/OFF switch for high current output
- Reset error flag
- 100% electrical burn-in in thermal limit

## Typical Application Circuit



TL/H/5232–1

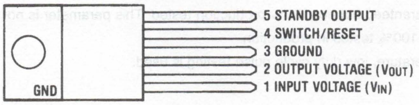
FIGURE 1. Test and Application Circuit

*Required if regulator is located far from power supply filter.

**$C_{OUT}$ must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

## Connection Diagram

**TO-220 5-Lead**



TL/H/5232–8

**Front View**

**Order Number LM2935T**
**See NS Package Number T05A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Operating Range | 26V |
| Overvoltage Protection | 60V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | −40°C to +125°C |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 230°C |

## Electrical Characteristics for $V_{OUT}$

$V_{IN}$ = 14V, $I_O$ = 500 mA, $T_J$ = 25°C (Note 4), C2 = 10 μF (unless otherwise specified)

| Parameter | Conditions | Typ | Tested Limit (Note 3) | Units Limit |
|---|---|---|---|---|
| Output Voltage | $6V \le V_{IN} \le 26V$, $5\ mA \le I_O \le 500\ mA$,<br>$-40°C \le T_J \le 125°C$ (Note 2) | 5.00 | 5.25<br>4.75 | $V_{MAX}$<br>$V_{MIN}$ |
| Line Regulation | $9V \le V_{IN} \le 16V$, $I_O = 5\ mA$ | 4 | 25 | $mV_{MAX}$ |
| | $6V \le V_{IN} \le 26V$, $I_O = 5\ mA$ | 10 | 50 | $mV_{MAX}$ |
| Load Regulation | $5\ mA \le I_O \le 500\ mA$ | 10 | 50 | $mV_{MAX}$ |
| Output Impedance | 500 $mA_{DC}$ and 10 $mA_{rms}$, 100 Hz–10 kHz | 200 | | mΩ |
| Quiescent Current | $I_O \le 10\ mA$, No Load on Standby | 3 | | mA |
| | $I_O = 500\ mA$, No Load on Standby | 40 | 100 | $mA_{MAX}$ |
| | $I_O = 750\ mA$, No Load on Standby | 90 | | mA |
| Output Noise Voltage | 10 Hz–100 kHz | 100 | | $\mu V_{rms}$ |
| Long Term Stability | | 20 | | mV/1000 hr |
| Ripple Rejection | $f_O = 120\ Hz$ | 66 | | dB |
| Dropout Voltage | $I_O = 500\ mA$ | 0.45 | 0.6 | $V_{MAX}$ |
| | $I_O = 750\ mA$ | 0.82 | | |
| Current Limit | | 1.2 | 0.75 | $A_{MIN}$ |
| Maximum Operational Input Voltage | | 31 | 26 | $V_{MIN}$ |
| Maximum Line Transient | $V_O \le 5.5V$ | 70 | 60 | V |
| Reverse Polarity Input Voltage, DC | | −30 | −15 | V |
| Reverse Polarity Input Voltage, Transient | 1% Duty Cycle, $\tau \le 100\ ms$,<br>10Ω Load | −80 | −50 | V |
| Reset Output Voltage | | | | |
| Low | $R1 = 20k$, $V_{IN} = 4.0V$ | 0.9 | 1.2 | $V_{MAX}$ |
| High | $R1 = 20k$, $V_{IN} = 14V$ | 5.0 | 6.0 | $V_{MAX}$ |
| | | | 4.5 | $V_{MIN}$ |
| Reset Output Current | Reset = 1.2V | 5 | | mA |
| ON/OFF Resistor | R1 (± 10% Tolerance) | | 20 | $k\Omega_{MAX}$ |

**Note 1:** Thermal resistance without a heat sink for junction to case temperature is 3°C/W(TO-220). Thermal resistance for TO-220 case to ambient temperature is 50° C/W.

**Note 2:** The temperature extremes are guaranteed but not 100% production tested. This parameter is not used to calculate outgoing AQL.

**Note 3:** Tested Limits are guaranteed and 100% tested in production.

**Note 4:** To ensure constant junction temperature, low duty cycle pulse testing is used.

## Electrical Characteristics for Standby Output

$I_O = 10$ mA, $V_{IN} = 14V$, S1 open, $C_{OUT} = 10\ \mu F$, $T_J = 25°C$ (Note 4), (unless otherwise specified)

| Parameter | Standby Output Conditions | Typ | Tested Limit | Units Limit |
|---|---|---|---|---|
| Output Voltage | $I_O \le 10$ mA, $6V \le V_{IN} \le 26V$,<br>$-40°C \le T_J \le 125°C$ | 5.00 | 5.25<br>4.75 | $V_{MAX}$<br>$V_{MIN}$ |
| Tracking | $V_{OUT}$–Standby Output Voltage | 50 | 200 | $mV_{MAX}$ |
| Line Regulation | $6V \le V_{IN} \le 26V$ | 4 | 50 | $mV_{MAX}$ |
| Load Regulation | $1\ mA \le I_O \le 10$ mA | 10 | 50 | $mV_{MAX}$ |
| Output Impedance | 10 $mA_{DC}$ and 1 $mA_{rms}$, 100 Hz–10 kHz | 1 |  | Ω |
| Quiescent Current | $I_O \le 10$ mA,<br>$V_{OUT}$ OFF (Note 2) | 2 | 3 | $mA_{MAX}$ |
| Output Noise Voltage | 10 Hz–100 kHz | 300 |  | μV |
| Long Term Stability |  | 20 |  | mV/1000 hr |
| Ripple Rejection | $f_O = 120$ Hz | 66 |  | dB |
| Dropout Voltage | $I_O \le 10$ mA | 0.55 | 0.7 | $V_{MAX}$ |
| Current Limit |  | 70 | 25 | $mA_{MIN}$ |
| Maximum Operational Input Voltage | $V_O \le 6V$ | 70 | 60 | $V_{MIN}$ |
| Reverse Polarity Input Voltage, DC | $V_O \ge -0.3V$, 510Ω Load | −30 | −15 | $V_{MIN}$ |
| Reverse Polarity Input Voltage, Transient | 1% Duty Cycle $T \le 100$ ms<br>500Ω Load | −80 | −50 | $V_{MIN}$ |

## Typical Circuit Waveforms

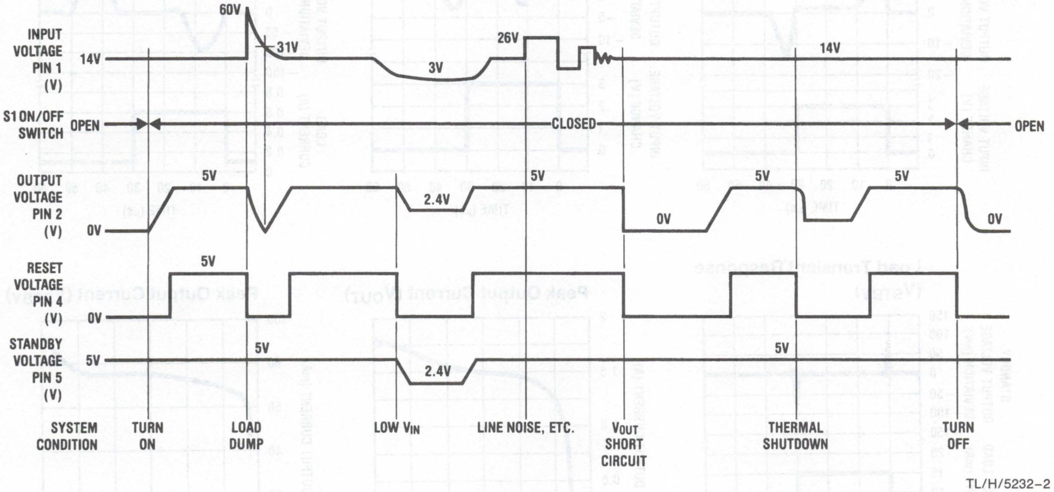
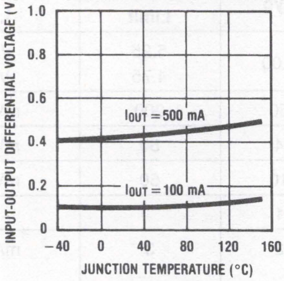

INPUT VOLTAGE PIN 1 (V)
14V
60V
31V
3V
26V
14V
S1 ON/OFF SWITCH
OPEN
CLOSED
OPEN
OUTPUT VOLTAGE PIN 2 (V)
0V
5V
2.4V
5V
0V
5V
5V
0V
RESET VOLTAGE PIN 4 (V)
0V
5V
STANDBY VOLTAGE PIN 5 (V)
5V
5V
2.4V
5V
SYSTEM CONDITION
TURN ON
LOAD DUMP
LOW $V_{IN}$
LINE NOISE, ETC.
$V_{OUT}$ SHORT CIRCUIT
THERMAL SHUTDOWN
TURN OFF
TL/H/5232–2

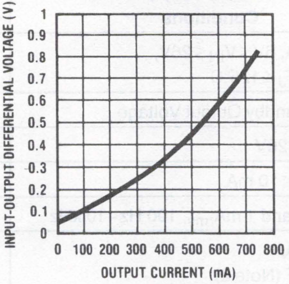
**FIGURE 2**

## Typical Performance Characteristics

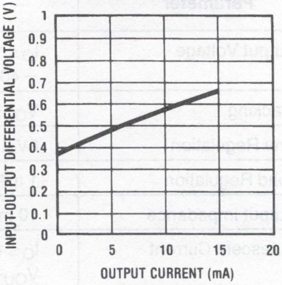
**Dropout Voltage ($V_{OUT}$)**



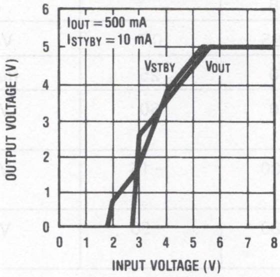
**Dropout Voltage ($V_{OUT}$)**



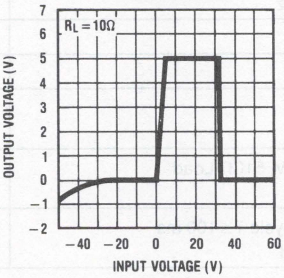
**Dropout Voltage ($V_{STBY}$)**



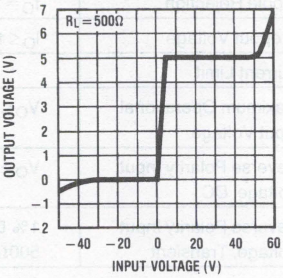
**Low Voltage Behavior**



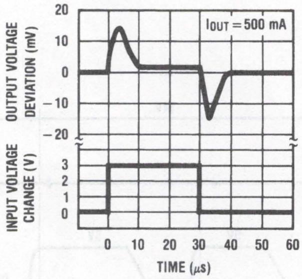
**Output Voltage ($V_{OUT}$)**



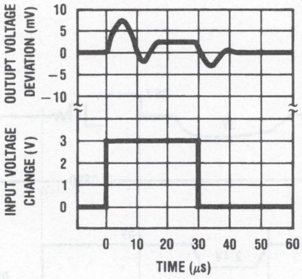
**Output Voltage ($V_{STBY}$)**



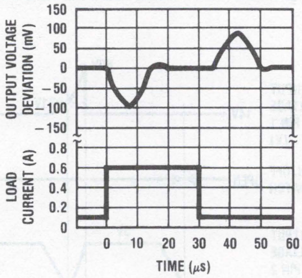
**Line Transient Response ($V_{OUT}$)**



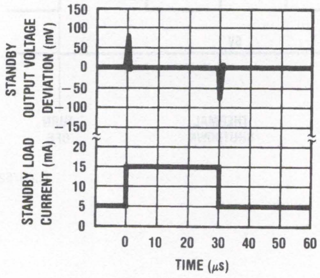
**Line Transient Response ($V_{STBY}$)**



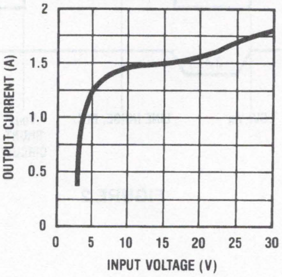
**Load Transient Response ($V_{OUT}$)**



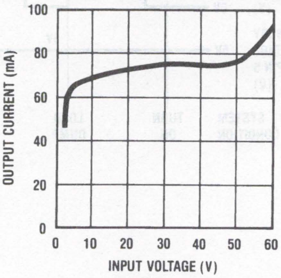
**Load Transient Response ($V_{STBY}$)**



**Peak Output Current ($V_{OUT}$)**



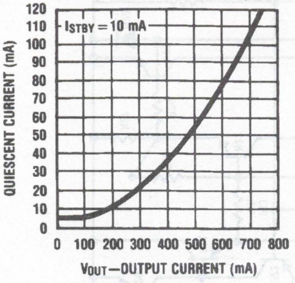
**Peak Output Current ($V_{STBY}$)**



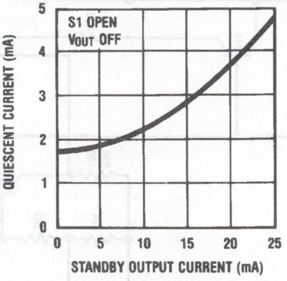
TL/H/5232–3

## Typical Performance Characteristics (Continued)

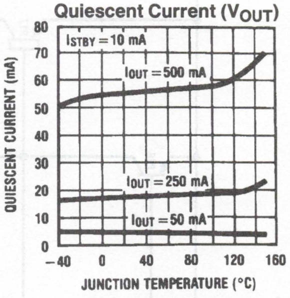
Quiescent Current ($V_{OUT}$)



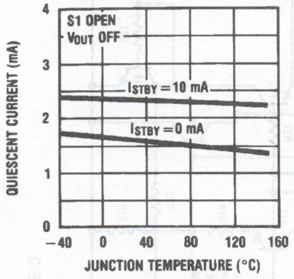
Quiescent Current ($V_{STBY}$)



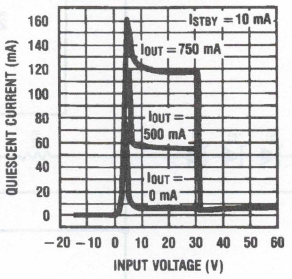
Quiescent Current ($V_{OUT}$)



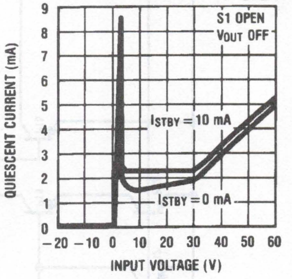
Quiescent Current ($V_{STBY}$)



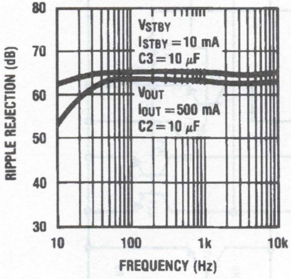
Quiescent Current



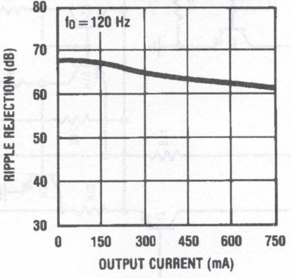
Quiescent Current ($V_{STBY}$)



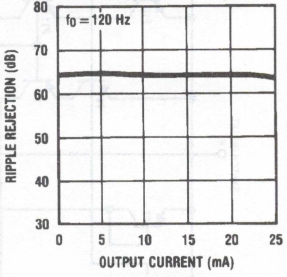
Ripple Rejection



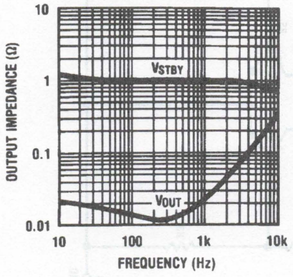
Ripple Rejection ($V_{OUT}$)



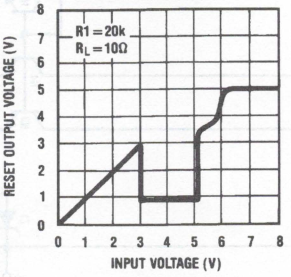
Ripple Rejection ($V_{STBY}$)



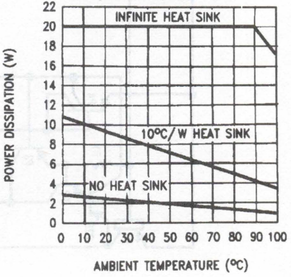
Output Impedance



Reset on Startup

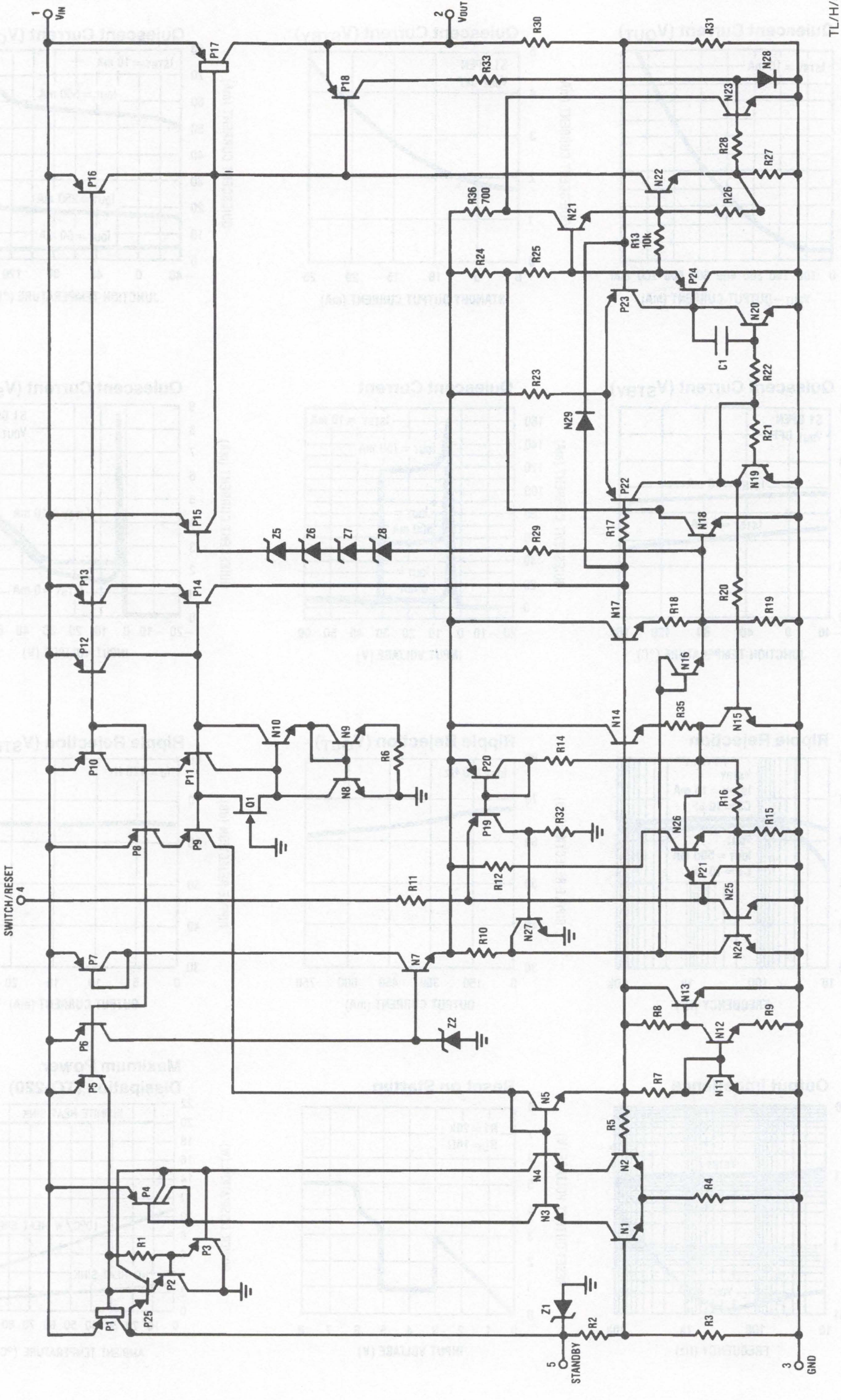


Maximum Power Dissipation (TO-220)



TL/H/5232–4

## Circuit Schematic


1 VIN
2 VOUT
SWITCH/RESET 4
5 STANDBY
3 GND
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
P25
N1
N2
N3
N4
N5
N7
N8
N9
N10
N11
N12
N13
N14
N15
N16
N17
N18
N19
N20
N21
N22
N23
N24
N25
N26
N27
N28
N29
Q1
Z1
Z2
Z5
Z6
Z7
Z8
C1
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13 10k
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R35
R36 700

TL/H/5232-5

FIGURE 3

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

## Application Hints

### EXTERNAL CAPACITORS

The LM2935 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

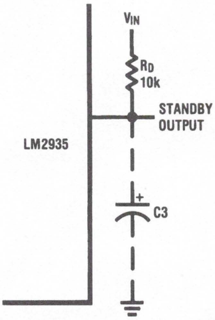
No capacitor must be attached to the ON/OFF and ERROR FLAG pin. Due to the internal circuits of the IC, oscillation on this pin could result.

### STANDBY OUTPUT

The LM2935 differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a more expensive capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener (*Figure 3*), the current through the external resistor should be sufficient to bias R2 and R3 up to this point. Approximately 60 μA will suffice, resulting in a 10k external resistor for most applications (*Figure 4*).



TL/H/5232–6

**FIGURE 4. Disabling Standby Output to Eliminate C3**

### HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

### ON/OFF AND ERROR FLAG PIN

This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in *Figure 1* (common in automotive systems where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions, the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current

## Application Hints (Continued)

output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

The ON/OFF pin can also be driven directly from logic circuits. The only requirement is that the 20k pull-up resistor remain in place *(Figure 5)*. This will not affect the logic gate since the voltage on this pin is limited by the internal clamp in the LM2935 to 5V. The error flag is sacrificed in this arrangement since the maximum sink capability of the pin in the active low state (approximately 5 mA) is usually not sufficient to pull down the active high logic gate. Of course, the flag can be retained if the driving gate is open collector logic.

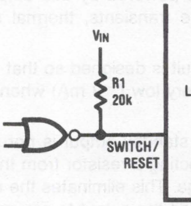

V_IN
R1
20k
LM2935
SWITCH/
RESET

**FIGURE 5. Controlling ON/OFF Terminal with a Typical CMOS or TTL Logic Gate**

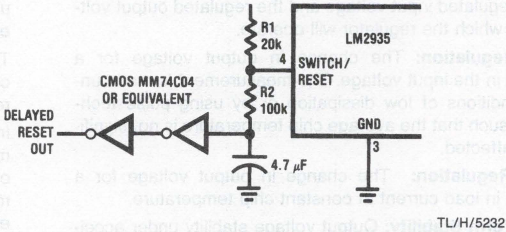

R1
20k
LM2935
4
SWITCH/
RESET
CMOS MM74C04
OR EQUIVALENT
R2
100k
DELAYED
RESET
OUT
GND
3
4.7 μF
TL/H/5232–7

**FIGURE 6. Reset Pulse on Power-Up (with approximately 300 ms delay)**

National Semiconductor Corporation

**PRELIMINARY**

# LM2940 1A Low Dropout Regulator

## General Description

The LM2940 positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Futhermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{in} - V_{out} \le 3V$).

Designed also for vehicular applications, the LM2940 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as load dump (60V) when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

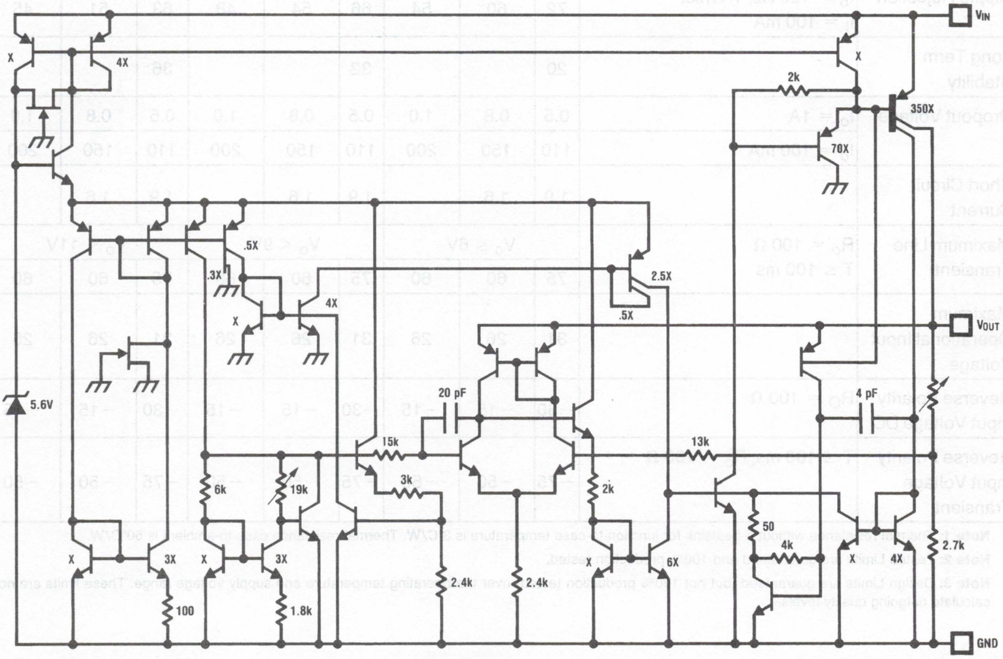
## Features

- Dropout voltage typically 0.5V @$I_o$ = 1A
- Output current in excess of 1A
- Output trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- 100% electrical burn-in in thermal limit

## Output Voltages

| | |
|---|---|
| LM2940T-5.0 | 5V |
| LM2940T-8.0 | 8V |
| LM2940T-10 | 10V |

## Equivalent Schematic Diagram



TL/H/8822–1

**Order Number LM2940T-5.0, LM2940T-8.0, LM2940T-10**
**See NS Package Number TO3B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Survival Voltage (≤100 ms) | 60V |
| Operational Voltage | 26V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range ($T_A$) | −40°C to +125°C |
| Maximum Junction Temperature | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 230°C |

ESD susceptibility rating is to be determined

## Electrical Characteristics $V_{in} = V_o + 5V$, $I_o = 1A$, $C_{out} = 22\ \mu F$, $T_j = 25°C$ unless otherwise specified.

| Output Voltage ($V_o$) | | 5V | | | 8V | | | 10V | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Conditions | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
| | | $6.25V \le V_{IN} \le 26V$ | | | $9.4V \le V_{IN} \le 26V$ | | | $11.5V \le V_{IN} \le 26V$ | | | |
| Output Voltage | $5\ mA \le I_O \le 1A$ | 5.00 | 4.85<br>5.15 | 4.75<br>5.25 | 8.00 | 7.76<br>8.24 | 7.60<br>8.40 | 10.00 | 9.70<br>10.30 | 9.50<br>10.50 | $V_{MIN}$<br>$V_{MAX}$ |
| Line Regulation | $V_O + 2V \le V_{in} \le 26V$, $I_O = 5\ mA$ | 20 | 50 | | 20 | 80 | | 20 | 100 | | $mV_{MAX}$ |
| Load Regulation | $50\ mA \le I_O \le 1A$ | 35 | 50 | 80 | 55 | 80 | 130 | 65 | 100 | 165 | $mV_{MAX}$ |
| Output Impedance | 100 mADC and 20 mArms $f_O = 120\ Hz$ | 35 | | | 55 | | | 65 | | | mΩ |
| Quiescent Current | $V_O + 2V \le V_{in} < 26V$, $I_O = 5\ mA$ | 10 | 15 | 20 | 10 | 15 | 20 | 10 | 15 | 20 | $mA_{MAX}$ |
| | $V_{in} = V_O + 5V$, $I_O = 1A$ | 30 | 45 | 60 | 30 | 45 | 60 | 30 | 45 | 60 | $mA_{MAX}$ |
| Output Noise Voltage | 10 Hz − 100 kHz $I_O = 5\ mA$ | 150 | | | 240 | | | 300 | | | $\mu V_{RMS}$ |
| Ripple Rejection | $f_O = 120\ Hz$, 1 Vrms; $I_l = 100\ mA$ | 72 | 60 | 54 | 66 | 54 | 48 | 63 | 51 | 45 | $dB_{MIN}$ |
| Long Term Stability | | 20 | | | 32 | | | 36 | | | mV/ 1000 Hr |
| Dropout Voltage | $I_O = 1A$ | 0.5 | 0.8 | 1.0 | 0.5 | 0.8 | 1.0 | 0.5 | 0.8 | 1.0 | $V_{MAX}$ |
| | $I_O = 100\ mA$ | 110 | 150 | 200 | 110 | 150 | 200 | 110 | 150 | 200 | $mV_{MAX}$ |
| Short Circuit Current | | 1.9 | 1.6 | | 1.9 | 1.6 | | 1.9 | 1.6 | | $A_{MIN}$ |
| Maximum Line Transient | $R_O = 100\ \Omega$ $T \le 100\ ms$ | $V_O \le 6V$ | | | $V_O < 9V$ | | | $V_O < 11V$ | | | |
| | | 75 | 60 | 60 | 75 | 60 | 60 | 75 | 60 | 60 | $V_{MIN}$ |
| Maximum Operational Input Voltage | | 31 | 26 | 26 | 31 | 26 | 26 | 31 | 26 | 26 | $V_{dc}$ |
| Reverse Polarity Input Voltage DC | $R_O = 100\ \Omega$ | −30 | −15 | −15 | −30 | −15 | −15 | −30 | −15 | −15 | $V_{MIN}$ |
| Reverse Polarity Input Voltage Transient | $T \le 100\ ms$, $R_o = 100\ \Omega$ | −75 | −50 | −50 | −75 | −50 | −50 | −75 | −50 | −50 | $V_{MIN}$ |

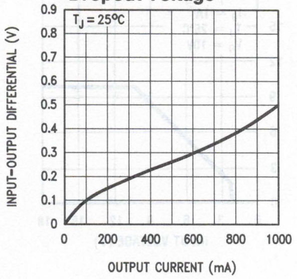
**Note 1:** Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

**Note 2:** Tested Limits are guaranteed and 100% production tested.

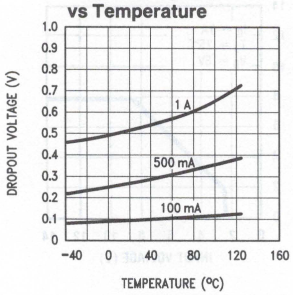
**Note 3:** Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

## Typical Performance Characteristics

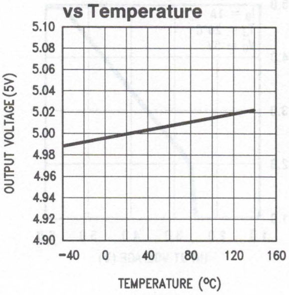
**Dropout Voltage**



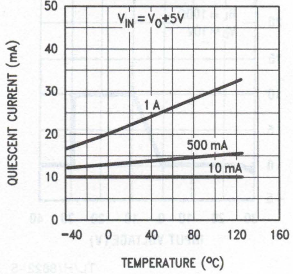
**Dropout Voltage vs Temperature**



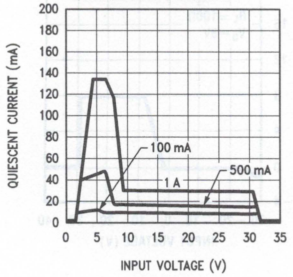
**Output Voltage vs Temperature**



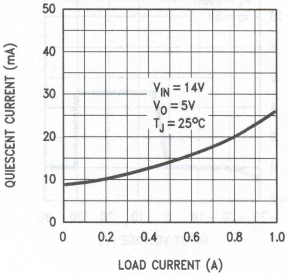
**Quiescent Current vs Temperature**



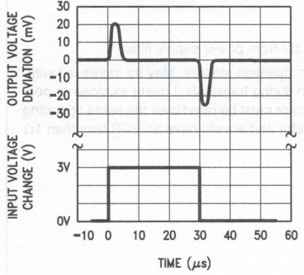
**Quiescent Current**



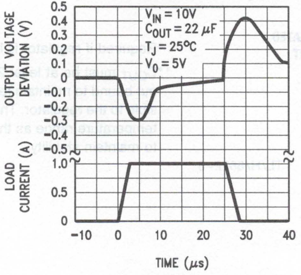
**Quiescent Current**



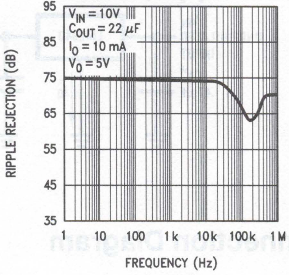
**Line Transient Response**



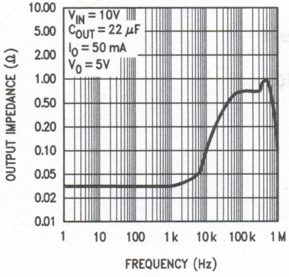
**Load Transient Response**



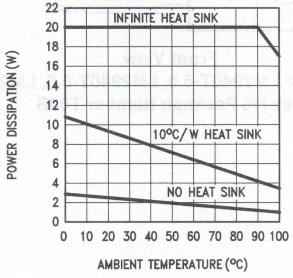
**Ripple Rejection**



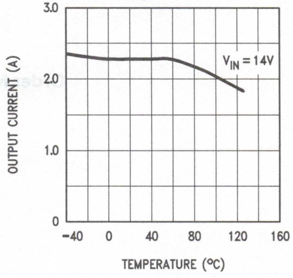
**Output Impedance**



**Maximum Power Dissipation (TO-220)**

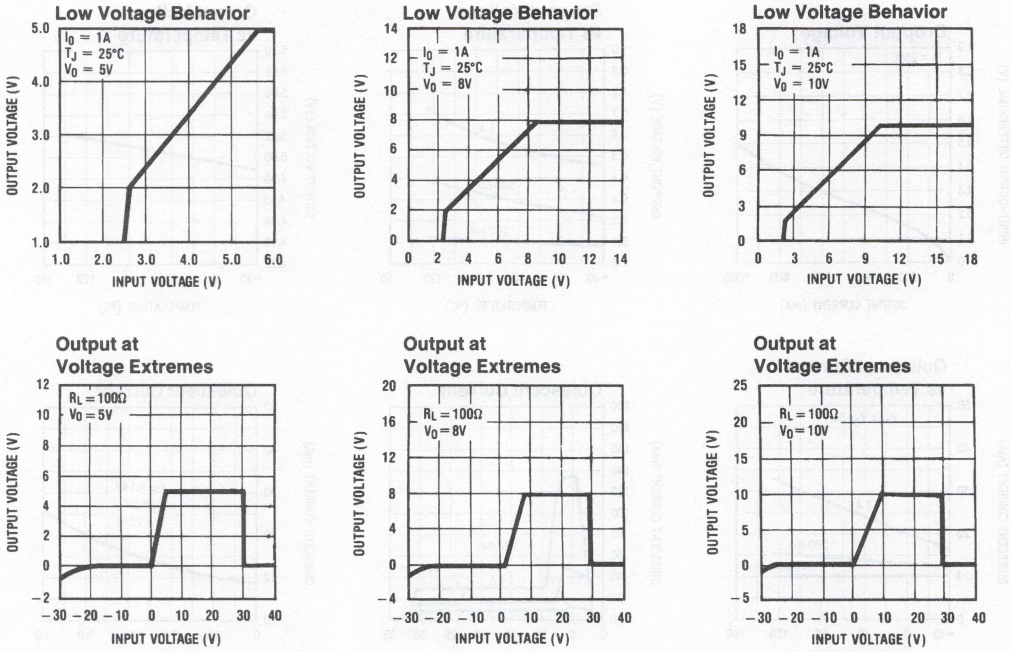


**Peak Output Current**



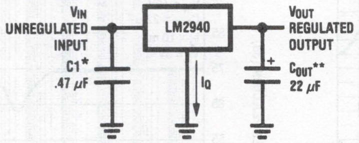
TL/H/8822–4

## Typical Performance Characteristics (Continued)



TL/H/8822-5

## Typical Application


$V_{IN}$
UNREGULATED INPUT
LM2940
$V_{OUT}$
REGULATED OUTPUT
C1*
.47 μF
$I_Q$
+
$C_{OUT}$**
22 μF

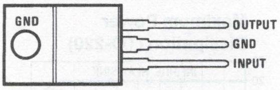
*Required if regulator is located far from power supply filter.

**$C_{OUT}$ must be at least 22 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and should have an ESR less than 1Ω to maintain stability.

TL/H/8822-3

## Connection Diagram

**(TO-220) Plastic Package**


GND
OUTPUT
GND
INPUT

TL/H/8822-2

**Front View**

**Order Number LM2940T-5.0, LM2940T-8.0, LM2940T-10**

**See NS Package Number T03B**

## Definition of Terms

**Dropout Voltage:** The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at ($V_O$ + 5V) input, dropout voltage is dependent upon load current and junction temperature.

**Input Voltage:** The DC voltage applied to the input terminals with respect to ground.

**Input-Output Differential:** The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation:** The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation:** The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability:** Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage:** The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current:** That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection:** The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

**Temperature Stability of $V_O$:** The percentange change in output voltage for a thermal variation from room temperature to either temperature extreme.

1

National Semiconductor Corporation

**PRELIMINARY**

# LM2984C Microprocessor Power Supply System

## General Description

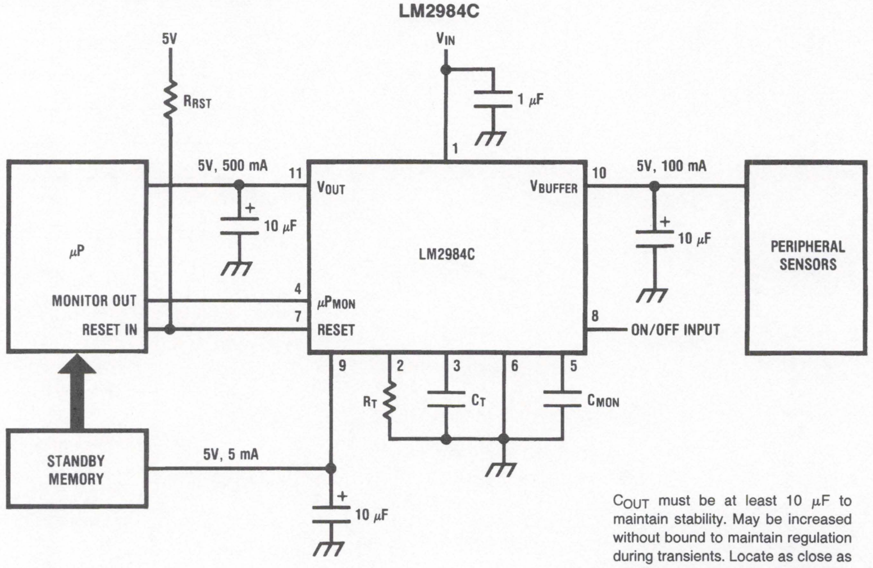
The LM2984C positive voltage regulator features three independent and tracking outputs capable of delivering the power for logic circuits, peripheral sensors and standby memory in a typical microprocessor system. The LM2984C includes circuitry which monitors both its own high-current output and also an external μP. If any error conditions are sensed in either, a reset error flag is set and maintained until the malfunction terminates. Since these functions are included in the same package with the three regulators, a great saving in board space can be realized in the typical microprocessor system. The LM2984C also features very low dropout voltages on each of its three regulator outputs (0.6V at the rated output current). Furthermore, the quiescent current can be reduced to 1 mA in the standby mode.

Designed also for vehicular applications, the LM2984C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. Familiar regulator features such as short circuit and thermal overload protection are also provided. Fixed outputs of 5V are available in the plastic TO-220 power package.

## Features

- Three low dropout tracking regulators
- Output current in excess of 500 mA
- Low quiescent current standby regulator
- Microprocessor malfunction RESET flag
- Delayed RESET on power-up
- Accurate pretrimmed 5V outputs
- Reverse battery protection
- Overvoltage protection
- Reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current outputs
- 100% electrical burn-in in thermal limit

## Typical Application Circuit



**Order Number LM2984CT**
**See NS Package Number TA11A**

$C_{OUT}$ must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

TL/H/8821–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| Survival Voltage (<100 ms) | 35V |
| Operational Voltage | 26V |
| Internal Power Dissipation | Internally Limited |
| Operating Temperature Range ($T_A$) | 0°C to +125°C |
| Maximum Junction Temperature (Note 1) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 230°C |

ESD rating is to be determined.

## Electrical Characteristics

$V_{IN} = 14V$, $I_{OUT} = 5$ mA, $C_{OUT} = 10$ μF, $T_j = 25°C$ (Note 6) unless otherwise indicated

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| **$V_{OUT}$ (Pin 11)** | | | | | |
| Output Voltage | 5 mA ≤ $I_o$ ≤ 500 mA<br>6V ≤ $V_{IN}$ ≤ 26V | 5.00 | 4.85<br>5.15 | 4.75<br>5.25 | $V_{min}$<br>$V_{max}$ |
| Line Regulation | 9V ≤ $V_{IN}$ ≤ 16V | 2 | 25 | | $mV_{max}$ |
| | 7V ≤ $V_{IN}$ ≤ 26V | 5 | 50 | | $mV_{max}$ |
| Load Regulation | 5 mA ≤ $I_{OUT}$ ≤ 500 mA | 12 | 50 | | $mV_{max}$ |
| Output Impedance | 250 $mA_{dc}$ and 10 $mA_{rms}$,<br>$f_o$ = 120 Hz | 24 | | | mΩ |
| Quiescent Current | $I_{OUT}$ = 500 mA | 38 | 100 | | $mA_{max}$ |
| | $I_{OUT}$ = 250 mA | 14 | 50 | | $mA_{max}$ |
| Output Noise Voltage | 10 Hz–100 kHz, $I_{OUT}$ = 100 mA | 100 | | | μV |
| Long Term Stability | | 20 | | | mV/1000 hr |
| Ripple Rejection | $f_o$ = 120 Hz | 70 | 60 | | $dB_{min}$ |
| Dropout Voltage | $I_{OUT}$ = 500 mA | 0.53 | 0.80 | 1.00 | $V_{max}$ |
| | $I_{OUT}$ = 250 mA | 0.28 | 0.50 | 0.60 | $V_{max}$ |
| Current Limit | | 0.92 | 0.75 | | $A_{min}$ |
| Maximum Operational Input Voltage | Continuous DC | 32 | 26 | 26 | $V_{min}$ |
| Maximum Line Transient | $V_{OUT}$ ≤ 6V, $R_{OUT}$ = 100Ω | 45 | 35 | 35 | $V_{min}$ |
| Reverse Polarity Input Voltage DC | $V_{OUT}$ ≥ −0.6V, $R_{OUT}$ = 100Ω | −30 | −15 | −15 | $V_{min}$ |
| Reverse Polarity Input Voltage Transient | T ≤ 100 ms, $R_{OUT}$ = 100Ω | −55 | −35 | −35 | $V_{min}$ |

## Electrical Characteristics (Continued)

$V_{IN} = 14V$, $I_{buf} = 5$ mA, $C_{buf} = 10$ $\mu$F, $T_j = 25°C$ (Note 6) unless otherwise indicated

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| **$V_{buffer}$ (Pin 10)** | | | | | |
| Output Voltage | $5\text{ mA} \leq I_o \leq 100\text{ mA}$<br>$6V \leq V_{IN} \leq 26V$ | 5.00 | 4.85<br>5.15 | 4.75<br>5.25 | $V_{min}$<br>$V_{max}$ |
| Line Regulation | $9V \leq V_{IN} \leq 16V$ | 2 | 25 | | $mV_{max}$ |
| | $7V \leq V_{IN} \leq 26V$ | 5 | 50 | | $mV_{max}$ |
| Load Regulation | $5\text{ mA} \leq I_{buf} \leq 100\text{ mA}$ | 15 | 50 | | $mV_{max}$ |
| Output Impedance | $50\text{ mA}_{dc}$ and $10\text{ mA}_{rms}$, | 200 | | | mΩ |
| Quiescent Current | $I_{buf} = 100$ mA | 8.0 | 15.0 | | $mA_{max}$ |
| Output Noise Voltage | 10 Hz–100 kHz, $I_{OUT} = 100$ mA | 100 | | | μV |
| Long Term Stability | | 20 | | | mV/1000 hr |
| Ripple Rejection | $f_o = 120$ Hz | 70 | 60 | | $dB_{min}$ |
| Dropout Voltage | $I_{buf} = 100$ mA | 0.35 | 0.50 | 0.60 | $V_{max}$ |
| Current Limit | | 0.23 | 0.15 | | $A_{min}$ |
| Maximum Operational Input Voltage | Continuous DC | 32 | 26 | 26 | $V_{min}$ |
| Maximum Line Transient | $V_{buf} \leq 6V$, $R_{buf} = 100\Omega$ | 45 | 35 | 35 | $V_{min}$ |
| Reverse Polarity Input Voltage DC | $V_{buf} \geq -0.6V$, $R_{buf} = 100\Omega$ | −30 | −15 | −15 | $V_{min}$ |
| Reverse Polarity Input Voltage Transient | $T \leq 100$ ms, $R_{buf} = 100\Omega$ | −55 | −35 | −35 | $V_{min}$ |

## Electrical Characteristics

$V_{IN} = 14V$, $I_{stby} = 1$ mA, $C_{stby} = 10$ $\mu$F, $T_j = 25°C$ (Note 6) unless otherwise indicated

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| **$V_{standby}$ (Pin 9)** | | | | | |
| Output Voltage | $1\text{ mA} \leq I_o \leq 7.5\text{ mA}$<br>$6V \leq V_{IN} \leq 26V$ | 5.00 | 4.85<br>5.15 | 4.75<br>5.25 | $V_{min}$<br>$V_{max}$ |
| Line Regulation | $9V \leq V_{IN} \leq 16V$ | 2 | 25 | | $mV_{max}$ |
| | $7V \leq V_{IN} \leq 26V$ | 5 | 50 | | $mV_{max}$ |
| Load Regulation | $0.5\text{ mA} \leq I_{stby} \leq 7.5\text{ mA}$ | 6 | 50 | | $mV_{max}$ |
| Output Impedance | $5\text{ mA}_{dc}$ and $1\text{ mA}_{rms}$, $f_o = 120$ Hz | 0.9 | | | Ω |
| Quiescent Current | $I_{stby} = 7.5$ mA | 1.2 | 2.0 | | $mA_{max}$ |
| | $I_{stby} = 2$ mA | 0.9 | 1.5 | | $mA_{max}$ |

## Electrical Characteristics (Continued)

$V_{IN} = 14V$, $I_{stby} = 1$ mA, $C_{stby} = 10$ $\mu$F, $T_j = 25°C$ (Note 6) unless otherwise indicated

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| $V_{standby}$ (Continued) | | | | | |
| Output Noise Voltage | 10 Hz–100 kHz, $I_{stby} = 1$ mA | 100 | | | $\mu$V |
| Long Term Stability | | 20 | | | mV/1000 hr |
| Ripple Rejection | $f_o = 120$ Hz | 70 | 60 | | $dB_{min}$ |
| Dropout Voltage | $I_{stby} = 1$ mA | 0.26 | 0.50 | 0.50 | $V_{max}$ |
| Dropout Voltage | $I_{stby} = 7.5$ mA | 0.38 | 0.60 | 0.70 | $V_{max}$ |
| Current Limit | | 15 | 12 | | $mA_{min}$ |
| Maximum Operational Input Voltage | $4.5V \leq V_{stby} \leq 6V$<br>$R_{stby} = 1000\Omega$ | 45 | 35 | 35 | $V_{min}$ |
| Maximum Line Transient | $V_{stby} \leq 6V$,<br>$R_{stby} = 1000\Omega$ | 45 | 35 | 35 | $V_{min}$ |
| Reverse Polarity Input Voltage DC | $V_{stby} \geq -0.6V$,<br>$R_{stby} = 1000\Omega$ | −30 | −15 | −15 | $V_{min}$ |
| Reverse Polarity Input Voltage Transient | $T \leq 100$ ms, $R_{stby} = 1000\Omega$ | −55 | −35 | −35 | $V_{min}$ |

## Electrical Characteristics

$V_{IN} = 14V$, $T_j = 25°C$ (Note 6) $C_{OUT} = 10$ $\mu$F, $C_{buf} = 10$ $\mu$F, $C_{stby} = 10$ $\mu$F unless otherwise specified

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| **Tracking and Isolation** | | | | | |
| Tracking $V_{OUT}-V_{stby}$ | $I_{OUT} \leq 500$ mA, $I_{buf} = 5$ mA,<br>$I_{stby} \leq 7.5$ mA | ±30 | ±100 | | $mV_{max}$ |
| Tracking $V_{buf}-V_{stby}$ | $I_{OUT} = 5$ mA, $I_{buf} \leq 100$ mA,<br>$I_{stby} \leq 7.5$ mA | ±30 | ±100 | | $mV_{max}$ |
| Tracking $V_{OUT}-V_{buf}$ | $I_{OUT} \leq 500$ mA, $I_{buf} \leq 100$ mA,<br>$I_{stby} = 1$ mA | ±30 | ±100 | | $mV_{max}$ |
| Isolation* $V_{buf}$ from $V_{OUT}$ | $R_{OUT} = 1\Omega$, $I_{buf} \leq 100$ mA | 5.00 | 4.50<br>5.50 | | $V_{min}$<br>$V_{max}$ |
| Isolation* $V_{stby}$ from $V_{OUT}$ | $R_{OUT} = 1\Omega$, $I_{stby} \leq 7.5$ mA | 5.00 | 4.50<br>5.50 | | $V_{min}$<br>$V_{max}$ |
| Isolation* $V_{OUT}$ from $V_{buf}$ | $R_{buf} = 1\Omega$, $I_{OUT} \leq 500$ mA | 5.00 | 4.50<br>5.50 | | $V_{min}$<br>$V_{max}$ |
| Isolation* $V_{stby}$ from $V_{buf}$ | $R_{buf} = 1\Omega$, $I_{stby} \leq 7.5$ mA | 5.00 | 4.50<br>5.50 | | $V_{min}$<br>$V_{max}$ |

*Isolation refers to the ability of the specified output to remain within the tested limits when the other output is shorted to ground.

## Electrical Characteristics (Continued)

$V_{IN}$ = 14V, $I_{OUT}$ = 5 mA, $I_{buf}$ = 5 mA, $I_{stby}$ = 5 mA, $R_t$ = 130k, $C_t$ = 0.33 μF, $C_{mon}$ = 0.47 μF, $T_j$ = 25°C (Note 6) unless otherwise specified

| Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units |
|---|---|---|---|---|---|
| **Computer Monitor/Reset Functions** | | | | | |
| $I_{reset}$ Low | $V_{IN}$ = 4V, $V_{rst}$ = 0.4V | 5 | 2 | 1 | $mA_{min}$ |
| $V_{reset}$ Low | $V_{IN}$ = 4V, $I_{rst}$ = 1 mA | 0.10 | 0.40 | | $V_{max}$ |
| $R_{t\ voltage}$ | (Pin 2) | 1.22 | 1.15 | | $V_{min}$ |
| | | 1.22 | 1.30 | | $V_{max}$ |
| Power On Reset Delay | $V\mu P_{mon}$ = 5V<br>($T_{dly}$ = 1.2 $R_t$ $C_t$) | 50 | 45 | | $ms_{min}$ |
| | | 50 | 55 | | $ms_{max}$ |
| $V_{OUT}$ Low Reset Threshold | (Note 4) | 4.00 | 3.60 | | $V_{min}$ |
| | | 4.00 | 4.40 | | $V_{max}$ |
| $V_{OUT}$ High Reset Threshold | (Note 4) | 5.50 | 5.25 | | $V_{min}$ |
| | | 5.50 | 6.00 | | $V_{max}$ |
| Reset Output Leakage | $V\mu P_{mon}$ = 5V, $V_{rst}$ = 12V | 0.01 | 1 | | $\mu A_{max}$ |
| $\mu P_{mon}$ Input Current (Pin 4) | $V\mu P_{mon}$ = 2.4V | 7.5 | 25 | | $\mu A_{max}$ |
| | $V\mu P_{mon}$ = 0.4V | 0.01 | 10 | | $\mu A_{max}$ |
| $\mu P_{mon}$ Input Threshold Voltage | | 1.22 | 0.80 | 0.80 | $V_{min}$ |
| | | 1.22 | 2.00 | 2.00 | $V_{max}$ |
| μP Monitor Reset Oscillator Period | $V\mu P_{mon}$ = 0V<br>($T_{window}$ = 0.82 $R_tC_{mon}$) | 50 | 45 | | $ms_{min}$ |
| | | 50 | 55 | | $ms_{max}$ |
| μP Monitor Reset Oscillator Pulse Width | $V\mu P_{mon}$ = 0V<br>($RESET_{pw}$ = 2000 $C_{mon}$) | 1.0 | 0.7 | 0.5 | $ms_{min}$ |
| | | 1.0 | 1.3 | 2.0 | $ms_{max}$ |
| Minimum μP Monitor Input Pulse Width | (Note 5) | 2 | | | $\mu s_{max}$ |
| Reset Fall Time | $R_{rst}$ = 10k, $V_{rst}$ = 5V, $C_{rst}$ ≤ 10 pF | 0.20 | 1.00 | | $\mu s_{max}$ |
| Reset Rise Time | $R_{rst}$ = 10k, $V_{rst}$ = 5V, $C_{rst}$ ≤ 10 pF | 0.60 | 1.00 | | $\mu s_{max}$ |
| On/Off Switch Input Current (Pin 8) | $V_{ON}$ = 2.4V | 7.5 | 25 | | $\mu A_{max}$ |
| | $V_{ON}$ = 0.4V | 0.01 | 10 | | $\mu A_{max}$ |
| On/Off Switch Input Threshold Voltage | | 1.22 | 0.80 | 0.80 | $V_{min}$ |
| | | 1.22 | 2.00 | 2.00 | $V_{max}$ |

**Note 1:** Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 40°C/W.

**Note 2:** Tested Limits are guaranteed and 100% production tested.

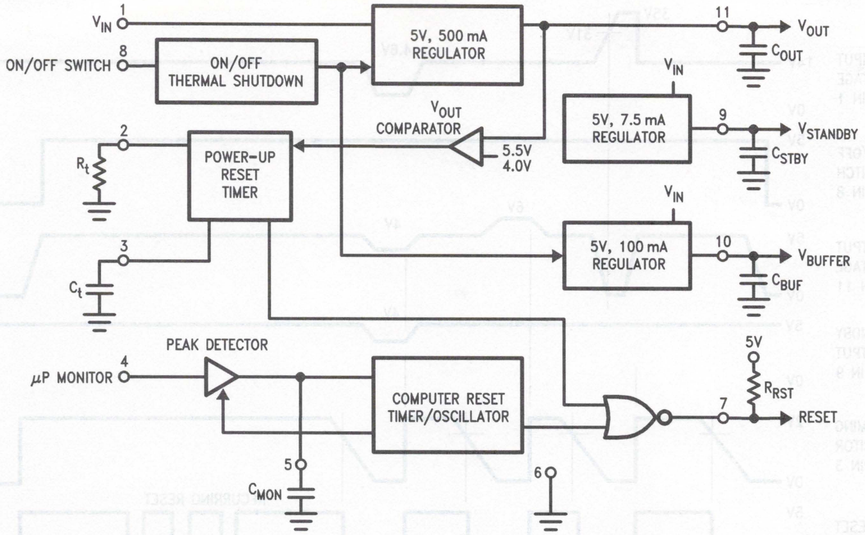
**Note 3:** Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

**Note 4:** An internal comparator detects when the main regulator output ($V_{OUT}$) drops below 4.0V or rises above 5.5V. If either condition exists at the output, the Reset Error Flag is held low until the error condition has terminated. The Reset Error Flag is then allowed to go high again after a delay set by $R_t$ and $C_t$. (See Applications Section.)

**Note 5:** This parameter is a measure of how short a pulse can be detected at the μP Monitor Input. This parameter is primarily influenced by the value of $C_{mon}$. (See Typical Performance Characteristics and Applications Section.)

**Note 6:** To ensure constant junction temperature, low duty cycle pulse testing is used.

## Block Diagram


VIN 1
ON/OFF SWITCH 8
ON/OFF THERMAL SHUTDOWN
5V, 500 mA REGULATOR
11
VOUT
COUT
VIN
VOUT COMPARATOR
5.5V
4.0V
5V, 7.5 mA REGULATOR
9
VSTANDBY
CSTBY
2
Rt
POWER-UP RESET TIMER
3
Ct
VIN
5V, 100 mA REGULATOR
10
VBUFFER
CBUF
PEAK DETECTOR
4
μP MONITOR
COMPUTER RESET TIMER/OSCILLATOR
5V
RRST
7
RESET
5
CMON
6

TL/H/8821-2

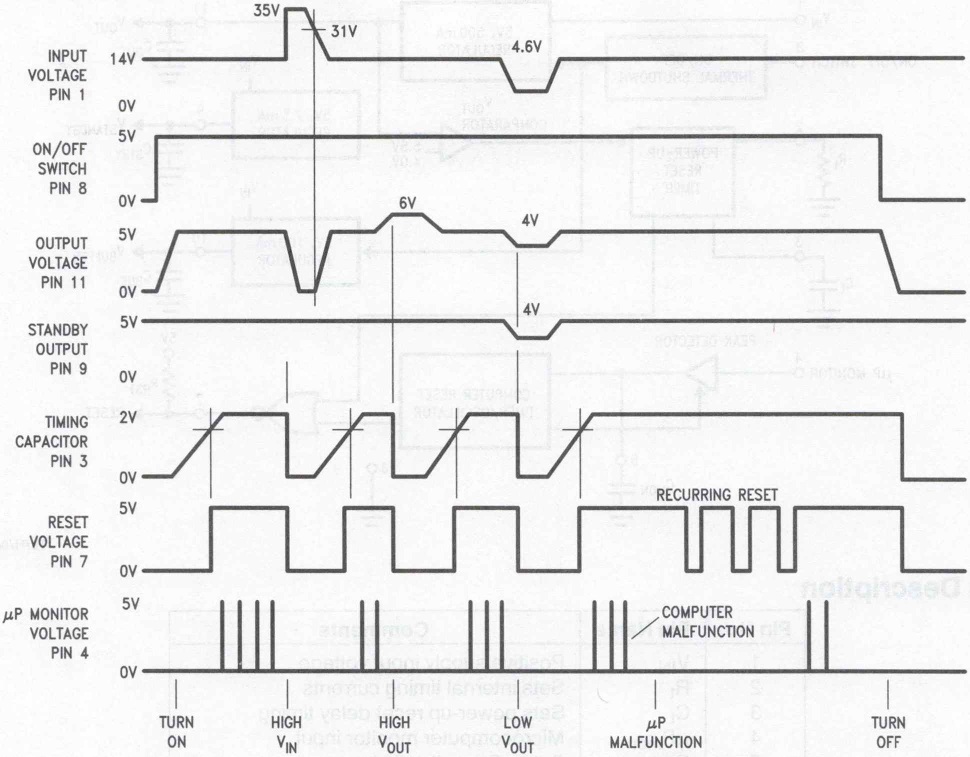
## Pin Description

| Pin No. | Pin Name | Comments |
|---|---|---|
| 1 | $V_{IN}$ | Positive supply input voltage |
| 2 | $R_t$ | Sets internal timing currents |
| 3 | $C_t$ | Sets power-up reset delay timing |
| 4 | $\mu P_{mon}$ | Microcomputer monitor input |
| 5 | $C_{mon}$ | Sets μC monitor timing |
| 6 | Ground | Regulator ground |
| 7 | Reset | Reset error flag output |
| 8 | ON/OFF | Enables/disables high current regulators |
| 9 | $V_{standby}$ | Standby regulator output (7.5 mA) |
| 10 | $V_{buffer}$ | Buffer regulator output (100 mA) |
| 11 | $V_{OUT}$ | Main regulator output (500 mA) |

## External Components

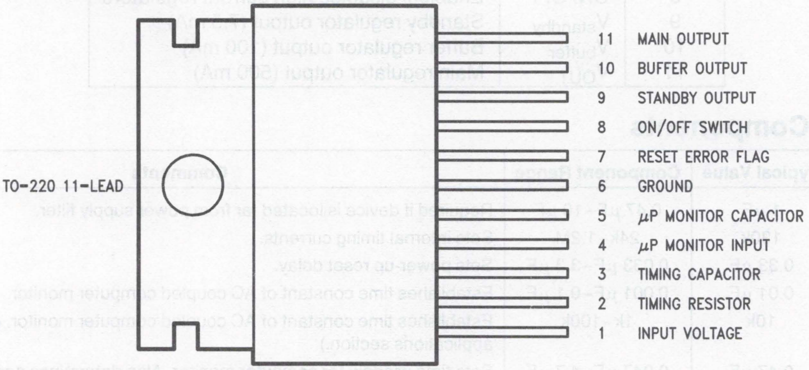
| Component | Typical Value | Component Range | Comments |
|---|---|---|---|
| $C_{IN}$ | 1 μF | 0.47 μF–10 μF | Required if device is located far from power supply filter. |
| $R_t$ | 130k | 24k–1.2M | Sets internal timing currents. |
| $C_t$ | 0.33 μF | 0.033 μF–3.3 μF | Sets power-up reset delay. |
| $C_{tc}$ | 0.01 μF | 0.001 μF–0.1 μF | Establishes time constant of AC coupled computer monitor. |
| $R_{tc}$ | 10k | 1k–100k | Establishes time constant of AC coupled computer monitor. (See applications section.) |
| $C_{mon}$ | 0.47 μF | 0.047 μF–4.7 μF | Sets time window for computer monitor. Also determines period and pulse width of computer malfunction reset. (See applications section.) |
| $R_{rst}$ | 10k | 5k–100k | Load for open collector reset output. Determined by computer reset input requirements. |
| $C_{stby}$ | 10 μF | 10 μF–no bound | A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions. |
| $C_{buf}$ | 10 μF | 10 μF–no bound | A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions. |
| $C_{OUT}$ | 10 μF | 10 μF–no bound | A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions. |

## Typical Circuit Waveforms



TL/H/8821-3

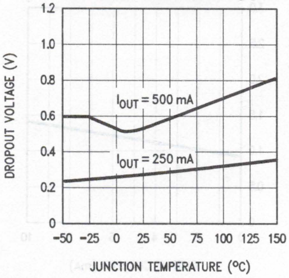
## Connection Diagram

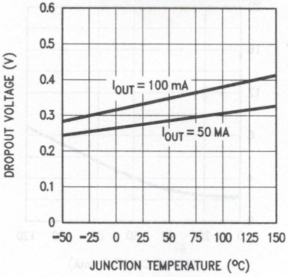

TO-220 11-LEAD
11 MAIN OUTPUT
10 BUFFER OUTPUT
9 STANDBY OUTPUT
8 ON/OFF SWITCH
7 RESET ERROR FLAG
6 GROUND
5 μP MONITOR CAPACITOR
4 μP MONITOR INPUT
3 TIMING CAPACITOR
2 TIMING RESISTOR
1 INPUT VOLTAGE

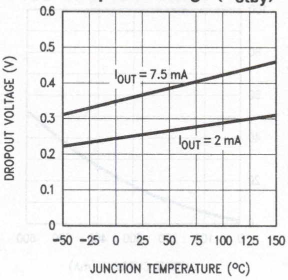
TL/H/8821-4

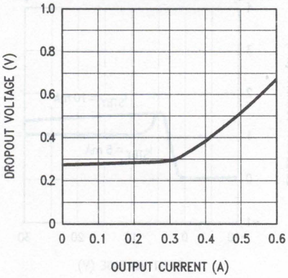
**Order Number LM2984CT**
**See NS Package Number T11A**

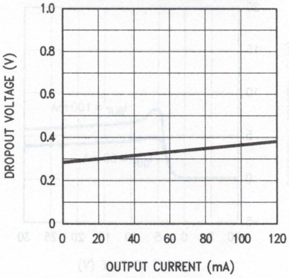
## Typical Performance Characteristics

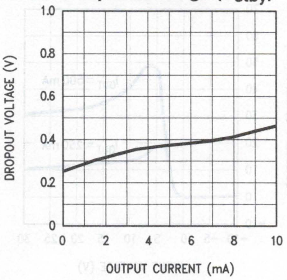


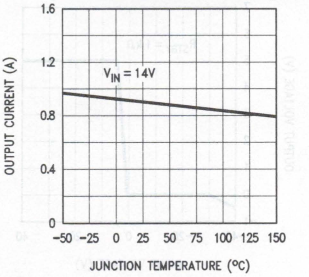


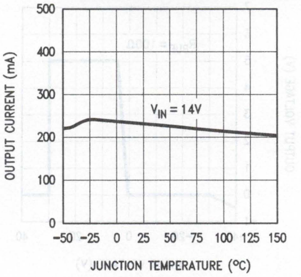


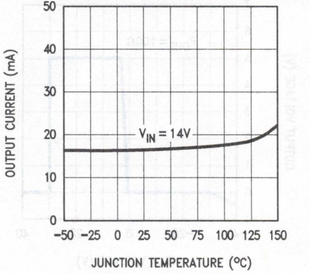


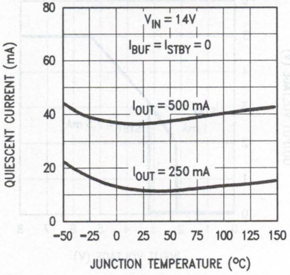


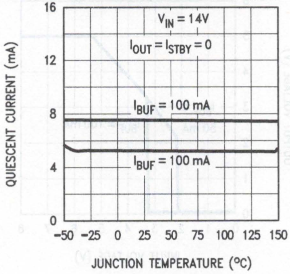


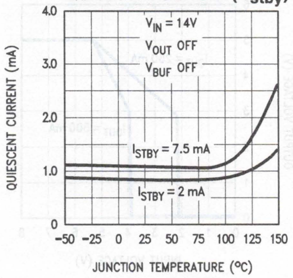












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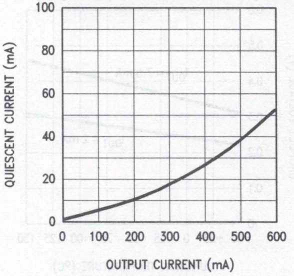
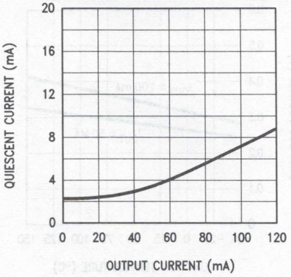
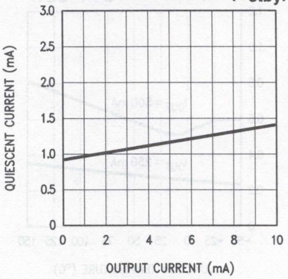
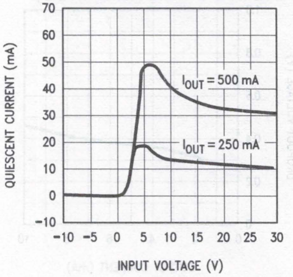
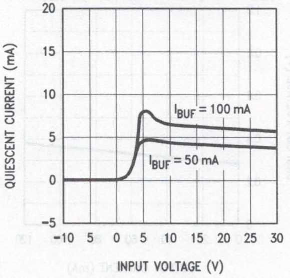
## Typical Performance Characteristics (Continued)

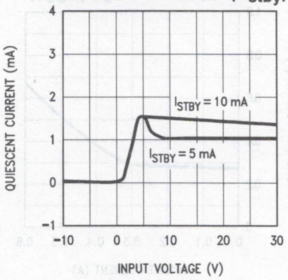

Quiescent Current ($V_{OUT}$)

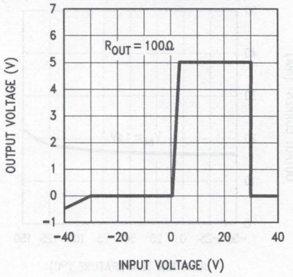

Quiescent Current ($V_{buf}$)

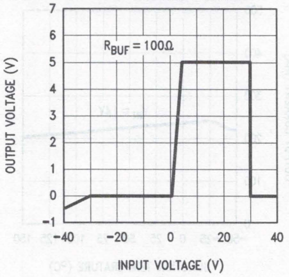

Quiescent Current ($V_{stby}$)

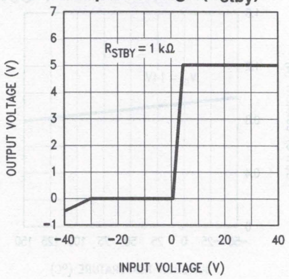

Quiescent Current ($V_{OUT}$)

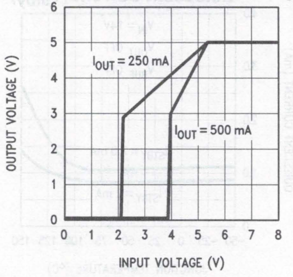

Quiescent Current ($V_{buf}$)

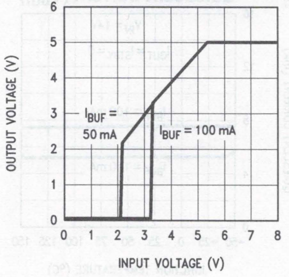

Quiescent Current ($V_{stby}$)

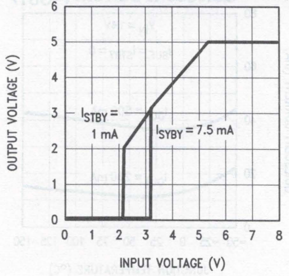

Output Voltage ($V_{OUT}$)


Output Voltage ($V_{buf}$)


Output Voltage ($V_{stby}$)


Low Voltage Behavior ($V_{OUT}$)


Low Voltage Behavior ($V_{buf}$)


Low Voltage Behavior ($V_{stby}$)

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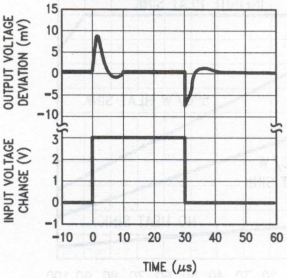
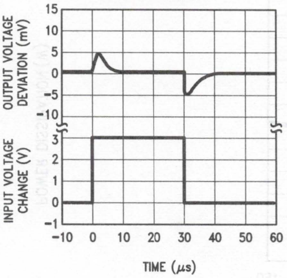
# Typical Performance Characteristics (Continued)

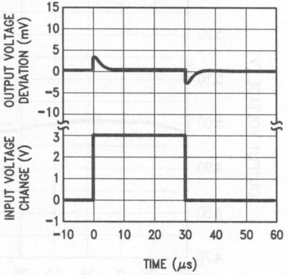
**Line Transient Response ($V_{OUT}$)**



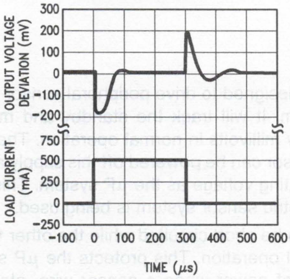
**Line Transient Response ($V_{buf}$)**



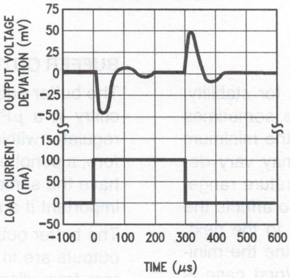
**Line Transient Response ($V_{stby}$)**



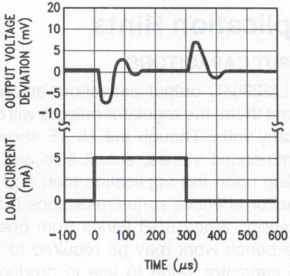
**Load Transient Response ($V_{OUT}$)**



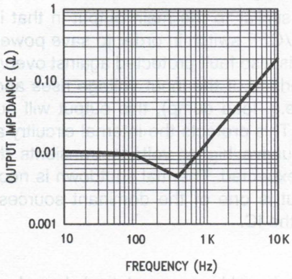
**Load Transient Response ($V_{buf}$)**



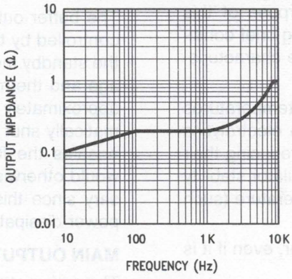
**Load Transient Response ($V_{stby}$)**



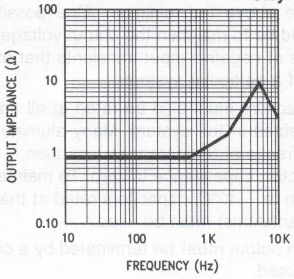
**Output Impedance ($V_{OUT}$)**



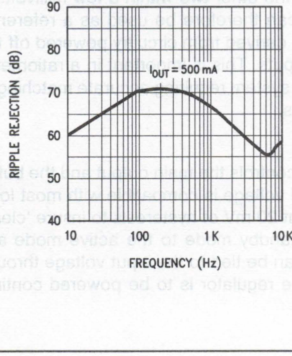
**Output Impedance ($V_{buf}$)**



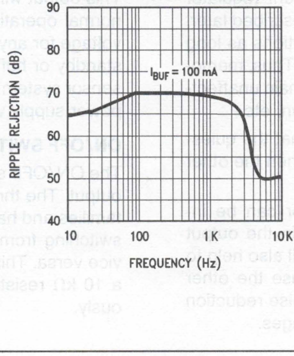
**Output Impedance ($V_{stby}$)**



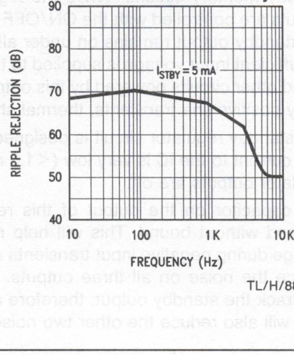
**Ripple Rejection ($V_{OUT}$)**



**Ripple Rejection ($V_{buf}$)**

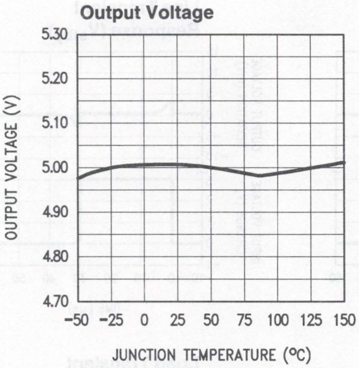


**Ripple Rejection ($V_{stby}$)**

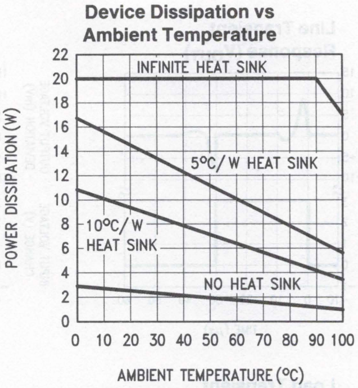


TL/H/8821–7

## Typical Performance Characteristics (Continued)



TL/H/8821-8



TL/H/8821-9

## Application Hints

### OUTPUT CAPACITORS

The LM2984C output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10 μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also affects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst case is usually determined at the minimum ambient temperature and the maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

Each output **must** be terminated by a capacitor, even if it is not used.

### STANDBY OUTPUT

The standby output is intended for use in systems requiring standby memory circuits. While the high current regulator outputs are controlled with the ON/OFF pin described later, the standby output remains on under all conditions as long as sufficient input voltage is supplied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5 mA) when the other regulator outputs are off.

The capacitor on the output of this regulator can be increased without bound. This will help maintain the output voltage during negative input transients and will also help to reduce the noise on all three outputs. Because the other two track the standby output: therefore any noise reduction here will also reduce the other two noise voltages.

### BUFFER OUTPUT

The buffer output is designed to drive peripheral sensor circuitry in a μP system. It will track the standby and main regulator within a few millivolts in normal operation. Therefore, a peripheral sensor can be powered off this supply and have the same operating voltage as the μP system. This is important if a ratiometric sensor system is being used.

The buffer output can be short circuited while the other two outputs are in normal operation. This protects the μP system from disruption of power when a sensor wire, etc. is temporarily shorted to ground, i.e. only the sensor signal would be interrupted, while the μP and memory circuits would remain operational.

The buffer output is similar to the main output in that it is controlled by the ON/OFF switch in order to save power in the standby mode. It is also fault protected against overvoltage and thermal overload. If the input voltage rises above approximately 30V (e.g. load dump), this output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is necessary since this output is one of the dominant sources of power dissipation in the IC.

### MAIN OUTPUT

The main output is designed to power relatively large loads, i.e. approximately 500 mA. It is therefore also protected against overvoltage and thermal overload.

This output will track the other two within a few millivolts in normal operation. It can therefore be used as a reference voltage for any signal derived from circuitry powered off the standby or buffer outputs. This is important in a ratiometric sensor system or any system requiring accurate matching of power supply voltages.

### ON/OFF SWITCH

The ON/OFF switch controls the main output and the buffer output. The threshold voltage is compatible with most logic families and has about 20 mV of hysteresis to insure 'clean' switching from the standby mode to the active mode and vice versa. This pin can be tied to the input voltage through a 10 kΩ resistor if the regulator is to be powered continuously.

## Application Hints (Continued)

### POWER DOWN OVERRIDE

Another possible approach is to use a diode in series with the ON/OFF signal and another in series with the main output in order to maintain power for some period of time after the ON/OFF signal has been removed (see *Figure 1*). When the ON/OFF switch is initially pulled high through diode D1, the main output will turn on and supply power through diode D2 to the ON/OFF switch effectively latching the main output. An open collector transistor Q1 is connected to the ON/OFF pin along with the two diodes and forces the regulators off after a period of time determined by the $\mu$P. In this way, the $\mu$P can override a power down command and store data, do housekeeping, etc. before reverting back to the standby mode.

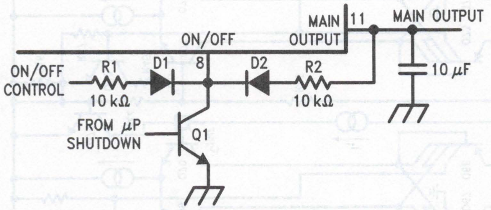


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**FIGURE 1. Power Down Override**

### RESET OUTPUT

This output is an open collector NPN transistor which is forced low whenever an error condition is present at the main output or when a $\mu$P error is sensed (see $\mu$P Monitor section). If the main output voltage drops below 4V or rises above 5.5V, the RESET output is forced low and held low for a period of time set by two external components, $R_t$ and $C_t$. There is a slight amount of hysteresis in these two threshold voltages so that the RESET output has a fast rise and fall time compatible with the requirements of most $\mu$P RESET inputs.

### DELAYED RESET

Resistor $R_t$ and capacitor $C_t$ set the period of time that the RESET output is held low after a main output error condition has been sensed. The delay is given by the formula:

$$T_{dly} = 1.2\, R_t C_t \text{ (seconds)}$$

The delayed RESET will be initiated any time the main output is outside the 4V to 5.5V window, i.e. during power-up, short circuit, overvoltage, low line, thermal shutdown or power-down. The $\mu$P is therefore RESET whenever the output voltage is out of regulation. (It is important to note that a RESET is only initiated when the main output is in error. The buffer and standby outputs are not directly monitored for error conditions.)

### $\mu$P MONITOR RESET

There are two distinct and independent error monitoring systems in the LM2984C. The one described above monitors the main regulator output and initiates a delayed RESET whenever this output is in error. The other error monitoring system is the $\mu$P watchdog. These two systems are OR'd together internally and both force the RESET output low when either type of error occurs.

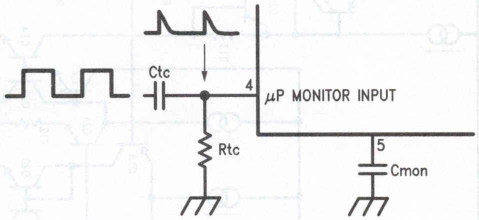
This watchdog circuitry continuously monitors a pin on the $\mu$P that generates a positive going pulse during normal operation. The period of this pulse is typically on the order of milliseconds and the pulse width is typically on the order of 10's of microseconds. If this pulse ever disappears, the watchdog circuitry will time out and a RESET low will be sent to the $\mu$P. The time out period is determined by two external components, $R_t$ and $C_{mon}$, according to the formula:

$$T_{window} = 0.82\, R_t C_{mon} \text{ (seconds)}$$

The width of the RESET pulse is set by $C_{mon}$ and an internal resistor according to the following:

$$RESET_{pw} = 2000\, C_{mon} \text{ (seconds)}$$

A square wave signal can also be monitored for errors by filtering the $C_{mon}$ input such that only the positive edges of the signal are detected. *Figure 2* is a schematic diagram of a typical circuit used to differentiate the input signal. Resistor $R_{tc}$ and capacitor $C_{tc}$ pass only the rising edge of the square wave and create a short positive pulse suitable for the $\mu$P monitor input. If the incoming signal continues in a high state or in a low state for too long a period of time, a RESET low will be generated.



TL/H/8821–11

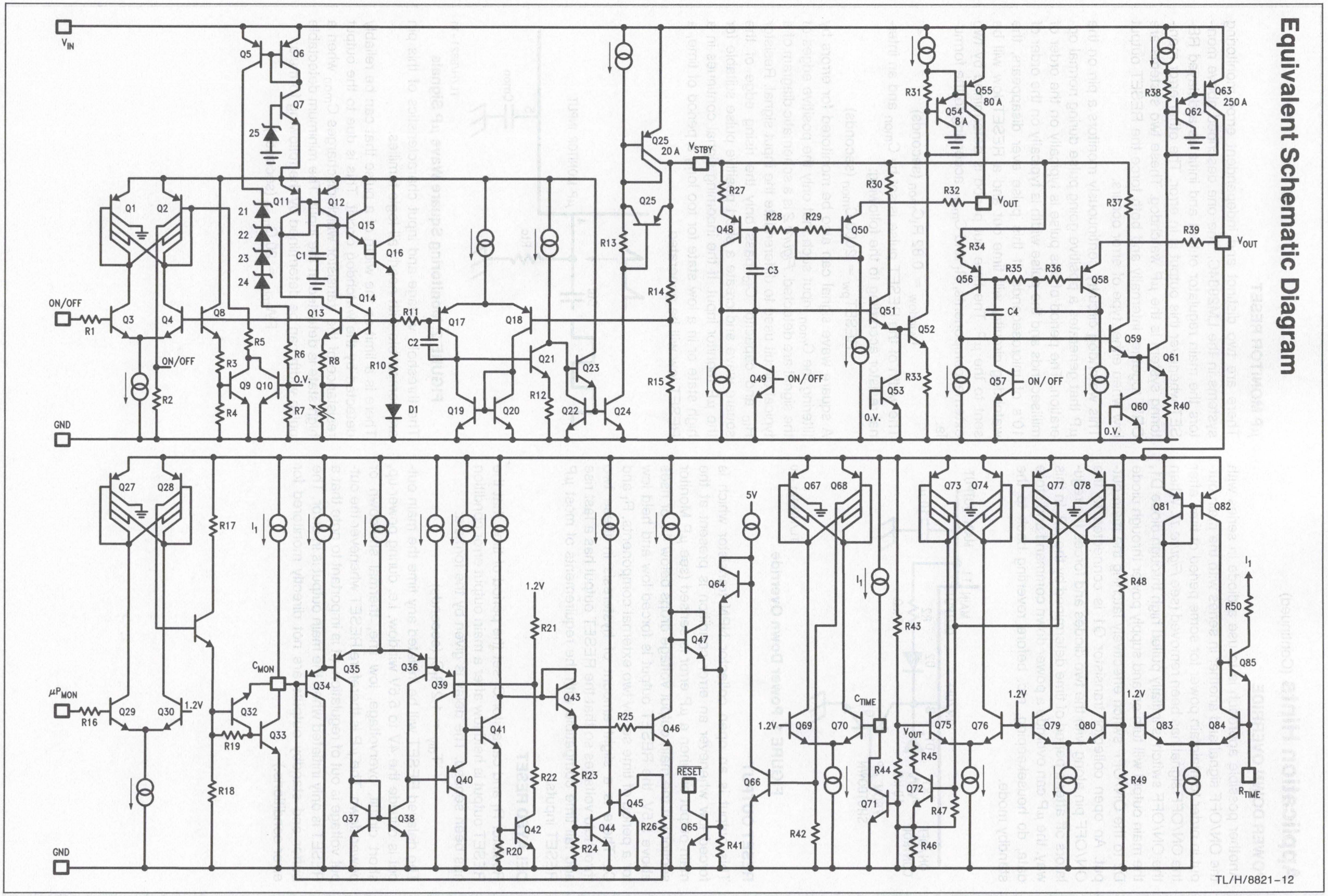
**FIGURE 2. Monitoring Square Wave $\mu$P Signals**

The threshold voltage and input characteristics of this pin are compatible with nearly all logic families.

There is a limit on the width of a pulse that can be reliably detected by the watchdog circuit. This is due to the output resistance of the transistor which discharges $C_{mon}$ when a high state is detected at the input. The minimum detectable pulse width can be determined by the following formula:

$$PW_{min} = 20\, C_{mon} \text{ (seconds)}$$

## Equivalent Schematic Diagram


VIN
Q5
Q6
Q7
25
Q1
Q2
Q11
Q12
21
22
23
24
C1
Q15
Q16
Q14
Q13
Q8
ON/OFF
R1
Q3
Q4
ON/OFF
R2
R3
R5
Q9
Q10
R4
R6
R8
O.V.
R7
R10
D1
R11
C2
Q17
Q18
Q19
Q20
Q21
R12
Q22
Q23
Q24
Q25
20 A
Q25
R13
R14
R15
VSTBY
R27
Q48
R28
R29
C3
Q50
R30
R32
VOUT
Q51
Q52
Q49
ON/OFF
Q53
O.V.
R33
R31
Q55
80 A
Q54
8 A
R34
Q56
R35
R36
Q58
C4
Q57
ON/OFF
Q59
Q61
Q60
O.V.
R40
R37
R39
VOUT
R38
Q63
250 A
Q62
GND
Q27
Q28
R17
I1
μPMON
R16
Q29
Q30
1.2V
Q32
R19
Q33
R18
CMON
Q34
Q35
Q36
Q39
Q37
Q38
Q40
Q41
Q42
R20
1.2V
R21
R22
Q43
R23
R24
Q44
Q45
R25
Q46
R26
RESET
Q65
R41
5V
Q64
Q47
Q66
R42
Q67
Q68
Q69
1.2V
Q70
I1
CTIME
Q71
R44
R43
VOUT
R45
Q72
R47
R46
Q73
Q74
Q75
Q76
1.2V
Q77
Q78
Q79
Q80
R48
R49
1.2V
Q81
Q82
Q83
Q84
Q85
R50
I1
RTIME
GND

TL/H/8821-12

**National Semiconductor Corporation**

# LM78XX Series Voltage Regulators

## General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and mininize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

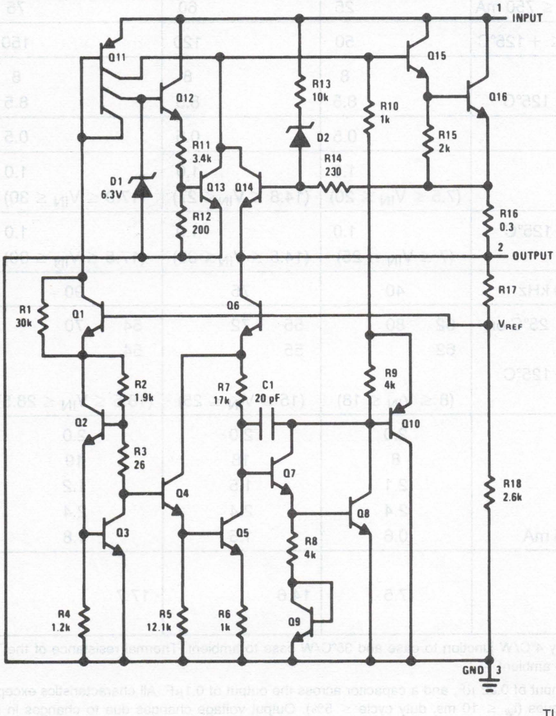
## Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

## Voltage Range

| | |
|---|---|
| LM7805C | 5V |
| LM7812C | 12V |
| LM7815C | 15V |

## Schematic and Connection Diagrams



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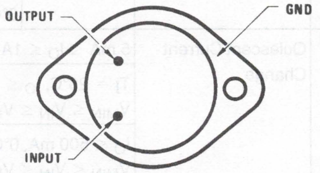
**Metal Can Package**
**TO-3 (K)**
**Aluminum**

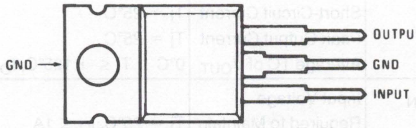


TL/H/7746–2

**Bottom View**

**Order Number LM7805CK,**
**LM7812CK or LM7815CK**
**See NS Package Number KC02A**

**Plastic Package**
**TO-220 (T)**



TL/H/7746–3

**Top View**

**Order Number LM7805CT,**
**LM7812CT or LM7815CT**
**See NS Package Number T03B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage ($V_O$ = 5V, 12V and 15V) | 35V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range ($T_A$) | 0°C to +70°C |
| Maximum Junction Temperature | |
| (K Package) | 150°C |
| (T Package) | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | |
| TO-3 Package K | 300°C |
| TO-220 Package T | 230°C |

## Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

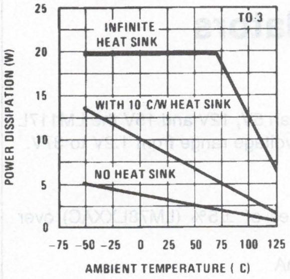
| | Output Voltage | | | | 5V | | | 12V | | | 15V | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Voltage (unless otherwise noted) | | | | 10V | | | 19V | | | 23V | | Units |
| **Symbol** | **Parameter** | **Conditions** | | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $V_O$ | Output Voltage | Tj = 25°C, 5 mA ≤ $I_O$ ≤ 1A | | 4.8 | 5 | 5.2 | 11.5 | 12 | 12.5 | 14.4 | 15 | 15.6 | V |
| | | $P_D$ ≤ 15W, 5 mA ≤ $I_O$ ≤ 1A | | 4.75 | | 5.25 | 11.4 | | 12.6 | 14.25 | | 15.75 | V |
| | | $V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | | (7.5 ≤ $V_{IN}$ ≤ 20) | | | (14.5 ≤ $V_{IN}$ ≤ 27) | | | (17.5 ≤ $V_{IN}$ ≤ 30) | | V |
| $\Delta V_O$ | Line Regulation | $I_O$ = 500 mA | Tj = 25°C | | 3 | 50 | | 4 | 120 | | 4 | 150 | mV |
| | | | $\Delta V_{IN}$ | | (7 ≤ $V_{IN}$ ≤ 25) | | | (14.5 ≤ $V_{IN}$ ≤ 30) | | | (17.5 ≤ $V_{IN}$ ≤ 30) | | V |
| | | | 0°C ≤ Tj ≤ +125°C | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | | (8 ≤ $V_{IN}$ ≤ 20) | | | (15 ≤ $V_{IN}$ ≤ 27) | | | (18.5 ≤ $V_{IN}$ ≤ 30) | | V |
| | | $I_O$ ≤ 1A | Tj = 25°C | | | 50 | | | 120 | | | 150 | mV |
| | | | $\Delta V_{IN}$ | | (7.5 ≤ $V_{IN}$ ≤ 20) | | | (14.6 ≤ $V_{IN}$ ≤ 27) | | | (17.7 ≤ $V_{IN}$ ≤ 30) | | V |
| | | | 0°C ≤ Tj ≤ +125°C | | | 25 | | | 60 | | | 75 | mV |
| | | | $\Delta V_{IN}$ | | (8 ≤ $V_{IN}$ ≤ 12) | | | (16 ≤ $V_{IN}$ ≤ 22) | | | (20 ≤ $V_{IN}$ ≤ 26) | | V |
| $\Delta V_O$ | Load Regulation | Tj = 25°C | 5 mA ≤ $I_O$ ≤ 1.5A | | 10 | 50 | | 12 | 120 | | 12 | 150 | mV |
| | | | 250 mA ≤ $I_O$ ≤ 750 mA | | | 25 | | | 60 | | | 75 | mV |
| | | 5 mA ≤ $I_O$ ≤ 1A, 0°C ≤ Tj ≤ +125°C | | | | 50 | | | 120 | | | 150 | mV |
| $I_Q$ | Quiescent Current | $I_O$ ≤ 1A | Tj = 25°C | | | 8 | | | 8 | | | 8 | mA |
| | | | 0°C ≤ Tj ≤ +125°C | | | 8.5 | | | 8.5 | | | 8.5 | mA |
| $\Delta I_Q$ | Quiescent Current Change | 5 mA ≤ $I_O$ ≤ 1A | | | | 0.5 | | | 0.5 | | | 0.5 | mA |
| | | Tj = 25°C, $I_O$ ≤ 1A | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| | | $V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | | (7.5 ≤ $V_{IN}$ ≤ 20) | | | (14.8 ≤ $V_{IN}$ ≤ 27) | | | (17.9 ≤ $V_{IN}$ ≤ 30) | | V |
| | | $I_O$ ≤ 500 mA, 0°C ≤ Tj ≤ +125°C | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| | | $V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | | (7 ≤ $V_{IN}$ ≤ 25) | | | (14.5 ≤ $V_{IN}$ ≤ 30) | | | (17.5 ≤ $V_{IN}$ ≤ 30) | | V |
| $V_N$ | Output Noise Voltage | $T_A$ = 25°C, 10 Hz ≤ f ≤ 100 kHz | | | 40 | | | 75 | | | 90 | | μV |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | f = 120 Hz | $I_O$ ≤ 1A, Tj = 25°C or | 62 | 80 | | 55 | 72 | | 54 | 70 | | dB |
| | | | $I_O$ ≤ 500 mA<br>0°C ≤ Tj ≤ +125°C | 62 | | | 55 | | | 54 | | | dB |
| | | $V_{MIN}$ ≤ $V_{IN}$ ≤ $V_{MAX}$ | | | (8 ≤ $V_{IN}$ ≤ 18) | | | (15 ≤ $V_{IN}$ ≤ 25) | | | (18.5 ≤ $V_{IN}$ ≤ 28.5) | | V |
| $R_O$ | Dropout Voltage | Tj = 25°C, $I_{OUT}$ = 1A | | | 2.0 | | | 2.0 | | | 2.0 | | V |
| | Output Resistance | f = 1 kHz | | | 8 | | | 18 | | | 19 | | mΩ |
| | Short-Circuit Current | Tj = 25°C | | | 2.1 | | | 1.5 | | | 1.2 | | A |
| | Peak Output Current | Tj = 25°C | | | 2.4 | | | 2.4 | | | 2.4 | | A |
| | Average TC of $V_{OUT}$ | 0°C ≤ Tj ≤ +125°C, $I_O$ = 5 mA | | | 0.6 | | | 1.5 | | | 1.8 | | mV/°C |
| $V_{IN}$ | Input Voltage Required to Maintain Line Regulation | Tj = 25°C, $I_O$ ≤ 1A | | | 7.5 | | 14.6 | | | 17.7 | | | V |

**Note 1:** Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

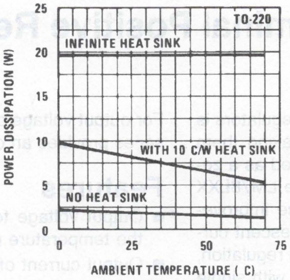
**Note 2:** All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w$ ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

# Typical Performance Characteristics

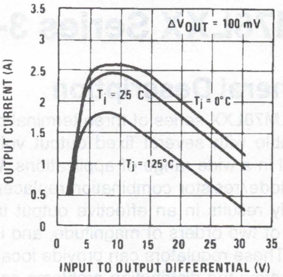
### Maximum Average Power Dissipation



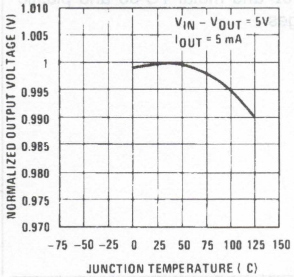
### Maximum Average Power Dissipation



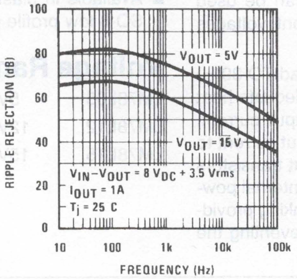
### Peak Output Current



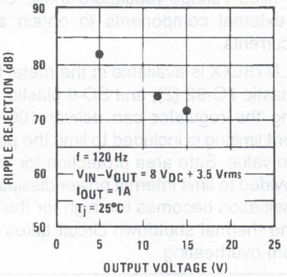
### Output Voltage (Normalized to 1V at Tj = 25°C)



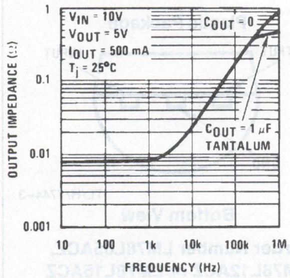
### Ripple Rejection



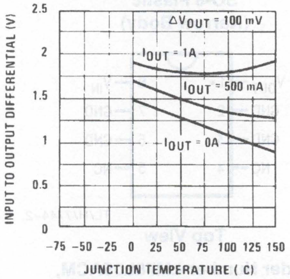
### Ripple Rejection



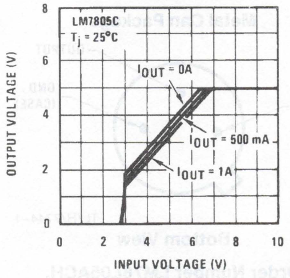
### Output Impedance



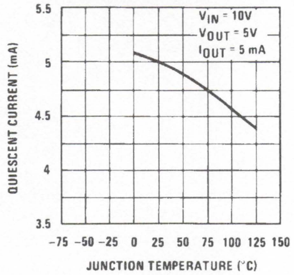
### Dropout Voltage



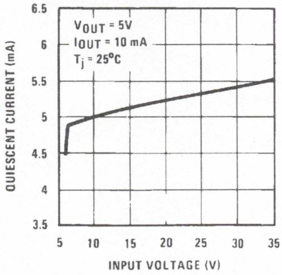
### Dropout Characteristics



### Quiescent Current



### Quiescent Current



TL/H/7746–4

**National Semiconductor Corporation**

# LM78LXX Series 3-Terminal Positive Regulators

## General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustment voltages and currents.

The LM78LXX is available in the metal three lead TO-39(H) the plastic TO-92 (Z), and SO-8 plastic. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

For output voltage other than 5V, 12V and 15V the LM117L series provides an output voltage range from 1.2V to 37V.

## Features

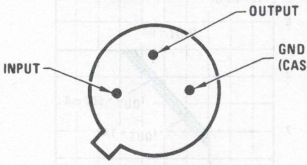
- Output voltage tolerances of ±5% (LM78LXXAC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 and plastic SO-8 low profile packages

## Voltage Range

| | |
|---|---|
| LM78L05 | 5V |
| LM78L12 | 12V |
| LM78L15 | 15V |

## Connection Diagrams

**Metal Can Package**

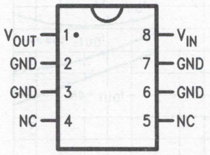


TL/H/7744–1

**Bottom View**

**Order Number LM78L05ACH, LM78L12ACH or LM78L15ACH**
**See NS Package Number H03A**

**SO-8 Plastic (Narrow Body)**

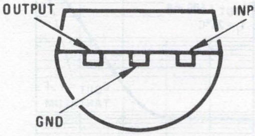


TL/H/7744–2

**Top View**

**Order Number LM78L05ACM, LM78L12ACM or LM78L15ACM**
**See NS Package Number M08A**

**Plastic Package**



TL/H/7744–3

**Bottom View**

**Order Number LM78L05ACZ, LM78L12ACZ or LM78L15ACZ**
**See NS Package Number Z03A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| $V_O = 5V$ | 30V |
| $V_O = 12V$ to 15V | 35V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | 0°C to +70°C |
| Maximum Junction Temperature | 125°C |
| Storage Temperature Range | |
| Metal Can (H Package) | −65°C to +150°C |
| Molded TO-92 (Z Package) | −55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## LM78LXXAC Electrical Characteristics

(Note 2) $T_j = 0°C$ to 125°C, $I_O = 40$ mA, $C_{IN} = 0.33$ µF, $C_O = 0.1$ µF (unless noted)

| LM78LXXAC Output Voltage | | | 5V | | | 12V | | | 15V | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input Voltage (unless otherwise noted)** | | | **10V** | | | **19V** | | | **23V** | | | **Units** |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $V_O$ | Output Voltage (Note 4) | Tj = 25°C | 4.8 | 5 | 5.2 | 11.5 | 12 | 12.5 | 14.4 | 15 | 15.6 | V |
| | | $1\ mA \le I_O \le 70\ mA$ | 4.75 | | 5.25 | 11.4 | | 12.6 | 14.25 | | 15.75 | V |
| | | $1\ mA \le I_O \le 40\ mA$ and | 4.75 | | 5.25 | 11.4 | | 12.6 | 14.25 | | 15.75 | V |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(7 \le V_{IN} \le 20)$ | | | $(14.5 \le V_{IN} \le 27)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| $\Delta V_O$ | Line Regulation | Tj = 25°C | | 10 | 54 | | 20 | 110 | | 25 | 140 | mV |
| | | | $(8 \le V_{IN} \le 20)$ | | | $(16 \le V_{IN} \le 27)$ | | | $(20 \le V_{IN} \le 30)$ | | | V |
| | | | | 18 | 75 | | 30 | 180 | | 37 | 250 | mV |
| | | | $(7 \le V_{IN} \le 20)$ | | | $(14.5 \le V_{IN} \le 27)$ | | | $(17.5 \le V_{IN} \le 30)$ | | | V |
| $\Delta V_O$ | Load Regulation | Tj = 25°C, $1\ mA \le I_O \le 40\ mA$ | | 5 | 30 | | 10 | 50 | | 12 | 75 | mV |
| | | Tj = 25°C, $1\ mA \le I_O \le 100\ mA$ | | 20 | 60 | | 30 | 100 | | 35 | 150 | mV |
| $\Delta V_O$ | Long Term Stability | | | 12 | | | 24 | | | 30 | | mV/1000 hrs |
| $I_Q$ | Quiescent Current | Tj = 25°C | | 3 | 5 | | 3 | 5 | | 3.1 | 5 | mA |
| | | Tj = 125°C | | | 4.7 | | | 4.7 | | | 4.7 | |
| $\Delta I_Q$ | Quiescent Current Change | $1\ mA \le I_O \le 40\ mA$ | | | 0.1 | | | 0.1 | | | 0.1 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| | | | $(8 \le V_{IN} \le 20)$ | | | $(16 \le V_{IN} \le 27)$ | | | $(20 \le V_{IN} \le 30)$ | | | V |
| $V_n$ | Output Noise Voltage | Tj = 25°C, (Note 3) f = 10 Hz − 10 kHz | | 40 | | | 80 | | | 90 | | µV |
| $\frac{\Delta V_{IN}}{\Delta V_{OUT}}$ | Ripple Rejection | f = 120 Hz | 47 | 62 | | 40 | 54 | | 37 | 51 | | dB |
| | | | $(8 \le V_{IN} \le 16)$ | | | $(15 \le V_{IN} \le 25)$ | | | $(18.5 \le V_{IN} \le 28.5)$ | | | V |
| | Input Voltage Required to Maintain Line Regulation | Tj = 25°C | 7 | | | 14.5 | | | 17.5 | | | V |

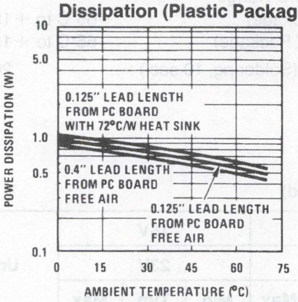
**Note 1:** Thermal resistance of H package is typically 26°C/W $\theta_{jc}$ still Air, and 94°C/W $\theta_{ja}$ 400 ft/min of air. For the Z package is 60°C/W $\theta_{jc}$, 232°C/W $\theta_{ja}$ still air, and 88°C/W $\theta_{ja}$ at 400 ft/min of air. The maximum junction temperature shall not exceed 125°C on Electrical parameters.

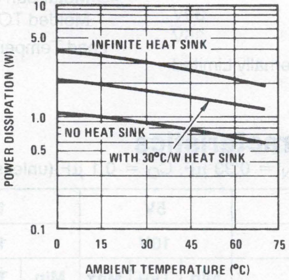
**Note 2:** The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

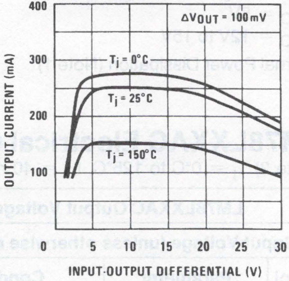
**Note 3:** Recommended minimum load capacitance of 0.01 µF to limit high frequency noise bandwidth.

**Note 4:** The temperature coefficient of $V_{OUT}$ is typically within ±0.01% $V_O$/°C.

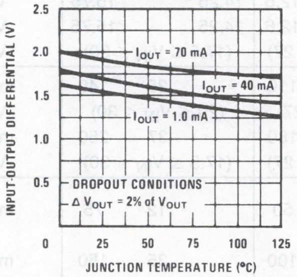
# Typical Performance Characteristics

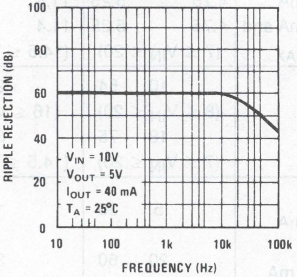

**Maximum Average Power Dissipation (Plastic Package)**

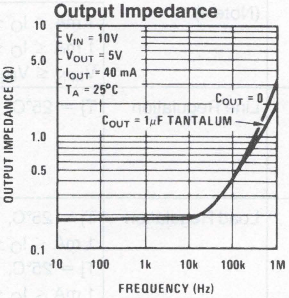

**Maximum Average Power Dissipation (Metal Can Package)**


**Peak Output Current**

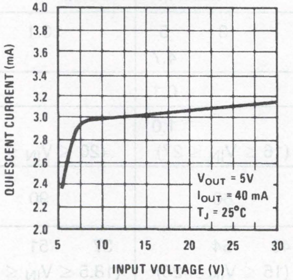
TL/H/7744–4

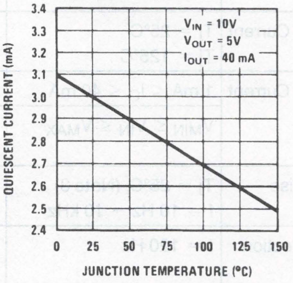

**Dropout Voltage**


**Ripple Rejection**


**Output Impedance**

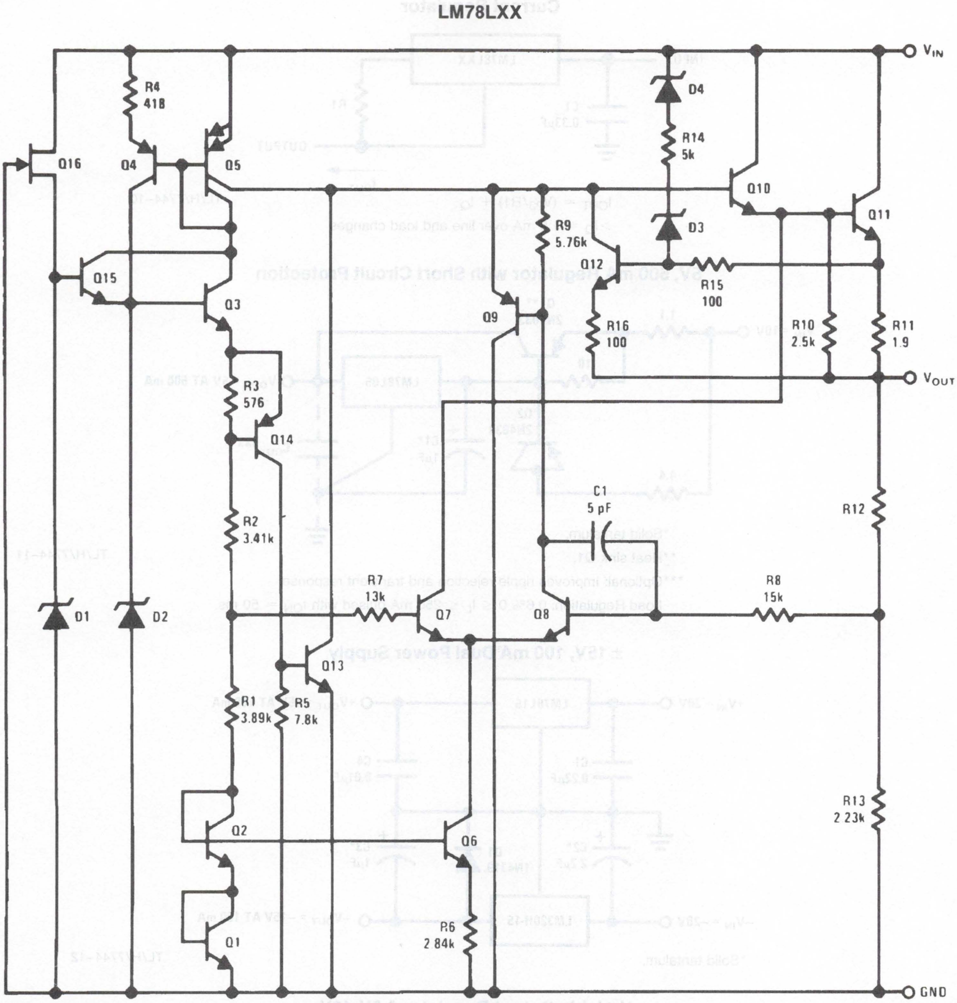
TL/H/7744–5


**Quiescent Current**


**Quiescent Current**

TL/H/7744–6

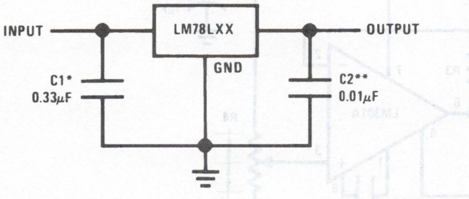
## Equivalent Circuit


LM78LXX
V_IN
R4
418
Q16
Q4
Q5
D4
R14
5k
Q10
Q11
D3
R9
5.76k
Q12
R15
100
R16
100
Q15
Q3
Q9
R10
2.5k
R11
1.9
V_OUT
R3
576
Q14
C1
5 pF
R2
3.41k
R12
R7
13k
R8
15k
D1
D2
Q7
Q8
Q13
R1
3.89k
R5
7.8k
R13
2.23k
Q2
Q6
Q1
R6
2.84k
GND

TL/H/7744-7

## Typical Applications

### Fixed Output Regulator

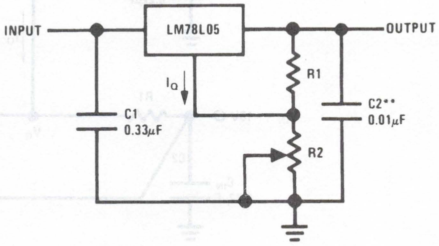

INPUT
LM78LXX
OUTPUT
GND
C1*
0.33μF
C2**
0.01μF

TL/H/7744-8

*Required if the regulator is located far from the power supply filter.

**See Note 3 in the electrical characteristics table.

### Adjustable Output Regulator


INPUT
LM78L05
OUTPUT
I_Q
C1
0.33μF
R1
R2
C2**
0.01μF

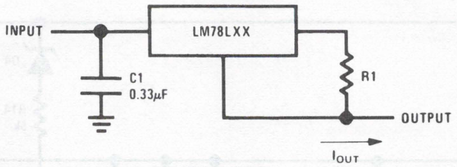
TL/H/7744-9

$V_{OUT} = 5V + (5V/R1 + I_Q) R2$

$5V/R1 > 3\ I_Q$, load regulation ($L_r$) ≈ [(R1 + R2)/R1] ($L_r$ of LM78L05)

## Typical Applications (Continued)

### Current Regulator

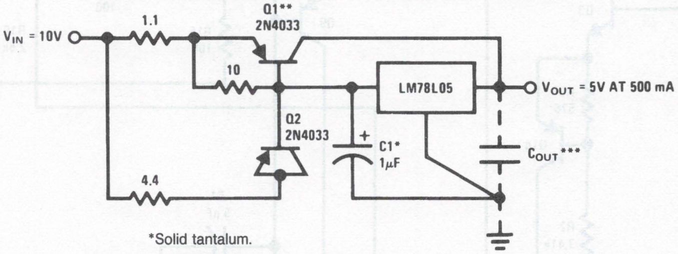

INPUT
LM78LXX
C1
0.33μF
R1
OUTPUT
$I_{OUT}$

TL/H/7744-10

$I_{OUT} = (V_{23}/R1) + I_Q$

$> I_Q = 1.5$ mA over line and load changes

### 5V, 500 mA Regulator with Short Circuit Protection


$V_{IN}$ = 10V
1.1
Q1**
2N4033
10
LM78L05
$V_{OUT}$ = 5V AT 500 mA
Q2
2N4033
C1*
1μF
$C_{OUT}$***
4.4

*Solid tantalum.

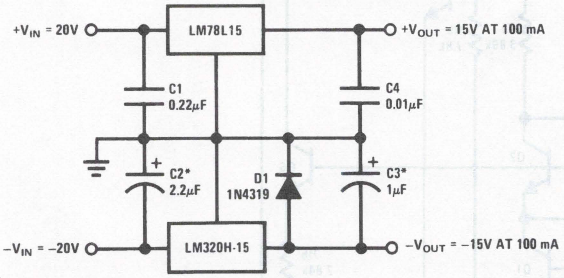
**Heat sink Q1.

***Optional: Improves ripple rejection and transient response.

Load Regulation: 0.6% $0 \le I_L \le 250$ mA pulsed with $t_{ON} = 50$ ms.

TL/H/7744-11

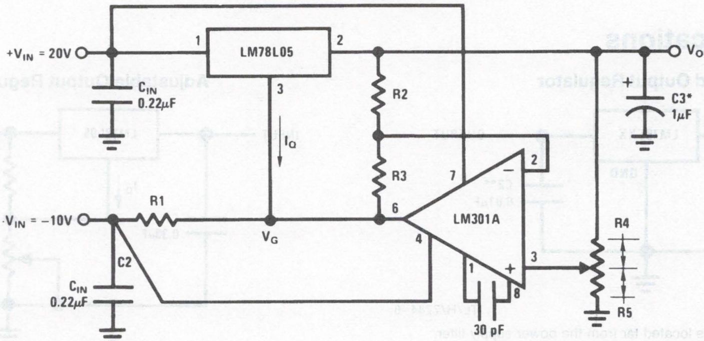
### ± 15V, 100 mA Dual Power Supply


$+V_{IN}$ = 20V
LM78L15
$+V_{OUT}$ = 15V AT 100 mA
C1
0.22μF
C4
0.01μF
C2*
2.2μF
D1
1N4319
C3*
1μF
$-V_{IN}$ = −20V
LM320H-15
$-V_{OUT}$ = −15V AT 100 mA

*Solid tantalum.

TL/H/7744-12

### Variable Output Regulator 0.5V-18V


$+V_{IN}$ = 20V
1
LM78L05
2
3
$C_{IN}$
0.22μF
$I_Q$
R2
R3
$V_{OUT}$
C3*
1μF
7
2
6
LM301A
$-V_{IN}$ = −10V
R1
$V_G$
4
C2
$C_{IN}$
0.22μF
R4
3
1
8
30 pF
R5

*Solid tantalum.

TL/H/7744-13

$V_{OUT} = V_G + 5V, R1 = (-V_{IN}/I_{Q\ LM78L05})$

$V_{OUT} = 5V (R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1$ $(R3/R4) = 0.9$

National Semiconductor Corporation

# LM79XX Series 3-Terminal Negative Regulators

## General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

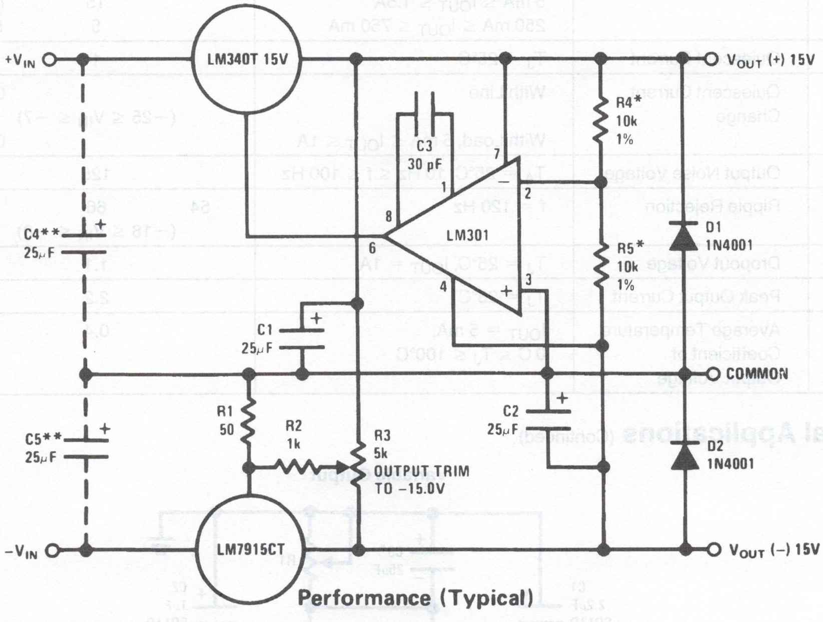
For applications requiring other voltages, see LM137 data sheet.

## Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

## Typical Applications

**±15V, 1 Amp Tracking Regulators**



+V_IN
LM340T 15V
V_OUT (+) 15V
C3
30 pF
7
1
2
8
6
LM301
4
3
R4*
10k
1%
R5*
10k
1%
D1
1N4001
C4**
25μF
C1
25μF
COMMON
R1
50
R2
1k
R3
5k
OUTPUT TRIM
TO −15.0V
C5**
25μF
C2
25μF
D2
1N4001
−V_IN
LM7915CT
V_OUT (−) 15V

TL/H/7340–1

**Performance (Typical)**

| | (−15) | (+15) |
|---|---|---|
| Load Regulation at $\Delta I_L = 1A$ | 40 mV | 2 mV |
| Output Ripple, $C_{IN} = 3000\ \mu F$, $I_L = 1A$ | 100 μVrms | 100 μVrms |
| Temperature Stability | 50 mV | 50 mV |
| Output Noise 10 Hz ≤ f ≤ 10 kHz | 150 μVrms | 150 μVrms |

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 3″ from regulators.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| ($V_o$ = 5V) | −35V |
| ($V_o$ = 12V and 15V) | −40V |
| Input-Output Differential | |
| ($V_o$ = 5V) | 25V |
| ($V_o$ = 12V and 15V) | 30V |
| Power Dissipation (Note 1) | Internally Limited |
| Operating Junction Temperature Range | 0°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 230°C |

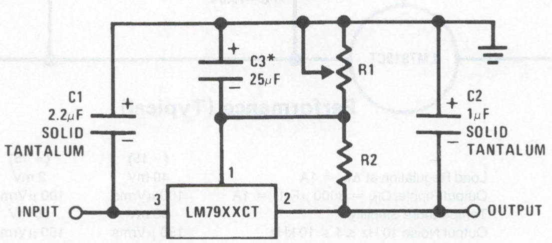
## Electrical Characteristics

Conditions unless otherwise noted: $I_{OUT}$ = 500 mA, $C_{IN}$ = 2.2 μF, $C_{OUT}$ = 1 μF, 0°C ≤ $T_J$ ≤ +125°C, Power Dissipation ≤ 1.5W.

| | | Part Number | LM7905C | | | Units |
|---|---|---|---|---|---|---|
| | | Output Voltage | 5V | | | |
| | | Input Voltage (unless otherwise specified) | −10V | | | |
| Symbol | Parameter | Conditions | Min | Typ | Max | |
| $V_O$ | Output Voltage | $T_J$ = 25°C | −4.8 | −5.0 | −5.2 | V |
| | | 5 mA ≤ $I_{OUT}$ ≤ 1A, | −4.75 | | −5.25 | V |
| | | P ≤ 15W | | (−20 ≤ $V_{IN}$ ≤ −7) | | V |
| $\Delta V_O$ | Line Regulation | $T_J$ = 25°C, (Note 2) | | 8 | 50 | mV |
| | | | | (−25 ≤ $V_{IN}$ ≤ −7) | | V |
| | | | | 2 | 15 | mV |
| | | | | (−12 ≤ $V_{IN}$ ≤ −8) | | V |
| $\Delta V_O$ | Load Regulation | $T_J$ = 25°C, (Note 2) | | | | mV |
| | | 5 mA ≤ $I_{OUT}$ ≤ 1.5A | | 15 | 100 | mV |
| | | 250 mA ≤ $I_{OUT}$ ≤ 750 mA | | 5 | 50 | mV |
| $I_Q$ | Quiescent Current | $T_J$ = 25°C | | 1 | 2 | mA |
| $\Delta I_Q$ | Quiescent Current Change | With Line | | | 0.5 | mA |
| | | | | (−25 ≤ $V_{IN}$ ≤ −7) | | V |
| | | With Load, 5 mA ≤ $I_{OUT}$ ≤ 1A | | | 0.5 | mA |
| $V_n$ | Output Noise Voltage | $T_A$ = 25°C, 10 Hz ≤ f ≤ 100 Hz | | 125 | | μV |
| | Ripple Rejection | f = 120 Hz | 54 | 66 | | dB |
| | | | | (−18 ≤ $V_{IN}$ ≤ −8) | | V |
| | Dropout Voltage | $T_J$ = 25°C, $I_{OUT}$ = 1A | | 1.1 | | V |
| $I_{OMAX}$ | Peak Output Current | $T_J$ = 25°C | | 2.2 | | A |
| | Average Temperature Coefficient of Output Voltage | $I_{OUT}$ = 5 mA, 0 C ≤ $T_J$ ≤ 100°C | | 0.4 | | mV/°C |

## Typical Applications (Continued)

### Variable Output



TL/H/7340-2

*Improves transient response and ripple rejection. Do not increase beyond 50 μF.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

| | |
|---|---|
| LM7905CT | 300Ω |
| LM7912CT | 750Ω |
| LM7915CT | 1k |

## Electrical Characteristics (Continued) Conditions unless otherwise noted: $I_{OUT}$ = 500 mA, $C_{IN}$ = 2.2 $\mu$F, $C_{OUT}$ = 1 $\mu$F, 0°C ≤ $T_J$ ≤ +125°C, Power Dissipation = 1.5W.

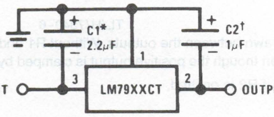
| Part Number | | | LM7912C | | | LM7915C | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| Output Voltage | | | 12V | | | 15V | | | |
| Input Voltage (unless otherwise specified) | | | −19V | | | −23V | | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $V_O$ | Output Voltage | $T_J$ = 25°C | −11.5 | −12.0 | −12.5 | −14.4 | −15.0 | −15.6 | V |
| | | 5 mA ≤ $I_{OUT}$ ≤ 1A, | −11.4 | | −12.6 | −14.25 | | −15.75 | V |
| | | P ≤ 15W | | (−27 ≤ $V_{IN}$ ≤ −14.5) | | | (−30 ≤ $V_{IN}$ ≤ −17.5) | | V |
| $\Delta V_O$ | Line Regulation | $T_J$ = 25°C, (Note 2) | | 5 | 80 | | 5 | 100 | mV |
| | | | | (−30 ≤ $V_{IN}$ ≤ −14.5) | | | (−30 ≤ $V_{IN}$ ≤ −17.5) | | V |
| | | | | 3 | 30 | | 3 | 50 | mV |
| | | | | (−22 ≤ $V_{IN}$ ≤ −16) | | | (−26 ≤ $V_{IN}$ ≤ −20) | | V |
| $\Delta V_O$ | Load Regulation | $T_J$ = 25°C, (Note 2) | | 15 | 200 | | 15 | 200 | mV |
| | | 5 mA ≤ $I_{OUT}$ ≤ 1.5A | | 15 | 200 | | 15 | 200 | mV |
| | | 250 mA ≤ $I_{OUT}$ ≤ 750 mA | | 5 | 75 | | 5 | 75 | mV |
| $I_Q$ | Quiescent Current | $T_J$ = 25°C | | 1.5 | 3 | | 1.5 | 3 | mA |
| $\Delta I_Q$ | Quiescent Current Change | With Line | | | 0.5 | | | 0.5 | mA |
| | | | | (−30 ≤ $V_{IN}$ ≤ −14.5) | | | (−30 ≤ $V_{IN}$ ≤ −17.5) | | V |
| | | With Load, 5 mA ≤ $I_{OUT}$ ≤ 1A | | | 0.5 | | | 0.5 | mA |
| $V_n$ | Output Noise Voltage | $T_A$ = 25°C, 10 Hz ≤ f ≤ 100 Hz | | 300 | | | 375 | | $\mu$V |
| | Ripple Rejection | f = 120 Hz | 54 | 70 | | 54 | 70 | | dB |
| | | | | (−25 ≤ $V_{IN}$ ≤ −15) | | | (−30 ≤ $V_{IN}$ ≤ −17.5) | | V |
| | Dropout Voltage | $T_J$ = 25°C, $I_{OUT}$ = 1A | | 1.1 | | | 1.1 | | V |
| $I_{OMAX}$ | Peak Output Current | $T_J$ = 25°C | | 2.2 | | | 2.2 | | A |
| | Average Temperature Coefficient of Output Voltage | $I_{OUT}$ = 5 mA, 0 C ≤ $T_J$ ≤ 100°C | | −0.8 | | | −1.0 | | mV/°C |

**Note 1:** For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient ($\theta_{JA}$) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

**Note 2:** Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

## Typical Applications (Continued)

### Fixed Regulator



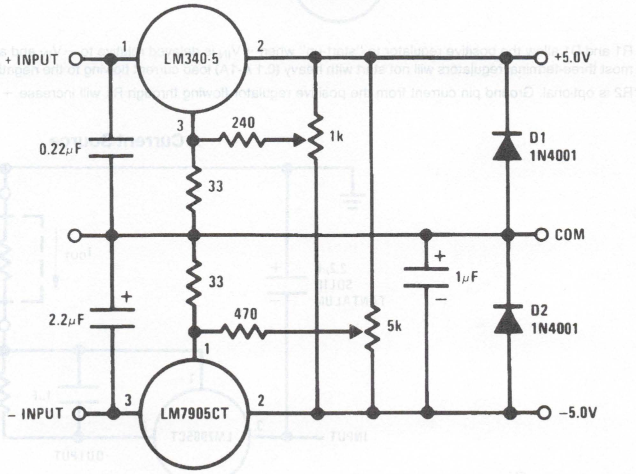
TL/H/7340-3

*Required if regulator is separated from filter capacitor by more than 3″. For value given, capacitor must be solid tantalum. 25 $\mu$F aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 $\mu$F aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100 $\mu$F, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

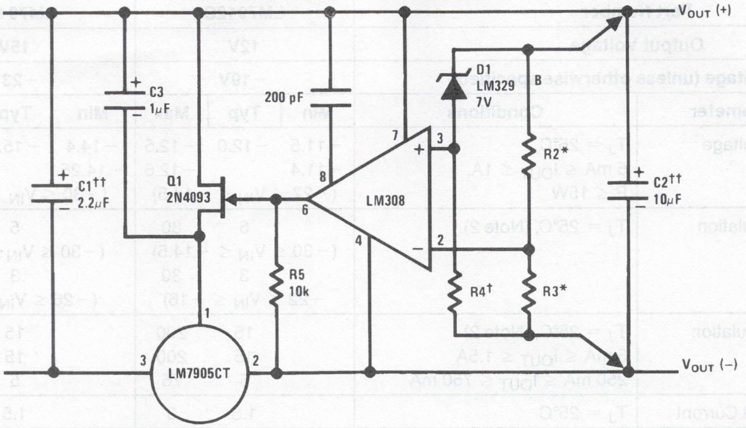
### Dual Trimmed Supply



TL/H/7340-4

# Typical Applications (Continued)

## High Stability 1 Amp Regulator



C3
1µF
200 pF
D1
LM329
7V
B
$V_{OUT}$ (+)
C1††
2.2µF
Q1
2N4093
7
3
8
6
LM308
4
2
R2*
C2††
10µF
R5
10k
R4†
R3*
1
3
2
LM7905CT
$V_{OUT}$ (−)

Load and line regulation < 0.01% temperature stability ≤ 0.2%

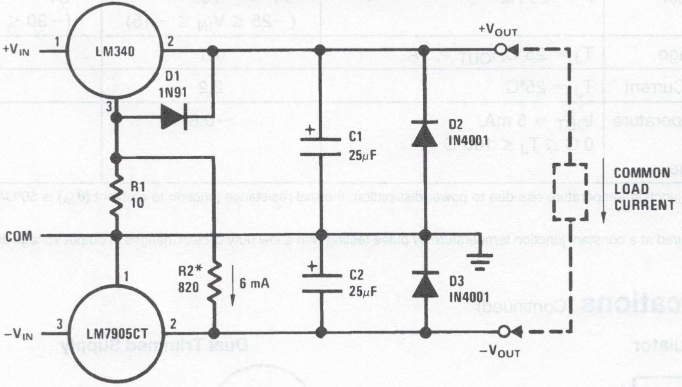
TL/H/7340-5

†Determine Zener current

††Solid tantalum

*Select resistors to set output voltage. 2 ppm/°C tracking suggested

## Preventing Positive Regulator Latch-Up



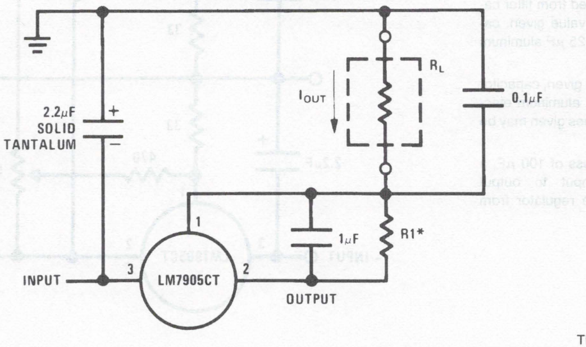
$+V_{IN}$
1
LM340
2
3
D1
1N91
+$V_{OUT}$
C1
25µF
D2
IN4001
COMMON
LOAD
CURRENT
R1
10
COM
R2*
820
6 mA
C2
25µF
D3
IN4001
1
$-V_{IN}$
3
LM7905CT
2
$-V_{OUT}$

TL/H/7340-6

R1 and D1 allow the positive regulator to "start-up" when $+V_{IN}$ is delayed relative to $-V_{IN}$ and a heavy load is drawn between the outputs. Without R1 and D1, most three-terminal regulators will not start with heavy (0.1 A-1A) load current flowing to the negative regulator, even though the positive output is clamped by D2.

*R2 is optional. Ground pin current from the positive regulator flowing through R1 will increase $+V_{OUT} \approx 60$ mV if R2 is omitted.

## Current Source



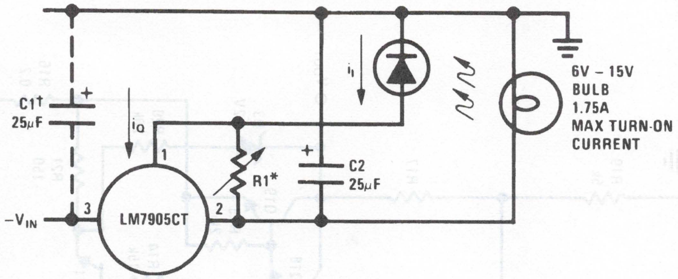
2.2µF
SOLID
TANTALUM
$I_{OUT}$
$R_L$
0.1µF
1µF
R1*
1
3
2
LM7905CT
INPUT
OUTPUT

$^*I_{OUT} = 1\text{ mA} + \frac{5V}{R1}$

TL/H/7340-7

## Typical Applications (Continued)

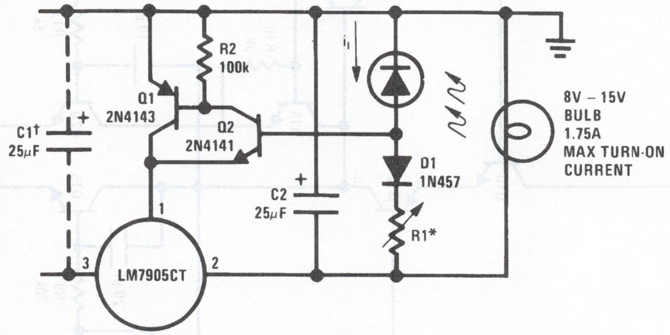
### Light Controllers Using Silicon Photo Cells


C1†
25μF
$i_Q$
$i_l$
1
2
3
$-V_{IN}$
LM7905CT
R1*
C2
25μF
6V – 15V
BULB
1.75A
MAX TURN-ON
CURRENT

TL/H/7340–8

*Lamp brightness increase until $i_l = i_Q$ (≈ 1 mA) + 5V/R1.

†Necessary only if raw supply filter capacitor is more than 2″ from LM7905CT


R2
100k
Q1
2N4143
Q2
2N4141
C1†
25μF
$i_l$
D1
1N457
C2
25μF
R1*
1
2
3
LM7905CT
8V – 15V
BULB
1.75A
MAX TURN-ON
CURRENT

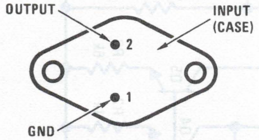
TL/H/7340–9

*Lamp brightness increases until $i_l$ = 5V/R1 ($I_l$ can be set as low as 1 μA)

†Necessary only if raw supply filter capacitor is more than 2″ from LM7905CT

## Connection Diagrams

### TO-3 Package


OUTPUT
INPUT
(CASE)
2
1
GND

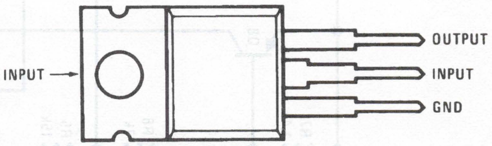
TL/H/7340–10

**Bottom View**

**Order Number LM7905CK, LM7912CK or LM7915CK**

**See NS Package Number KC02A**

**TO-220 Package**


INPUT
OUTPUT
INPUT
GND

TL/H/7340–11

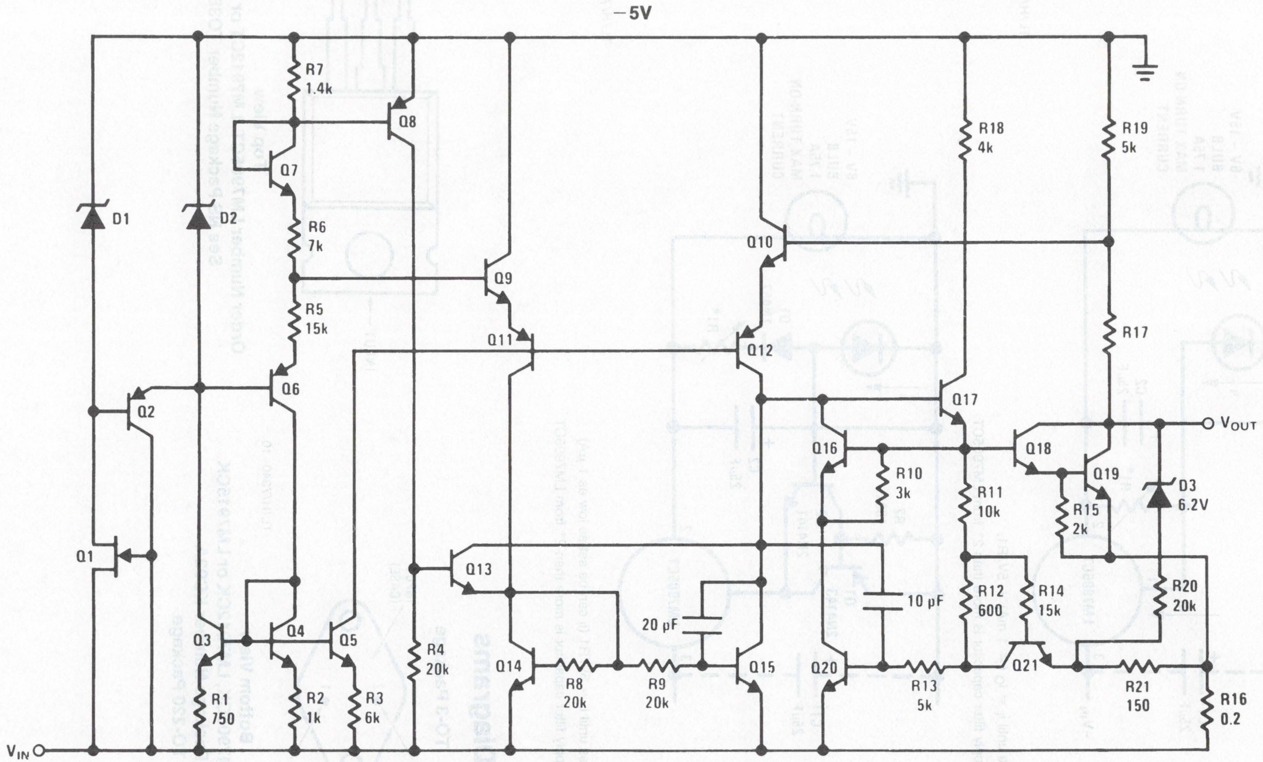
**Top View**

**Order Number LM7905CT, LM7912CT or LM7915CT**

**See NS Package Number TO3B**

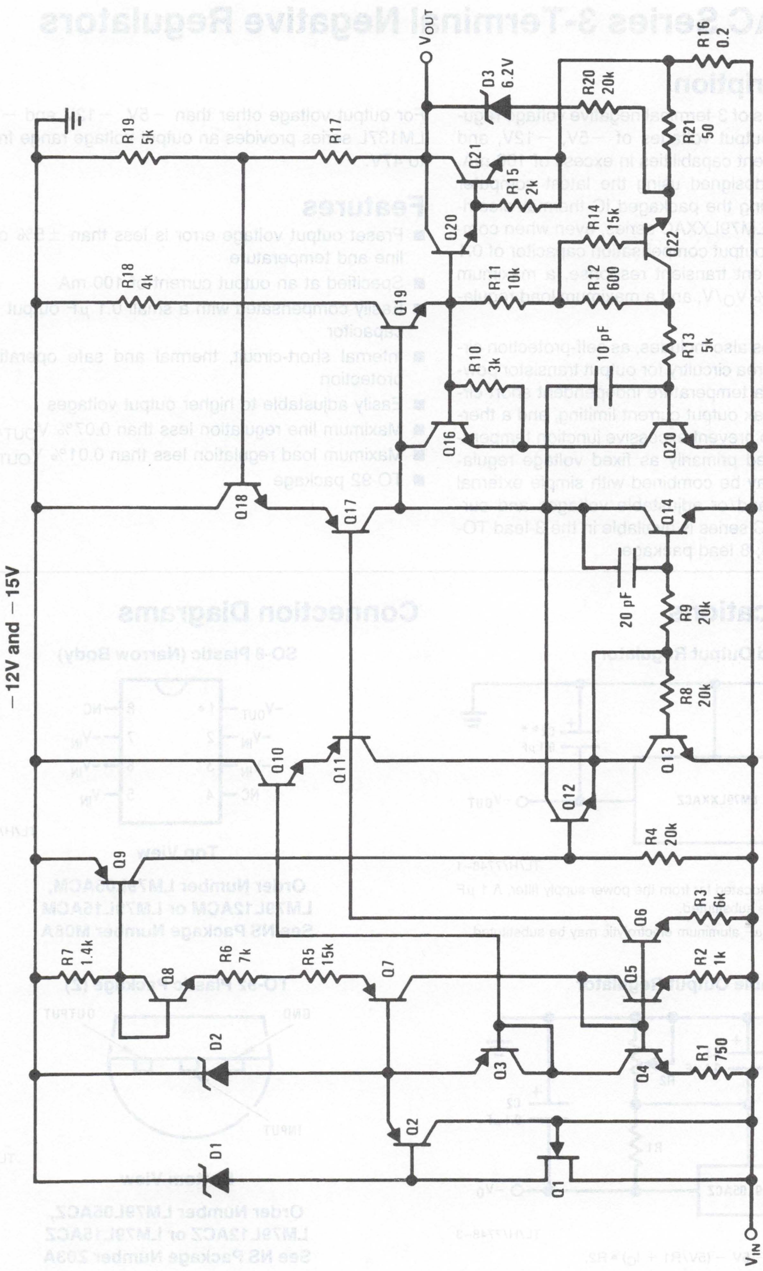
1

## Schematic Diagrams


−5V
R7
1.4k
Q8
Q7
D1
D2
R6
7k
Q9
Q10
R18
4k
R19
5k
R5
15k
Q11
Q12
R17
Q6
Q2
Q17
Q16
Q18
VOUT
Q19
R10
3k
R11
10k
R15
2k
D3
6.2V
Q1
Q13
10 pF
20 pF
R12
600
R14
15k
R20
20k
Q3
Q4
Q5
R4
20k
Q14
Q15
Q20
Q21
R1
750
R2
1k
R3
6k
R8
20k
R9
20k
R13
5k
R21
150
R16
0.2
VIN

TL/H/7340–12

## Schematic Diagrams (Continued)



−12V and −15V
R7
1.4k
Q9
Q8
R6
7k
R5
15k
D1
D2
Q2
Q7
Q3
Q1
Q4
Q5
Q6
R1
750
R2
1k
R3
6k
R4
20k
Q10
Q11
Q12
Q13
R8
20k
R9
20k
20 pF
Q14
Q17
Q18
R18
4k
R19
5k
R17
Q19
Q16
R10
3k
10 pF
Q20
R11
10k
R12
600
R13
5k
R14
15k
Q22
Q20
Q21
R15
2k
D3
6.2V
R20
20k
R21
50
R16
0.2
V_OUT
V_IN

TL/H/7340–13

**National Semiconductor Corporation**

# LM79LXXAC Series 3-Terminal Negative Regulators

## General Description

The LM79LXXAC series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% $V_O$/V, and a maximum load regulation of 0.01% $V_O$/mA.

The LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead TO-92 package, and SO-8; 8 lead package.

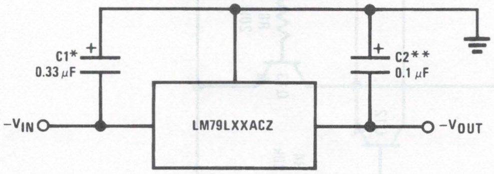
For output voltage other than −5V, −12V and −15V the LM137L series provides an output voltage range from 1.2V to 47V.

## Features

- Preset output voltage error is less than ±5% overload, line and temperature
- Specified at an output current of 100 mA
- Easily compensated with a small 0.1 μF output capacitor
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% $V_{OUT}$/V
- Maximum load regulation less than 0.01% $V_{OUT}$mA
- TO-92 package

## Typical Applications

### Fixed Output Regulator

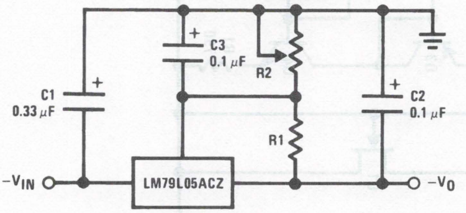


TL/H/7748-1

*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

**Required for stability. A 1 μF aluminum electrolytic may be substituted.

### Adjustable Output Regulator

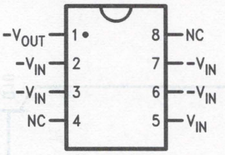


TL/H/7748-3

$$-V_O = -5V - (5V/R1 + I_Q) \bullet R2,$$
$$5V/R1 > 3\,I_Q$$

## Connection Diagrams

### SO-8 Plastic (Narrow Body)

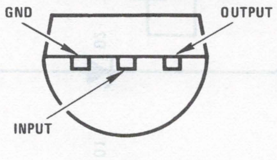


TL/H/7748-4

**Top View**

**Order Number LM79L05ACM, LM79L12ACM or LM79L15ACM**
**See NS Package Number M08A**

### TO-92 Plastic Package (Z)



TL/H/7748-2

**Bottom View**

**Order Number LM79L05ACZ, LM79L12ACZ or LM79L15ACZ**
**See NS Package Number Z03A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | |
| $V_O = -5V, -12V, -15V$ | −35V |
| Internal Power Dissipation (Note 1) | Internally Limited |
| Operating Temperature Range | 0°C to +70°C |
| Maximum Junction Temperature | +125°C |
| Storage Temperature Range | −55°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## Electrical Characteristics (Note 2) $T_A = 0°C$ to $+70°C$ unless otherwise noted.

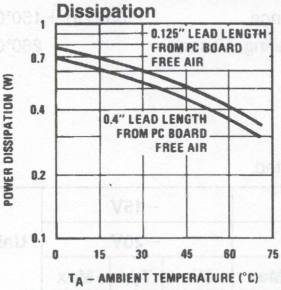
| | | Output Voltage | −5V | | | −12V | | | −15V | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Input Voltage (unless otherwise noted)** | −10V | | | −17V | | | −20V | | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| $V_O$ | Output Voltage | Tj = 25°C, $I_O$ = 100 mA | −5.2 | −5 | −4.8 | −12.5 | −12 | −11.5 | −15.6 | −15 | −14.4 | |
| | | 1 mA ≤ $I_O$ ≤ 100 mA | −5.25 | | −4.75 | −12.6 | | −11.4 | −15.75 | | −14.25 | |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(-20 \le V_{IN} \le -7.5)$ | | | $(-27 \le V_{IN} \le -14.8)$ | | | $(-30 \le V_{IN} \le -18)$ | | | V |
| | | 1 mA ≤ $I_O$ ≤ 40 mA | −5.25 | | −4.75 | | −12.6 | −11.4 | −15.75 | | −14.25 | |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(-20 \le V_{IN} \le -7)$ | | | $(-27 \le V_{IN} \le -14.5)$ | | | $(-30 \le V_{IN} \le -17.5)$ | | | |
| $\Delta V_O$ | Line Regulation | Tj = 25°C, $I_O$ = 100 mA | | | 60 | | | 45 | | | 45 | mV |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(-20 \le V_{IN} \le -7.3)$ | | | $(-27 \le V_{IN} \le -14.6)$ | | | $(-30 \le V_{IN} \le -17.7)$ | | | V |
| | | Tj = 25°C, $I_O$ = 40 mA | | | 60 | | | 45 | | | 45 | mV |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(-20 \le V_{IN} \le -7)$ | | | $(-27 \le V_{IN} \le -14.5)$ | | | $(-30 \le V_{IN} \le -17.5)$ | | | V |
| $\Delta$ | Load Regulation | Tj = 25°C<br>1 mA ≤ $I_O$ ≤ 100 mA | | | 50 | | | 100 | | | 125 | mV |
| $\Delta V_O$ | Long Term Stability | $I_O$ = 100 mA | | 20 | | | 48 | | | 60 | | mV/khrs |
| $I_Q$ | Quiescent Current | $I_O$ = 100 mA | | 2 | 6 | | 2 | 6 | | 2 | 6 | mA |
| $\Delta I_Q$ | Quiescent Current Change | 1 mA ≤ $I_O$ ≤ 100 mA | | | 0.3 | | | 0.3 | | | 0.3 | mA |
| | | 1 mA ≤ $I_O$ ≤ 40 mA | | | 0.1 | | | 0.1 | | | 0.1 | |
| | | $I_O$ = 100 mA | | | 0.25 | | | 0.25 | | | 0.25 | mA |
| | | $V_{MIN} \le V_{IN} \le V_{MAX}$ | $(-20 \le V_{IN} \le -7.5)$ | | | $(-27 \le V_{IN} \le -14.8)$ | | | $(-30 \le V_{IN} \le -18)$ | | | V |
| $V_n$ | Output Noise Voltage | Tj = 25°C, $I_O$ = 100 mA<br>f = 10 Hz − 10 kHz | | 40 | | | 96 | | | 120 | | µV |
| $\frac{\Delta V_{IN}}{\Delta V_O}$ | Ripple Rejection | Tj = 25°C, $I_O$ = 100 mA<br>f = 120 Hz | 50 | | | 52 | | | 50 | | | dB |
| | Input Voltage Required to Maintain Line Regulation | Tj = 25°C, $I_O$ = 100 mA | | | −7.3 | | | −14.6 | | | −17.7 | V |
| | | $I_O$ = 40 mA | | | −7.0 | | | −14.5 | | | −17.5 | V |

**Note 1:** Thermal resistance of Z package is 60°c/w $\theta_{jc}$, 232°c/w $\theta_{ja}$ at still air, and 88°c/w at 400 ft/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

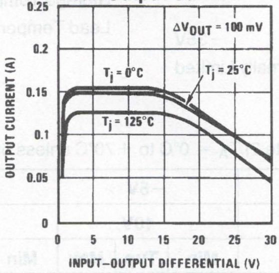
**Note 2:** To ensure constant junction temperature, low duty cycle pulse testing is used.

## Typical Performance Characteristics

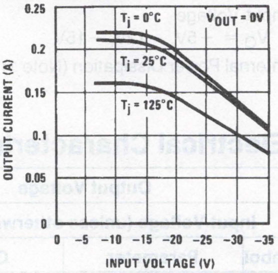
### Maximum Average Power Dissipation



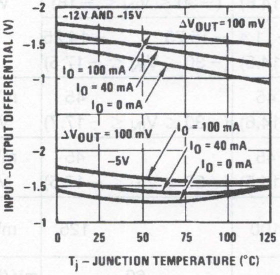
### Peak Output Current



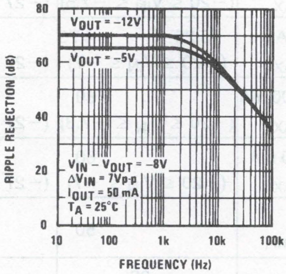
### Short Circuit Output Current



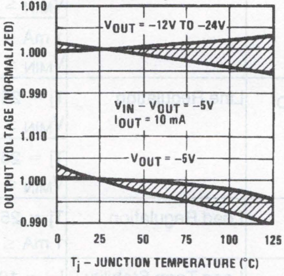
### Dropout Voltage



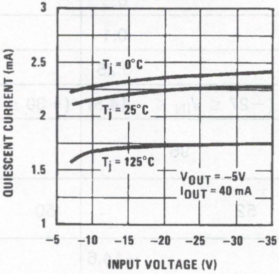
### Ripple Rejection



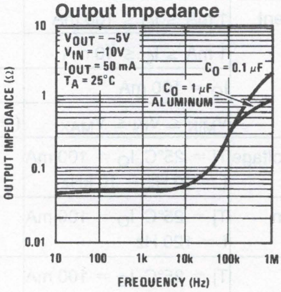
### Output Voltage vs. Temperature (Normalized to 1V @ 25°C)



### Quiescent Current



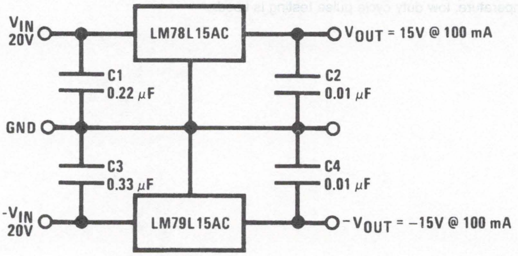
### Output Impedance



TL/H/7748–5

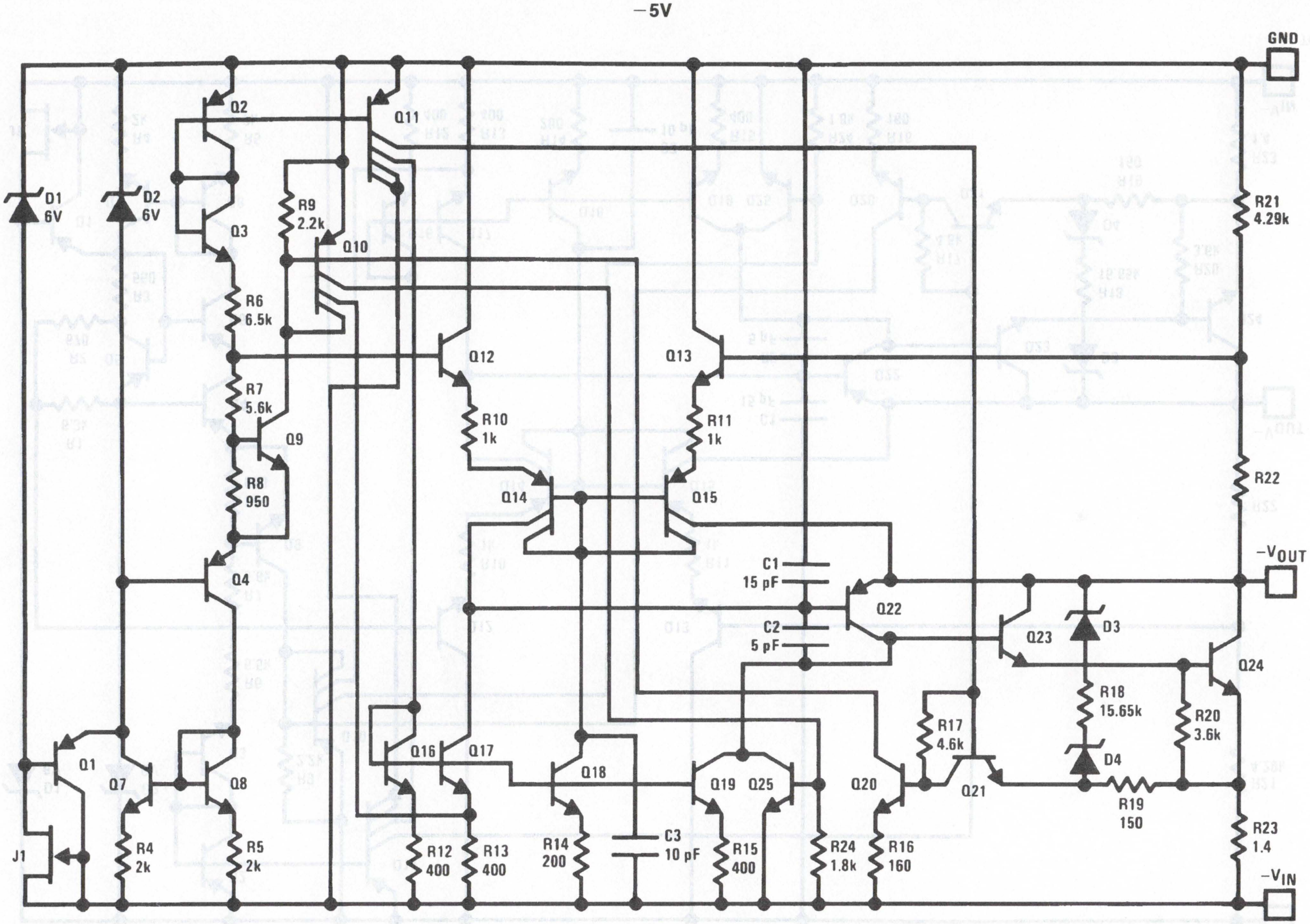
## Typical Applications (Continued)

### ± 15V, 100 mA Dual Power Supply


$V_{IN}$ 20V
LM78L15AC
$V_{OUT}$ = 15V @ 100 mA
C1 0.22 μF
C2 0.01 μF
GND
C3 0.33 μF
C4 0.01 μF
$-V_{IN}$ 20V
LM79L15AC
$-V_{OUT}$ = −15V @ 100 mA

TL/H/7748–6

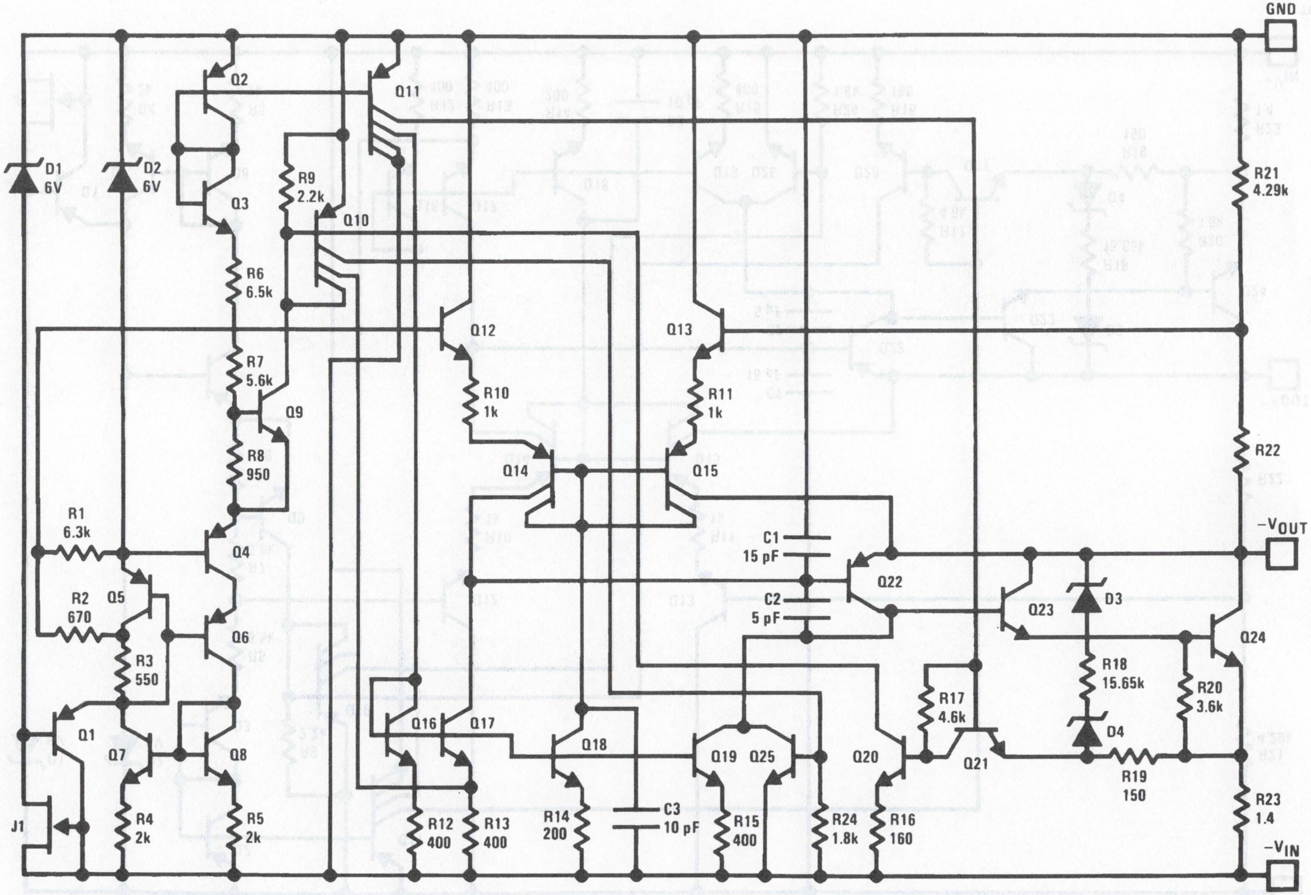
## Schematic Diagrams


−5V
GND
−VOUT
−VIN
D1 6V
D2 6V
Q1
Q2
Q3
Q4
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
J1
R4 2k
R5 2k
R6 6.5k
R7 5.6k
R8 950
R9 2.2k
R10 1k
R11 1k
R12 400
R13 400
R14 200
R15 400
R16 160
R17 4.6k
R18 15.65k
R19 150
R20 3.6k
R21 4.29k
R22
R23 1.4
R24 1.8k
C1 15 pF
C2 5 pF
C3 10 pF
D3
D4

TL/H/7748–7

## Schematic Diagrams (Continued)

−12V and −15V


GND
D1
6V
D2
6V
Q2
Q3
Q11
R9
2.2k
Q10
R6
6.5k
R7
5.6k
Q9
R8
950
Q12
R10
1k
Q13
R11
1k
Q14
Q15
R21
4.29k
R22
R1
6.3k
Q4
R2
670
Q5
Q6
R3
550
C1
15 pF
C2
5 pF
Q22
Q23
D3
Q24
−V_OUT
R18
15.65k
R20
3.6k
R17
4.6k
D4
Q1
Q7
Q8
Q16
Q17
Q18
Q19
Q25
Q20
Q21
R19
150
R23
1.4
J1
R4
2k
R5
2k
R12
400
R13
400
R14
200
C3
10 pF
R15
400
R24
1.8k
R16
160
−V_IN

TL/H/7748-8

National Semiconductor Corporation

**PRELIMINARY**

# LMC7660/7669 Switched Capacitor Voltage Converter

## General Description

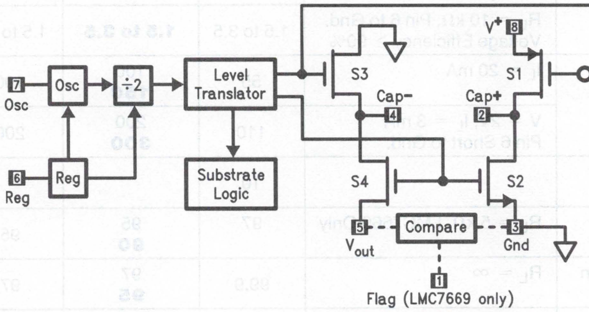
The LMC7660 and LMC7669 are CMOS voltage converters capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage of −1.5V to −10V. The LMC7660 is a pin-for-pin replacement for the popular 7660, while the LMC7669 incorporates a unique error flag to detect output fault conditions. Both converters feature: operation over full temperature and voltage range without need for an external diode, low quiescent current, and high power efficiency.

The LMC7660 uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolytic capacitors. The LMC7669 requires only one additional external resistor to detect output faults.

## Features

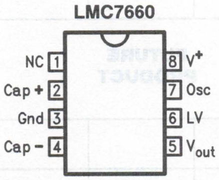
- Operation over full temperature and voltage range without an external diode
- Low supply current, 200 μA max (7660)
- Error flag to detect output faults (7669)
- Pin-for-pin replacement for the 7660
- Wide operating range 1.5V to 10V
- 97% Voltage Conversion Efficiency
- 95% Power Conversion Efficiency
- Easy to use, only 2 external components
- Extended temperature range

## Block Diagram

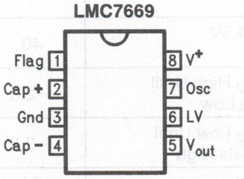

V+ 8
7 Osc
Osc
÷2
Level Translator
6 Reg
Reg
Substrate Logic
S3
S1
Cap− 4
Cap+ 2
S4
S2
5 Vout
Compare
3 Gnd
1
Flag (LMC7669 only)

TL/H/9136–1

## Pin Configuration


LMC7660
NC 1
Cap+ 2
Gnd 3
Cap− 4
8 V+
7 Osc
6 LV
5 Vout

TL/H/9136–2


LMC7669
Flag 1
Cap+ 2
Gnd 3
Cap− 4
8 V+
7 Osc
6 LV
5 Vout

TL/H/9136–3

## Ordering Information

LMC7660MJ −55°C ≤ $T_A$ ≤ +125°C
LMC7669MJ −55°C ≤ $T_A$ ≤ +125°C
LMC7660IN −40°C ≤ $T_A$ ≤ +85°C
LMC7669IN −40°C ≤ $T_A$ ≤ +85°C

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 10.5V |
| Input Voltage on Pin 1, 6, 7 (Note 2) | −0.3V to ($V^+$ + 0.3V) for $V^+ < 5.5V$<br>($V^+$ − 5.5V) to ($V^+$ + 0.3V) for $V^+ > 5.5V$ |
| Current into Pin 6 (Note 2) | 20 μA |
| Output Short Circuit Duration ($V^+ \leq 5.5V$) | Continuous |

| | Package J | Package N |
|---|---|---|
| Power Dissipation (Note 3) | 0.9W | 1.4W |
| $T_j$ Max | 150°C | 150°C |
| $\theta_{ja}$ | 140°C/W | 90°C/W |
| Storage Temp. Range | −65°C ≤ T ≤ 150°C | |
| Lead Temp. (Soldering, 5 sec) | 260°C | 260°C |
| ESD Tolerance (Note 1) | ±2000V | |

## Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | Typ | LMC7660MJ<br>LMC7669MJ<br>Tested Limit (Note 5) | LMC7660IN<br>LMC7669IN<br>Tested Limit (Note 5) | Design Limit (Note 6) | Units Limits |
|---|---|---|---|---|---|---|---|
| $I_s$ | Supply Current | $R_L = \infty$, LMC7660 Only | 120 | 200<br>**400** | 200 | **400** | μA max |
| $V^+_H$ | Supply Voltage Range High (Note 7) | $R_L$ = 10 kΩ, Pin 6 Open<br>Voltage Efficiency ≥ 90% | 3 to 10 | **3 to 10** | 3 to 10 | **3 to 10** | V |
| $V^+_L$ | Supply Voltage Range Low | $R_L$ = 10 kΩ, Pin 6 to Gnd.<br>Voltage Efficiency ≥ 90% | 1.5 to 3.5 | **1.5 to 3.5** | 1.5 to 3.5 | **1.5 to 3.5** | V |
| $R_{out}$ | Output Source Resistance | $I_L$ = 20 mA | 55 | 100<br>**150** | 100 | **120** | Ω max |
| | | V = 2V, $I_L$ = 3 mA<br>Pin 6 Short to Gnd. | 110 | 200<br>**300** | 200 | **300** | Ω max |
| $F_{osc}$ | Oscillator Frequency | | 10 | | | | kHz |
| $P_{eff}$ | Power Efficiency | $R_L$ = 5 kΩ, LMC7660 Only | 97 | 95<br>**90** | 95 | **90** | % min |
| $V_{o\ eff}$ | Voltage Conversion Efficiency | $R_L = \infty$ | 99.9 | 97<br>**95** | 97 | **95** | % min |
| $I_{osc}$ | Oscillator Sink or Source Current | Pin 7 = Gnd. or $V^+$ | 3 | | | | μA |
| **The following applies to the LMC7669, $R_{flag}$ = 1 MΩ, (Note 4).** ***Figure 1.*** | | | | | | | |
| $I_s$ | Supply Current | $R_L = \infty$, LMC7669 Only | 200 | | **FUTURE PRODUCT** | | μA max |
| $I_{flag}$ | Pin 1 Source Current | $V_{pin\ 1}$ = 4.5V | 40 | | | | μA min |
| Flag L | $V_{out}$ When Pin 1 Sets Low | Force $V_{out}$ High Until Pin 1 Sets Low | −2.3 | | | | V min |
| Flag H | $V_{out}$ When Pin 1 Resets High | Force $V_{out}$ Low Until Pin 1 Resets High | −3.6 | | | | V max |
| $P_{eff}$ | Power Efficiency | $R_L$ = 5 kΩ | 94 | | | | % |

**Note 1:** Absolute Maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 4 for conditions.

**Note 2:** Connecting any input terminal to voltages greater than $V^+$ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power-up" of the LMC7660 or the LMC7669.

**Note 3:** For operation at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{ja}$ and $T_j$ max, $T_j = T_A + \theta_{ja} P_D$.

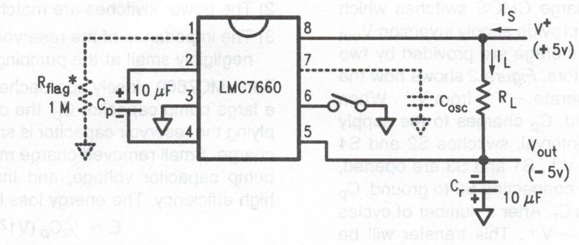
**Note 4:** **Boldface** numbers apply at temperature extremes. All other numbers apply at $T_A$ = 25°C, $V^+$ = 5V, $C_{osc}$ = 0, and apply for the LMC7660 and the LMC7669 unless otherwise specified. Test circuit is shown in *Figure 1*.

**Note 5:** Guaranteed and 100% production tested.

**Note 6:** Guaranteed over the operating temperature range (but not 100% tested). These limits are not used to calculate outgoing quality levels.

**Note 7:** The LMC7660 and the LMC7669 can operate without an external diode over the full temperature and voltage range. The LMC7660 can also be used with the external diode Dx, when replacing previous 7660 designs.

**Note 8:** The test circuit consists of the human body model of 100 pF in series with 1500Ω.

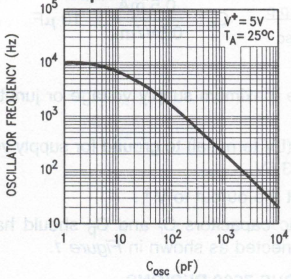

1
2
3
4
8
7
6
5
LMC7660
R_flag*
1 M
C_p
10 µF
S
V+
(+5v)
I_L
C_osc
R_L
V_out
(−5v)
C_r
10 µF
TL/H/9136-5

*Pull down resistor (LMC7669 only)

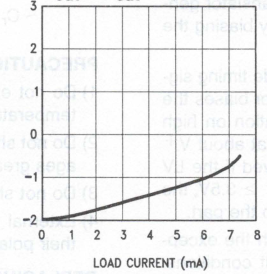
**FIGURE 1. LMC7660/LMC7669 Test Circuit**

# Typical Performance Characteristics

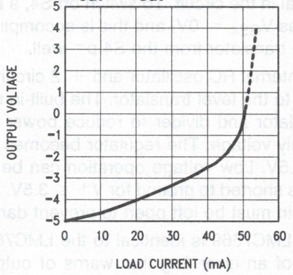
**OSC Freq. vs OSC Capacitance**



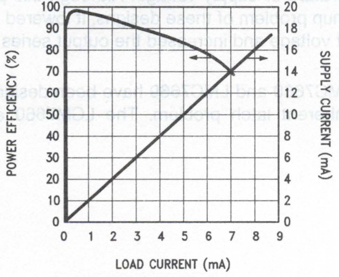
**$V_{out}$ vs $I_{out}$ @ $V^+ = 2V$**



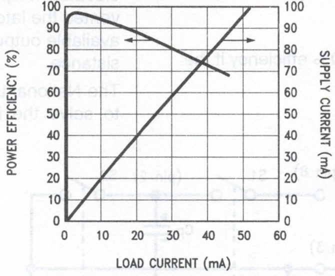
**$V_{out}$ vs $I_{out}$ @ $V^+ = 5V$**



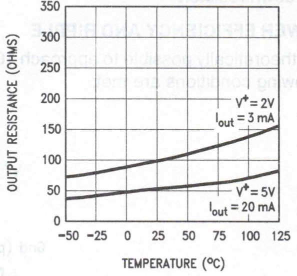
**Supply Current & Power Efficiency vs Load Current ($V^+ = 2V$)**



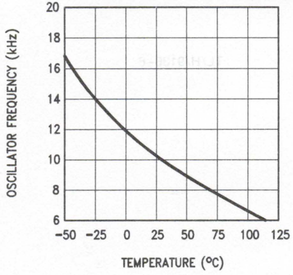
**Supply Current & Power Efficiency vs Load Current ($V^+ = 5V$)**



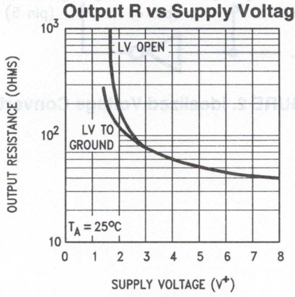
**Output Source Resistance as a Function of Temperature**



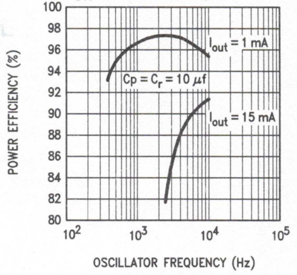
**Unloaded Oscillator Frequency as a Function of Temperature**



**Output R vs Supply Voltage**



**$P_{eff}$ vs OSC Freq. @ $V^+ = 5V$**



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## CIRCUIT DESCRIPTION

The LMC7660 contains four large CMOS switches which are switched in a sequence to provide supply inversion $V_{out} = -V_{in}$. Energy transfer and storage are provided by two inexpensive electrolytic capacitors. *Figure 2* shows how the LMC7660 can be used to generate $-V^+$ from $V^+$. When switches S1 and S3 are closed, $C_p$ charges to the supply voltage $V^+$. During this time interval, switches S2 and S4 are open. After $C_p$ charges to $V^+$, S1 and S3 are opened, S2 and S4 are then closed. By connecting S2 to ground, $C_p$ develops a voltage $-V^+/2$ on $C_r$. After a number of cycles $C_r$ will be pumped to exactly $-V^+$. This transfer will be exact assuming no load on $C_r$, and no loss in the switches.

In the circuit of *Figure 2*, S1 is a P-channel device and S2, S3, and S4 are N-channel devices. Because the output is biased below ground, it is important that the $p^-$ wells of S3 and S4 never become forward biased with respect to either their sources or drains. A substrate logic circuit guarantees that these $p^-$ wells are always held at the proper voltage. Under all conditions S4 $p^-$ well must be at the lowest potential in the circuit. To switch off S4, a level translator generates $V_{GS4} = 0V$, and this is accomplished by biasing the level translator from the S4 $p^-$ well.

An internal RC oscillator and ÷ 2 circuit provide timing signals to the level translator. The built-in regulator biases the oscillator and divider to reduce power dissipation on high supply voltage. The regulator becomes active at about $V^+ = 6.5V$. Low voltage operation can be improved if the LV pin is shorted to ground for $V^+ \leq 3.5V$. For $V^+ \geq 3.5V$, the LV pin must be left open to prevent damage to the part.

The LMC7669 is identical to the LMC7660 with the exception of an error flag that warns of output fault conditions. The flag goes low when a fault pulls the output to about $-0.5V^+$. Hysteresis provides a reset to the flag when $V_{out} = -0.75V^+$. The only additional component required is a pull down resistor.

## POWER EFFICIENCY AND RIPPLE

It is theoretically possible to approach 100% efficiency if the following conditions are met:

1) The drive circuitry consumes little power.

2) The power switches are matched and have low $R_{on}$.

3) The impedance of the reservoir and pump capacitors are negligibly small at the pumping frequency.

The LMC7660 closely approaches 1 and 2 above. By using a large pump capacitor $C_p$, the charge removed while supplying the reservoir capacitor is small compared to $C_p$'s total charge. Small removed charge means small changes in the pump capacitor voltage, and thus small energy loss and high efficiency. The energy loss by $C_p$ is:

$$E = \tfrac{1}{2} C_p \left( V1^2 - V2^2 \right)$$

By using a large reservoir capacitor, the output ripple can be reduced to an acceptable level. For example, if the load current is 5 mA and the accepted ripple is 200 mV, then the reservoir capacitor can omit approximately be calculated from:

$$I_s = C_r \frac{dv}{dt}$$

$$\sim C_r \times \frac{V_{ripple\ p\text{-}p}}{4/F_{osc}} \quad C_r = \frac{0.5\ mA}{0.5V/ms} = 10\ \mu F$$

## PRECAUTIONS

1) Do not exceed the maximum supply voltage or junction temperature.

2) Do not short pin 6 (LV terminal) to ground for supply voltages greater than 3.5V.

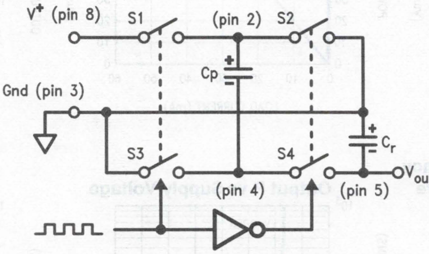
3) Do not short circuit the output to $V^+$.

4) External electrolytic capacitors $C_r$ and $C_p$ should have their polarities connected as shown in *Figure 1*.

## REPLACING PREVIOUS 7660 DESIGNS

To prevent destructive latchup, previous 7660 designs require a diode in series with the output when operated at elevated temperature or supply voltage. Although this prevented the latchup problem of these designs, it lowered the available output voltage and increased the output series resistance.

The National LMC7660 and LMC7669 have been designed to solve the inherent latch problem. The LCM7660 and



TL/H/9136-6

**FIGURE 2. Idealized Voltage Converter**

LMC7669 can operate over the entire supply voltage and temperature range without the need for an output diode. When replacing existing designs, the LMC7660 can be operated with diode Dx.

## Typical Applications

### Changing Oscillator Frequency

It is possible to dramatically reduce the quiescent operating current of the LMC7660/7669 by lowering the oscillator frequency. The oscillator frequency can be lowered from a nominal 10 kHz to several hundred hertz, by adding a slow-down capacitor $C_{osc}$ *(Figure 3)*. As shown in the Typical Performance Curves the supply current can be lowered to the 10 μA range. This low current drain can be extremely useful when used in μPower and battery back-up equipment. It must be understood that the lower operating frequency and supply current cause an increased impedance of $C_r$ and $C_p$. The increased impedance, due to a lower switching rate, can be offset by raising $C_r$ and $C_p$ until ripple and load current requirements are met.

### Synchronizing to an External Clock

*Figure 4* shows an LMC7660 synchronized to an external clock. The CMOS gate overrides the internal oscillator when it is necessary to switch faster or reduce power supply interference. The external clock still passes through the ÷2 circuit in the 7660, so the pumping frequency will be ½ the external clock frequency.

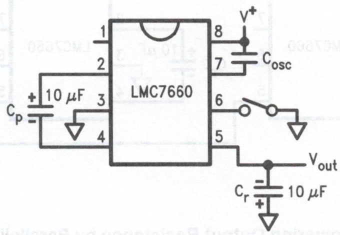


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FIGURE 3. Reduce Supply Current by Lowering Oscillator Frequency

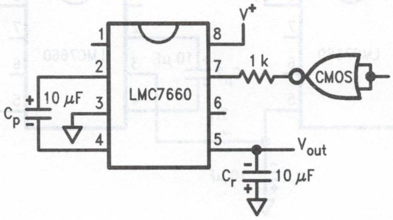

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FIGURE 4. Synchronizing to an External Clock

## Typical Applications (Continued)

### Lowering Output Impedance

Paralleling two or more LMC7660's lowers output impedance. Each device must have it's own pumping capacitor $C_p$, but the reservoir capacitor $C_r$ is shared as depicted in *Figure 5*. The composite output resistance is:

$$R_{out} = \frac{R_{out}\text{ of one LMC7660}}{\text{Number of devices}}$$

### Increasing Output Voltage

Stacking the LMC7660s is an easy way to produce a greater negative voltage. It should be noted that the input current required for each stage is twice the load current on that stage as shown in *Figure 6A*. The effective output resistance is approximately the sum of the individual $R_{out}$ values, and so only a few levels of multiplication can be used.

It is possible to generate −15V from +5V by connecting the second 7660's pin 8 to +5V instead of ground as shown in *Figure 6B*. Note that the second 7660 sees a full 20V and the input supply should not be increased beyond +5V.

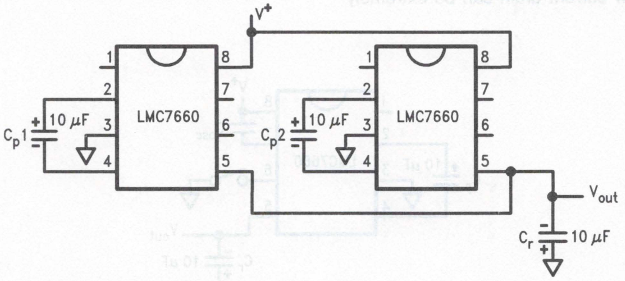
V+
LMC7660
LMC7660
1
2
3
4
5
6
7
8
$C_p1$
10 μF
$C_p2$
10 μF
$V_{out}$
$C_r$
10 μF

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**FIGURE 5. Lowering Output Resistance by Paralleling Devices**

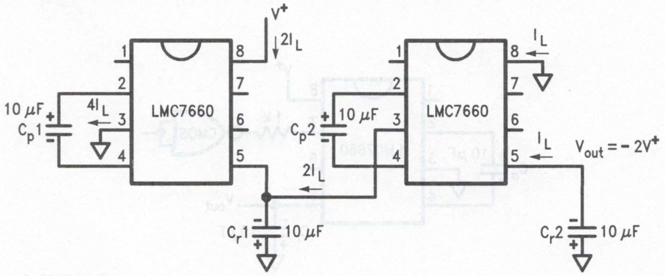
V+
2I L
LMC7660
LMC7660
1
2
3
4
5
6
7
8
10 μF
$C_p1$
4I L
$C_p2$
10 μF
2I L
I L
I L
$V_{out}$ = −2V+
$C_r1$
10 μF
$C_r2$
10 μF

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**FIGURE 6A. Higher Voltage by Cascade**

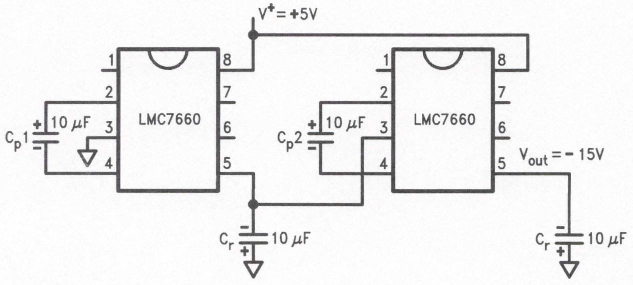
V+ = +5V
LMC7660
LMC7660
1
2
3
4
5
6
7
8
$C_p1$
10 μF
$C_p2$
10 μF
$V_{out}$ = −15V
$C_r$
10 μF
$C_r$
10 μF

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**FIGURE 6B. Getting −15V from +5V**

## Typical Applications (Continued)

### Split V$^+$ In Half

*Figure 7* is one of the more interesting applications for the LMC7660. The circuit can be used as a precision voltage divider (for very light loads), alternately it is used to generate a ½ supply point in battery applications. In the ½ cycle when S1 and S3 are closed, the supply voltage divides across the capacitors in a conventional way proportional to their value. In the ½ cycle when S2 and S4 are closed, the capacitors switch from a series connection to a parallel connection. This forces the capacitors to have the same voltage; the charge redistributes to maintain precisely V$^+$/2, across $C_p$ and $C_r$. In this application all devices are only V$^+$/2, and the supply voltage can be raised to 20V giving exactly 10V at $V_{out}$.

### Getting Up . . . and Down

The LMC7660 can also be used as a positive voltage multiplier. This application, shown in *Figure 8*, requires 2 additional diodes. During the first ½ cycle S2 charges $C_p1$ through D1; D2 is reverse biased. In the next ½ cycle S2 is open and S1 is closed. Since $C_p1$ is charged to $V^+ - V_{D1}$ and is referenced to V$^+$ through S1, the junction of D1 and D2 is at $V^+ + (V^+ - V_{D1})$. D1 is reverse biased in this interval. This application uses only two of the four switches in the 7660. The other two switches can be put to use in performing a negative conversion at the same time as shown in *Figure 9*. In the ½ cycle that D1 is charging $C_p1$, $C_p2$ is connected from ground to $-V_{out}$ via S2 and S4, and $C_r2$ is storing $C_p2$'s charge. In the interval that S1 and S3 are closed, $C_p1$ pumps the junction of D1 and D2 above V$^+$, while $C_p2$ is refreshed from V$^+$.

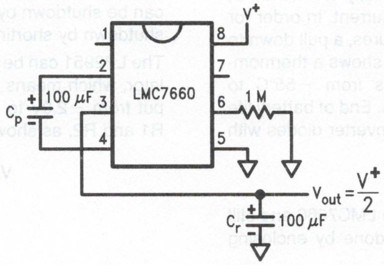

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**FIGURE 7. Split V$^+$ in Half**

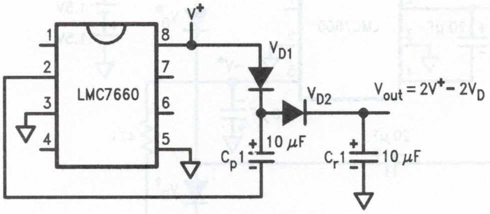

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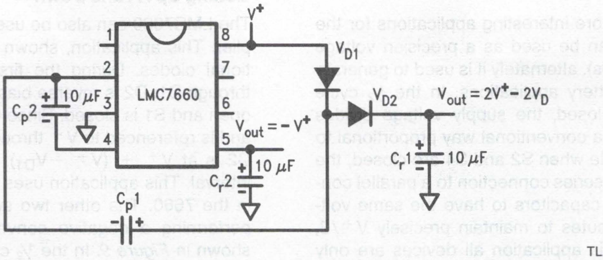
**FIGURE 8. Positive Voltage Multiplier**

## Typical Applications (Continued)


V+
1
8
2
7
$C_p2$
10 µF
3
LMC7660
6
4
5
$V_{out} = -V^+$
10 µF
$C_r2$
$C_p1$
$V_{D1}$
$V_{D2}$
$V_{out} = 2V^+ - 2V_D$
$C_r1$
10 µF

TL/H/9136–14

**FIGURE 9. Combined Negative Converter and Positive Multiplier**

### Thermometer Spans 180°C

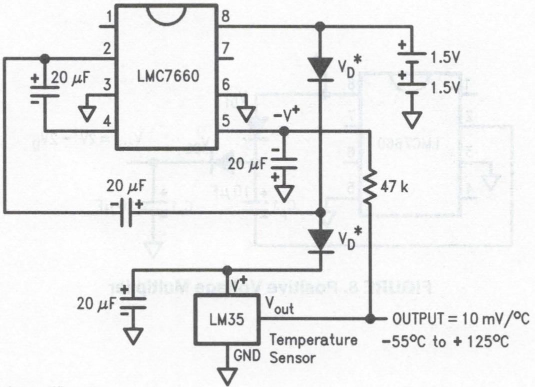
Using the combined negative and positive multiplier of *Figure 10* with an LM35 it is possible to make a µPower thermometer that spans a 180°C temperature range. The LM35 temperature sensor has an output sensitivity of 10 mV/°C, while drawing only 50 µA of quiescent current. In order for the LM35 to measure negative temperatures, a pull down to a negative voltage is required. *Figure 10* shows a thermometer circuit for measuring temperatures from −55°C to +125°C and requiring only two 1.5V cells. End of battery life can be extended by replacing the up converter diodes with Schottky's.

### Regulating $-V_{out}$

It is possible to regulate the output of the LMC7660 and still maintain µPower performance. This is done by enclosing the LMC7660 in a loop with a LP2951. The circuit of *Figure 11* will regulate $V_{out}$ to −5V for $I_L = 10$ mA, and $V_{in} = 6V$. For $V_{in} > 7V$, the output stays in regulation up to $I_L = 25$ mA. The error flag on pin 5 of the LP2951 sets low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high; the LMC7660 can be shutdown by shorting pin 7 and pin 8.

The LP2951 can be reconfigured to an adjustable type regulator, which means the LMC7660 can give a regulated output from −2.0V to −10V dependent on the resistor ratios R1 and R2, as shown in *Figure 12*, $V_{ref} = 1.235V$:

$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

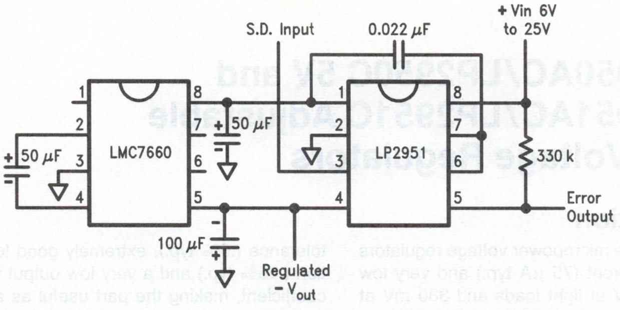

1
2
3
4
8
7
6
5
20 µF
LMC7660
$V_D$*
1.5V
1.5V
$-V^+$
20 µF
47 k
20 µF
$V_D$*
V+
20 µF
LM35
$V_{out}$
GND
Temperature Sensor
OUTPUT = 10 mV/°C
−55°C to +125°C

*For lower voltage operation, use Schottky rectifiers

TL/H/9136–15

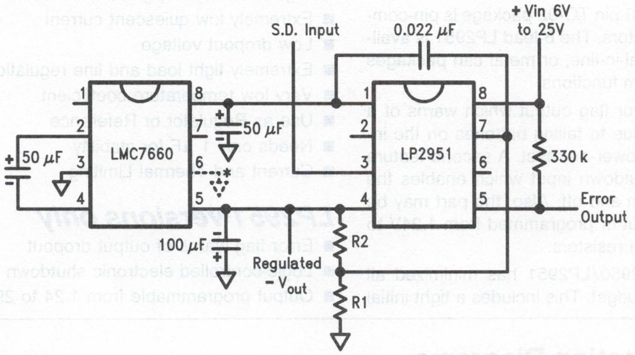
**FIGURE 10. µPower Thermometer Spans 180°C, and Pulls Only 150 µA**

## Typical Applications (Continued)


S.D. Input
0.022 μF
+ Vin 6V to 25V
LMC7660
LP2951
50 μF
50 μF
330 k
Error Output
100 μF
Regulated − Vout
1
2
3
4
5
6
7
8

TL/H/9136–16

**FIGURE 11. Regulated −5V with 200 μA Standby Current**


S.D. Input
0.022 μF
+ Vin 6V to 25V
LMC7660
LP2951
50 μF
50 μF
330 k
Error Output
100 μF
Regulated − Vout
R2
R1
*
1
2
3
4
5
6
7
8

$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$

$V_{ref} = 1.235V$

*Low voltage operation

TL/H/9136–17

**FIGURE 12. LMC7660 and LP2951 Make a Negative Adjustable Regulator**

National
Semiconductor
Corporation

# LP2950/LP2950AC/LP2950C 5V and LP2951/LP2951AC/LP2951C Adjustable Micropower Voltage Regulators

## General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 μA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950 in the popular 3-pin TO-92 package is pin-compatible with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

## Features

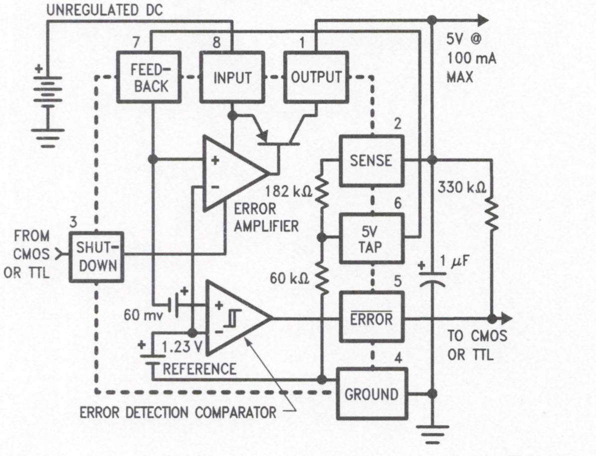
- High accuracy 5V, guaranteed 100 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs only 1 μF for stability
- Current and Thermal Limiting

### *LP2951 versions only*

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

## Block and Connection Diagrams

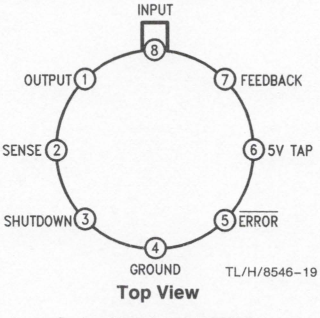
**(LP2951 Pinout)**


UNREGULATED DC
7
8
1
FEED-BACK
INPUT
OUTPUT
5V @ 100 mA MAX
2
SENSE
+
−
ERROR AMPLIFIER
182 kΩ
330 kΩ
6
5V TAP
3
FROM CMOS OR TTL
SHUT-DOWN
60 kΩ
1 μF
5
60 mv
1.23 V
REFERENCE
ERROR
TO CMOS OR TTL
4
GROUND
ERROR DETECTION COMPARATOR

TL/H/8546-1

**Order Number LP2951J, LP2951ACJ, LP2951CJ, LP2951ACN or LP2951CN**
**See NS Package Number J08A or N08E**

**Metal Can Package (H)**

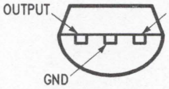

INPUT
8
OUTPUT 1
7 FEEDBACK
SENSE 2
6 5V TAP
SHUTDOWN 3
5 ERROR
4
GROUND

TL/H/8546-19

**Top View**

**Order Number LP2951H**
**See NS Package Number H08C**

**TO-92 Plastic Package (Z)**


OUTPUT
INPUT
GND

TL/H/8546-2

**Bottom View**
**Order Number LP2950ACZ-5.0**
**or LP2950CZ-5.0**
**See NS Package Number Z03A**

**Order Number LP2951ACM or LP2951CM for SO-8**
**See NS Package Number M08A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

Power Dissipation Internally Limited

Lead Temp. (Soldering, 5 seconds) 260°C

Storage Temperature Range −65° to +150°C

Operating Junction Temperature Range (Note 8)

LP2951 −55° to +150°C

LP2950AC/LP2950C,
LP2951AC/LP2951C −40° to +125°C

Input Supply Voltage −0.3 to +30V

Feedback Input Voltage (Notes 9 and 10) −1.5 to +30V

Shutdown Input Voltage (Note 9) −0.3 to +30V

Error Comparator Output Voltage (Note 9) −0.3 to +30V

ESD Rating is to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions (Note 2) | LP2951 | | LP2950AC LP2951AC | | | LP2950C LP2951C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Tested Limit (Note 3) | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | |
| Output Voltage | $T_J = 25^\circ C$ | 5.0 | 5.025<br>4.975 | 5.0 | 5.025<br>4.975 | | 5.0 | 5.05<br>4.95 | | V max<br>V min |
| | $-25^\circ C \le T_J \le 85^\circ C$ | | | | | 5.05<br>4.95 | | | 5.075<br>4.925 | V max<br>V min |
| | Full Operating Temperature Range | | **5.06**<br>**4.94** | | | **5.06**<br>**4.94** | | | **5.1**<br>**4.9** | V max<br>V min |
| Output Voltage | $100\ \mu A \le I_L \le 100\ mA$<br>$T_J \le T_{J_{MAX}}$ | | **5.075**<br>**4.925** | | | **5.07**<br>**4.93** | | | **5.12**<br>**4.88** | V max<br>V min |
| Output Voltage Temperature Coefficient | (Note 12) | **20** | **120** | **20** | | **100** | **50** | | **150** | ppm/°C |
| Line Regulation (Note 14) | $6V \le V_{in} \le 30V$ (Note 15) | 0.03 | 0.1<br>**0.5** | 0.03 | 0.1 | **0.2** | 0.04 | 0.2 | **0.4** | % max<br>% max |
| Load Regulation (Note 14) | $100\ \mu A \le I_L \le 100\ mA$ | 0.04 | 0.1<br>**0.3** | 0.04 | 0.1 | **0.2** | 0.1 | 0.2 | **0.3** | % max<br>% max |
| Dropout Voltage (Note 5) | $I_L = 100\ \mu A$ | 50 | 80<br>**150** | 50 | 80 | **150** | 50 | 80 | **150** | mV max<br>mV max |
| | $I_L = 100\ mA$ | 380 | 450<br>**600** | 380 | 450 | **600** | 380 | 450 | **600** | mV max<br>mV max |
| Ground Current | $I_L = 100\ \mu A$ | 75 | 120<br>**140** | 75 | 120 | **140** | 75 | 120 | **140** | μA max<br>μA max |
| | $I_L = 100\ mA$ | 8 | 12<br>**14** | 8 | 12 | **14** | 8 | 12 | **14** | mA max<br>mA max |
| Dropout Ground Current | $V_{in} = 4.5V$<br>$I_L = 100\ \mu A$ | 110 | 170<br>**200** | 110 | 170 | **200** | 110 | 170 | **200** | μA max<br>μA max |
| Current Limit | $V_{out} = 0$ | 160 | 200<br>**220** | 160 | 200 | **220** | 160 | 200 | **220** | mA max<br>mA max |
| Thermal Regulation | (Note 13) | 0.05 | 0.2 | 0.05 | 0.2 | | 0.05 | 0.2 | | %/W max |
| Output Noise, 10 Hz to 100 KHz | $C_L = 1\ \mu F$ | 430 | | 430 | | | 430 | | | μV rms |
| | $C_L = 200\ \mu F$ | 160 | | 160 | | | 160 | | | μV rms |
| | $C_L = 3.3\ \mu F$ (Bypass = $0.01\ \mu F$ Pins 7 to 1 (LP2951)) | 100 | | 100 | | | 100 | | | μV rms |
| **8-Pin Versions only** | | **LP2951** | | **LP2951AC** | | | **LP2951C** | | | |
| Reference Voltage | | 1.235 | 1.25<br>**1.26**<br>1.22<br>**1.2** | 1.235 | 1.25<br>1.22 | **1.26**<br>**1.2** | 1.235 | 1.26<br>1.21 | **1.27**<br>**1.2** | V max<br>V max<br>V min<br>V min |
| Reference Voltage | (Note 7) | | **1.27**<br>**1.19** | | | **1.27**<br>**1.19** | | | **1.285**<br>**1.185** | V max<br>V min |

## Electrical Characteristics (Note 1) (Continued)

| Parameter | Conditions (Note 2) | LP2951 | | LP2951AC | | | LP2951C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Tested Limit (Note 3) | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | Typ | Tested Limit (Note 3) | Design Limit (Note 4) | |
| **8-Pin Versions only** (Continued) | | | | | | | | | | |
| Feedback Pin Bias Current | | 20 | 40<br>**60** | 20 | 40 | <br>**60** | 20 | 40 | <br>**60** | nA max<br>nA max |
| Reference Voltage Temperature Coefficient | (Note 12) | 20 | | 20 | | | 50 | | | ppm/°C |
| Feedback Pin Bias Current Temperature Coefficient | | 0.1 | | 0.1 | | | 0.1 | | | nA/°C |
| **Error Comparator** | | | | | | | | | | |
| Output Leakage Current | $V_{OH} = 30V$ | 0.01 | 1<br>**2** | 0.01 | 1 | <br>**2** | 0.01 | 1 | <br>**2** | μA max<br>μA max |
| Output Low Voltage | $V_{in} = 4.5V$<br>$I_{OL} = 400\ \mu A$ | 150 | 250<br>**400** | 150 | 250 | <br>**400** | 150 | 250 | <br>**400** | mV max<br>mV max |
| Upper Threshold Voltage | (Note 6) | 60 | 40<br>**25** | 60 | 40 | <br>**25** | 60 | 40 | <br>**25** | mV min<br>mV min |
| Lower Threshold Voltage | (Note 6) | 75 | 95<br>**140** | 75 | 95 | <br>**140** | 75 | 95 | <br>**140** | mV max<br>mV max |
| Hysteresis | (Note 6) | 15 | | 15 | | | 15 | | | mV |
| **Shutdown Input** | | | | | | | | | | |
| Input Logic Voltage | <br>Low<br>High | 1.3 | <br>**0.6**<br>**2.0** | 1.3 | | <br>**0.7**<br>**2.0** | 1.3 | | <br>**0.7**<br>**2.0** | V<br>V max<br>V min |
| Shutdown Pin Input Current | $V_{shutdown} = 2.4V$ | 30 | 50<br>**100** | 30 | 50 | <br>**100** | 30 | 50 | <br>**100** | μA max<br>μA max |
| | $V_{shutdown} = 30V$ | 450 | 600<br>**750** | 450 | 600 | <br>**750** | 450 | 600 | <br>**750** | μA max<br>μA max |
| Regulator Output Current in Shutdown | (Note 11) | 3 | 10<br>**20** | 3 | 10 | <br>**20** | 3 | 10 | <br>**20** | μA max<br>μA max |

**Note 1: Boldface limits apply at temperature extremes.**

**Note 2:** Unless otherwise specified all limits guaranteed for $T_J = 25°C$, $V_{in} = 6V$, $I_L = 100\ \mu A$ and $C_L = 1\ \mu f$. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense ($V_{out} = 5V$) and $V_{shutdown} \leq 0.8V$.

**Note 3:** Guaranteed and 100% production tested.

**Note 4:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

**Note 5:** Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V **(2.3V over temperature)** must be taken into account.

**Note 6:** Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain $= V_{out}/V_{ref} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of $V_{out}$ as $V_{out}$ is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

**Note 7:** $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, $2.3V \leq V_{in} \leq 30V$, $100\ \mu A \leq I_L \leq 100\ mA$, $T_J \leq T_{JMAX}$.

**Note 8:** The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4″ leads and 160°C/W with 0.25″ leads to a PC board. The thermal resistance of the 8-pin DIP packages is 105°C/W for the molded plastic (N) and 130°C/W for the cerdip (J) junction to ambient when soldered directly to a PC board. Thermal resistance for the metal can (H) is 160°C/W junction to ambient and 20°C/W junction to case. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W.

**Note 9:** May exceed input supply voltage.

**Note 10:** When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

**Note 11:** $V_{shutdown} \geq 2V$, $V_{in} \leq 30V$, $V_{out} = 0$, Feedback pin tied 5V Tap.

**Note 12:** Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

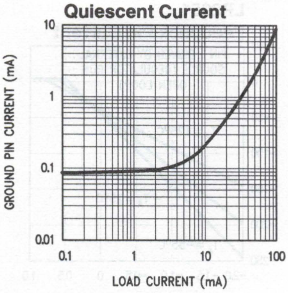
**Note 13:** Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at $V_{IN} = 30V$ (1.25W pulse) for T = 10 ms.

**Note 14:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

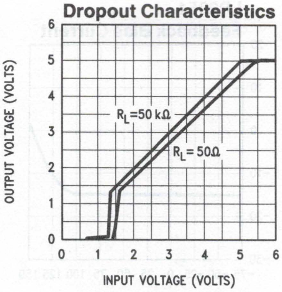
**Note 15:** Line regulation for the LP2951 is tested at 150°C for $I_L = 1$ mA. For $I_L = 100\ \mu A$ and $T_J = 125°C$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

## Typical Performance Characteristics

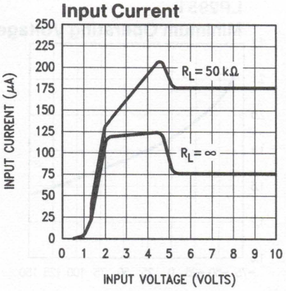
Quiescent Current



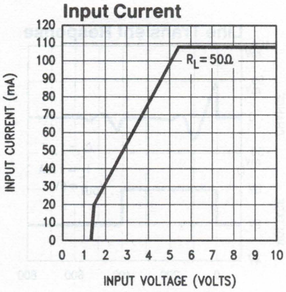
Dropout Characteristics



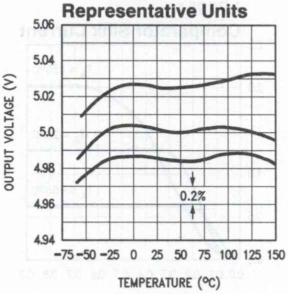
Input Current



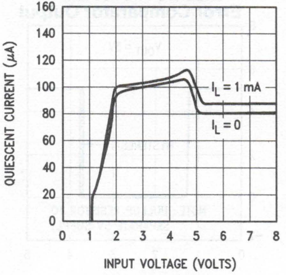
Input Current



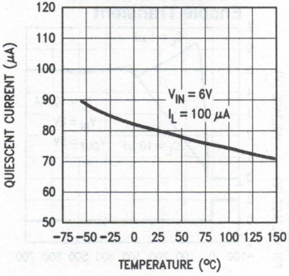
Output Voltage vs. Temperature of 3 Representative Units



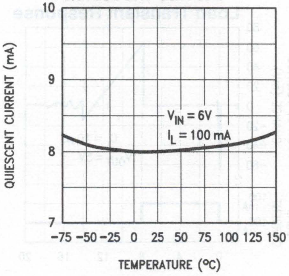
Quiescent Current



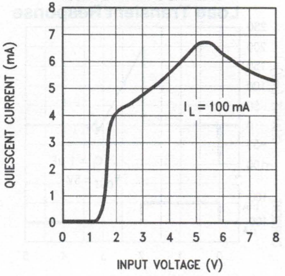
Quiescent Current



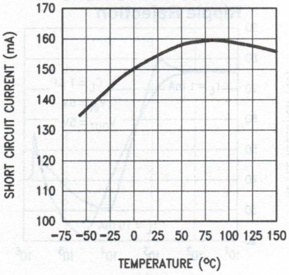
Quiescent Current



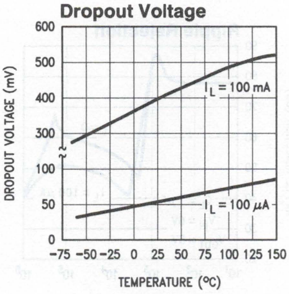
Quiescent Current



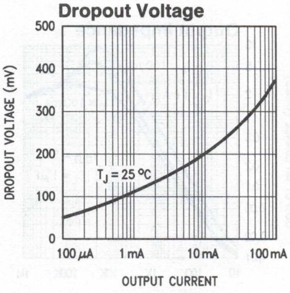
Short Circuit Current



Dropout Voltage

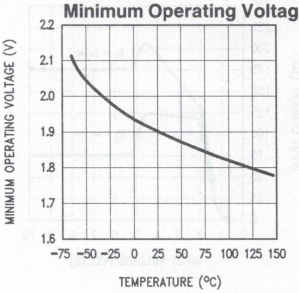


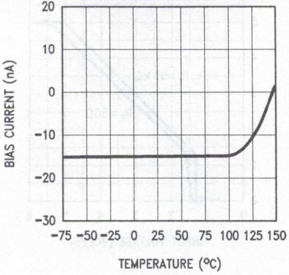
Dropout Voltage

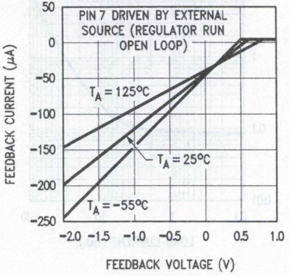


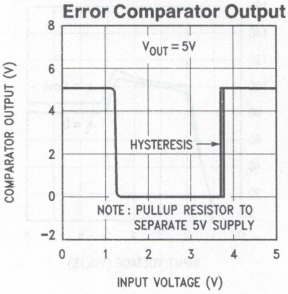
TL/H/8546–3

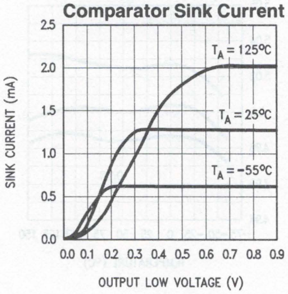
## Typical Performance Characteristics (Continued)

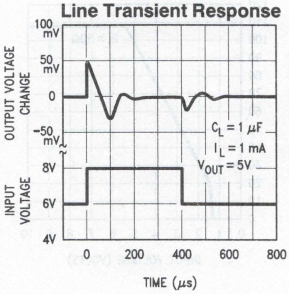

**LP2951**
**Minimum Operating Voltage**

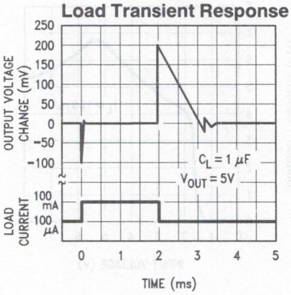

**LP2951**
**Feedback Bias Current**

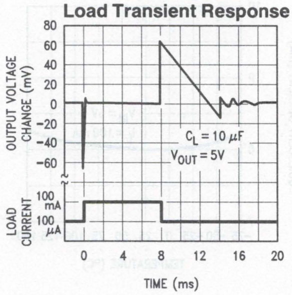

**LP2951**
**Feedback Pin Current**

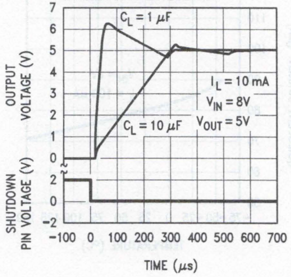

**LP2951**
**Error Comparator Output**

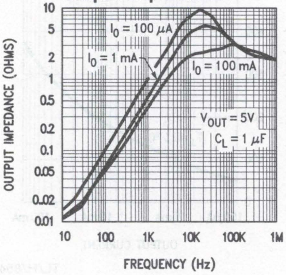

**LP2951**
**Comparator Sink Current**

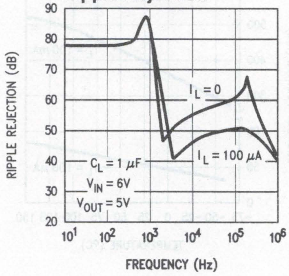

**Line Transient Response**

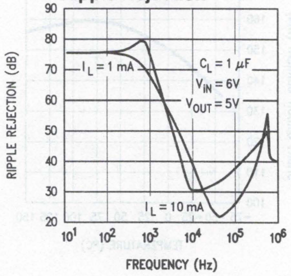

**Load Transient Response**


**Load Transient Response**


**LP2951**
**Enable Transient**


**Output Impedance**


**Ripple Rejection**


**Ripple Rejection**

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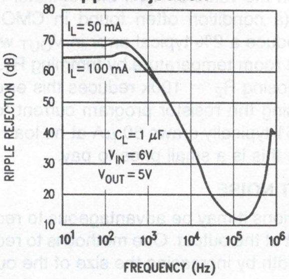
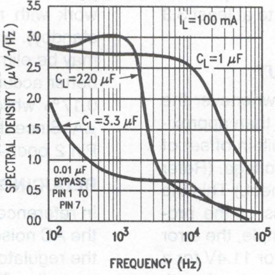
## Typical Performance Characteristics (Continued)

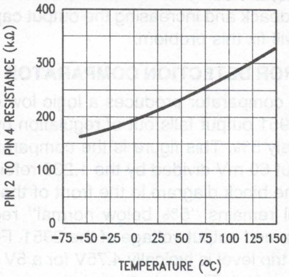
**Ripple Rejection**



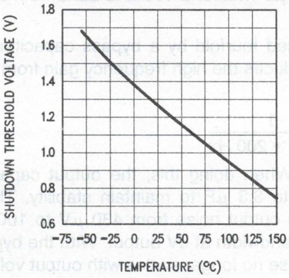
**Output Noise**



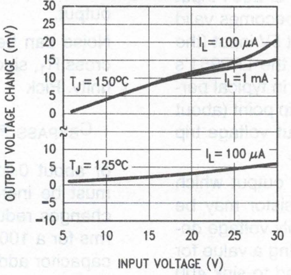
**LP2951 Divider Resistance**



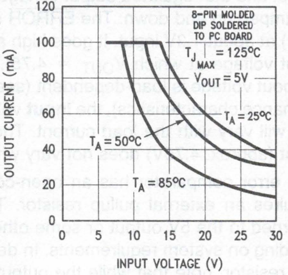
**Shutdown Threshold Voltage**



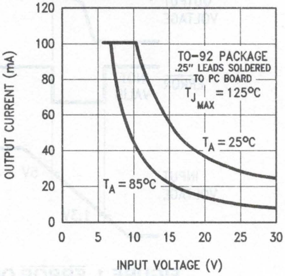
**Line Regulation**



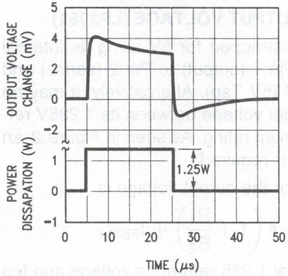
**LP2950 Maximum Rated Output Current**



**LP2950 Maximum Rated Output Current**



**Thermal Response**



TL/H/8546-5

## Application Hints

### EXTERNAL CAPACITORS

A 1.0 μf (or greater) capacitor is required between the LP2950/LP2951 output and ground for stability. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 μf for currents below 10 mA or 0.1 μf for currents below 1 mA. Using the 8-Pin versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 μf (or greater) capacitor should be used.

Unlike many other regulators, the L2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 version with external resistors, a minimum load of 1 μA is recommended.

A 0.1 μf capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem

## Application Hints (Continued)

when using high value external resistors to set the output voltage. Adding a 100 pf capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 $\mu$f will fix this problem.

### ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

*Figure 1* below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{OUT} = 4.75$). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the 5V output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 $\mu$A, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 M$\Omega$. The resistor is not required if this output is unused.

### PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2,* an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where $V_{REF}$ is the nominal 1.235 reference voltage and $I_{FB}$ is the feedback pin bias current, nominally $-20$ nA. The minimum recommended load current of 1 $\mu$A forces an upper limit of 1.2 M$\Omega$ on the value of $R_2$, if the regulator must work with no load (a condition often found in CMOS in standby). $I_{FB}$ will produce a 2% typical error in $V_{OUT}$ which may be eliminated at room temperature by trimming $R_1$. For better accuracy, choosing $R_2 = 100$k reduces this error to 0.17% while increasing the resistor program current to 12 $\mu$A. Since the LP2951 typically draws 60 $\mu$A at no load with Pin 2 open-circuited, this is a small price to pay.

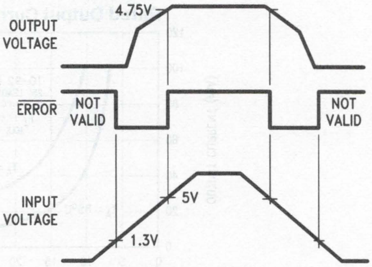
### REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 $\mu$F to 220 $\mu$F only decreases the noise from 430 $\mu$V to 160 $\mu$V rms for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across $R_1$, since it reduces the high frequency gain from 4 to unity. Pick

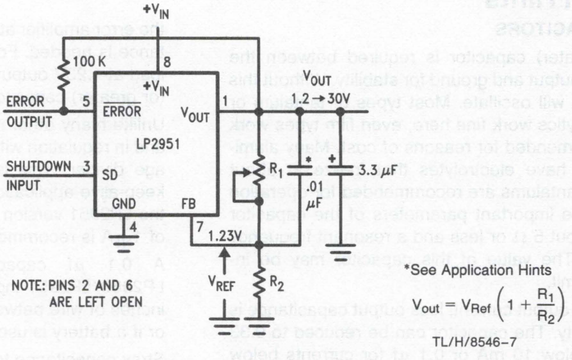
$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\text{ Hz}}$$

or about 0.01 $\mu$F. When doing this, the output capacitor must be increased to 3.3 $\mu$F to maintain stability. These changes reduce the output noise from 430 $\mu$V to 100 $\mu$V rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



TL/H/8546-20

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing



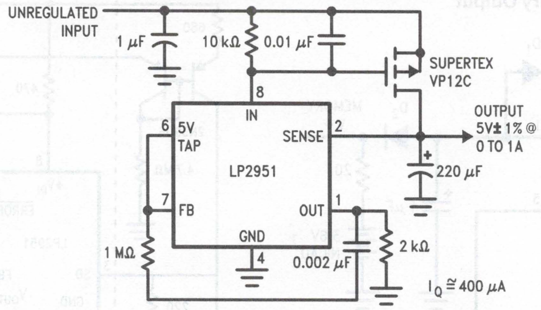
$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

TL/H/8546-7

FIGURE 2. Adjustable Regulator

# Typical Applications

## 1A Regulator with 1.2V Dropout


UNREGULATED INPUT
1 μF
10 kΩ
0.01 μF
SUPERTEX VP12C
8
IN
6
5V TAP
SENSE
2
OUTPUT 5V± 1% @ 0 TO 1A
LP2951
220 μF
7
FB
OUT
1
GND
4
1 MΩ
0.002 μF
2 kΩ
I_Q ≅ 400 μA

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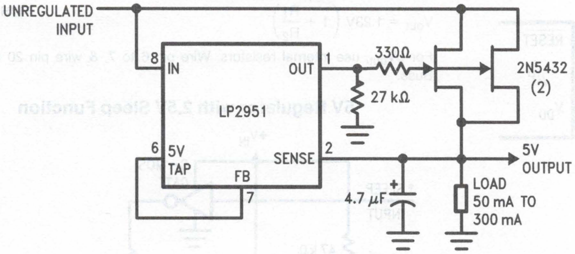
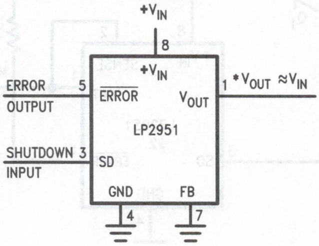
## 300 mA Regulator with 0.75V Dropout


UNREGULATED INPUT
8
IN
OUT
1
330Ω
27 kΩ
2N5432 (2)
LP2951
6
5V TAP
SENSE
2
FB
7
5V OUTPUT
4.7 μF
LOAD 50 mA TO 300 mA

TL/H/8546-21

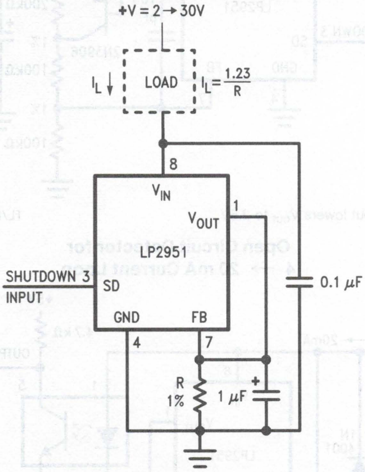
## Wide Input Voltage Range Current Limiter


+V_IN
8
+V_IN
ERROR OUTPUT
5
ERROR
V_OUT
1
*V_OUT ≈V_IN
LP2951
SHUTDOWN INPUT
3
SD
GND
FB
4
7

TL/H/8546-9

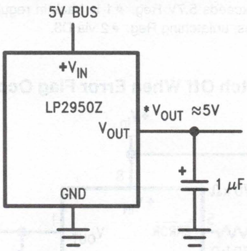
*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

## Low Drift Current Source


+V = 2 → 30V
I_L
LOAD
I_L = 1.23/R
8
V_IN
1
V_OUT
LP2951
SHUTDOWN INPUT
3
SD
0.1 μF
GND
FB
4
7
R 1%
1 μF

TL/H/8546-8

## 5 Volt Current Limiter

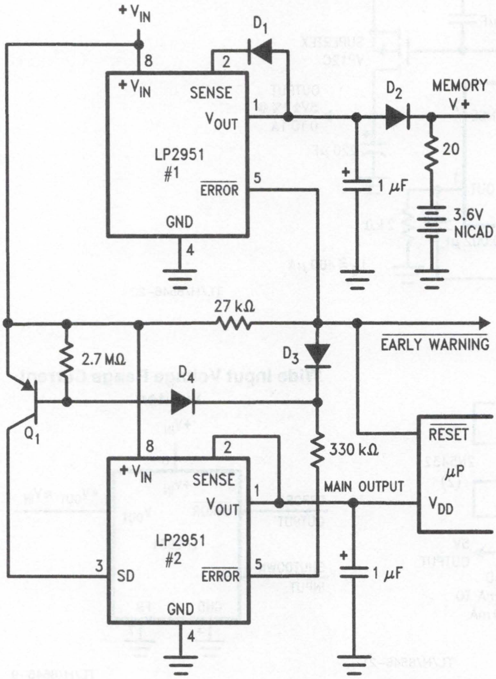

5V BUS
+V_IN
LP2950Z
*V_OUT ≈5V
V_OUT
1 μF
GND

TL/H/8546-10

*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

## Typical Applications (Continued)

### Regulator with Early Warning and Auxiliary Output

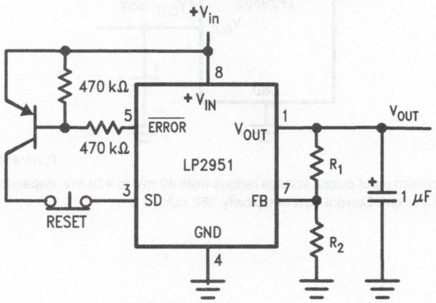

+VIN
D1
8
2
+VIN
SENSE
VOUT
1
D2
MEMORY V+
20
LP2951 #1
ERROR
5
1 μF
3.6V NICAD
GND
4
27 kΩ
2.7 MΩ
D3
EARLY WARNING
D4
Q1
8
2
330 kΩ
RESET
μP
VDD
+VIN
SENSE
VOUT
1
MAIN OUTPUT
LP2951 #2
3
SD
ERROR
5
1 μF
GND
4

TL/H/8546-11

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

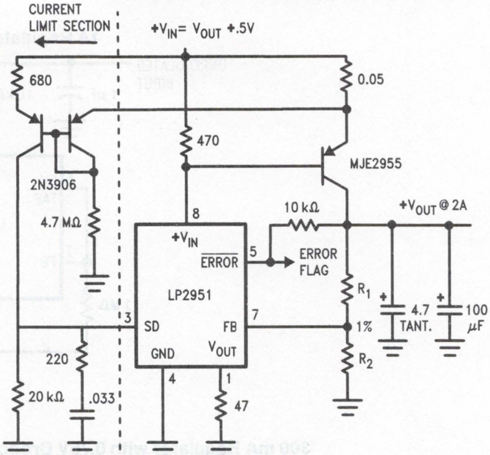
Operation: Reg. #1's $V_{out}$ is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When $V_{in}$ drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When $V_{in}$ again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

### Latch Off When Error Flag Occurs


+Vin
470 kΩ
8
+VIN
5
470 kΩ
ERROR
VOUT
1
VOUT
LP2951
R1
3
SD
FB
7
1 μF
RESET
GND
R2
4

TL/H/8546-12

### 2 Ampere Low Dropout Regulator

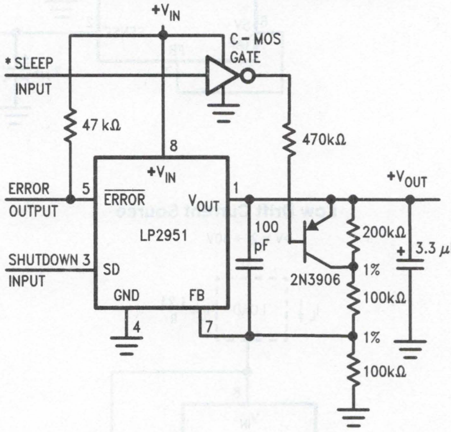

CURRENT LIMIT SECTION
+VIN = VOUT +.5V
680
0.05
470
2N3906
MJE2955
4.7 MΩ
8
10 kΩ
+VOUT @ 2A
+VIN
5
ERROR
ERROR FLAG
LP2951
R1
3
SD
FB
7
1%
4.7 TANT.
100 μF
220
GND
VOUT
R2
4
1
20 kΩ
.033
47

TL/H/8546-13

$$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$$

For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 20 to $+V_{out}$ Buss.

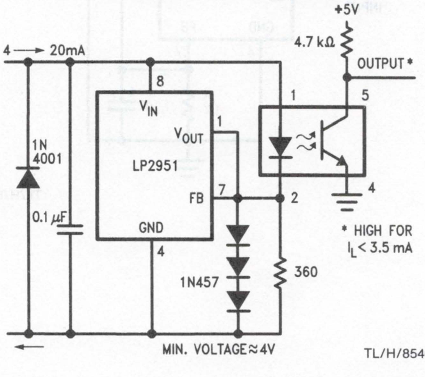
### 5V Regulator with 2.5V Sleep Function


+VIN
C-MOS GATE
*SLEEP INPUT
47 kΩ
470kΩ
8
+VIN
+VOUT
ERROR OUTPUT
5
ERROR
VOUT
1
LP2951
100 pF
200kΩ
3.3 μF
SHUTDOWN INPUT
3
SD
2N3906
1%
GND
FB
100kΩ
4
7
1%
100kΩ

*High input lowers $V_{out}$ to 2.5V

TL/H/8546-14

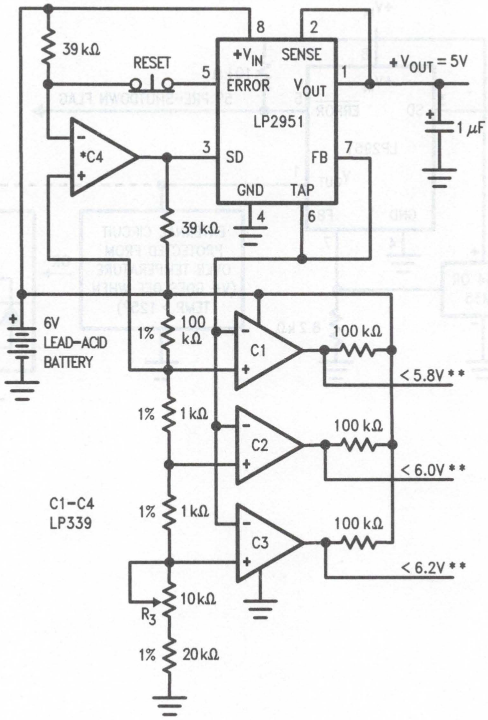
### Open Circuit Detector for 4 → 20 mA Current Loop


+5V
4.7 kΩ
4 → 20mA
OUTPUT*
8
VIN
1
5
VOUT
1
1N 4001
LP2951
FB
7
2
4
0.1 μF
GND
* HIGH FOR IL < 3.5 mA
4
360
1N457
MIN. VOLTAGE≈4V

TL/H/8546-15

## Typical Applications (Continued)

### Regulator with State-of-Charge Indicator


39 kΩ
RESET
5
8
2
+V_IN
SENSE
ERROR
V_OUT
1
+V_OUT = 5V
LP2951
1 μF
*C4
3
SD
FB
7
GND
TAP
4
6
39 kΩ
6V
LEAD-ACID
BATTERY
1%
100 kΩ
C1
100 kΩ
< 5.8V **
1%
1 kΩ
C2
100 kΩ
< 6.0V **
C1–C4
LP339
1%
1 kΩ
C3
100 kΩ
< 6.2V **
10kΩ
R3
1%
20kΩ

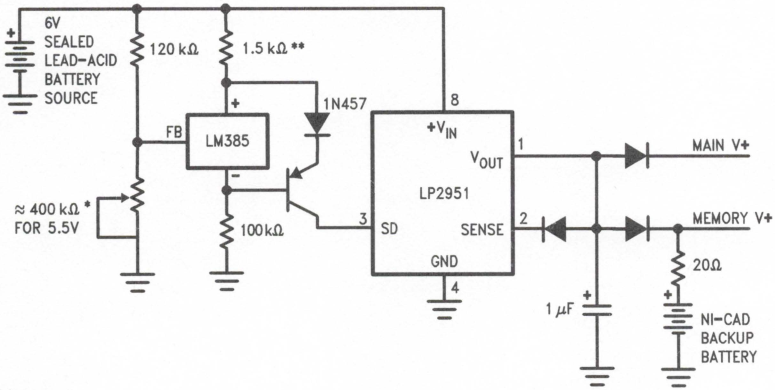
TL/H/8546–16

*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when $V_{in}$ is 6.0V.

**Outputs go low when $V_{in}$ drops below designated thresholds.

### Low Battery Disconnect

For values shown, Regulator shuts down when $V_{in} < 5.5V$ and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 μA.


6V
SEALED
LEAD–ACID
BATTERY
SOURCE
120 kΩ
1.5 kΩ **
1N457
FB
LM385
8
+V_IN
V_OUT
1
MAIN V+
≈ 400 kΩ *
FOR 5.5V
100kΩ
3
LP2951
SD
SENSE
2
MEMORY V+
GND
4
20Ω
1 μF
NI–CAD
BACKUP
BATTERY

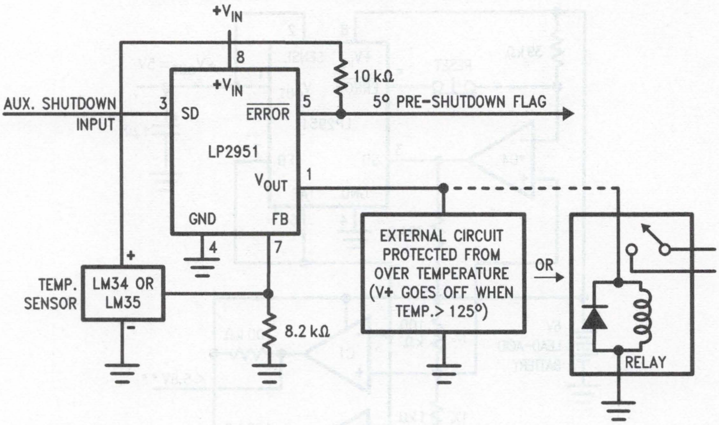
TL/H/8546–17

*Sets disconnect Voltage

**Sets disconnect Hysteresis

## Typical Applications (Continued)

### System Overtemperature Protection Circuit

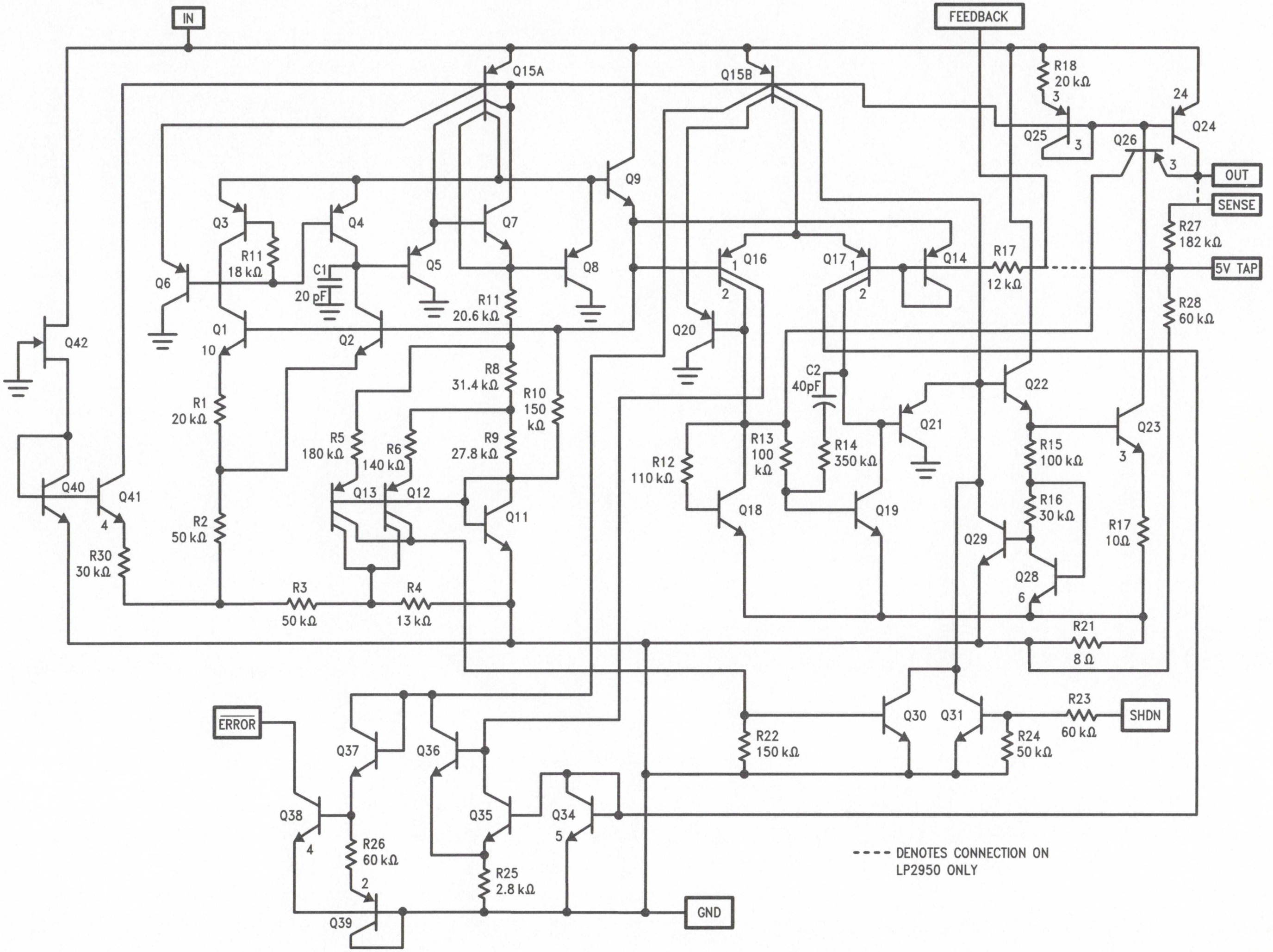

+V_IN
8
+V_IN
10 kΩ
AUX. SHUTDOWN INPUT
3
SD
ERROR
5
5° PRE-SHUTDOWN FLAG
LP2951
V_OUT
1
GND
FB
4
7
+
TEMP. SENSOR
LM34 OR LM35
-
8.2 kΩ
EXTERNAL CIRCUIT PROTECTED FROM OVER TEMPERATURE (V+ GOES OFF WHEN TEMP.> 125°)
OR
RELAY

TL/H/8546-18

LM34 for 125°F Shutdown

LM35 for 125°C Shutdown

## Schematic Diagram


IN
FEEDBACK
Q15A
Q15B
R18 20 kΩ
3
24
Q24
Q25
3
Q26
3
OUT
SENSE
R27 182 kΩ
5V TAP
R28 60 kΩ
Q9
Q3
Q4
Q7
R11 18 kΩ
Q5
Q8
C1
20 pF
Q6
R11 20.6 kΩ
Q1
10
Q2
Q42
R1 20 kΩ
R8 31.4 kΩ
R10 150 kΩ
R5 180 kΩ
R6 140 kΩ
R9 27.8 kΩ
Q13
Q12
Q11
Q40
Q41
4
R2 50 kΩ
R30 30 kΩ
R3 50 kΩ
R4 13 kΩ
Q16
Q17
1
2
Q14
R17 12 kΩ
Q20
C2 40pF
Q22
Q21
R13 100 kΩ
R14 350 kΩ
R12 110 kΩ
Q18
Q19
Q23
R15 100 kΩ
R16 30 kΩ
Q29
Q28
6
R17 10Ω
R21 8 Ω
ERROR
Q37
Q36
Q38
Q35
Q34
5
4
R26 60 kΩ
2
Q39
R25 2.8 kΩ
Q30
Q31
R22 150 kΩ
R23 60 kΩ
SHDN
R24 50 kΩ
GND
---- DENOTES CONNECTION ON LP2950 ONLY

TL/H/8546-23

# Section 2

# Operational Amplifiers

## Section 2 Contents

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LF156, LF156A, LF256, LF356, LF356A, LF356B Wide Band . . . . . 2-23
LF157, LF157A, LF257, LF357, LF357A, LF357B Wide Band Decompensated (AVMIN = 5) . 2-23
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***Devices Not Covered In Last Publication**

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# Operational Amplifiers
# Definition of Terms

**Bandwidth:** That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

**Common-Mode Rejection Ratio:** The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

**Harmonic Distortion:** That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

**Input Bias Current:** The average of the two input currents.

**Input Common-Mode Voltage Range:** The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

**Input Impedance:** The ratio of input voltage to input current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Input Offset Current:** The difference in the currents into the two input terminals when the output is at zero.

**Input Offset Voltage:** That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Input Voltage Range:** The range of voltages on the input terminals for which the amplifier operates within specifications.

**Large-Signal Voltage Gain:** The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**Output Impedance:** The ratio of output voltage to output current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Output Resistance:** The small signal resistance seen at the output with the output voltage near zero.

**Output Voltage Swing:** The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Offset Voltage Temperature Drift:** The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

**Power Supply Rejection:** The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Settling Time:** The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**Slew Rate:** The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

**Supply Current:** The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

**Transient Response:** The closed-loop step-function response of the amplifier under small-signal conditions.

**Unity Gain Bandwidth:** The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

**Voltage Gain:** The ratio of output voltage to input voltage under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

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# General Purpose Operational Amplifier Selection Guide

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| Military Temperature Range (−55°C to +125°C) Specs at $T_A$ = 25°C (Note 1) | | | | | | | | |
| LH0044A | 0.025 | 15 | 0.4 | 0.06 | 3 | ±3 | ±20 | |
| LM607A | 0.025 | 2 | 1.8 | 0.7 | 1.5 | * | ±22 | |
| LH0044 | 0.05 | 30 | 0.4 | 0.06 | 4 | ±3 | ±20 | |
| LM607B | 0.05 | 3 | 1.8 | 0.7 | 1.5 | * | ±22 | |
| LM11 | 0.3 | 0.05 | * | 0.3 | 0.6 | * | ±20 | |
| LF411A | 0.5 | 0.2 | 4 | 15 | 2.8 | ±6 | ±22 | |
| LF441A | 0.5 | 0.05 | 1 | 1 | 0.2 | ±6 | ±22 | |
| LH0052 | 0.5 | 0.003 | 1 | 3 | 3.5 | ±5 | ±22 | |
| LM108A | 0.5 | 2 | 1 | 0.3 | 0.4 | ±2 | ±20 | |
| LF412A | 1 | 0.2 | 4 | 15 | 5.6 | ±6 | ±22 | Dual BiFet |
| LF442A | 1 | 0.05 | 1 | 1 | 0.4 | ±6 | ±22 | Dual BiFet |
| LH0004 | 1 | 100 | * | * | 0.15 | ±5 | ±45 | |
| LM604A | 1 | 40 | 7 | 2 | 8 | 4 | 36 | Multiplexed OA |
| LF155A | 2 | 0.05 | 2.5 | 5 | 4 | ±5 | ±22 | |
| LF156A | 2 | 0.05 | 5 | 12 | 7 | ±5 | ±22 | |
| LF157A | 2 | 0.05 | 25 | 50 | 7 | ±5 | ±22 | Minimum Gain of 5 |
| LF411 | 2 | 0.2 | 4 | 15 | 3.4 | ±6 | ±18 | |
| LMC660A | 2 | 0.02 | 1.5 | 1.7 | 2.2 | 5 | 15 | Quad CMOS |
| LM10 | 2 | 20 | * | * | 0.4 | (Note 4) | | OA + Reference |
| LM101A | 2 | 75 | 1 | 0.5 | 3 | ±3 | ±22 | |
| LM107 | 2 | 75 | 1 | 0.5 | 3 | ±3 | ±22 | |
| LM108 | 2 | 2 | 1 | 0.3 | 0.4 | ±2 | ±20 | |
| LM112 | 2 | 2 | 1 | 0.2 | 0.6 | ±2 | ±20 | Compensated LM108 |
| LM124A | 2 | 50 | * | * | 3 | 3 | 32 | Quad |
| LM158A | 2 | 50 | * | * | 1.2 | 3 | 32 | Dual |
| LP124 | 2 | 4 | 0.1 | 0.05 | 0.13 | 3 | 32 | Quad |
| LH0020 | 2.5 | 250 | * | * | 5 | ±5 | ±22 | |
| LF412 | 3 | 0.2 | 4 | 15 | 6.8 | ±6 | ±22 | Dual |
| LM741A | 3 | 80 | 1.5 | 0.7 | 2.8 | ±3 | ±22 | |
| LH0022 | 4 | 0.01 | 1 | 3 | 3.5 | ±5 | ±22 | |
| LF155 | 5 | 0.1 | 2.5 | 5 | 4 | ±5 | ±22 | |

## General Purpose Operational Amplifier Selection Guide (Continued)

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/$\mu$s (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| Military Temperature Range (−55°C to +125°C) Specs at $T_A$ = 25°C (continued) | | | | | | | | |
| LF156 | 5 | 0.1 | 5 | 12 | 7 | ±5 | ±22 | |
| LF157 | 5 | 0.1 | 20 | 50 | 7 | ±5 | ±22 | Minimum Gain of 5 |
| LF147 | 5 | 0.2 | 4 | 13 | 11 | ±6 | ±22 | Quad BiFet |
| LF412 | 5 | 0.2 | 4 | 15 | 6.8 | ±6 | ±18 | Dual BiFet |
| LF442 | 5 | 0.1 | 1 | 1 | 0.5 | ±6 | ±18 | Dual BiFet |
| LF444A | 5 | 0.1 | 1 | 1 | 0.80 | ±6 | ±22 | Quad BiFet |
| LH0086 | 5 | 0.5 | 3 | 10 | 15.5 | ±8 | ±18 | Programmable Gain OA |
| LM124 | 5 | 150 | * | * | 3 | 3 | 32 | Quad |
| LM143 | 5 | 20 | 1 | 2.5 | 4 | ±4 | ±40 | |
| LM144 | 5 | 20 | 1 | 2.5 | 4 | ±4 | ±40 | Minimum Gain of 10 |
| LM146 | 5 | 100 | 1.2 | 0.4 | 2 | ±1.5 | ±22 | (Note 5) |
| LM148 | 5 | 100 | 1 | 0.5 | 3.6 | ±5 | ±22 | Quad |
| LM149 | 5 | 100 | 4 | 2 | 3.6 | ±5 | ±22 | Minimum Gain of 5, Quad |
| LM158 | 5 | 150 | * | * | 1.2 | 3 | 32 | Dual |
| LM192 | 5 | 150 | * | * | 2 | 3 | 32 | Comparator and Op Amp |
| LM741 | 5 | 500 | * | 0.5 | 2.8 | ±3 | ±22 | |
| LM1558 | 5 | 500 | * | * | 5 | ±3 | ±22 | Dual |
| LM4250 | 5 | 50 | 0.2 | 0.2 | 0.1 | ±1 | ±18 | (Note 5) |
| LH0042 | 20 | 0.025 | 1 | 3 | 3.5 | ±5 | ±22 | |

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/$\mu$s (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| Industrial Temperature Range (−25°C to +85°C) (Note 1) | | | | | | | | |
| LMC669B | 0.025 | 0.1 | * | * | 6 | ±8 | ±22 | Autozero Block |
| LH0044B | 0.05 | 30 | 0.4 | 0.06 | 4 | ±3 | ±20 | |
| LH0044C | 0.05 | 30 | 0.4 | 0.06 | 4 | ±3 | ±20 | |
| LMC669C | 0.05 | 0.1 | * | * | 6 | ±8 | ±22 | Autozero Block |
| LM208A | 0.5 | 2 | 1 | 0.3 | 0.6 | ±2 | ±20 | |
| LH0052C | 1 | 0.005 | 1 | 3 | 3.8 | ±5 | ±22 | |
| LMC660A | 2 | 0.02 | 1.5 | 1.7 | 2.2 | 5 | 15 | Quad CMOS |
| LM10B(L) | 2 | 20 | * | * | 0.4 | (Note 4) | | Op Amp and Reference |
| LM201A | 2 | 75 | 1 | 0.5 | 3 | ±3 | ±22 | |
| LM207 | 2 | 75 | 1 | 0.5 | 3 | ±3 | ±22 | |
| LM208 | 2 | 2 | 1 | 0.3 | 0.6 | ±2 | ±20 | |
| LM212 | 2 | 2 | 1 | 0.3 | 0.6 | ±2 | ±20 | Compensated LM208 |
| LM224A | 3 | 80 | * | * | 2 | 3 | 32 | Quad |

## General Purpose Operational Amplifier Selection Guide (Continued)

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| **Industrial Temperature Range (−25°C to +85°C) (continued)** | | | | | | | | |
| LM258A | 3 | 80 | * | * | 1.2 | 3 | 32 | Dual |
| LF255 | 5 | 0.1 | 2.5 | 5 | 4 | ±5 | ±22 | |
| LF256 | 5 | 0.1 | 5 | 12 | 7 | ±5 | ±22 | |
| LF257 | 5 | 0.1 | 20 | 50 | 7 | ±5 | ±22 | Minimum Gain of 5 |
| LM224 | 5 | 150 | * | * | 2 | 3 | 32 | Quad |
| LM258 | 5 | 150 | * | * | 1.2 | 3 | 32 | Dual |
| LM292 | 5 | 250 | * | * | 2 | 3 | 32 | Comparator and Op Amp |
| LH0020C | 6 | 500 | * | * | 6 | ±5 | ±22 | |
| LH0022C | 6 | 0.025 | 1 | 3 | 4 | ±5 | ±22 | |
| LM246 | 6 | 250 | 0.5 | 0.4 | 2.5 | ±2 | ±18 | (Note 5) |
| LM248 | 6 | 200 | 1 | 0.5 | 4.5 | ±5 | ±18 | Quad |
| LM249 | 6 | 200 | 4 | 2 | 4.5 | ±5 | ±18 | Minimum Gain of 5, Quad |
| LH0086C | 10 | 0.5 | 3 | 10 | 15.5 | ±8 | ±18 | Programmable Gain 1 to 200 |
| LH0042C | 20 | 0.05 | 1 | 3 | 4 | ±5 | ±22 | |

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| **Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2)** | | | | | | | | |
| LMC668A | 0.005 | 0.06 | 1 | 2.5 | 3.5 | * | 18 | Commutating Autozero |
| LMC668 | 0.01 | 0.06 | 1 | 2.5 | 3.5 | * | 18 | Commutating Autozero |
| LMC669B | 0.025 | 0.1 | * | * | 6 | ±8 | ±22 | Autozero Block |
| LM607A | 0.025 | 2 | 1.8 | 0.7 | 1.5 | * | ±22 | |
| LMC669C | 0.05 | 0.1 | * | * | 6 | ±8 | ±22 | Autozero Block |
| LM607B | 0.05 | 3 | 1.8 | 0.7 | 1.5 | * | ±22 | |
| LM607 | 0.15 | 10 | 1.8 | 0.7 | 1.8 | * | ±22 | |
| LF411A | 0.5 | 0.2 | 4 | 15 | 2.8 | ±6 | ±22 | |
| LF441A | 0.5 | 0.05 | 1 | 1 | 0.2 | ±6 | ±22 | |
| LM308A | 0.5 | 7 | 1 | 0.3 | 0.8 | ±2 | ±20 | |
| LM11C | 0.6 | 0.1 | * | 0.3 | 0.8 | * | ±20 | |
| LF412A | 1 | 0.2 | 4 | 15 | 5.6 | ±6 | ±22 | Dual |
| LF442A | 1 | 0.05 | 1 | 1 | 0.4 | ±6 | ±22 | Dual |
| LM604A | 1 | 40 | 5 | 3 | 9 | 4 | 36 | Multiplexed Op Amp |
| LF355A | 2 | 0.05 | 2.5 | 5 | 4 | ±5 | ±22 | |
| LF356A | 2 | 0.05 | 5 | 12 | 10 | ±5 | ±22 | |
| LF357A | 2 | 0.05 | 20 | 50 | 10 | ±5 | ±22 | Minimum Gain of 5 |

## General Purpose Operational Amplifier Selection Guide (Continued)

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| **Commercial Temperature Range (0°C to +70°C) (continued)** | | | | | | | | |
| LF411 | 2 | 0.2 | 4 | 15 | 3.4 | ±6 | ±22 | |
| LF412 | 3 | 0.2 | 4 | 15 | 6.8 | ±6 | ±22 | Dual |
| LM324A | 3 | 100 | * | * | 3 | 3 | 32 | Quad |
| LM358A | 3 | 100 | * | * | 2 | 3 | 32 | Dual |
| LM604 | 3 | 60 | 5 | 7 | 9 | 4 | 36 | Multiplexed Op Amp |
| LM741E | 3 | 80 | 1.5 | 0.7 | 2.8 | ±3 | ±22 | |
| LM10C(L) | 4 | 30 | * | * | 0.5 | (Note 4) | | OA and Reference |
| LP324 | 4 | 10 | 0.1 | 0.05 | 0.15 | 3 | 32 | |
| LF347B | 5 | 0.2 | 4 | 13 | 11 | ±6 | ±22 | Quad |
| LF355B | 5 | 0.1 | 2.5 | 5 | 4 | ±5 | ±22 | |
| LF356B | 5 | 0.1 | 5 | 12 | 4 | ±5 | ±22 | |
| LF357B | 5 | 0.1 | 20 | 50 | 7 | ±5 | ±22 | |
| LF441 | 5 | 0.1 | 1 | 1 | 0.25 | ±6 | ±22 | |
| LF442 | 5 | 0.1 | 1 | 1 | 0.5 | ±6 | ±22 | Dual |
| LM11CL | 5 | 0.2 | * | 0.3 | 0.8 | * | ±20 | |
| LM392 | 5 | 250 | * | * | 2 | 3 | 32 | |
| LM833 | 5 | 1000 | 10 | 5 | 8 | * | ±18 | Dual Low Noise |
| LMC660 | 6 | 0.02 | 1.5 | 1.7 | 2.7 | 5 | 15 | Quad CMOS |
| LM346 | 6 | 250 | 0.5 | 0.4 | 2.5 | ±1.5 | ±22 | (Note 5) |
| LM348 | 6 | 200 | 1 | 0.5 | 4.5 | ±5 | ±18 | |
| LM349 | 6 | 200 | 4 | 2 | 4.5 | ±5 | ±18 | |
| LM741C | 6 | 500 | 1.5 | 0.5 | 2.8 | ±3 | ±18 | |
| LM1458 | 6 | 500 | * | * | 5.6 | ±3 | ±18 | |
| LM4250C | 6 | 75 | 0.2 | 0.2 | 0.1 | ±1 | ±18 | (Note 5) |
| LM324 | 7 | 250 | * | * | 3 | 3 | 32 | |
| LM358 | 7 | 250 | * | * | 2 | 3 | 32 | |
| LM301A | 7.5 | 250 | 1 | 0.5 | 3 | ±3 | ±18 | |
| LM307 | 7.5 | 250 | 1 | 0.5 | 3 | ±3 | ±18 | |
| LM308 | 7.5 | 7 | 1 | 0.3 | 0.8 | ±2 | ±18 | |
| LM312 | 7.5 | 7 | 1 | 0.2 | 0.8 | ±2 | ±18 | Compensated LM308 |
| LM343 | 8 | 40 | 1 | 2.5 | 5 | ±4 | ±34 | |
| LM344 | 8 | 40 | 1 | 2.5 | 5 | ±4 | ±34 | Minimum Gain of 10 |
| LF347 | 10 | 0.2 | 4 | 13 | 11 | ±6 | ±18 | Quad BiFet |
| LF351 | 10 | 0.2 | 4 | 13 | 3.4 | ±6 | ±18 | |
| LF353 | 10 | 0.2 | 4 | 13 | 6.8 | ±6 | ±18 | Dual BiFet |
| LF355 | 10 | 0.2 | 2.5 | 5 | 4 | ±5 | ±18 | |
| LF356 | 10 | 0.2 | 5 | 12 | 10 | ±5 | ±18 | |
| LF357 | 10 | 0.2 | 20 | 50 | 10 | ±5 | ±18 | Minimum Gain of 5 |

## General Purpose Operational Amplifier Selection Guide (Continued)

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| **Commercial Temperature Range (0°C to +70°C)** (continued) | | | | | | | | |
| LF444 | 10 | 0.1 | 1 | 1 | 1 | ±6 | ±18 | Quad BiFet |
| LF13741 | 15 | 0.2 | 1 | 0.5 | 4 | * | ±18 | |
| TL081C | 15 | 0.2 | 4 | 13 | 2.8 | ±6 | ±18 | |
| TL082C | 15 | 0.2 | 4 | 13 | 5.6 | ±6 | ±18 | Dual BiFet |

| Part # | $V_{OS}$ mV (Max) | $I_B$ nA (Max) | GBW MHz (Typ) | Slew Rate V/µs (Typ) | Supply Current (Note 3) mA (Max) | Supply Voltage | | Special Features |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min V | Max V | |
| **Automotive Temperature Range (−40°C to +85°C)** | | | | | | | | |
| LM604 | 3 | 60 | 7 | 3 | 9 | 4 | 36 | Multiplexed Op Amp |
| LP2902 | 4 | 20 | 0.1 | 0.05 | 0.15 | 3 | 26 | Quad |
| LM2902 | 7 | 250 | * | * | 3 | 3 | 26 | Quad |
| LM2904 | 7 | 250 | * | * | 2 | 3 | 26 | Quad |
| LM2924 | 7 | 250 | * | * | 2 | 3 | 26 | Comparator Plus Op Amp |

*Not Specified.

**Note 1:** Datasheet should be referred to for test conditions and more detailed information.

**Note 2:** Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

**Note 3:** Supply current is for all amplifiers in a package.

**Note 4:** The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

**Note 5:** The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

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# Low $I_{BIAS}$ Selection Guide

| ≤5 pA | ≤20 pA | ≤50 pA | ≤100 pA | ≤200 pA | ≤500 pA | ≤1 nA |
|---|---|---|---|---|---|---|
| **$T_A$ = 25°C** | | | | | | |
| LH0022 | LMC668 | LH0032A | LH0032 | LF401A | LH4101 | LH4104 |
| LH0022C | LMC660 | LF155A/156A | LF155/156 | LF401 | LH0032C | |
| LH0042 | | LF157A | LF157 | LF400A | LH0086 | |
| LH0042C | | LF355A/356A | LF255/256 | LF400 | LH0086C | |
| LH0052 | | LF357A | LF257 | TL081 | | |
| LH0052C | | LF441A | LF355B/356B | LH0032AC | | |
| LH0062 | | LF442A | LF357B | LF351 | | |
| | | LF444A | LF441 | LF411A/411 | | |
| | | LM11 | LF442 | LF355/356 | | |
| | | | LF444 | LF357 | | |
| | | | LM11C | LF147/347B/347 | | |
| | | | LH0062C | LF353 | | |
| | | | | LF412A/412 | | |
| | | | | LF13741 | | |
| | | | | LM11CL | | |

**Note:** Datasheet should be referred to for conditions and more detailed information.

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# High Speed Operational Amplifier Selection Guide

| Part # | Slew Rate V/μs (Typ) | GBW MHz (Typ) | $V_{OS}$ mV (Max) | $I_S$ mA (Max) (Note 2) | Notes |
|---|---|---|---|---|---|
| **GBW ≥ 4 MHz, $T_A$ = 25°C** | | | | | |
| LH0024 | 500 | 70 | 8 | 15 | |
| LH0032 | 500 | 70 | 15 | 22 | FET Input |
| LM6361 | 300 | 50 | 20 | 6.8 | |
| LM6364 | 300 | 175 | 9 | 6.8 | Min Gain of 5 |
| LM6365 | 300 | 725 | 7 | 6.8 | Min Gain of 25 |
| LH4101 | 250 | 40 | 15 | 40 | Medium Power JFET |
| LF400 | 70 | 16 | 2.5 | 12 | Fast Settling JFET |
| LF401 | 70 | 16 | 0.5 | 12 | Precision Fast Settling JFET |
| LH0003 | 70 | 30 | 3 | 3 | |
| LH0062 | 70 | 15 | 15 | 12 | FET Input |
| LM318 | 70 | 15 | 10 | 10 | |
| LF357 | 50 | 20 | 10 | 10 | Min Gain of 5, JFET |
| LH4104 | 40 | 16 | 10 | 25 | Medium Power Fast Settling JFET |
| LM359 | 30 | 30 | * | 22 | Dual Current Mode (Norton) Amp |
| LF411 | 15 | 4 | 2 | 3.4 | JFET |
| LF412 | 15 | 4 | 3 | 6.8 | Dual JFET |
| LF347 | 13 | 4 | 10 | 11 | Quad JFET |
| LF351 | 13 | 4 | 10 | 3.4 | JFET |
| LF353 | 13 | 4 | 10 | 6.8 | Dual JFET |
| LF356 | 12 | 4.5 | 10 | 10 | JFET |
| LM833 | 7 | 15 | 5 | 8 | Dual Low Noise |

*Not specified.

**Note 1:** Datasheet should be referred to for conditions and more detailed information. Many versions with better DC specs are available in addition to those listed above.

**Note 2:** Supply current is for all amplifiers in a package.

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# Medium and High Power Operational Amplifier Selection Guide (≥ 0.1A Output)

| Part # | $I_{OUT}$ A (Typ) | $V_{OS}$ mV (Max) | $I_S$ mA (Max) | Slew Rate V/μS (Typ) | PBW kHz (Typ) |
|---|---|---|---|---|---|
| LH4104 | 0.1 | 10 | 25 | 40 | * |
| LH4101 | 0.1 | 15 | 40 | 250 | * |
| LH0041 | 0.2 | 6 | 4 | 1 | 20 |
| LH0061 | 0.5 | 15 | 15 | 25 | 1000 |
| LH0021 | 1.0 | 6 | 4 | 1 | 20 |
| LH0101A | 2 | 3 | 35 | 10 | 300 |
| LH0101 | 2 | 10 | 35 | 10 | 300 |
| LM675 | 3 | 10 | 50 | 8 | * |
| LM12(L) | (Note 2) | 7 | 80 | 9 | 60 |
| LM12C(L) | (Note 2) | 15 | 120 | 9 | 60 |

*Not Specified

**Note 1:** Refer to Datasheet for conditions and more detailed information.

**Note 2:** $I_{OUT}$ for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

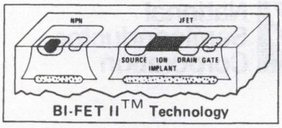
National
Semiconductor
Corporation

# Special Amplifier Selection Guide

| | |
|---|---|
| LH0045 | Two Wire Transmitter |
| LH0082 | 20 MHz Transimpedance Amplifier |
| LH0086 | Programmable Gain Operational Amplifier |
| LM359 | Dual Current Mode (Norton) Amplifier |
| LM2900, 3900, 3301, 3401 | Quad Current Mode (Norton) Amplifier |
| LM3080 | Operational Transconductance Amplifier |
| LM13600 | Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers |
| 13700 | Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers |
| LM604 | 4 In, 1 Out Multiplexed Op Amp |

**Note:** Refer to the datasheet for specifications.

**National Semiconductor Corporation**



BI-FET II™ Technology

# LF147/LF347/LF347B Wide Bandwidth Quad JFET Input Operational Amplifiers

## General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

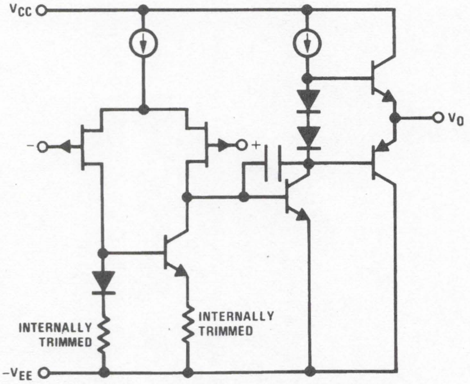
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

## Features

| | |
|---|---|
| ■ Internally trimmed offset voltage | 2 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise current | 0.01 pA/$\sqrt{\text{Hz}}$ |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/µs |
| ■ Low supply current | 7.2 mA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V = 10$,<br>$R_L$ 10k, $V_O = 20$ Vp-p, BW = 20 Hz – 20 kHz | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 µs |

## Simplified Schematic

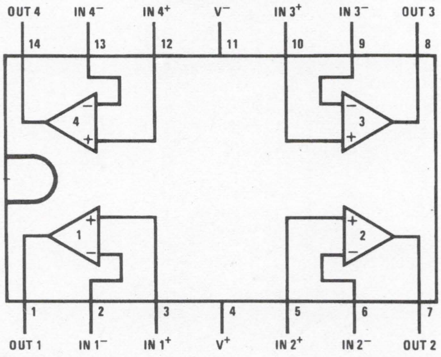
¼ Quad



TL/H/5647-13

## Connection Diagram

Dual-In-Line Package



TL/H/5647-1

**Top View**

**Order Number LF147D, LF347D, LF147J, LF347BJ, LF347J, LF347M, LF347WM, LF347BN or LF347N**
**See NS Package Number D14E, J14A, M14A, M14B or N14A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | LF147 | LF347B/LF347 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |
| Power Dissipation (Notes 3 and 9) | 900 mW | 1000 mW |
| $T_j$ max | 150°C | 150°C |
| $\theta_{jA}$ | 105°C/W | 90°C/W |
| Operating Temperature Range | (Note 4) | (Note 4) |

| | LF147 | LF347B/LF347 |
|---|---|---|
| Storage Temperature Range | $-65°C \leq T_A \leq 150°C$ | |
| Lead Temperature (Soldering, 10 sec.) | 260°C | 260°C |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | | 215°C |
| Infrared (15 seconds) | | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega, T_A = 25°C$ | | 1 | 5 | | 3 | 5 | | 5 | 10 | mV |
| | | Over Temperature | | | 8 | | | 7 | | | 13 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | 10 | | | 10 | | | 10 | | µV/°C |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 5, 6) | | 25 | 100 | | 25 | 100 | | 25 | 100 | pA |
| | | Over Temperature | | | 25 | | | 4 | | | 4 | nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Notes 5, 6) | | 50 | 200 | | 50 | 200 | | 50 | 200 | pA |
| | | Over Temperature | | | 50 | | | 8 | | | 8 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V, T_A = 25°C$<br>$V_O = \pm 10V, R_L = 2\ k\Omega$ | 50 | 100 | | 50 | 100 | | 25 | 100 | | V/mV |
| | | Over Temperature | 25 | | | 25 | | | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V, R_L = 10\ k\Omega$ | ±12 | ±13.5 | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15<br>−12 | | ±11 | +15<br>−12 | | ±11 | +15<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\ k\Omega$ | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | 7.2 | 11 | | 7.2 | 11 | | 7.2 | 11 | mA |

2

## AC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25°C$, $f = 1\ Hz - 20\ kHz$ (Input Referred) | | −120 | | | −120 | | | −120 | | dB |
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | | 13 | | | 13 | | | 13 | | V/µs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | | 4 | | | 4 | | | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$, $f = 1000\ Hz$ | | 20 | | | 20 | | | 20 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_j = 25°C$, $f = 1000\ Hz$ | | 0.01 | | | 0.01 | | | 0.01 | | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{jA}$.

**Note 4:** The LF147 is available In the military temperature range $-55°C \le T_A \le 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \le T_A \le 70°C$. Junction temperature can rise to $T_j$ max = 25°C.

**Note 5:** Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

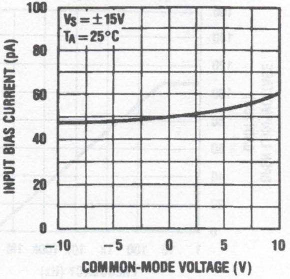
**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

**Note 8:** Refer to RETS147X for LF147D and LF147J military specifications.

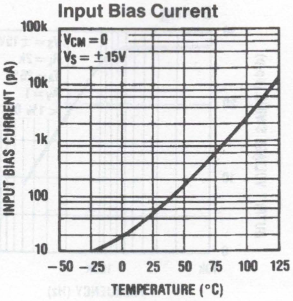
**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

## Typical Performance Characteristics

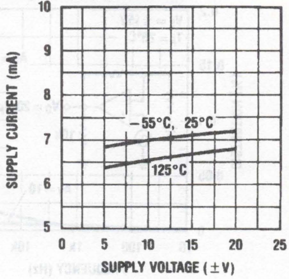
### Input Bias Current



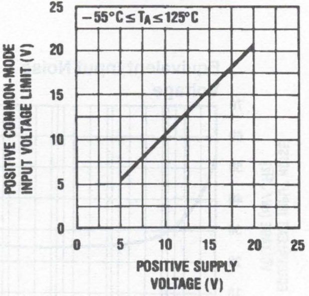
### Input Bias Current



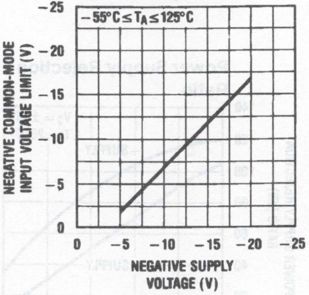
### Supply Current



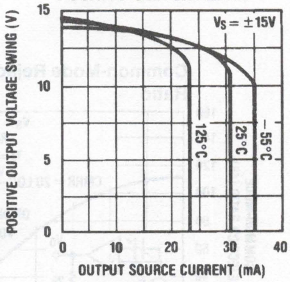
### Positive Common-Mode Input Voltage Limit



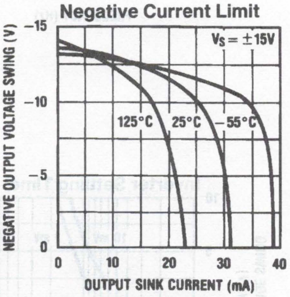
### Negative Common-Mode Input Voltage Limit



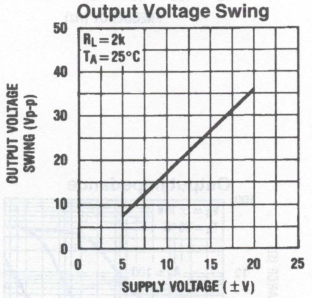
### Positive Current Limit



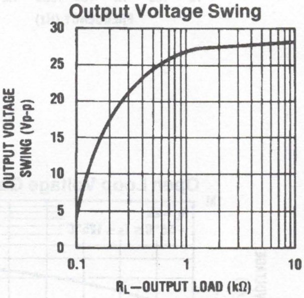
### Negative Current Limit



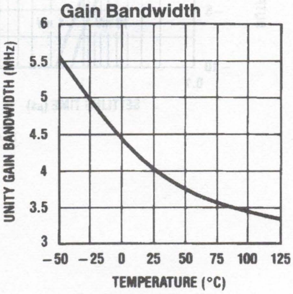
### Output Voltage Swing



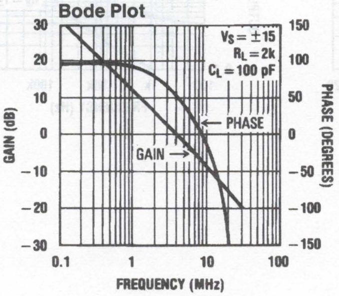
### Output Voltage Swing



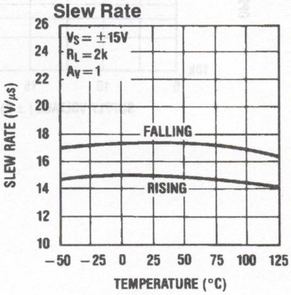
### Gain Bandwidth



### Bode Plot

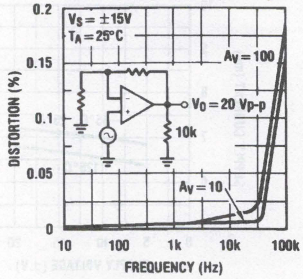


### Slew Rate

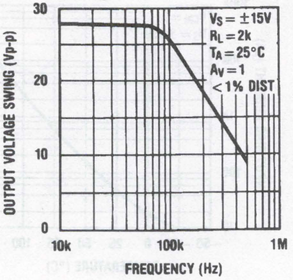


TL/H/5647-2

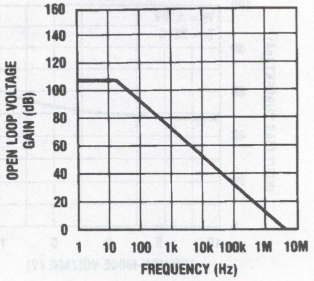
## Typical Performance Characteristics (Continued)



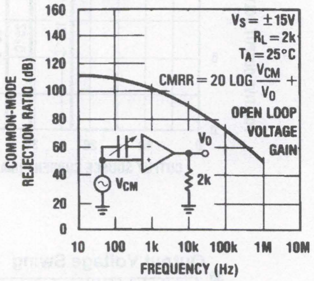
Distortion vs Frequency



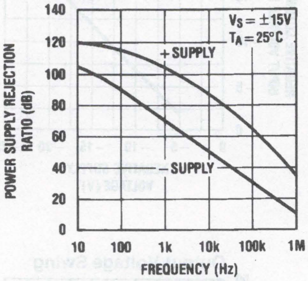
Undistorted Output Voltage Swing



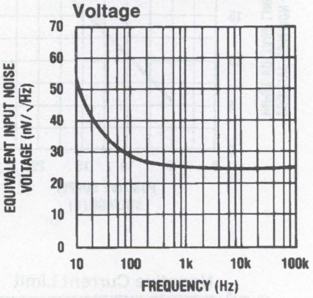
Open Loop Frequency Response



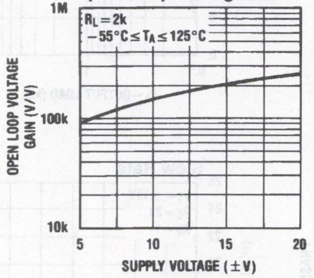
Common-Mode Rejection Ratio



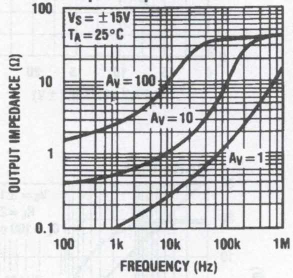
Power Supply Rejection Ratio



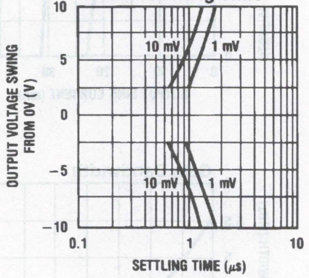
Equivalent Input Noise Voltage



Open Loop Voltage Gain



Output Impedance

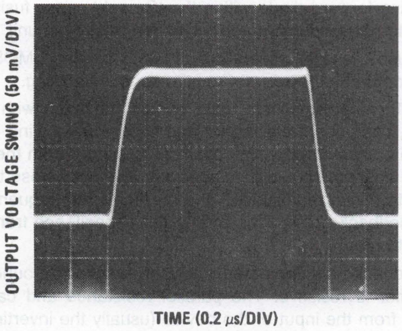


Inverter Settling Time

TL/H/5647–3

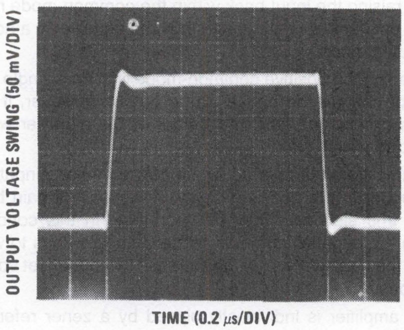
## Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

**Small Signal Inverting**



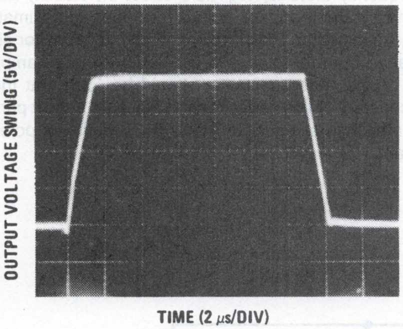
TL/H/5647–4

**Small Signal Non-Inverting**



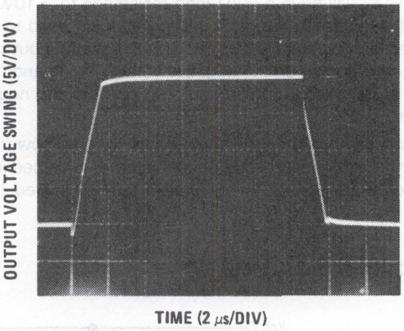
TL/H/5647–5

**Large Signal Inverting**



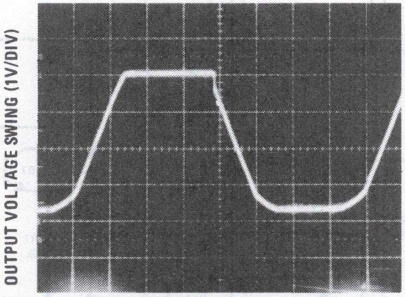
TL/H/5647–6

**Large Signal Non-Inverting**



TL/H/5647–7

**Current Limit ($R_L = 100\Omega$)**



TL/H/5647–8

## Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

## Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

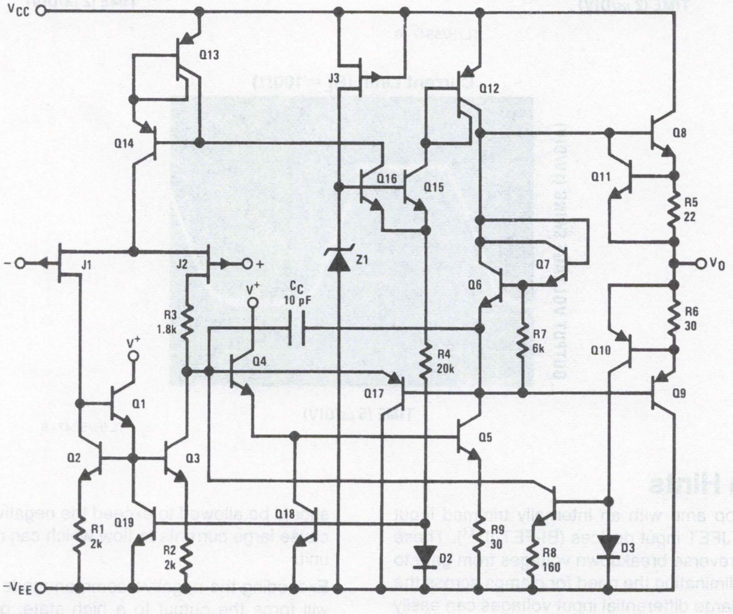
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

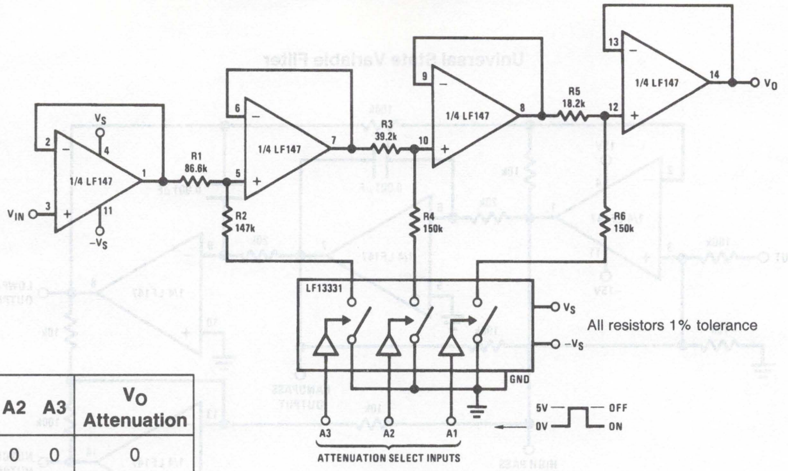
## Detailed Schematic



TL/H/5647–9

## Typical Applications

### Digitally Selectable Precision Attenuator


VS
2
4
1/4 LF147
1
3
11
VIN
−VS
R1
86.6k
6
5
1/4 LF147
7
R2
147k
R3
39.2k
10
9
1/4 LF147
8
R4
150k
R5
18.2k
12
13
1/4 LF147
14
VO
R6
150k
LF13331
VS
−VS
GND
A3
A2
A1
ATTENUATION SELECT INPUTS
5V
0V
OFF
ON

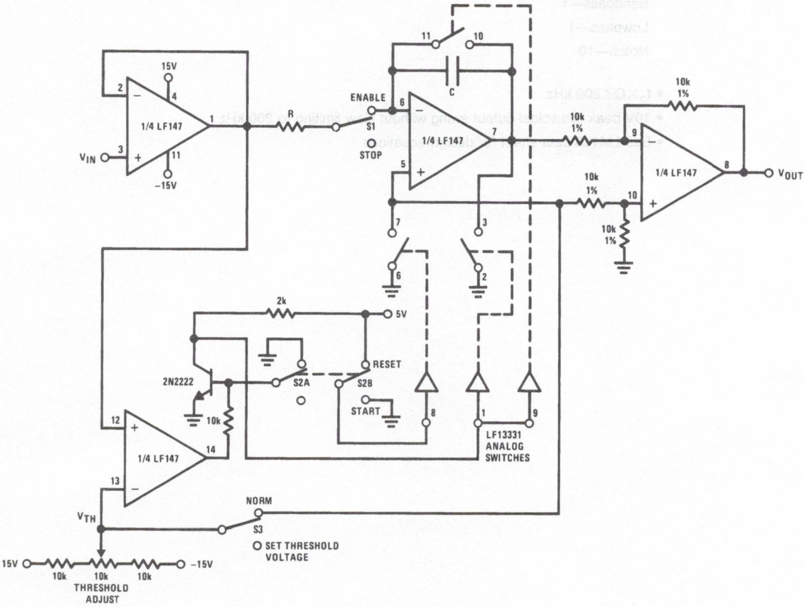
All resistors 1% tolerance

| A1 | A2 | A3 | $V_O$ Attenuation |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | −1 dB |
| 0 | 1 | 0 | −2 dB |
| 0 | 1 | 1 | −3 dB |
| 1 | 0 | 0 | −4 dB |
| 1 | 0 | 1 | −5 dB |
| 1 | 1 | 0 | −6 dB |
| 1 | 1 | 1 | −7 dB |

TL/H/5647-10

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

### Long Time Integrator with Reset, Hold and Starting Threshold Adjustment


15V
2
4
1/4 LF147
1
3
11
VIN
−15V
R
ENABLE
S1
STOP
11
10
C
6
1/4 LF147
7
5
10k
1%
9
1/4 LF147
8
VOUT
10k
1%
10
10k
1%
10k
1%
7
3
6
2
2k
5V
RESET
2N2222
S2A
S2B
START
10k
8
1
9
LF13331
ANALOG
SWITCHES
12
1/4 LF147
14
13
VTH
NORM
S3
SET THRESHOLD
VOLTAGE
15V
10k
10k
10k
−15V
THRESHOLD
ADJUST

TL/H/5647-11

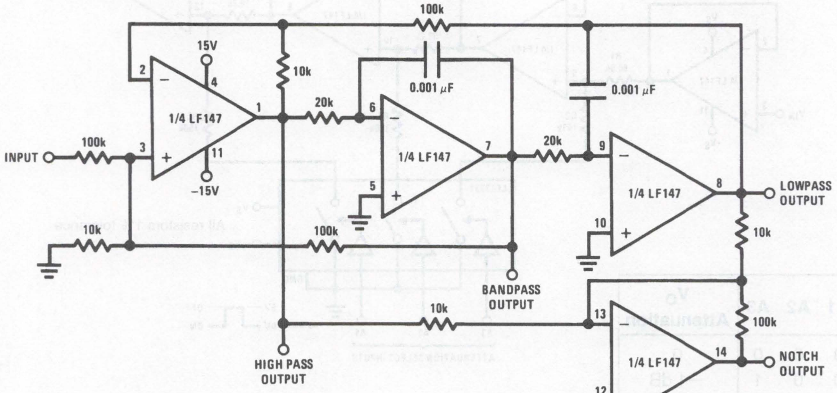
- $V_{OUT}$ starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

## Typical Applications (Continued)

### Universal State Variable Filter


100k
0.001 μF
15V
10k
0.001 μF
2
4
1/4 LF147
1
20k
6
INPUT
100k
3
11
−15V
1/4 LF147
7
20k
9
5
1/4 LF147
8
LOWPASS OUTPUT
10k
100k
10
10k
10k
BANDPASS OUTPUT
10k
13
100k
1/4 LF147
14
NOTCH OUTPUT
12
HIGH PASS OUTPUT

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For circuit shown:

$f_o = 3$ kHz, $f_{NOTCH} = 9.5$ kHz

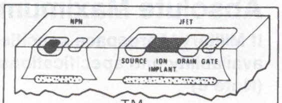
$Q = 3.4$

Passband gain:

- Highpass—0.1
- Bandpass—1
- Lowpass—1
- Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

**National Semiconductor Corporation**



BI-FET II™ Technology

# LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

## LF155, LF155A, LF255, LF355, LF355A, LF355B Low Supply Current
## LF156, LF156A, LF256, LF356, LF356A, LF356B Wide Band
## LF157, LF157A, LF257, LF357, LF357A, LF357B Wide Band Decompensated ($A_{VMIN} = 5$)

## General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

## Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

## Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

## Common Features

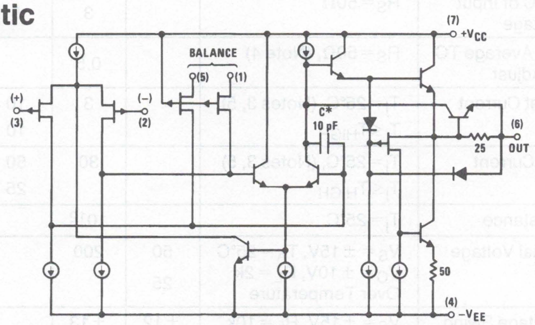
(LF155A, LF156A, LF157A)

| | |
|---|---|
| ■ Low input bias current | 30 pA |
| ■ Low Input Offset Current | 3 pA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low input offset voltage | 1 mV |
| ■ Low input offset voltage temp. drift | 3 μV/°C |
| ■ Low input noise current | 0.01 pA/$\sqrt{\text{Hz}}$ |
| ■ High common-mode rejection ratio | 100 dB |
| ■ Large dc voltage gain | 106 dB |

## Uncommon Features

| | LF155A | LF156A | LF157A ($A_V = 5$) | Units |
|---|---|---|---|---|
| ■ Extremely fast settling time to 0.01% | 4 | 1.5 | 1.5 | μs |
| ■ Fast slew rate | 5 | 12 | 50 | V/μs |
| ■ Wide gain bandwidth | 2.5 | 5 | 20 | MHz |
| ■ Low input noise voltage | 20 | 12 | 12 | nV/$\sqrt{\text{Hz}}$ |

## Simplified Schematic



*3 pF in LF157 series.

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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 8)**

| | LF155A/6A/7A | LF155/6/7 | LF355B/6B/7B<br>LF255/6/7 | LF355/6/7<br>LF355A/6A/7A |
|---|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±22V | ±18V |
| Differential Input Voltage | ±40V | ±40V | ±40V | ±30V |
| Input Voltage Range (Note 2) | ±20V | ±20V | ±20V | ±16V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous | Continuous |
| $T_{jMAX}$ | | | | |
| H-Package | 150°C | 150°C | 115°C | 115°C |
| N-Package | | | 100°C | 100°C |
| J-Package | | 150°C | 115°C | 115°C |
| M-Package | | | 100°C | 100°C |
| Power Dissipation at $T_A$ = 25°C (Notes 1 and 9) | | | | |
| H-Package (Still Air) | 560 mW | 560 mW | 400 mW | 400 mW |
| H-Package (400 LF/Min Air Flow) | 1200 mW | 1200 mW | 1000 mW | 1000 mW |
| N-Package | | | 670 mW | 670 mW |
| J-Package | | 1260 mW | 900 mW | 900 mW |
| M-Package | | | 380 mW | 380 mW |
| Thermal Resistance (Typical) $\theta_{JA}$ | | | | |
| H-Package (Still Air) | 225°C/W | 225°C/W | 225°C/W | 225°C/W |
| H-Package (400 LF/Min Air Flow) | 90°C/W | 90°C/W | 90°C/W | 90°C/W |
| N-Package | | | 130°C/W | 130°C/W |
| J-Package | | 100°C/W | 100°C/W | 100°C/W |
| M-Package | | | 195°C/W | 195°C/W |
| (Typical) $\theta_{JC}$ | | | | |
| H-Package (Still Air) | 23°C/W | 23°C/W | 23°C/W | 23°C/W |
| H-Package (400 LF/Min Air Flow) | 10°C/W | 10°C/W | 10°C/W | 10°C/W |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temp. (Soldering, 10 sec.) Metal Can | 300°C | 300°C | 300°C | 300°C |
| Lead Temp. (Soldering, 10 sec.) Plastic Dip | 260°C | 260°C | 260°C | 260°C |
| Soldering Information | | | | |
| Dual-In-Line Package | | | | |
| Soldering (10 sec.) | 260°C | | | |
| Small Outline Package | | | | |
| Vapor Phase (60 sec.) | 215°C | | | |
| Infrared (15 sec.) | 220°C | | | |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

| Symbol | Parameter | Conditions | LF155A/6A/7A | | | LF355A/6A/7A | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25°C$<br>Over Temperature | | 1 | 2<br>2.5 | | 1 | 2<br>2.3 | mV<br>mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 50\Omega$ | | 3 | 5 | | 3 | 5 | μV/°C |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with $V_{OS}$ Adjust | $R_S = 50\Omega$, (Note 4) | | 0.5 | | | 0.5 | | μV/°C per mV |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3, 5)<br>$T_j \leq T_{HIGH}$ | | 3 | 10<br>10 | | 3 | 10<br>1 | pA<br>nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Notes 3, 5)<br>$T_j \leq T_{HIGH}$ | | 30 | 50<br>25 | | 30 | 50<br>5 | pA<br>nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 2k$<br>Over Temperature | 50<br>25 | 200 | | 50<br>25 | 200 | | V/mV<br>V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$<br>$V_S = \pm 15V$, $R_L = 2k$ | ±12<br>±10 | ±13<br>±12 | | ±12<br>±10 | ±13<br>±12 | | V<br>V |

## DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

| Symbol | Parameter | Conditions | LF155A/6A/7A | | | LF355A/6A/7A | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15.1<br>−12 | | ±11 | +15.1<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | dB |

## AC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

| Symbol | Parameter | Conditions | LF155A/355A | | | LF156A/356A | | | LF157A/357A | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SR | Slew Rate | LF155A/6A; $A_V = 1$,<br>LF157A; $A_V = 5$ | 3 | 5 | | 10 | 12 | | 40 | 50 | | V/μs<br>V/μs |
| GBW | Gain Bandwidth Product | | | 2.5 | | 4 | 4.5 | | 15 | 20 | | MHz |
| $t_s$ | Settling Time to 0.01% | (Note 7) | | 4 | | | 1.5 | | | 1.5 | | μs |
| $e_n$ | Equivalent Input Noise Voltage | $R_S = 100\Omega$<br>f = 100 Hz<br>f = 1000 Hz | | 25<br>25 | | | 15<br>12 | | | 15<br>12 | | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | f = 100 Hz<br>f = 1000 Hz | | 0.01<br>0.01 | | | 0.01<br>0.01 | | | 0.01<br>0.01 | | $pA/\sqrt{Hz}$<br>$pA/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | | | 3 | | | 3 | | | 3 | | pF |

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | LF155/6/7 | | | LF255/6/7 LF355B/6B/7B | | | LF355/6/7 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25°C$<br>Over Temperature | | 3 | 5<br>7 | | 3 | 5<br>6.5 | | 3 | 10<br>13 | mV<br>mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 50\Omega$ | | 5 | | | 5 | | | 5 | | μV/°C |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with $V_{OS}$ Adjust | $R_S = 50\Omega$, (Note 4) | | 0.5 | | | 0.5 | | | 0.5 | | μV/°C per mV |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3, 5)<br>$T_j \le T_{HIGH}$ | | 3 | 20<br>20 | | 3 | 20<br>1 | | 3 | 50<br>2 | pA<br>nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Notes 3, 5)<br>$T_j \le T_{HIGH}$ | | 30 | 100<br>50 | | 30 | 100<br>5 | | 30 | 200<br>8 | pA<br>nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 2k$<br>Over Temperature | 50<br><br>25 | 200 | | 50<br><br>25 | 200 | | 25<br><br>15 | 200 | | V/mV<br><br>V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$<br>$V_S = \pm 15V$, $R_L = 2k$ | ±12<br>±10 | ±13<br>±12 | | ±12<br>±10 | ±13<br>±12 | | ±12<br>±10 | ±13<br>±12 | | V<br>V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15.1<br>−12 | | ±11 | ±15.1<br>−12 | | +10 | +15.1<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |

## DC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

| Parameter | LF155A/155, LF255, LF355A/355B | | LF355 | | LF156A/156, LF256/356B | | LF356A/356 | | LF157A/157 LF257/357B | | LF357A/357 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Supply Current | 2 | 4 | 2 | 4 | 5 | 7 | 5 | 10 | 5 | 7 | 5 | 10 | mA |

## AC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

| Symbol | Parameter | Conditions | LF155/255/ 355/355B | LF156/256, LF356B | LF156/256/ 356/356B | LF157/257, LF357B | LF157/257/ 357/357B | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Typ | Min | Typ | Min | Typ | |
| SR | Slew Rate | LF155/6: $A_V = 1$,<br>LF157: $A_V = 5$ | 5 | 7.5 | 12 | 30 | 50 | V/$\mu$s<br>V/$\mu$s |
| GBW | Gain Bandwidth Product | | 2.5 | | 5 | | 20 | MHz |
| $t_s$ | Settling Time to 0.01% | (Note 7) | 4 | | 1.5 | | 1.5 | $\mu$s |
| $e_n$ | Equivalent Input Noise Voltage | $R_S = 100\Omega$<br>f = 100 Hz<br>f = 1000 Hz | <br>25<br>20 | | <br>15<br>12 | | <br>15<br>12 | <br>nV/$\sqrt{Hz}$<br>nV/$\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Current Noise | f = 100 Hz<br>f = 1000 Hz | 0.01<br>0.01 | | 0.01<br>0.01 | | 0.01<br>0.01 | pA/$\sqrt{Hz}$<br>pA/$\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | | 3 | | 3 | | 3 | pF |

## Notes for Electrical Characteristics

**Note 1:** The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{jMAX}$, $\theta_{jA}$, and the ambient temperature, $T_A$. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C $P_{dMAX}$, whichever is less.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 3:** Unless otherwise stated, these test conditions apply:

| | LF155A/6A/7A LF155//6/7 | LF255//6/7 | LF355A/6A/7A | LF355B/6B/7B | LF355//6/7 |
|---|---|---|---|---|---|
| Supply Voltage, $V_S$ | $\pm 15V \le V_S \le \pm 20V$ | $\pm 15V \le V_S \le \pm 20V$ | $\pm 15V \le V_S \le \pm 18V$ | $\pm 15V \le V_S \pm 20V$ | $V_S = \pm 15V$ |
| $T_A$ | $-55°C \le T_A \le +125°C$ | $-25°C \le T_A \le +85°C$ | $0°C \le T_A \le +70°C$ | $0°C \le T_A \le +70°C$ | $0°C \le T_A \le +70°C$ |
| $T_{HIGH}$ | +125°C | +85°C | +70°C | +70°C | +70°C |

and $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 4:** The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5$\mu$V/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_J$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 6:** Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

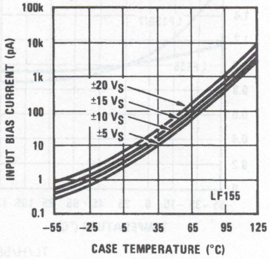
**Note 7:** Settling time is defined here, for a unity gain inverter connection using 2 k$\Omega$ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 k$\Omega$ and the output step is 10V (See Settling Time Test Circuit).

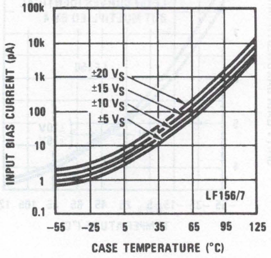
**Note 8:** Refer to RETS155AX for LF155A, RETS155X for LF155, RETSF156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

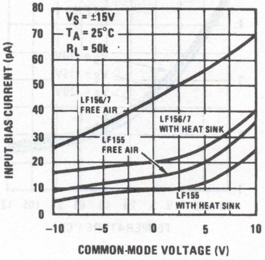
**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

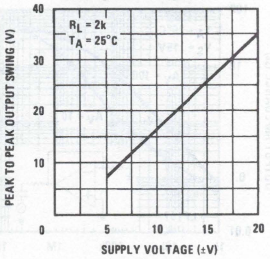
## Typical DC Performance Characteristics

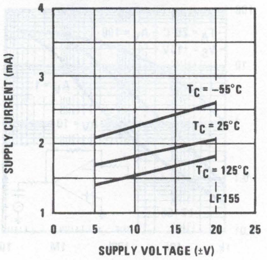
Curves are for LF155, LF156 and LF157 unless otherwise specified.

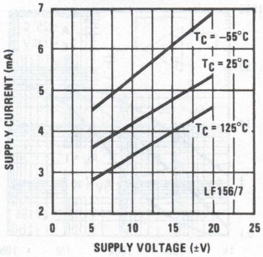

Input Bias Current

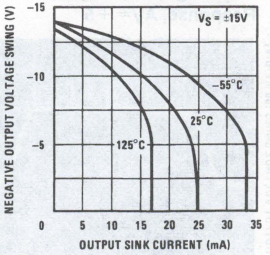

Input Bias Current

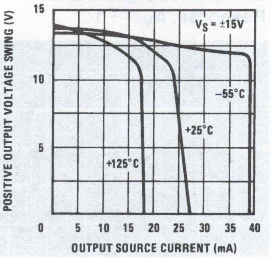

Input Bias Current

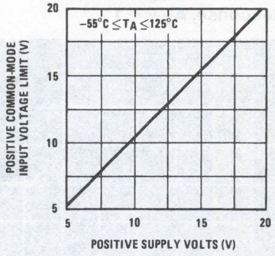

Voltage Swing


Supply Current


Supply Current


Negative Current Limit


Positive Current Limit


Positive Common-Mode Input Voltage Limit

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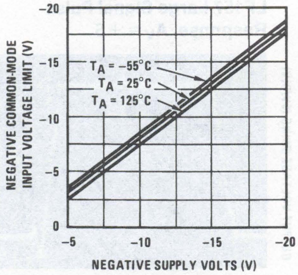
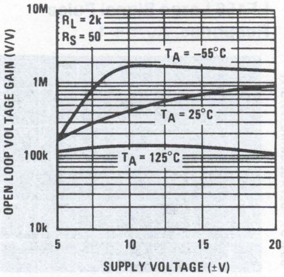
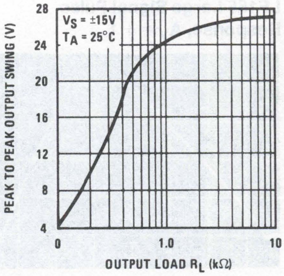

Negative Common-Mode Input Voltage Limit


Open Loop Voltage Gain


Output Voltage Swing

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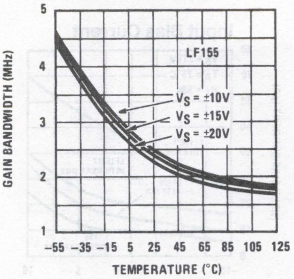
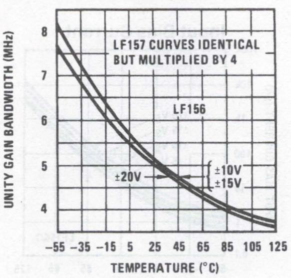
## Typical AC Performance Characteristics

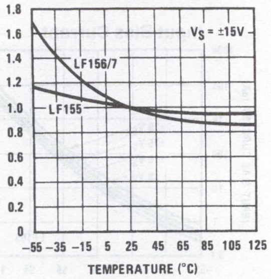
**Gain Bandwidth**



**Gain Bandwidth**



**Normalized Slew Rate**



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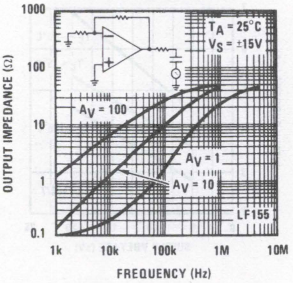
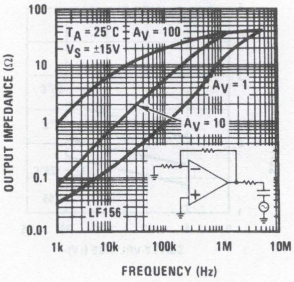
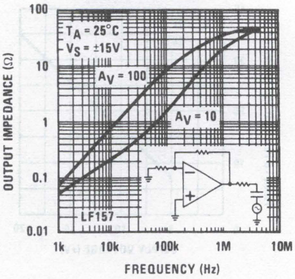
**Output Impedance**



**Output Impedance**



**Output Impedance**



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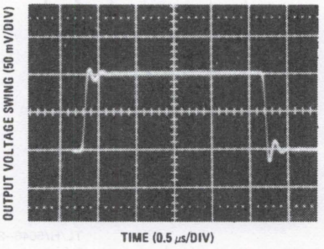
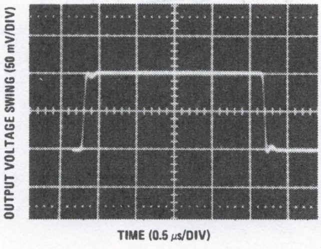
**LF155 Small Signal Pulse Response, $A_V = +1$**



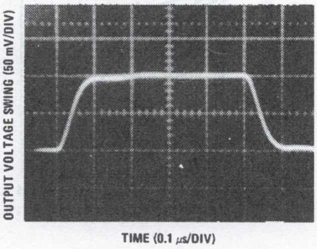
TL/H/5646–5

**LF156 Small Signal Pulse Response, $A_V = +1$**



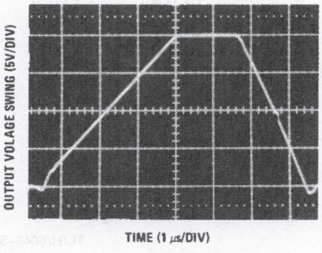
TL/H/5646–6

**Small Signal Pulse Response, $A_V = +5$**



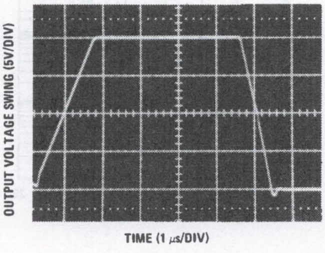
TL/H/5646–7

**LF155 Large Signal Pulse Response, $A_V = +1$**



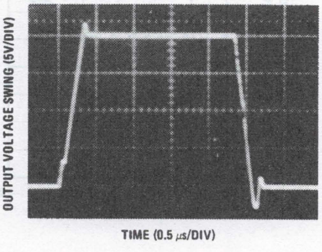
TL/H/5646–8

**LF156 Large Signal Pulse Response, $A_V = +1$**



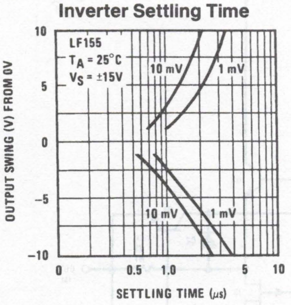
TL/H/5646–9

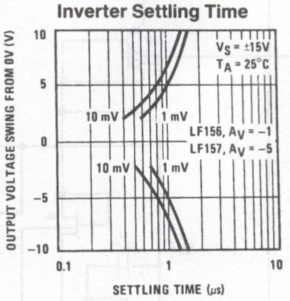
**LF157 Large Signal Pulse Response, $A_V = +5$**

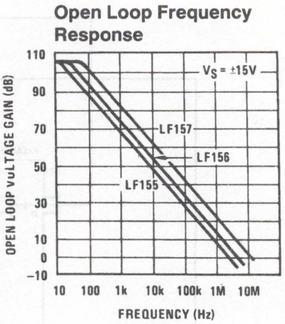


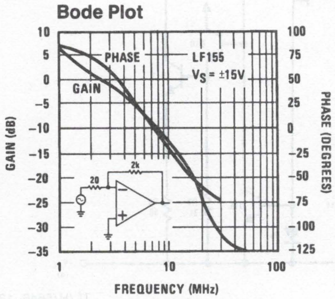
TL/H/5646–10

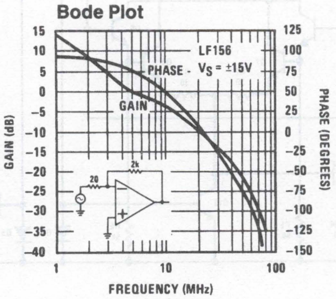
## Typical AC Performance Characteristics (Continued)

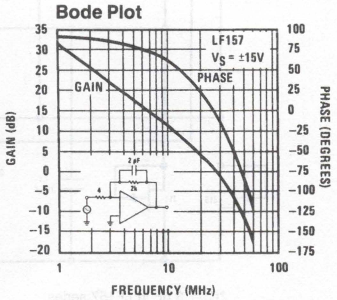

Inverter Settling Time

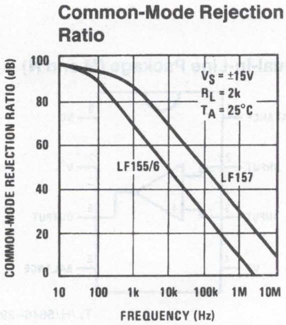

Inverter Settling Time

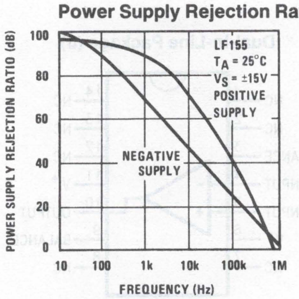

Open Loop Frequency Response

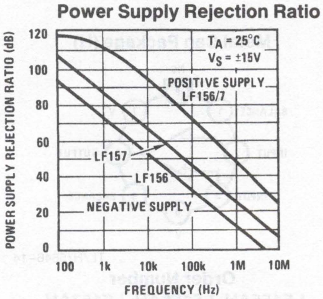

Bode Plot

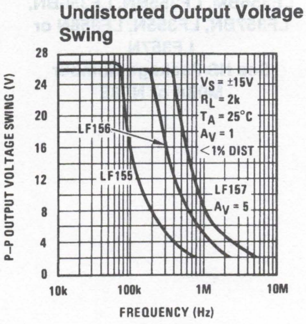

Bode Plot

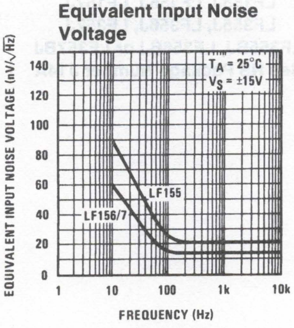

Bode Plot

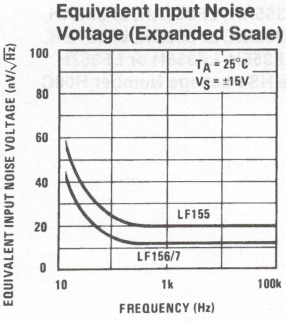

Common-Mode Rejection Ratio


Power Supply Rejection Ratio


Power Supply Rejection Ratio

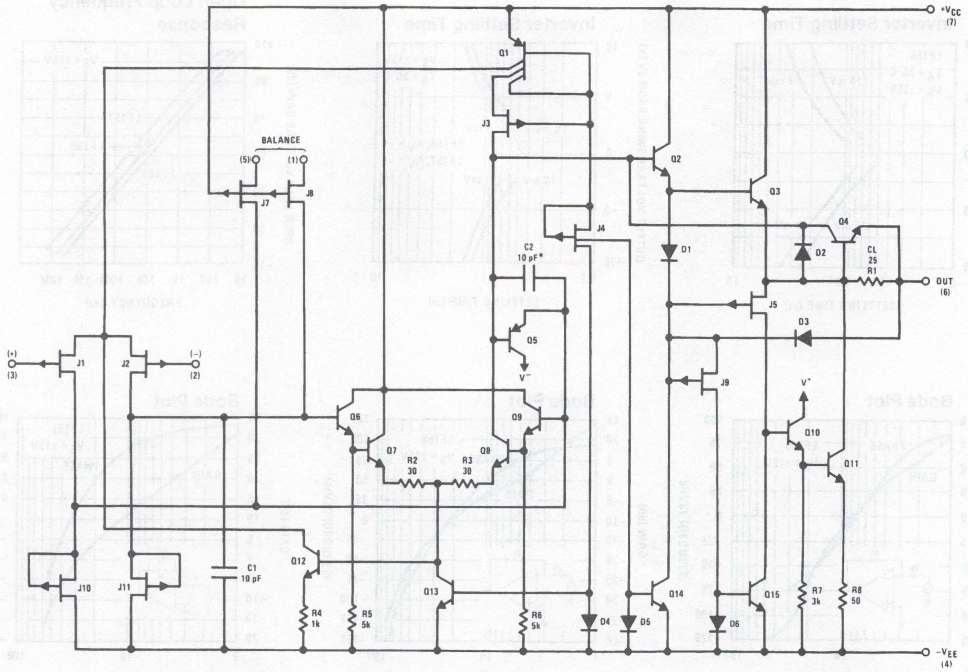

Undistorted Output Voltage Swing


Equivalent Input Noise Voltage


Equivalent Input Noise Voltage (Expanded Scale)

TL/H/5646–11

## Detailed Schematic

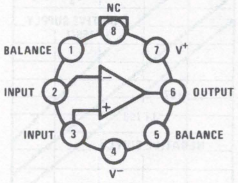

+VCC (7)
Q1
J3
Q2
Q3
Q4
BALANCE
(5)
(1)
J7
J8
J4
C2 10 pF*
D1
D2
CL 25
R1
OUT (6)
J5
D3
Q5
V⁻
(+) (3)
J1
J2
(−) (2)
J9
Q6
Q9
Q7
Q8
R2 30
R3 30
V⁺
Q10
Q11
J10
J11
C1 10 pF
Q12
Q13
R4 1k
R5 5k
R6 5k
D4
D5
Q14
D6
Q15
R7 3k
R8 50
−VEE (4)

*C = 3 pF in LF157 series.

TL/H/5646-13

## Connection Diagrams (Top Views)

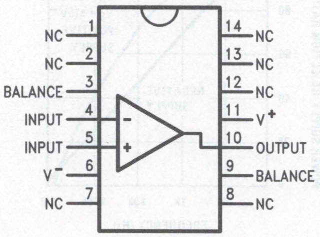
**Metal Can Package (H)**


NC 8
BALANCE 1
7 V⁺
INPUT 2
6 OUTPUT
INPUT 3
5 BALANCE
4
V⁻
−
+

TL/H/5646-14

**Order Number**
**LF155AH, LF156AH, LF157AH, LF155H, LF156H, LF157H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF355BH, LF356BH, LF357BH, LF355H, LF356H or LF357H**
**See NS Package Number H08C**

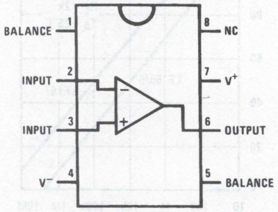
**Dual-In-Line Package (J)**


NC 1
NC 2
BALANCE 3
INPUT 4
INPUT 5
V⁻ 6
NC 7
14 NC
13 NC
12 NC
11 V⁺
10 OUTPUT
9 BALANCE
8 NC
−
+

TL/H/5646-30

**Order Number**
**LF155J, LF156J, LF157J, LF355J, LF356J, LF357J, LF355BJ, LF356BJ or LF357BJ**
**See NS Package Number J14A**

**Dual-In-Line Package (M and N)**


BALANCE 1
INPUT 2
INPUT 3
V⁻ 4
8 NC
7 V⁺
6 OUTPUT
5 BALANCE
−
+

TL/H/5646-29

**Order Number**
**LF355M, LF356M, LF357M, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N**
**See NS Package Number M08A or N08E**

## Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

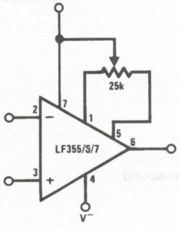
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

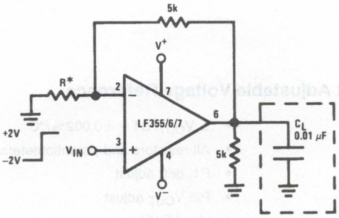
## Typical Circuit Connections

### $V_{OS}$ Adjustment



- $V_{OS}$ is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 $\mu V/°C/mV$ of adjustment
- Typical overall drift: 5 $\mu V/°C \pm (0.5\ \mu V/°C/mV$ of adj.)

### Driving Capacitive Loads



*LF155/6 R = 5k

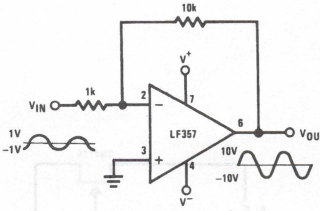
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot ≤ 20%

Settling time ($t_s$) ≅ 5 $\mu s$

### LF157. A Large Power BW Amplifier

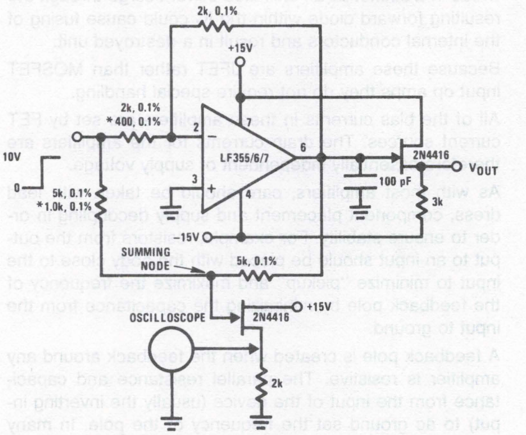


TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p $V_{OUT}$ swing, power bandwidth is: 500 kHz.

## Typical Applications

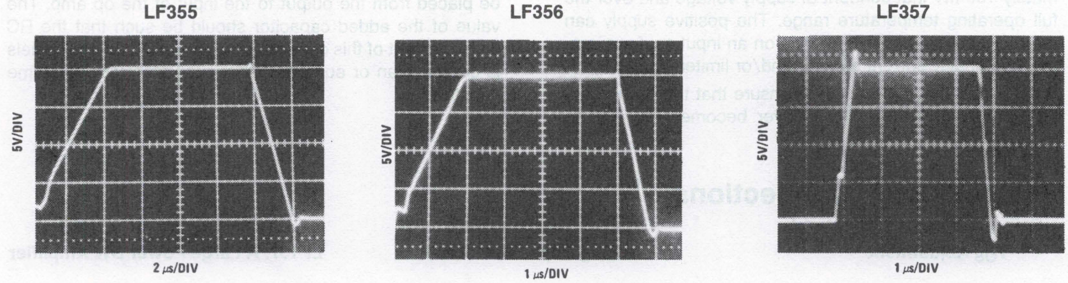
### Settling Time Test Circuit


2k, 0.1%
+15V
2k, 0.1%
*400, 0.1%
2
7
6
LF355/6/7
3
4
10V
0
5k, 0.1%
*1.0k, 0.1%
100 pF
2N4416
VOUT
3k
15V
SUMMING NODE
5k, 0.1%
+15V
OSCILLOSCOPE
2N4416
2k

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

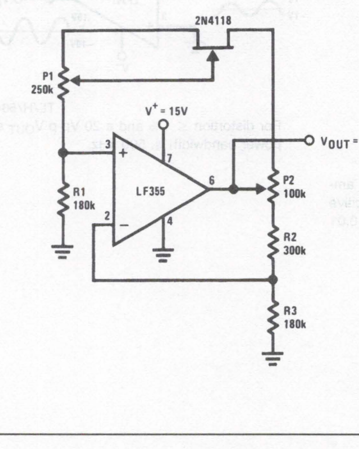
TL/H/5646-16

### Large Signal inverter Output, $V_{OUT}$ (from Settling Time Circuit)



TL/H/5646-17 TL/H/5646-18 TL/H/5646-19

### Low Drift Adjustable Voltage Reference

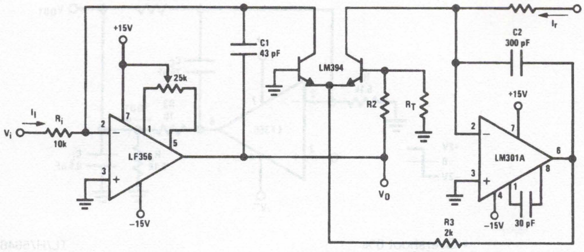

2N4118
P1
250k
V+ = 15V
3
7
6
VOUT = 10V
R1
180k
LF355
2
4
P2
100k
R2
300k
R3
180k

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: $V_{OUT}$ adjust
- Use LF155 for
  - ■ Low $I_B$
  - ■ Low drift
  - ■ Low supply current

TL/H/5646-20

## Typical Applications (Continued)

### Fast Logarithmic Converter

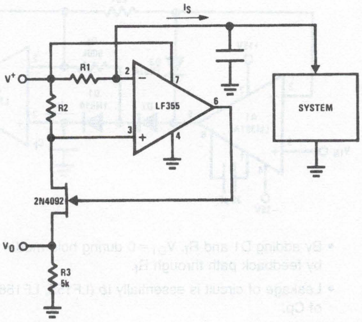

+15V
25k
2
3
7
5
LF356
-15V
Vi
Ii
Ri
10k
C1
43 pF
LM394
R2
RT
VO
Rr
50k
VREF = 5V
Ir
C2
300 pF
+15V
LM301A
2
3
7
6
8
4
1
-15V
30 pF
R3
2k

TL/H/5646-21

- Dynamic range: 100 μA ≤ $I_i$ ≤ 1 mA (5 decades), $|V_O| = 1V/\text{decade}$
- Transient response: 3 μs for $\Delta I_i = 1$ decade
- C1, C2, R2, R3: added dynamic compensation
- $V_{OS}$ adjust the LF156 to minimize quiescent error
- $R_T$: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r}\; R2 = 15.7\text{k},\; R_T = 1\text{k},\; 0.3\%/^\circ\text{C (for temperature compensation)}$$

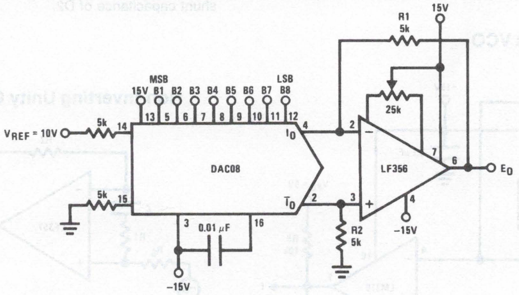
### Precision Current Monitor


IS
V+
R1
R2
2
3
7
6
4
LF355
SYSTEM
2N4092
VO
R3
5k

- $V_O = 5\ R1/R2$ (V/mA of $I_S$)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low $I_B$
  - Low $V_{OS}$
  - Low Supply Current

TL/H/5646-31

### 8-Bit D/A Converter with Symmetrical Offset Binary Operation


MSB
15V
B1
B2
B3
B4
B5
B6
B7
LSB
B8
13
5
6
7
8
9
10
11
12
VREF = 10V
5k
14
5k
15
DAC08
IO
4
ĪO
2
3
0.01 μF
16
-15V
R1
5k
15V
25k
2
3
7
6
4
LF356
R2
5k
-15V
EO

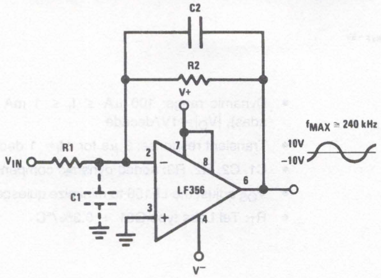
TL/H/5646-32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

| $E_O$ | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | Comments |
|---|---|---|---|---|---|---|---|---|---|
| +9.920 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Positive Full-Scale |
| +0.040 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (+) Zero-Scale |
| −0.040 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (−) Zero-Scale |
| −9.920 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Negative Full-Scale |

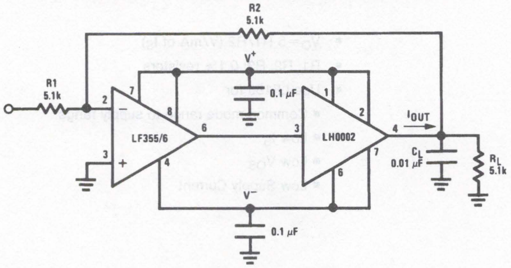
## Typical Applications (Continued)

### Wide BW Low Noise, Low Drift Amplifier


C2
R2
V+
$f_{MAX}$ ≅ 240 kHz
10V
−10V
R1
$V_{IN}$
C1
LF356
2
3
7
8
6
4
V−

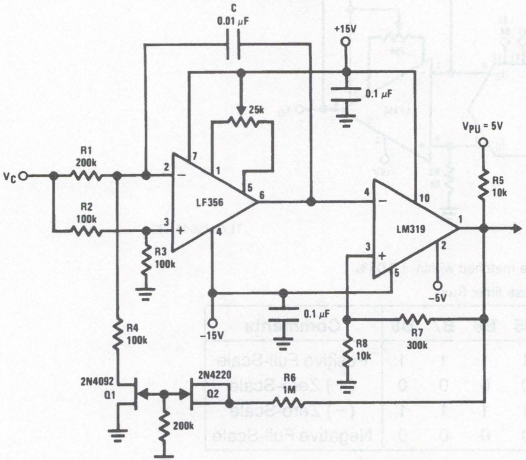
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

### Boosting the LF156 with a Current Amplifier


R2
5.1k
R1
5.1k
V+
0.1 µF
LF355/6
LH0002
$I_{OUT}$
$C_L$
0.01 µF
$R_L$
5.1k
V−
0.1 µF
2
3
7
8
6
4
1
2
3
4
7
6

- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with $C_L$ shown)
- No additional phase shift added by the current amplifier

### 3 Decades VCO

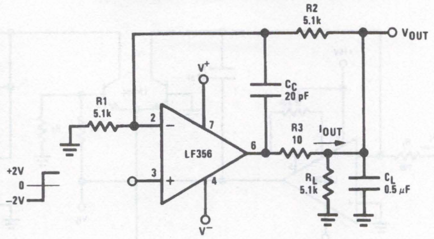

C
0.01 µF
+15V
0.1 µF
25k
$V_{PU}$ = 5V
R5
10k
$V_C$
R1
200k
R2
100k
R3
100k
LF356
LM319
f
−5V
−15V
0.1 µF
R7
300k
R8
10k
R4
100k
2N4092
Q1
2N4220
Q2
R6
1M
200k
2
3
7
1
5
6
4
4
3
10
1
2
5

TL/H/5646-24

$f = \frac{V_C\,(R8+R7)}{(8\,V_{PU}\,R8\,R1)\,C}$, $0 \leq V_C \leq 30V$, $10\text{ Hz} \leq f \leq 10\text{ kHz}$

R1, R4 matched. Linearity 0.1% over 2 decades.

### Isolating Large Capacitive Loads

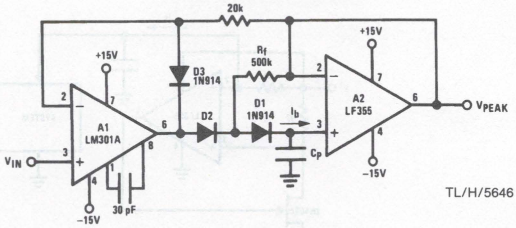

R2
5.1k
$V_{OUT}$
V+
$C_C$
20 pF
R1
5.1k
R3
10
$I_{OUT}$
LF356
+2V
0
−2V
$R_L$
5.1k
$C_L$
0.5 µF
V−
2
3
7
6
4

TL/H/5646-22

- Overshoot 6%
- $t_s$ 10 µs
- When driving large $C_L$, the $V_{OUT}$ slew rate determined by $C_L$ and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\text{ V/}\mu\text{s} = 0.04\text{ V/}\mu\text{s (with } C_L \text{ shown)}$$

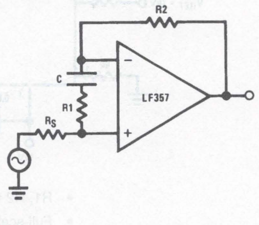
### Low Drift Peak Detector


20k
+15V
+15V
$R_f$
500k
D3
1N914
A1
LM301A
D2
D1
1N914
$I_b$
A2
LF355
$V_{PEAK}$
$V_{IN}$
$C_P$
−15V
−15V
30 pF
2
3
7
6
8
4
1
5
2
3
7
6
4

TL/H/5646

- By adding D1 and $R_f$, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through $R_f$.
- Leakage of circuit is essentially *Ib* (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps $V_{OUT}$ (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $\frac{1}{2}\pi R_f C_{D2}$ where $C_{D2}$ is the shunt capacitance of D2.

### Non-Inverting Unity Gain Operation for LF157


R2
C
R1
$R_S$
LF357

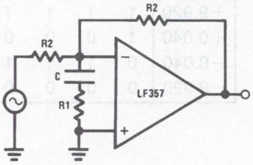
$$R1C \geq \frac{1}{(2\pi)\,(5\text{ MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3\text{ dB}} \approx 5$ MHz

### Inverting Unity Gain for LF157


R2
R2
C
R1
LF357

$$R1C \geq \frac{1}{(2\pi)\,(5\text{ MHz})}$$

$$R1 = \frac{R2}{4}$$

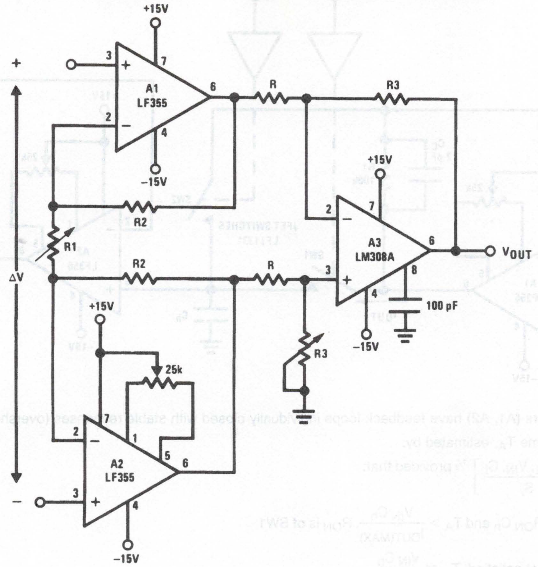
$A_{V(DC)} = -1$

$f_{-3\text{ dB}} \approx 5$ MHz

TL/H/5646-25

## Typical Applications (Continued)

### High Impedance, Low Drift Instrumentation Amplifier

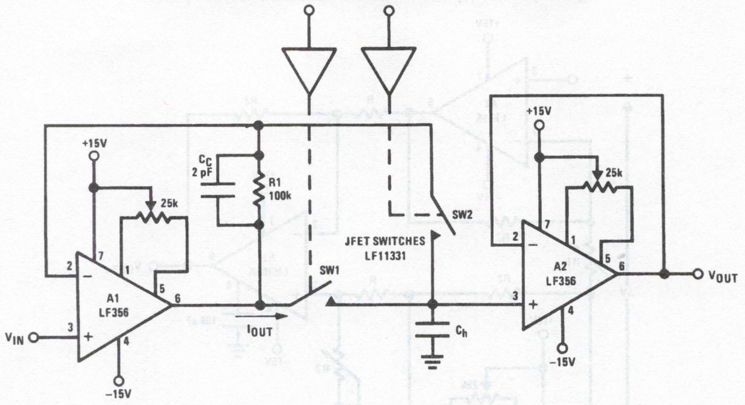

+15V
+
3
+
7
A1
LF355
6
2
−
4
−15V
R
R3
R2
R1
ΔV
R2
R
+15V
2
−
7
A3
LM308A
6
V_OUT
3
+
4
8
100 pF
−15V
R3
+15V
25k
7
2
−
1
5
6
A2
LF355
3
+
4
−15V
−

TL/H/5646–26

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^{-} + 2V \leq V_{IN}$ common-mode $\leq V^{+}$
- System $V_{OS}$ adjusted via A2 $V_{OS}$ adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

## Typical Applications (Continued)

### Fast Sample and Hold


+15V
25k
2
7
1
5
6
3
4
A1
LF356
V_IN
-15V
C_C
2 pF
R1
100k
I_OUT
SW1
SW2
JFET SWITCHES
LF11331
C_h
+15V
25k
7
1
2
5
6
3
4
A2
LF356
-15V
V_OUT

TL/H/5646–33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time $T_A$, estimated by:

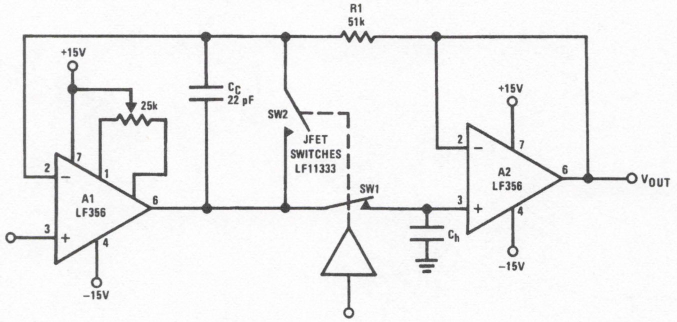
$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right]^{1/2} \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

If inequality not satisfied: $T_A \cong \dfrac{V_{IN} C_h}{20 \text{ mA}}$

- LF156 develops full $S_r$ output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

### High Accuracy Sample and Hold

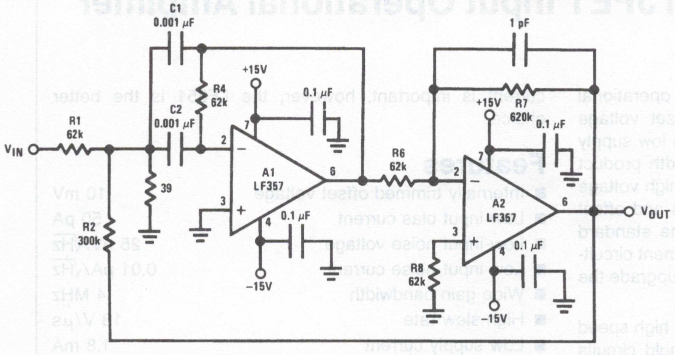

R1
51k
+15V
25k
7
2
1
6
3
4
A1
LF356
-15V
C_C
22 pF
SW2
JFET SWITCHES
LF11333
SW1
C_h
+15V
2
7
6
3
4
A2
LF356
-15V
V_OUT

TL/H/5646–27

- By closing the loop through A2, the $V_{OUT}$ accuracy will be determined uniquely by A1. No $V_{OS}$ adjust required for A2.
- $T_A$ can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, $C_C$: additional compensation
- Use LF156 for
  - Fast settling time
  - Low $V_{OS}$

## Typical Applications (Continued)

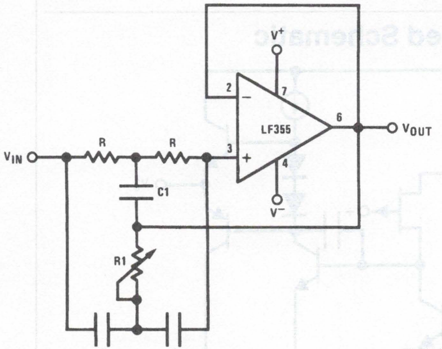
### High Q Band Pass Filter


C1
0.001 μF
R4
62k
C2
0.001 μF
+15V
0.1 μF
R1
62k
V<sub>IN</sub>
39
R2
300k
A1
LF357
7
2
3
4
6
−15V
0.1 μF
1 pF
+15V
R7
620k
0.1 μF
R6
62k
A2
LF357
R8
62k
0.1 μF
−15V
V<sub>OUT</sub>

TL/H/5646-28

- By adding positive feedback (R2) Q increases to 40
- $f_{BP} = 100$ kHz
- $\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

### High Q Notch Filter


V+
7
2
6
LF355
V<sub>OUT</sub>
R
R
V<sub>IN</sub>
3
4
V−
C1
R1
C
C

TL/H/5646-34

- $2R1 = R = 10\ M\Omega$

  $2C = C1 = 300$ pF
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120$ Hz, notch $= -55$ dB, $Q > 100$
- Use LF155 for
  - Low $I_B$
  - Low supply current

National Semiconductor Corporation

# LF351 Wide Bandwidth JFET Input Operational Amplifier

## General Description

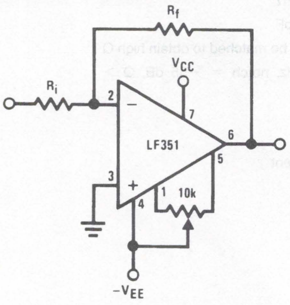
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

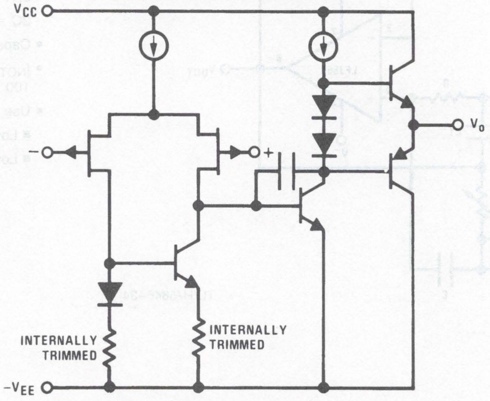
## Features

| | |
|---|---|
| ■ Internally trimmed offset voltage | 10 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise voltage | $25\ nV/\sqrt{Hz}$ |
| ■ Low input noise current | $0.01\ pA/\sqrt{Hz}$ |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/µs |
| ■ Low supply current | 1.8 mA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 µs |

## Typical Connection

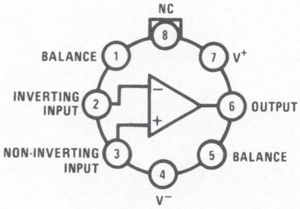

Rf
Ri
VCC
2
−
7
LF351
6
5
3
+
1
10k
4
−VEE

## Simplified Schematic


VCC
−
+
Vo
INTERNALLY TRIMMED
INTERNALLY TRIMMED
−VEE

## Connection Diagrams (Top Views)

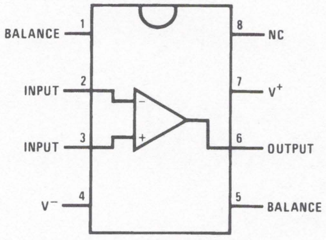
**Metal Can Package**


NC
8
BALANCE
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE
4
V−

Note. Pin 4 connected to case.

**Order Number LF351H**
**See NS Package Number H08C**

**Dual-In-Line Package**


BALANCE
1
8
NC
INPUT
2
7
V+
INPUT
3
6
OUTPUT
V−
4
5
BALANCE

TOP VIEW

**Order Number LF351J,**
**LF351M or LF351N**
**See NS Package Number J08A, M08A or N08E**

TL/H/5648-1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Notes 1 and 6) | 670 mW |
| Operating Temperature Range | 0°C to +70°C |
| $T_{j(MAX)}$ | 115°C |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 2) | ±15V |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 sec.) | |
| Metal Can | 300°C |
| DIP | 260°C |

| | H Package | N Package |
|---|---|---|
| $\theta_{jA}$ | 225°C/W (Still Air)<br>160°C/W<br>(400 LF/min Air Flow) | 120°C/W |
| $\theta_{jC}$ | 25°C/W | |

| | |
|---|---|
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | LF351 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega$, $T_A = 25°C$<br>Over Temperature | | 5 | 10<br>13 | mV<br>mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | 10 | | $\mu$V/°C |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3, 4)<br>$T_j \leq 70°C$ | | 25 | 100<br>4 | pA<br>nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Notes 3, 4)<br>$T_j \leq \pm 70°C$ | | 50 | 200<br>8 | pA<br>nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 2\ k\Omega$<br>Over Temperature | 25<br>15 | 100 | | V/mV<br>V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\ k\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 5) | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | 1.8 | 3.4 | mA |

## AC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | LF351 Min | LF351 Typ | LF351 Max | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ |  | 13 |  | V/$\mu$s |
| GBW | Gain Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ |  | 4 |  | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$,<br>$f = 1000$ Hz |  | 25 |  | nV/$\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_j = 25°C$, $f = 1000$ Hz |  | 0.01 |  | pA/$\sqrt{Hz}$ |

**Note 1:** For operating at elevated temperature, the device must be derated based on the thermal resistance, $\theta_{JA}$.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 3:** These specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le +70°C$. $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM} = 0$.

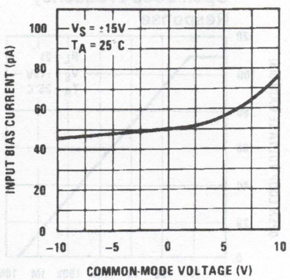
**Note 4:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 5:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

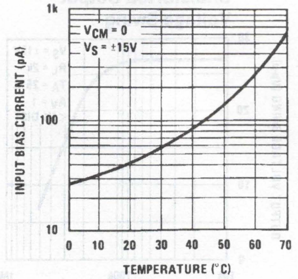
**Note 6:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

## Typical Performance Characteristics

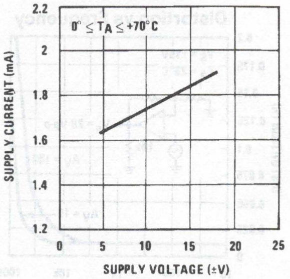
**Input Bias Current**



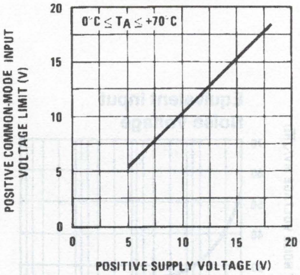
**Input Bias Current**



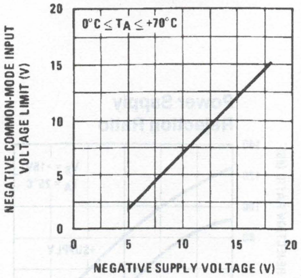
**Supply Current**



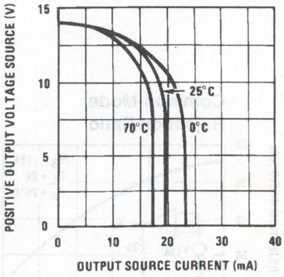
**Positive Common-Mode Input Voltage Limit**



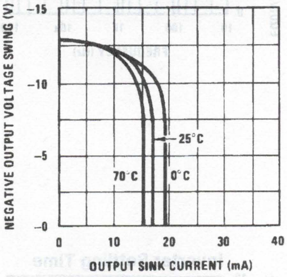
**Negative Common-Mode Input Voltage Limit**



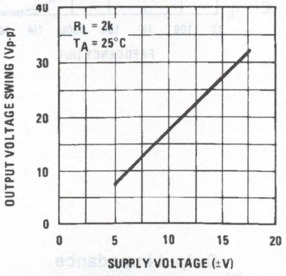
**Positive Current Limit**



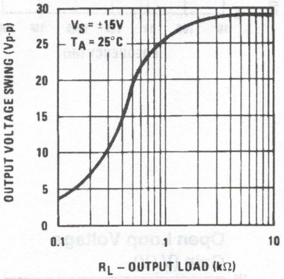
**Negative Current Limit**



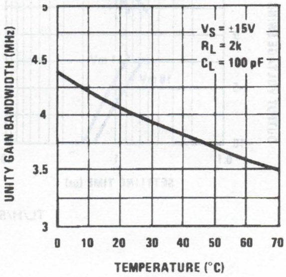
**Voltage Swing**



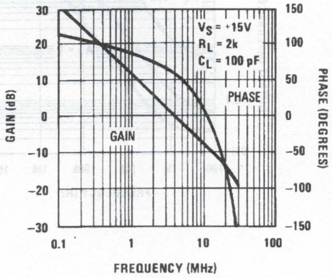
**Output Voltage Swing**



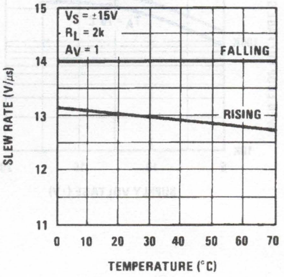
**Gain Bandwidth**



**Bode Plot**

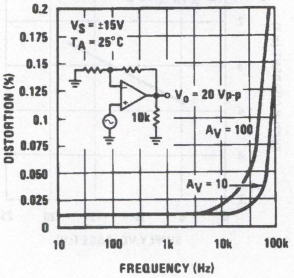


**Slew Rate**

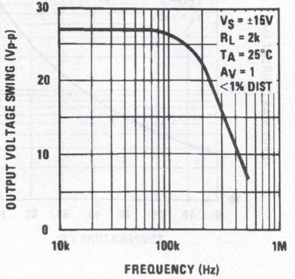


TL/H/5648-2

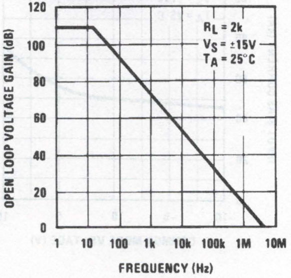
## Typical Performance Characteristics (Continued)



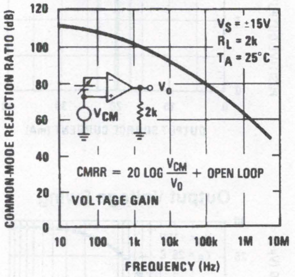
**Distortion vs Frequency**



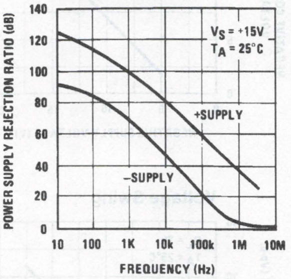
**Undistorted Output Voltage Swing**



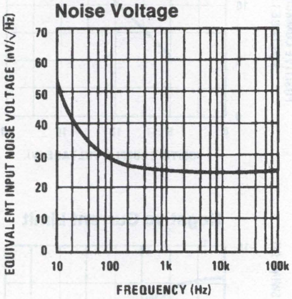
**Open Loop Frequency Response**



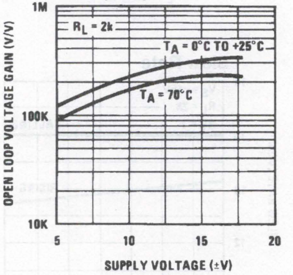
**Common-Mode Rejection Ratio**



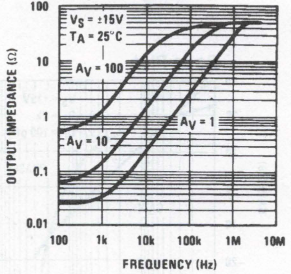
**Power Supply Rejection Ratio**



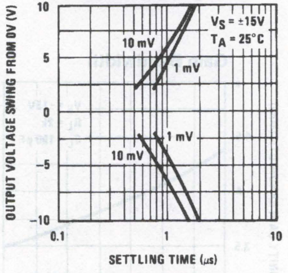
**Equivalent Input Noise Voltage**



**Open Loop Voltage Gain (V/V)**



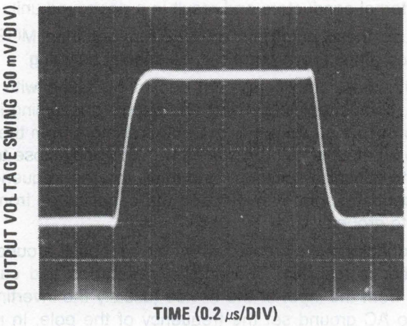
**Output Impedance**



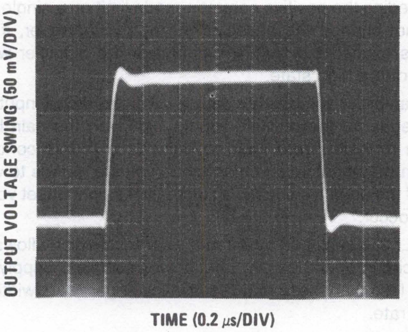
**Inverter Settling Time**

TL/H/5648–3

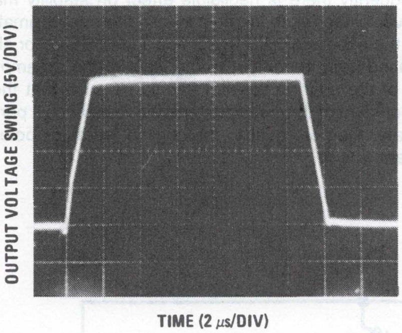
## Pulse Response


Small Signal Inverting

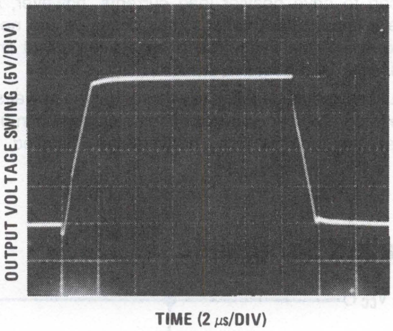
TL/H/5648-4


Small Signal Non-Inverting

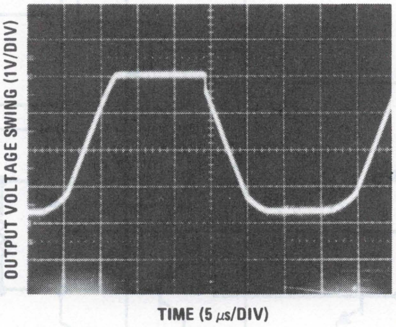
TL/H/5648-5


Large Signal Inverting

TL/H/5648-6


Large Signal Non-Inverting

TL/H/5648-7


Current Limit ($R_L = 100\Omega$)

TL/H/5648-8

## Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

## Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

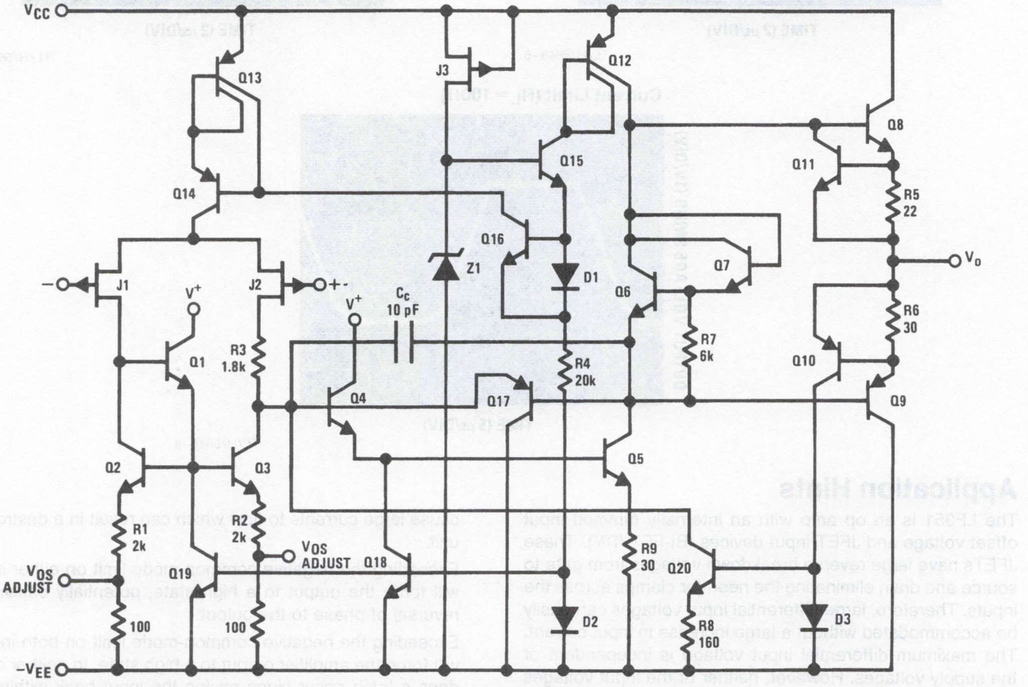
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

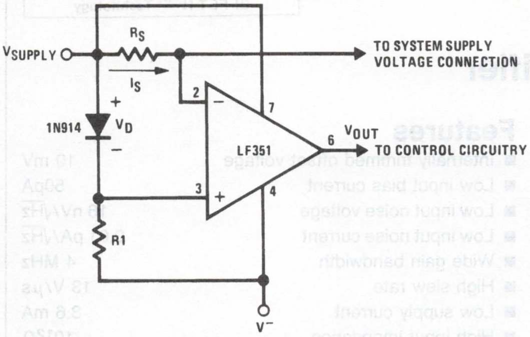
## Detailed Schematic



TL/H/5648-9

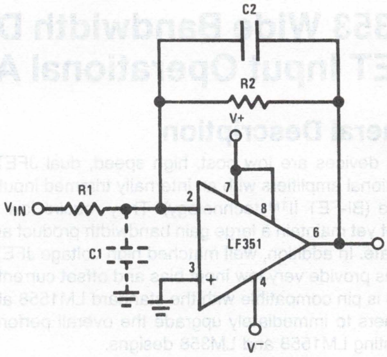
## Typical Applications

### Supply Current Indicator/Limiter


V_SUPPLY
R_S
I_S
TO SYSTEM SUPPLY VOLTAGE CONNECTION
1N914
V_D
+
−
2
3
7
4
6
LF351
V_OUT
TO CONTROL CIRCUITRY
R1
V−

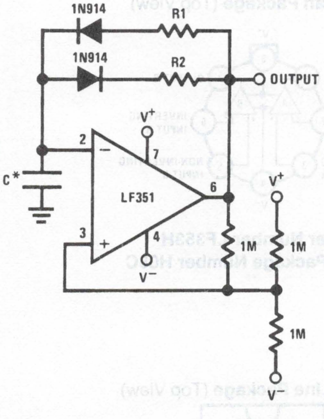
- $V_{OUT}$ switches high when $R_S I_S > V_D$

### Hi-$Z_{IN}$ Inverting Amplifier


C2
R2
V+
R1
V_IN
2
7
8
6
3
4
C1
LF351
V−

Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

### Ultra-Low (or High) Duty Cycle Pulse Generator

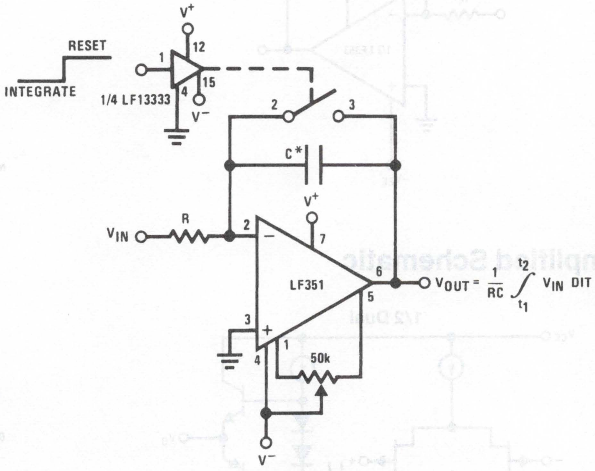

1N914
R1
1N914
R2
OUTPUT
V+
2
7
C*
LF351
6
3
4
V−
V+
1M
1M
1M
V−

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \dfrac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \dfrac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

### Long Time Integrator

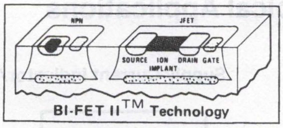

RESET
INTEGRATE
V+
1
12
4
15
1/4 LF13333
V−
2
3
C*
V+
R
V_IN
2
7
LF351
6
5
3
1
4
50k
V−
V_OUT = 1/RC ∫_{t1}^{t2} V_IN DIT

TL/H/5648-10

*Low leakage capacitor

- 50k pot used for less sensitive $V_{OS}$ adjust

**National Semiconductor Corporation**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE

BI-FET II™ Technology

# LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

## General Description

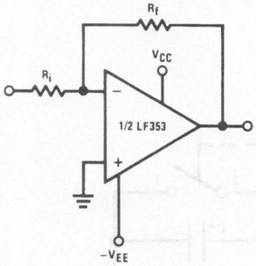
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

## Features

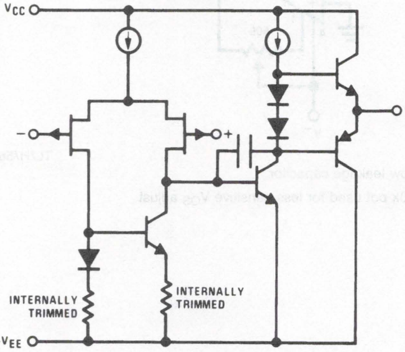
| | |
|---|---|
| ■ Internally trimmed offset voltage | 10 mV |
| ■ Low input bias current | 50pA |
| ■ Low input noise voltage | $16\ nV/\sqrt{Hz}$ |
| ■ Low input noise current | $0.01\ pA/\sqrt{Hz}$ |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/μs |
| ■ Low supply current | 3.6 mA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V=10$, $RL=10k$, $V_O=20Vp-p$, $BW=20\ Hz\text{-}20\ kHz$ | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 μs |

## Typical Connection


Rf
VCC
Ri
1/2 LF353
-VEE

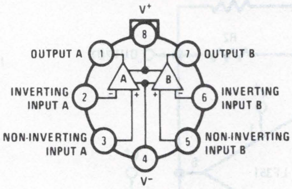
## Simplified Schematic

1/2 Dual


VCC
-
+
VO
INTERNALLY TRIMMED
INTERNALLY TRIMMED
-VEE

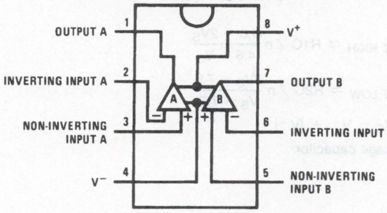
## Connection Diagrams

**Metal Can Package** (Top View)


V+
8
OUTPUT A
1
7
OUTPUT B
INVERTING INPUT A
2
A
B
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V-

**Order Number LF353H**
**See NS Package Number H08C**

**Dual-In-Line Package** (Top View)


OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V-
4
5
NON-INVERTING INPUT B

**Order Number LF353J, LF353M or LF353N**
**See NS Package Number J08A, M08A or N08E**

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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation | (Note 1) |
| Operating Temperature Range | 0°C to +70°C |
| $T_j$(MAX) | 150°C |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 2) | ±15V |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF353 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S=10k\Omega$, $T_A=25°C$<br>Over Temperature | | 5 | 10<br>13 | mV<br>mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S=10\ k\Omega$ | | 10 | | $\mu$V/°C |
| $I_{OS}$ | Input Offset Current | $T_j=25°C$, (Notes 4, 5)<br>$T_j \leq 70°C$ | | 25 | 100<br>4 | pA<br>nA |
| $I_B$ | Input Bias Current | $T_j=25°C$, (Notes 4, 5)<br>$T_j \leq 70°C$ | | 50 | 200<br>8 | pA<br>nA |
| $R_{IN}$ | Input Resistance | $T_j=25°C$ | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S=\pm15V$, $T_A=25°C$<br>$V_O=\pm10V$, $R_L=2\ k\Omega$<br>Over Temperature | 25<br>15 | 100 | | V/mV<br>V/mV |
| $V_O$ | Output Voltage Swing | $V_S=\pm15V$, $R_L=10k\Omega$ | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S=\pm15V$ | ±11 | +15<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10k\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | 3.6 | 6.5 | mA |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF353 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A=25°C$, f=1 Hz−20 kHz (Input Referred) | | −120 | | dB |
| SR | Slew Rate | $V_S=\pm15V$, $T_A=25°C$ | 8.0 | 13 | | V/$\mu$s |
| GBW | Gain Bandwidth Product | $V_S=\pm15V$, $T_A=25°C$ | 2.7 | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A=25°C$, $R_S=100\Omega$, f=1000 Hz | | 25 | | nV/$\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_j=25°C$, f=1000 Hz | | 0.01 | | pA/$\sqrt{Hz}$ |

**Note 1:** For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 195°C/W typ junction to ambient for the H package.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

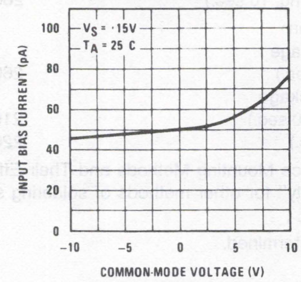
**Note 3:** The power dissipation limit, however, cannot be exceeded.

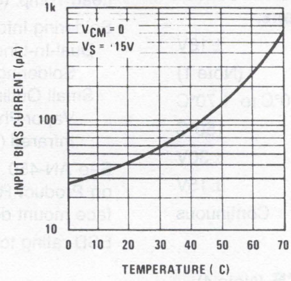
**Note 4:** These specifications apply for $V_S=\pm15V$ and $0°C \leq T_A \leq +70°C$. $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM}=0$.

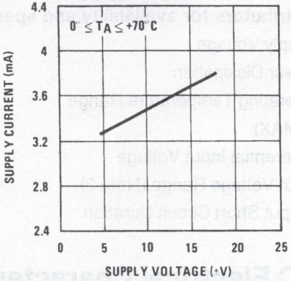
**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j=T_A+\theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

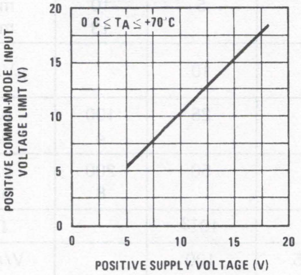
**Note 6:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm6V$ to $\pm15V$.

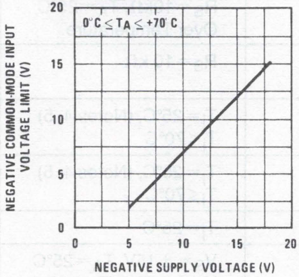
## Typical Performance Characteristics

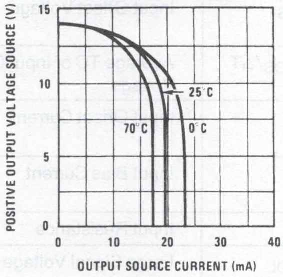

**Input Bias Current**

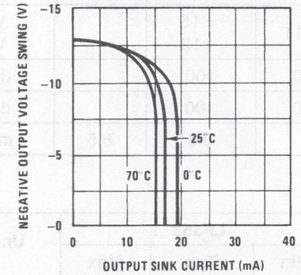

**Input Bias Current**

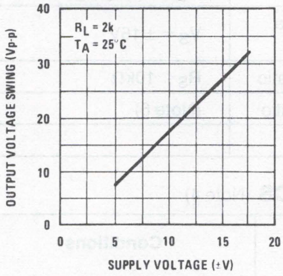

**Supply Current**

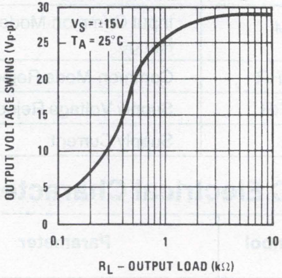

**Positive Common-Mode Input Voltage Limit**

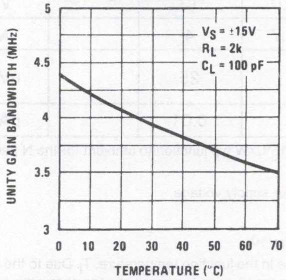

**Negative Common-Mode Input Voltage Limit**

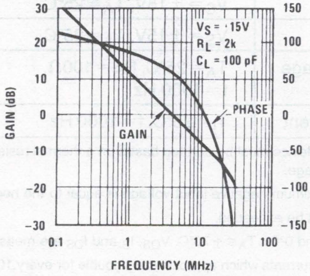

**Positive Current Limit**

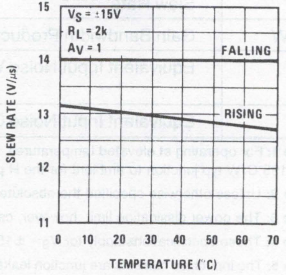

**Negative Current Limit**


**Voltage Swing**


**Output Voltage Swing**


**Gain Bandwidth**


**Bode Plot**


**Slew Rate**

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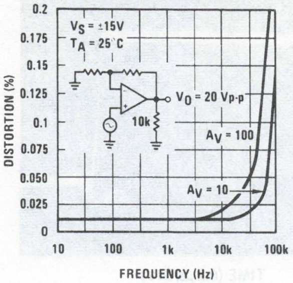
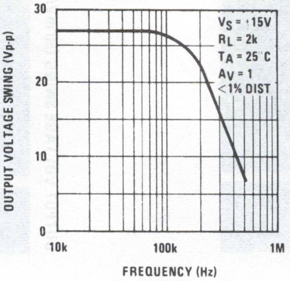
## Typical Performance Characteristics (Continued)

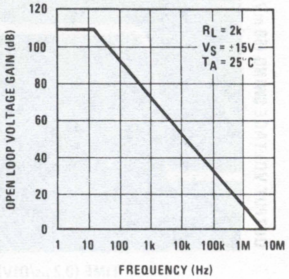
**Distortion vs Frequency**



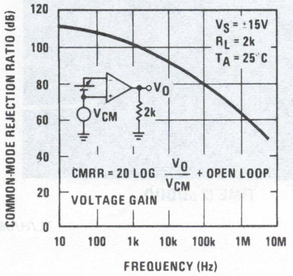
**Undistorted Output Voltage Swing**



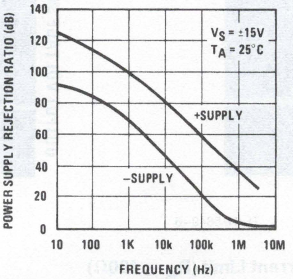
**Open Loop Frequency Response**



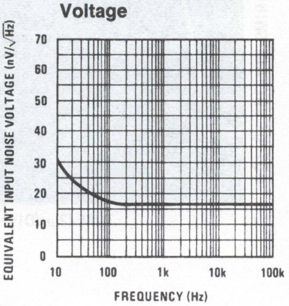
**Common-Mode Rejection Ratio**



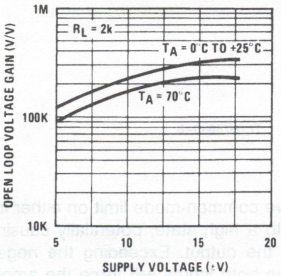
**Power Supply Rejection Ratio**



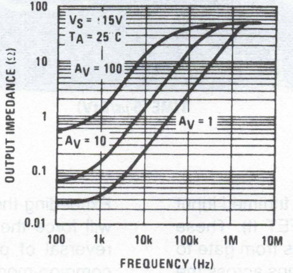
**Equivalent Input Noise Voltage**



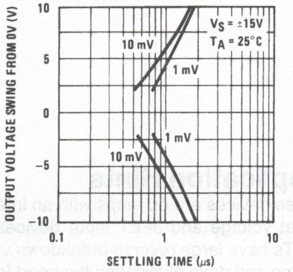
**Open Loop Voltage Gain (V/V)**



**Output Impedance**



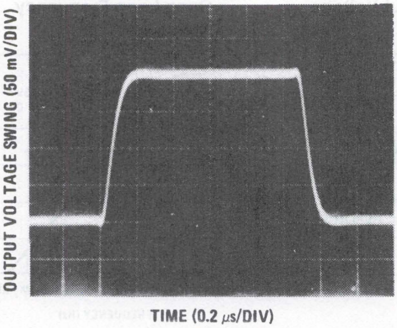
**Inverter Settling Time**



TL/H/5649–3

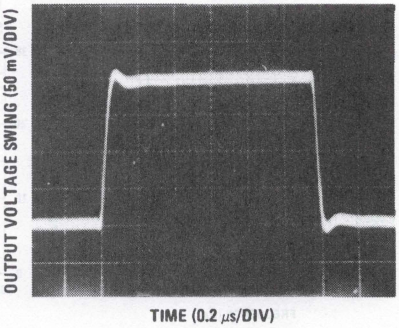
## Pulse Response

**Small Signaling Inverting**



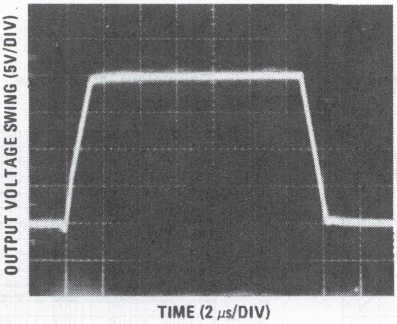
TL/H/5649–4

**Small Signal Non-Inverting**



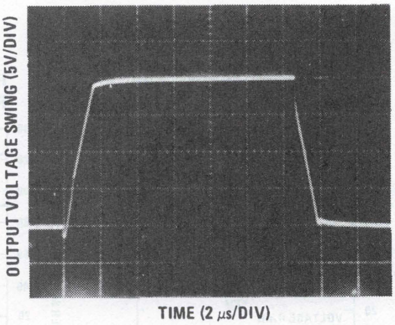
TL/H/5649–5

**Large Signal Inverting**



TL/H/5649–6

**Large Signal Non-Inverting**



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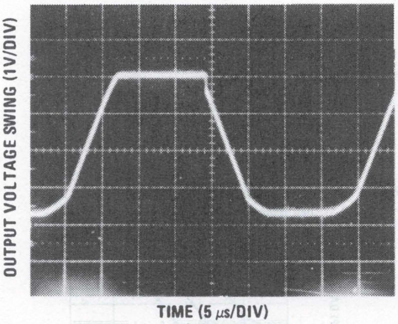
**Current Limit ($R_L = 100\Omega$)**



TL/H/5649–8

## Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

## Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

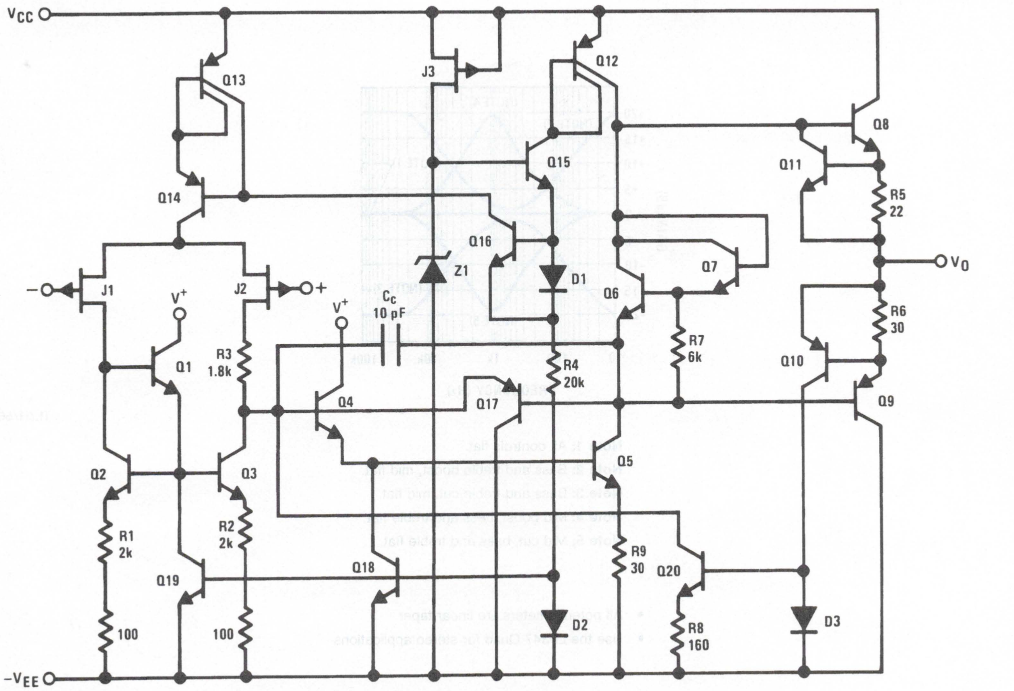
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through theresulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

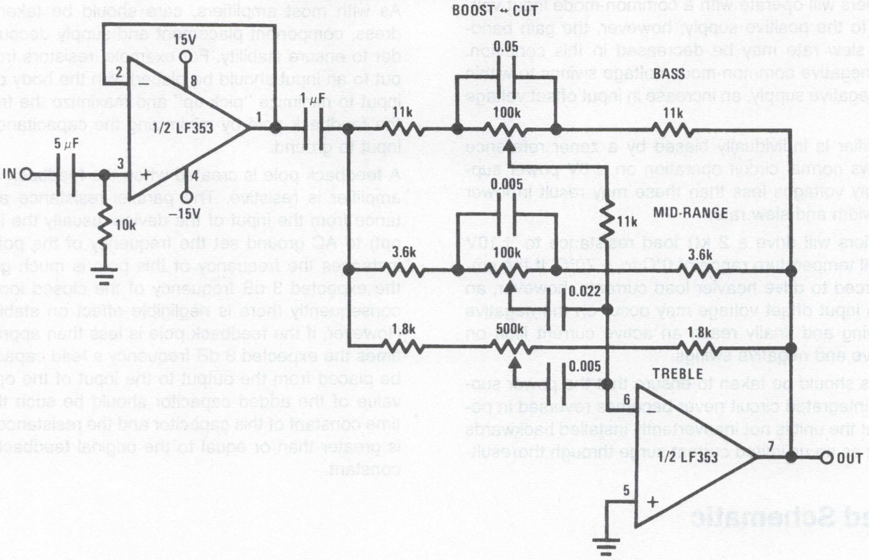
## Detailed Schematic

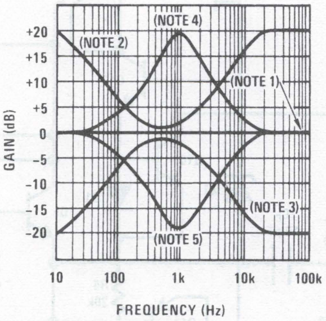


TL/H/5649-9

## Typical Applications

**Three-Band Active Tone Control**


BOOST ↔ CUT
15V
2
−
8
1/2 LF353
1
1 μF
11k
0.05
BASS
100k
11k
5 μF
IN
3
+
4
−15V
10k
0.005
11k
MID-RANGE
3.6k
100k
3.6k
0.022
1.8k
500k
1.8k
0.005
TREBLE
6
−
1/2 LF353
7
OUT
5
+



TL/H/5649–10

**Note 1:** All controls flat.

**Note 2:** Bass and treble boost, mid flat.

**Note 3:** Bass and treble cut, mid flat.

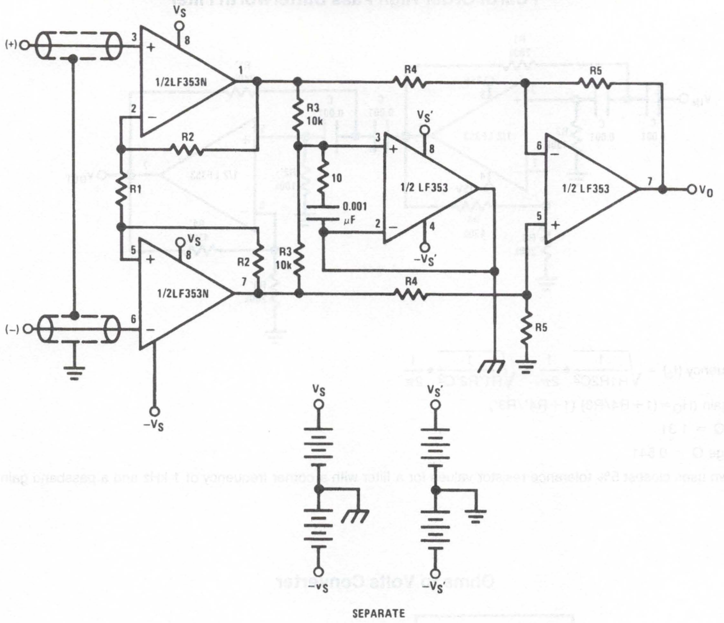
**Note 4:** Mid boost, bass and treble flat.

**Note 5:** Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

## Typical Applications (Continued)

### Improved CMRR Instrumentation Amplifier


VS
(+)
3
8
1/2LF353N
1
2
R2
R1
5
VS
8
R2
7
1/2LF353N
6
(–)
–VS
R3
10k
10
0.001
μF
R3
10k
R4
VS'
3
8
1/2 LF353
2
4
–VS'
R4
R5
6
1/2 LF353
7
VO
5
R5
VS
–vS
VS'
–VS'
SEPARATE

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

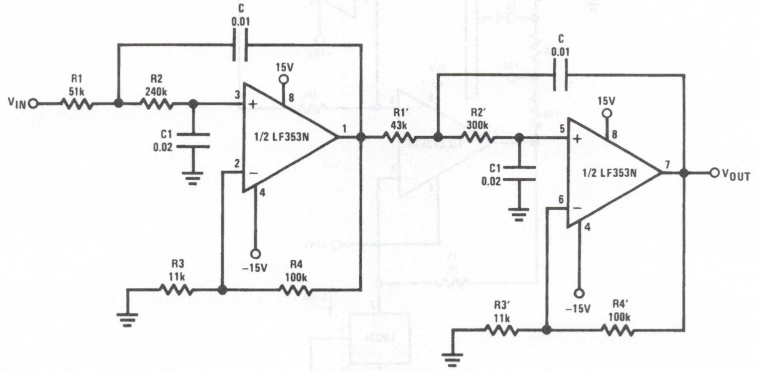
⏊ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With $A_{V_T}$ = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

### Fourth Order Low Pass Butterworth Filter

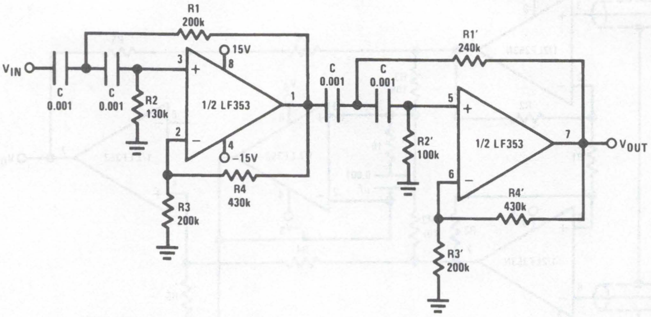

C
0.01
VIN
R1
51k
R2
240k
C1
0.02
15V
3
8
1/2 LF353N
1
2
4
–15V
R3
11k
R4
100k
R1'
43k
R2'
300k
C1
0.02
C
0.01
15V
5
8
1/2 LF353N
7
VOUT
6
4
–15V
R3'
11k
R4'
100k

- Corner frequency ($f_c$) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain ($H_O$) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

TL/H/5649–11

## Typical Applications (Continued)

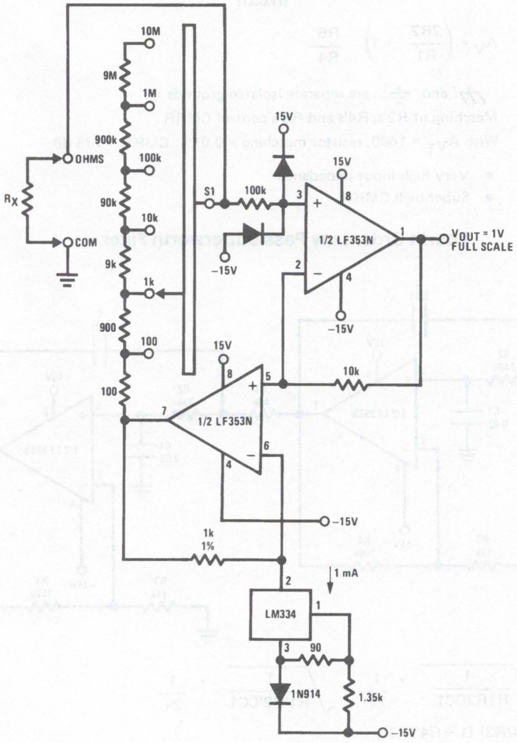
### Fourth Order High Pass Butterworth Filter



R1
200k
15V
8
3
+
V_IN
C
0.001
C
0.001
R2
130k
1/2 LF353
1
2
−
4
−15V
R4
430k
R3
200k
C
0.001
C
0.001
R1'
240k
5
+
R2'
100k
1/2 LF353
7
V_OUT
6
−
R4'
430k
R3'
200k

- Corner frequency ($f_C$) $= \sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain ($H_O = (1 + R4/R3)\ (1 + R4'/R3')$)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

### Ohms to Volts Converter



10M
9M
1M
900k
100k
OHMS
R_X
COM
90k
10k
9k
1k
900
100
100
S1
100k
15V
15V
3
8
+
1/2 LF353N
1
V_OUT = 1V
FULL SCALE
2
−
4
−15V
−15V
15V
8
5
+
10k
7
1/2 LF353N
6
−
4
−15V
1k
1%
1 mA
2
LM334
1
3
90
1N914
1.35k
−15V

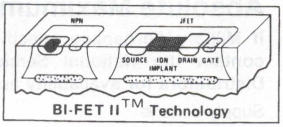
TL/H/5649–13

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where $R_{LADDER}$ is the resistance from switch S1 pole to pin 7 of the LF353.

**National Semiconductor Corporation**

**PRELIMINARY**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# LF400C Fast Settling JFET Input Operational Amplifier

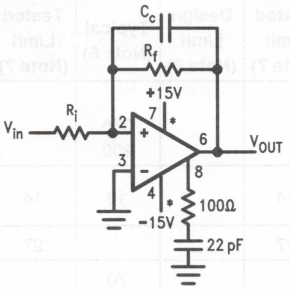
## General Description

The LF400C is a fast settling (under 400 ns to 0.01% for a 10V output step) BI-FET operational amplifier. It also features 16 MHz bandwidth, 70 V/μs inverting slew rate and adjustable short circuit current limit, enabling it to drive 600Ω loads easily.

## Applications

- DAC output amplifiers
- High speed ramp generators
- Fast buffers
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

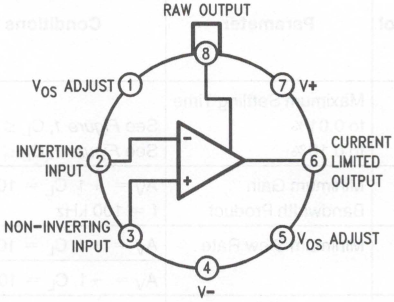
## Typical Connection


C_C
R_f
+15V
7
R_i
V_in
2
+
−
*
6
V_OUT
3
8
4
*
100Ω
−15V
22 pF

TL/H/8393-1

*See *Figure 2* for Power Supply Bypassing.

## Connection Diagram


RAW OUTPUT
8
V_OS ADJUST 1
7 V+
INVERTING INPUT 2
6 CURRENT LIMITED OUTPUT
NON-INVERTING INPUT 3
5 V_OS ADJUST
4
V−

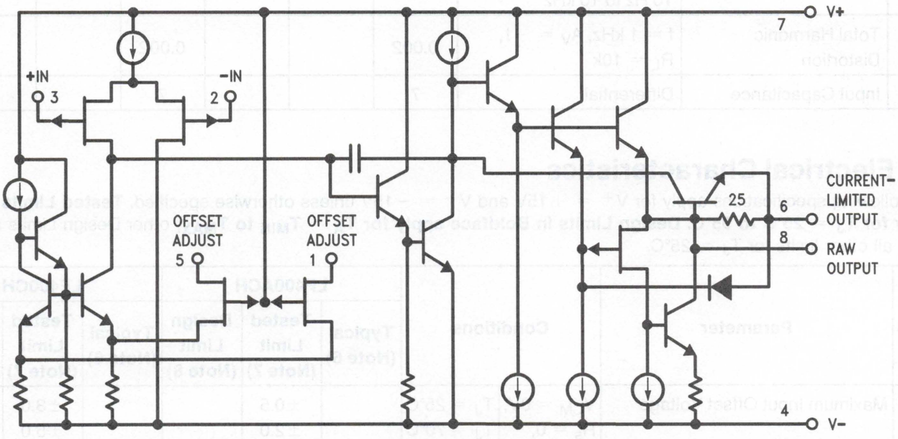
TL/H/8393-2

**Top View**

**Note:** Pin 4 connected to case.

**Order Number LF400ACH, LF400CH**
**See NS Package Number H08A**

## Simplified Schematic


V+
7
+IN
3
−IN
2
OFFSET ADJUST
5
OFFSET ADJUST
1
25
6
CURRENT-LIMITED OUTPUT
8
RAW OUTPUT
4
V−

TL/H/8393-3

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±32V |
| Input Voltage Range (Note 3) | ±16V |
| Output Short Circuit Duration (Pin 6) | CONTINUOUS |
| Power Dissipation (Note 4) H Package | 500 mW |
| Junction Temperature ($T_{JMAX}$) | 115°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| ESD Susceptibility (Note 9) | 800V |

## Operating Ratings (Notes 1 & 2)

| | |
|---|---|
| Temperature Range | $T_{MIN} \leq T_A \leq T_{MAX}$ |
| LF400ACH, LF400CH | $0°C \leq T_A \leq +70°C$ |
| Positive Supply Voltage | +10V to +16V |
| Negative Supply Voltage | −10V to −16V |

## AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for $T_J$ = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to $T_{MAX}$**; other Design Limits are for $T_A$ = 25°C; all other limits for $T_J$ = 25°C.

| Symbol | Parameter | Conditions | LF400ACH | | | LF400CH | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| $t_s$ | Maximum Settling Time<br>to 0.01%<br>to 0.10% | See *Figure 1*, $C_L \leq 50$ pF<br>See *Figure 1*, $C_L \leq 50$ pF | 365<br>200 | | | 365<br>200 | | | ns<br>ns |
| GBW | Minimum Gain Bandwidth Product | $A_V = +1$, $C_L = 10$ pF<br>f = 100 kHz | 16 | 14 | | 16 | 14 | | MHz |
| SR | Minimum Slew Rate | $A_V = +1$, $C_L = 10$ pF | | 27 | | | 27 | | V/μs |
| | | $A_V = -1$, $C_L = 10$ pF | 70 | | | 70 | | | V/μs |
| $\phi$ | Minimum Phase Margin | $A_{vol} = +1$, $C_L = 10$ pF | 60 | | | 60 | | | Degrees |
| $e_n$ | Input Noise Voltage | f = 1 kHz, Rs = 100Ω<br>Broadband, Rs = 100Ω<br>10 Hz to 10 kHz | 23<br>2.3 | | | 23<br>2.3 | | | nV/$\sqrt{Hz}$<br>μV rms |
| $i_n$ | Input Noise Current | f = 1 kHz<br>Broadband<br>10 Hz to 10 kHz | 0.01<br>2.0 | | | 0.01<br>2.0 | | | pA/$\sqrt{Hz}$<br>pA rms |
| THD | Total Harmonic Distortion | f = 1 kHz, $A_V = -1$,<br>$R_L$ = 10k | 0.002 | | | 0.002 | | | % |
| CIN | Input Capacitance | Differential | 7 | | | 7 | | | pF |

## DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for $T_J$ = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to $T_{MAX}$**; other Design Limits are for $T_A$ = 25°C; all other limits for $T_J$ = 25°C.

| Symbol | Parameter | Conditions | | LF400ACH | | | LF400CH | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| $V_{OS}$ | Maximum Input Offset Voltage | $V_{CM}$ = 0V,<br>$R_s$ = 0,<br>$R_L = \infty$ | $T_J$ = 25°C<br>$T_J$ = 70°C | | ±0.5<br>±2.0 | | | ±3.0<br>±5.0 | | mV<br>mV |
| $I_{OS}$ | Maximum Input Offset Current | $V_{CM}$ = 0V, (Note 5) | | | ±100 | ±400<br>±**2.5** | | ±100 | ±400<br>±**2.5** | pA<br>nA |

## DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for $T_J$ = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to $T_{MAX}$;** other Design Limits are for $T_A$ = 25°C; all other limits for $T_J$ = 25°C.

| Symbol | Parameter | | Conditions | LF400ACH | | | LF400CH | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| $I_B$ | Maximum Input Bias Current | | $V_{CM}$ = 0V, (Note 5) | | 200 | | | 200 | | pA |
| | | | | | | **26** | | | **26** | nA |
| $R_{IN}$ | Input Resistance | | $T_j$ = 25°C | $10^{11}$ | | | $10^{11}$ | | | Ω |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | +14/−12 | ±11 | | +14/−12 | ±11 | | V |
| $A_{VOL}$ | Minimum Large Signal Voltage Gain | Using Pin 6 | $V_O = \pm 10V$, $R_L = 2\ K\Omega$ | 300 | 100 | | 300 | 100 | | V/mV |
| | | Using Pin 8 | $V_O = \pm 10V$, $R_L = 600\Omega$ | 300 | 100 | | 300 | 100 | | V/mV |
| $V_O$ | Minimum Output Voltage Swing | Using Pin 6 | $R_L = 2\ K\Omega$ | ±12.5 | ±12 | | ±12.5 | ±12 | | V |
| | | Using Pin 8 | $R_L = 600\Omega$ | ±12 | ±11 | | ±12 | ±11 | | V |
| $I_{SC}$ | Output Short Circuit Current | MIN Using Pin 6 | | | 15 | | | 15 | | mA |
| | | MAX Using Pin 6 | | | 45 | | | 45 | | mA |
| | | MIN Using Pin 8 | Pulse Test | | 100 | | | 100 | | mA |
| $R_O$ | Output Resistance | Using Pin 6 | Open Loop, DC | 75 | | | 75 | | | Ω |
| | | Using Pin 8 | Open Loop, DC | 50 | | | 50 | | | Ω |
| CMRR | Minimum DC Common Mode Rejection Ratio | | $-11V \le V_{IN} \le +11V$ | 100 | 90 | | 100 | 80 | | dB |
| PSRR | Minimum DC Power Supply Rejection Ratio | | $+10V \le V^+ < +15V$,<br>$-15V \le V^- < -10V$,<br>$V_{CM} = 0V$ | 100 | 90 | | 100 | 80 | | dB |
| $I_S$ | Maximum Supply Current | | $V_O = 0V$, $R_L = \infty$ | 9 | 12 | | 9 | 12 | | mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are with respect to ground.

**Note 3:** Unless otherwise specified, the Absolute Maximum Negative Input Voltage is equal to the negative power supply voltage.

**Note 4:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\Theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T)/\Theta_{JA}$ or 500 mW, whichever is less. $\Theta_{JA}$ for the LF400H is typically 150°C/W.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature $T_J$. Due to limited production test time, input bias currents are measured at $T_J$=25°C. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation $P_D$. Use of a heat sink is recommended when input bias current must be minimized.

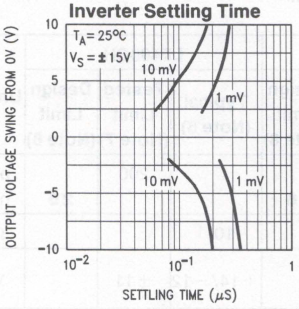
**Note 6:** Typicals represent the most likely parametric norm.

**Note 7:** Guaranteed to National's AOQL (Average Outgoing Quality Level).

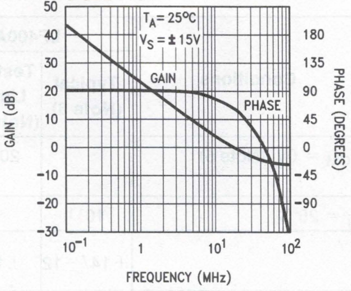
**Note 8:** Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

**Note 9:** Human body model, 100 pF discharged through a 1500Ω resistor.

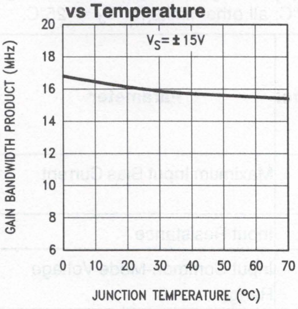
# Typical Performance Characteristics



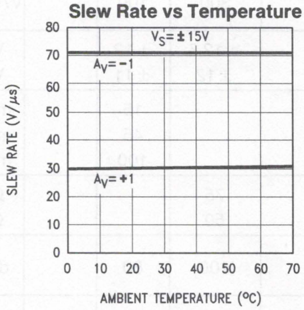
**Inverter Settling Time**



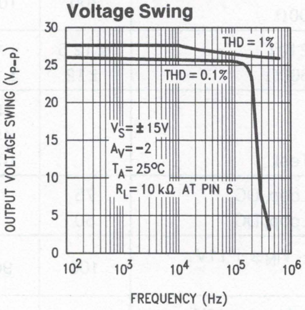
**Bode Plot**



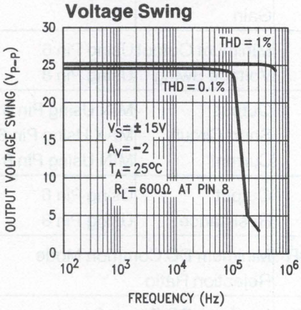
**Gain Bandwidth vs Temperature**



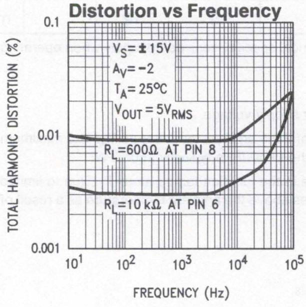
**Slew Rate vs Temperature**



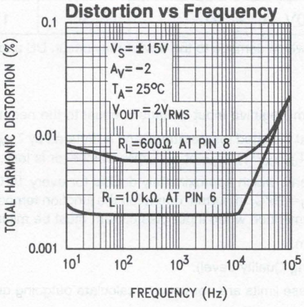
**Undistorted Output Voltage Swing**



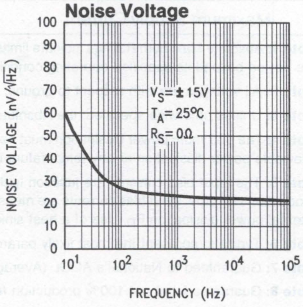
**Undistorted Output Voltage Swing**



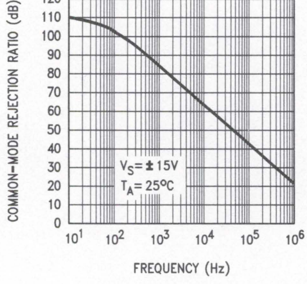
**Distortion vs Frequency**



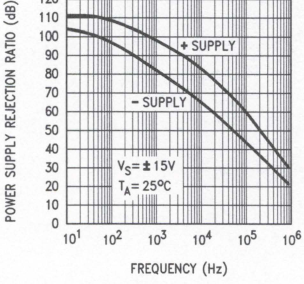
**Distortion vs Frequency**



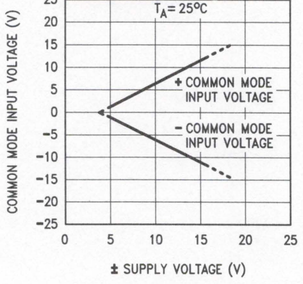
**Equivalent Input Noise Voltage**



**AC Common-Mode Rejection**



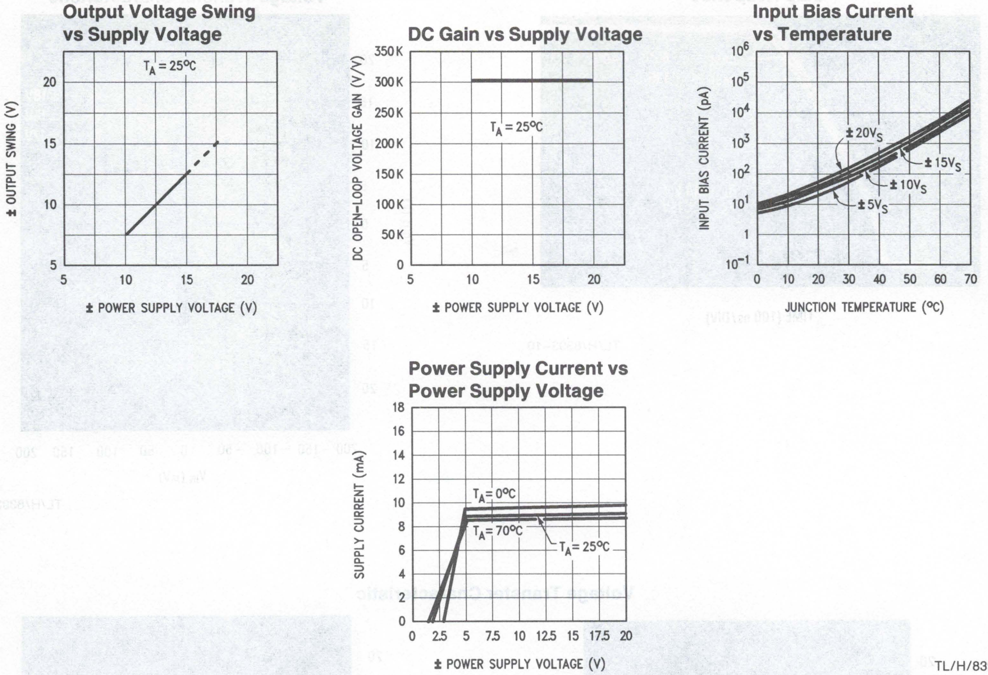
**AC Power Supply Rejection**



**Common-Mode Input Voltage Range**

TL/H/8393-4

## Typical Performance Characteristics (Continued)



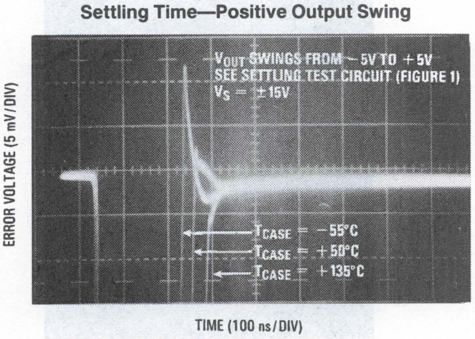
Output Voltage Swing vs Supply Voltage

DC Gain vs Supply Voltage

Input Bias Current vs Temperature

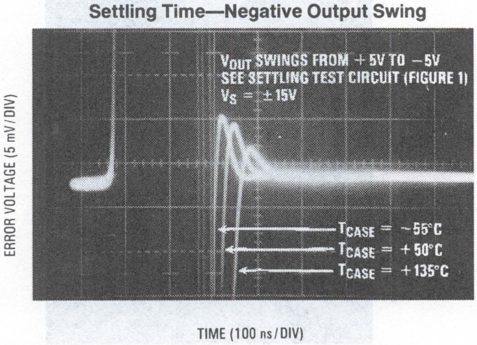
Power Supply Current vs Power Supply Voltage

TL/H/8393-5



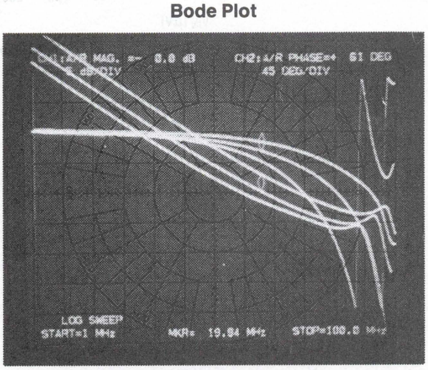
Settling Time—Positive Output Swing

TL/H/8393-6



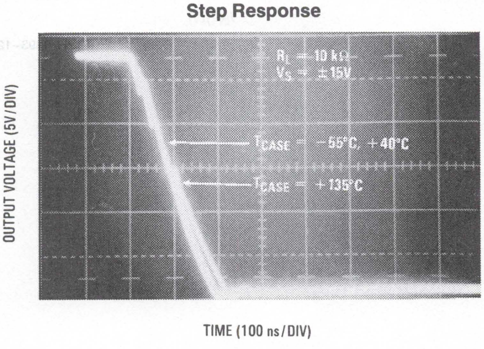
Settling Time—Negative Output Swing

TL/H/8393-7



Bode Plot

TL/H/8393-8

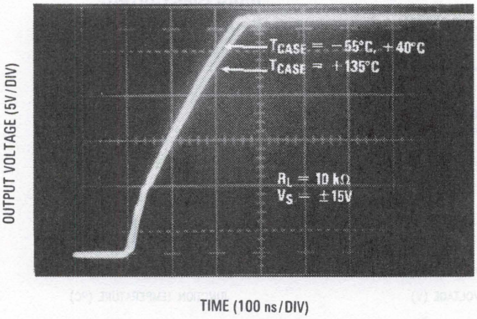


Step Response

TL/H/8393-9

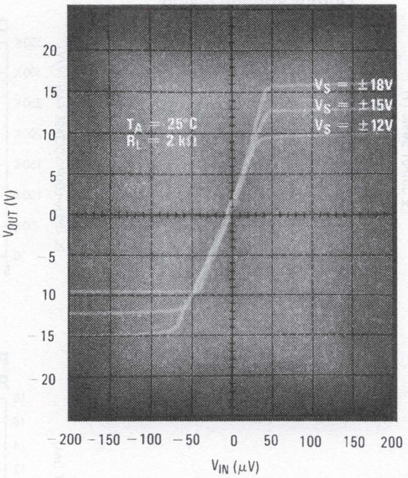
## Typical Performance Characteristics (Continued)

**Step Response**



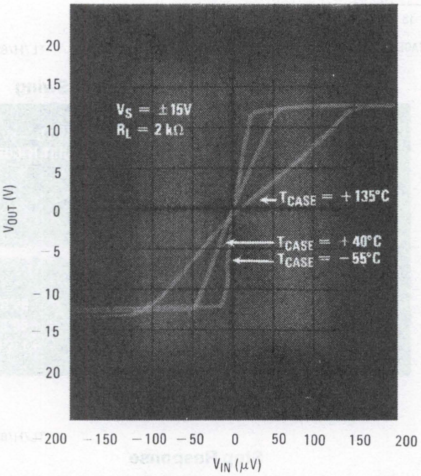
TL/H/8393–10

**Voltage Transfer Characteristic**

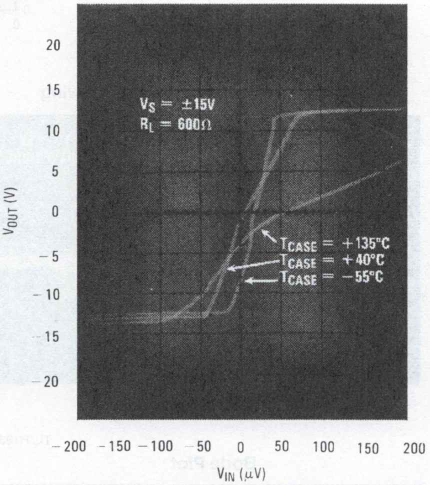


TL/H/8393–11

**Voltage Transfer Characteristic**



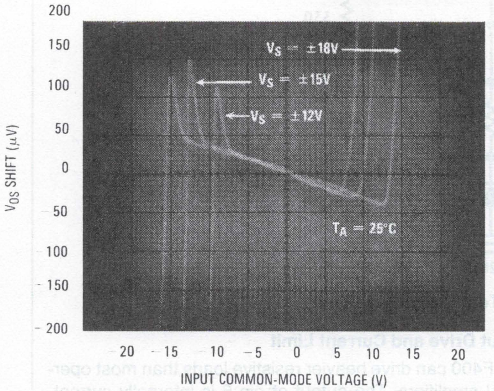
TL/H/8393–12



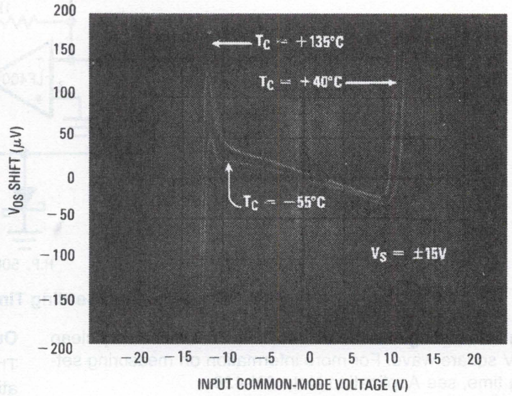
TL/H/8393–13

## Typical Performance Characteristics (Continued)

**Common—Mode Voltage Transfer Characteristic**



TL/H/8393–14



TL/H/8393–15

## Application Hints

The LF400 is a high-speed, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the common-mode input range will not damage the device as long as the Absolute Maximum Ratings are not violated, but it will result in a high output voltage. Latching will not occur, however, and when the offending signal is removed the LF400 will recover quickly.

The nominal power supply voltage is ±15V, but the LF400 will operate satisfactorily from ±10V to ±16V. The LF400 is functional down to ±5V, but performance will be degraded. (See Typical Performance curves.)

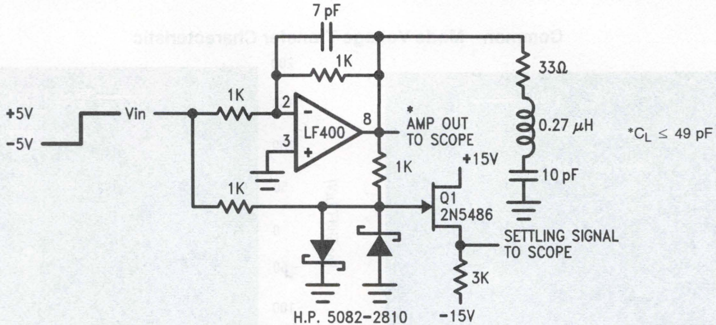
### Settling Time Considerations

The settling performance of any high-speed operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor $C_C$ between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF400 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF400's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time—Positive Output Swing" and "Settling Time—Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than ½ mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF400's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for set-

## Application Hints (Continued)



TL/H/8393-16

**FIGURE 1. Simplified Settling Time Test Circuit (see Text)**

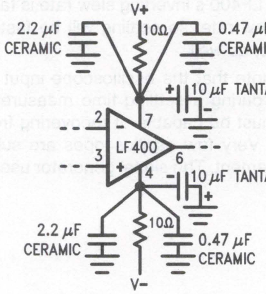
tling time testing must be able to drive $50\Omega$ with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

### Output Compensation

When operating at very low temperatures, a compensation network should be added to the LF400's output. The $100\Omega$/22 pF network shown on the first page of this data sheet should be used when the junction temperature might reach 25°C (roughly 0°C ambient when the LF400 is "warmed up"). In applications where the device will be operating with a junction temperature near 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.

### Supply Bypassing

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 $\mu$F tantalum, a 2.2 $\mu$F ceramic, and a 0.47 $\mu$F ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.



TL/H/8393-17

**FIGURE 2. Power Supply Bypassing (see Text)**

### Output Drive and Current Limit

The LF400 can drive heavier resistive loads than most operational amplifiers. The output at pin 6 is internally current-limited when the voltage drop across the $25\Omega$ output resistor reaches about 0.55V ($I_{OUT}$ = 22 mA). When more output current is needed, pin 8 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 8 to pin 6, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 6 and 8 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF400, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.

The effective load impedance (including feedback resistance) should be kept above $500\Omega$ for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1 k$\Omega$ to 2 k$\Omega$ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

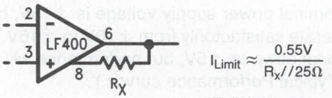


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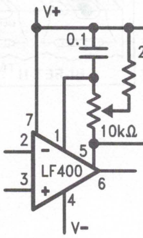
**FIGURE 3. Increasing the current limit using pin 8. Current limit is now determined by $R_X$ in parallel with the internal $25\Omega$ sense resistor.**

### $V_{OS}$ Adjustment

Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 5 as shown in *Figure 4a*. Bypassing the $V_{OS}$ adjust pins with 0.1 $\mu$F capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 5 can often be left open, but to minimize the possibility of noise pickup the unused $V_{OS}$ trim pins should be connected to ground or $V^-$.

## Application Hints (Continued)


V+
0.1
27kΩ
0.1
10kΩ
7
2
1
5
3
6
4
LF400
V−

TL/H/8393-19

**FIGURE 4a. V$_{OS}$ Adjust Circuit**

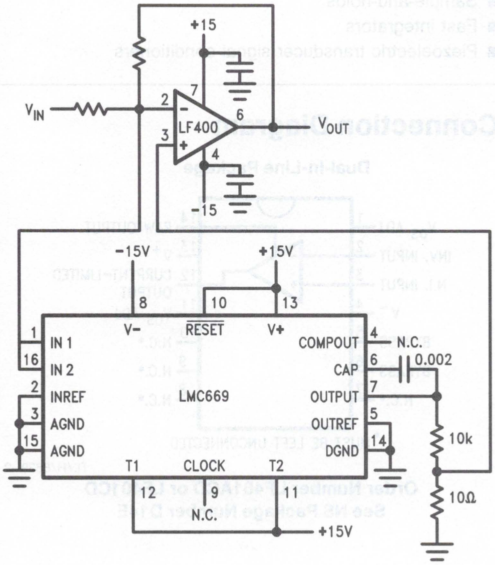

+15
V$_{IN}$
2
7
6
LF400
V$_{OUT}$
3
4
−15
−15V
+15V
8
10
13
V−
RESET
V+
1
IN 1
16
IN 2
2
INREF
3
AGND
15
AGND
LMC669
COMPOUT
4
N.C.
CAP
6
0.002
OUTPUT
7
OUTREF
5
DGND
14
10k
T1
CLOCK
T2
12
9
11
N.C.
10Ω
+15V

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**FIGURE 4b. Automatic Offset Adjustment Using LMC669**

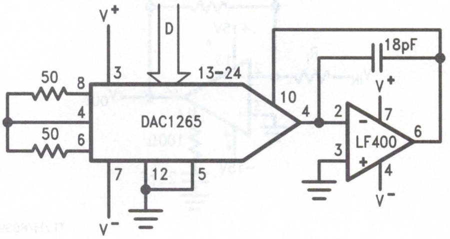
In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF400 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

### Input Bias Current

The JFET input stage of the LF400 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF400. "Press on" heat sinks from manufacturers such as Thermalloy and AAVID can reduce junction temperature by roughly 10°C to 40°C.

## Typical Applications

**High-Speed DAC with Voltage Output**


V+
D
3
13–24
50
8
4
DAC1265
50
6
7
12
5
10
4
V−
18pF
V+
2
7
LF400
6
3
4
V−

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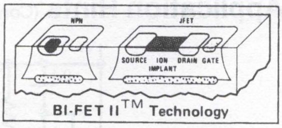
**National Semiconductor Corporation**

**PRELIMINARY**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# LF401 Precision Fast Settling JFET Input Operational Amplifier

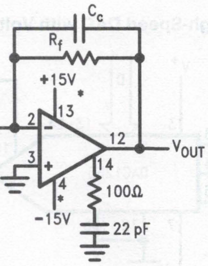
## General Description

The LF401A is a fast settling (guaranteed under 400 ns to 0.01% for a 10V output step) BI-FET operational amplifier. The input offset voltage of the LF401A is guaranteed less than 200 μV maximum at 25°C. The LF401 also features 16 MHz bandwidth, 70 V/μs inverting slew rate and adjustable short circuit current limit, enabling it to drive 600Ω loads easily.

## Applications

- DAC output amplifiers
- Fast buffers
- High speed ramp generators
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

## Typical Connection


C_c
R_f
+15V
*
R_i
V_IN
2
13
3
12
V_OUT
14
4
*
100Ω
-15V
22 pF

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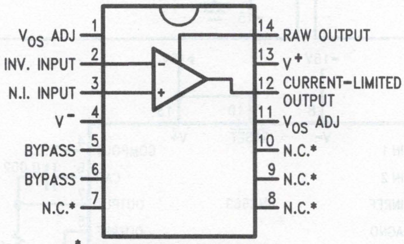
*See *Figure 2* for Power Supply Bypassing.

## Connection Diagram

### Dual-In-Line Package

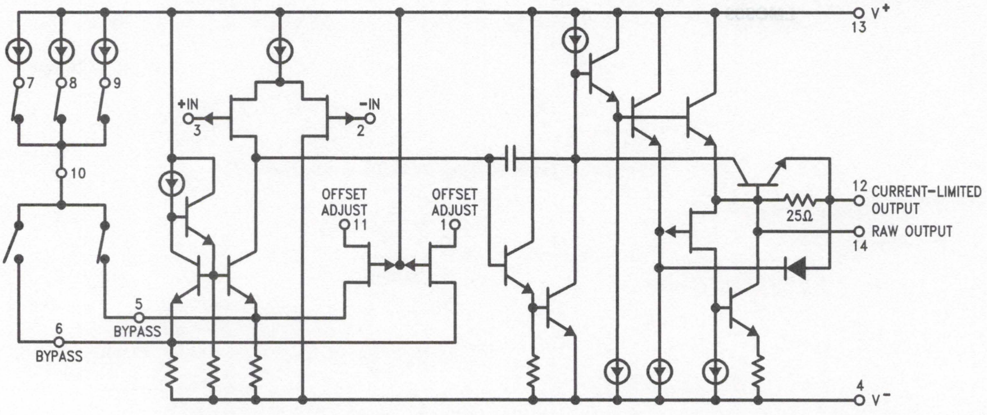

V_OS ADJ 1
INV. INPUT 2
N.I. INPUT 3
V⁻ 4
BYPASS 5
BYPASS 6
N.C.* 7
14 RAW OUTPUT
13 V⁺
12 CURRENT-LIMITED OUTPUT
11 V_OS ADJ
10 N.C.*
9 N.C.*
8 N.C.*
-
+

* MUST BE LEFT UNCONNECTED

TL/H/8839-2

**Order Number LF401ACD or LF401CD**
**See NS Package Number D14E**

## Simplified Schematic


7
8
9
10
6
BYPASS
5
BYPASS
+IN
3
-IN
2
OFFSET ADJUST
11
OFFSET ADJUST
1
V⁺
13
12 CURRENT-LIMITED OUTPUT
25Ω
RAW OUTPUT
14
4
V⁻

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## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+ - V^-$) | ±18V |
| Differential Input Voltage | ±32V |
| Input Voltage Range (Note 3) | ±16V |
| Output Short Circuit Duration (Pin 12) | CONTINUOUS |
| Power Dissipation (Note 4) D package | 500 mW |
| Junction Temperature ($T_{JMAX}$) | 115°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |
| ESD Susceptibility (Note 10) | 500V |

## Operating Ratings (Notes 1 & 2)

| | |
|---|---|
| Temperature Range | $T_{MIN} \leq T_A \leq T_{MAX}$ |
| LF401ACD, LF401CD | $0°C \leq T_A \leq +70°C$ |
| Positive Supply Voltage | +10V to +16V |
| Negative Supply Voltage | −10V to −16V |
| Total Supply Voltage ($V^+ - V^-$) | 20V to 32V |

## AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for $T_J = 25°C$ to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to $T_{MAX}$;** other Design Limits are for $T_A = 25°C$; all other limits for $T_J = 25°C$.

| Symbol | Parameter | Conditions | LF401ACD Typical (Note 6) | LF401ACD Tested Limit (Note 7) | LF401ACD Design Limit (Note 8) | LF401CD Typical (Note 6) | LF401CD Tested Limit (Note 7) | LF401CD Design Limit (Note 8) | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_s$ | Maximum Settling Time to 0.01%<br>to 0.10% | See *Figure 1*, $C_L \leq 50$ pF<br>See *Figure 1*, $C_L \leq 50$ pF | 335<br>200 | 400 | | 335<br>200 | 500 | | ns<br>ns |
| GBW | Minimum Gain Bandwidth Product | $A_v = +1$, $C_L = 10$ pF, f = 100 kHz | 16 | 14 | | 16 | 14 | | MHz |
| SR | Minimum Slew Rate | $A_v = +1$, $C_L = 10$ pF | | 27 | | | 27 | | V/µs |
| | | $A_v = -1$, $C_L = 10$ pF | 70 | | | 70 | | | V/µs |
| $\phi$ | Minimum Phase Margin | $A_{vol} = +1$, $C_L = 10$ pF | 60 | | | 60 | | | ° |
| $e_n$ | Input Noise Voltage | f = 1 KHz, Rs = 100Ω<br>Broadband, Rs = 100Ω, 10 Hz to 10 kHz | 23<br>2.3 | | | 23<br>2.3 | | | nV/√Hz<br>µV rms |
| $i_n$ | Input Noise Current | f = 1 kHz<br>Broadband 10 Hz to 10 kHz | 0.01<br>2.0 | | | 0.01<br>2.0 | | | pA/√Hz<br>pA rms |
| THD | Total Harmonic Distortion (Max) | f = 1 kHz, Av = −1, $R_L$ = 10k | 0.002 | | | 0.002 | | | % |
| CIN | Input Capacitance | Differential | 7 | | | 7 | | | pF |

## DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for $T_J = 25°C$ to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to $T_{MAX}$;** other Design Limits are for $T_A = 25°C$; all other limits for $T_J = 25°C$.

| Symbol | Parameter | Conditions | LF401ACD | | | LF401CD | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| $V_{OS}$ | Maximum Input Offset Voltage (Note 9) | $V_{CM} = 0V$, $R_S = 0$, $R_L = \infty$; $T_A = 25°C$<br>$T_A = 70°C$ | | ±200<br>±600 | | | ±500<br>±1500 | | µV<br>µV |
| $I_{OS}$ | Maximum Input Offset Current | $V_{CM} = 0V$, (Note 5) | | ±100 | ±400<br>**±2.5** | | ±100 | ±400<br>**±2.5** | pA<br>nA |
| $I_B$ | Maximum Input Bias Current | $V_{CM} = 0V$, (Note 5) | | 200 | <br>**26** | | 200 | <br>**26** | pA<br>nA |
| $R_{IN}$ | Input Resistance | $T_J = 25°C$ | $10^{11}$ | | | $10^{11}$ | | | Ω |
| $V_{CM}$ | Input Common-Mode Voltage Range | | +14/−12 | ±11 | | +14/−12 | ±11 | | V |
| $A_{VOL}$ | Minimum Large Signal Voltage Gain: Using Pin 12<br>Using Pin 14 | $V_o = \pm 10V$, $R_L = 2\ k\Omega$<br>$V_o = \pm 10V$, $R_L = 600\Omega$ | 300<br>300 | 100<br>100 | | 300<br>300 | 100<br>100 | | V/mV<br>V/mV |
| $V_O$ | Minimum Output Voltage Swing: Using Pin 12<br>Using Pin 14 | $R_L = 2\ k\Omega$<br>$R_L = 600\Omega$ | ±12.5<br>±12 | ±12<br>±11 | | ±12.5<br>±12 | ±12<br>±11 | | V<br>V |
| $I_{SC}$ | Output Short Circuit Current: MIN Using Pin 12<br>MAX Using Pin 12<br>MIN Using Pin 14 | <br><br>Pulse Test | | 15<br>45<br>100 | | | 15<br>45<br>100 | | mA<br>mA<br>mA |
| $R_O$ | Output Resistance: Using Pin 12<br>Using Pin 14 | Open Loop, DC<br>Open Loop, DC | 75<br>50 | | | 75<br>50 | | | Ω<br>Ω |
| CMRR | Minimum DC Common Mode Rejection Ratio | $-11V \leq V_{IN} \leq +11V$ | 100 | 90 | | 100 | 80 | | dB |
| PSRR | Minimum DC Power Supply Rejection Ratio | $+10V \leq V^+ < +15V$, $-15V \leq V^- < -10V$, $V_{CM} = 0V$ | 100 | 90 | | 100 | 80 | | dB |
| $I_S$ | Maximum Supply Current | $V_o = 0V$, $R_L = \infty$ | 9 | 12 | | 9 | 12 | | mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are with respect to ground.

**Note 3:** Unless otherwise specified, the Absolute Maximum Negative Input Voltage is equal to the negative power supply voltage.

**Note 4:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or 500 mW, whichever is less. $\theta_{JA}$ for the LF401D is typically 87°C/W.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature $T_J$. Due to limited production test time, input bias currents are measured at $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation $P_D$. Use of a heat sink is recommended when input bias current must be minimized.

**Note 6:** Typicals represent the most likely parametric norm.

**Note 7:** Guaranteed to National's AOQL (Average Outgoing Quality Level).

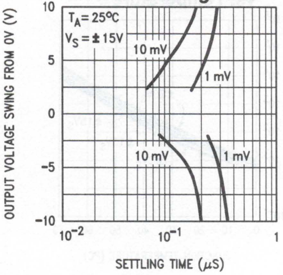
**Note 8:** Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

**Note 9:** Tested and correlated to a 10 minute warm up period.

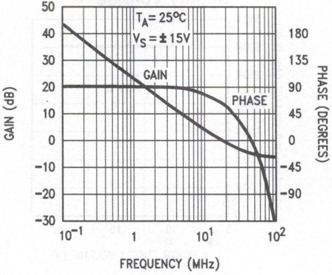
**Note 10:** Human body model, 100 pF discharged through a 1500Ω resistor.

## Typical Performance Characteristics

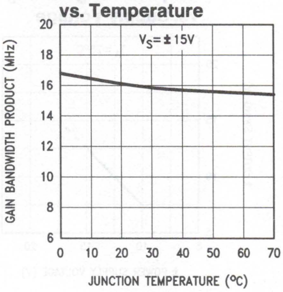
**Inverter Settling Time**



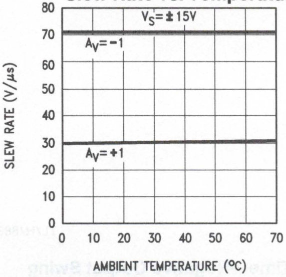
**Bode Plot**



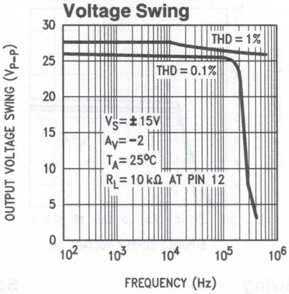
**Gain Bandwidth vs. Temperature**



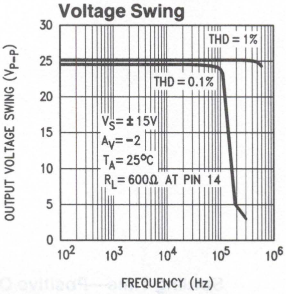
**Slew Rate vs. Temperature**



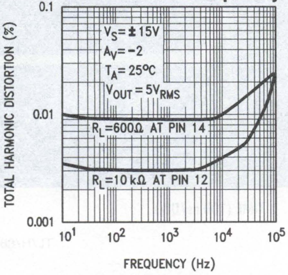
**Undistorted Output Voltage Swing**



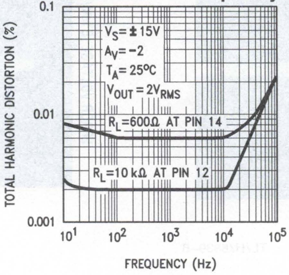
**Undistorted Output Voltage Swing**



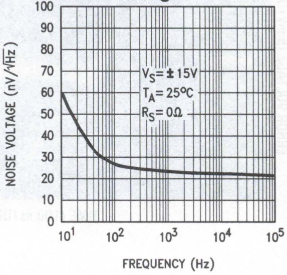
**Distortion vs. Frequency**



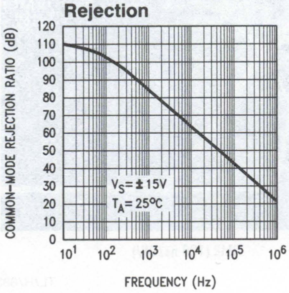
**Distortion vs. Frequency**



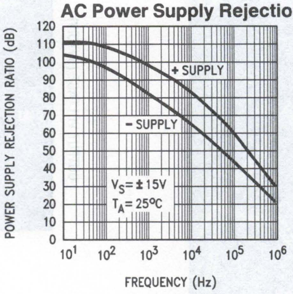
**Equivalent Input Noise Voltage**



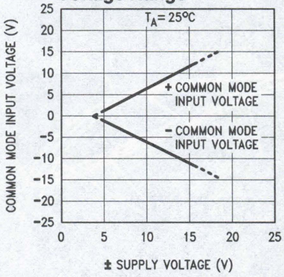
**AC Common-Mode Rejection**



**AC Power Supply Rejection**



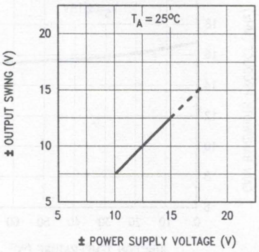
**Common-Mode Input Voltage Range**



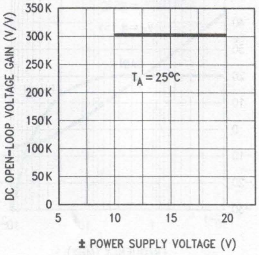
TL/H/8839-4

## Typical Performance Characteristics (Continued)

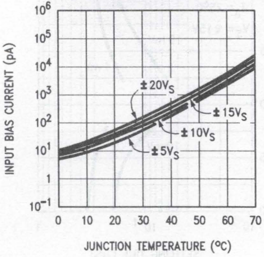
**Output Voltage Swing vs. Supply Voltage**



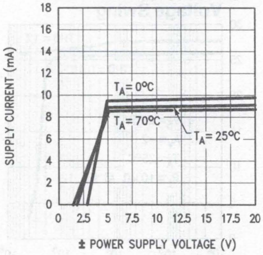
**DC Gain vs. Supply Voltage**



**Input Bias Current vs. Temperature**

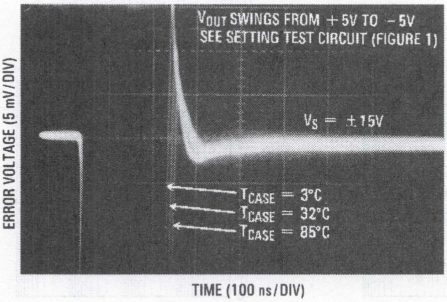


**Power Supply Current vs. Power Supply Voltage**



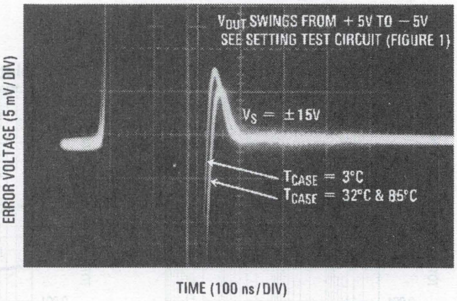
TL/H/8839-5

**Settling Time—Positive Output Swing**



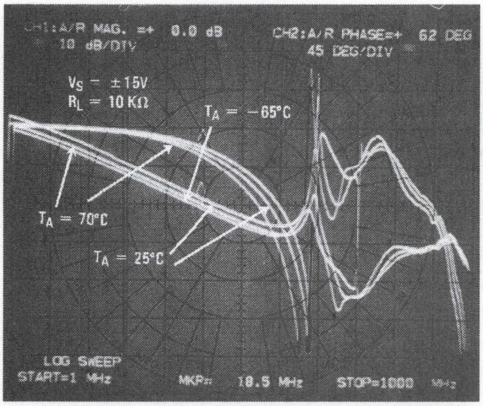
TL/H/8839-6

**Settling Time—Negative Output Swing**



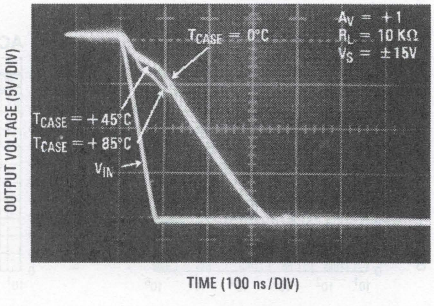
TL/H/8839-7

**Bode Plot**



TL/H/8839-8

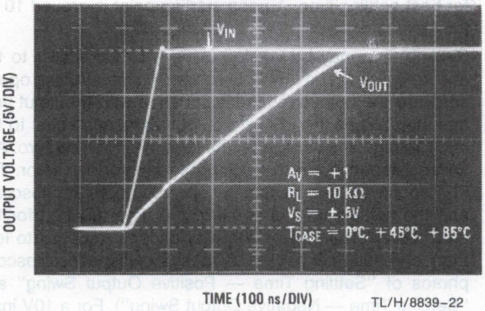
**Step Response**



TL/H/8839-9

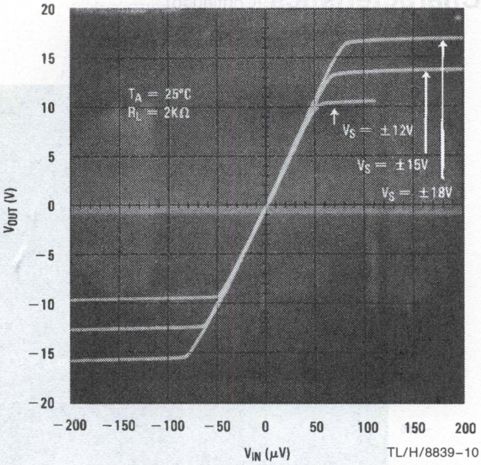
## Typical Performance Characteristics (Continued)

### Step Response



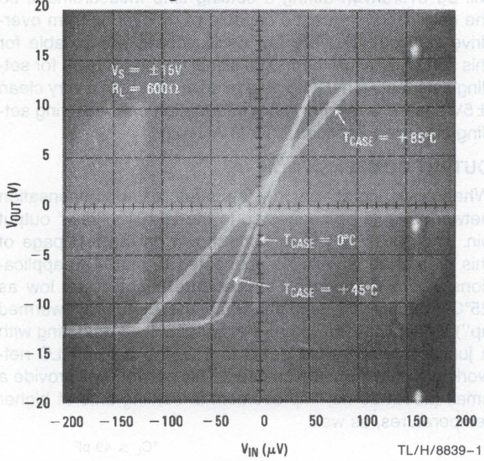
TL/H/8839-22

### Voltage Transfer Characteristic



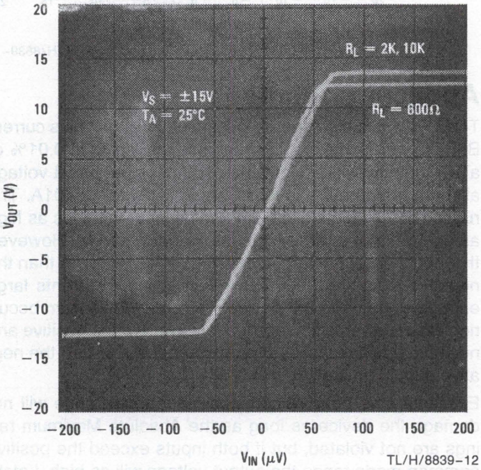
TL/H/8839-10

### Voltage Transfer Characteristic



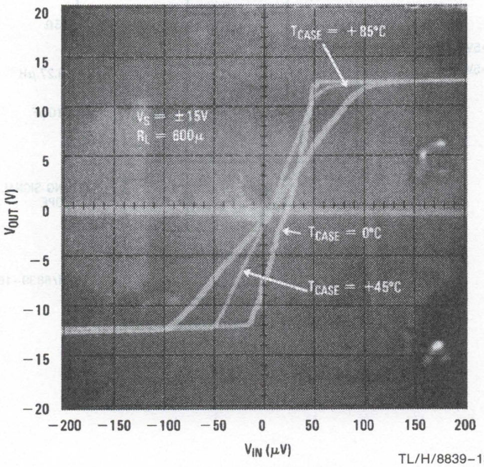
TL/H/8839-11

### Voltage Transfer Characteristic



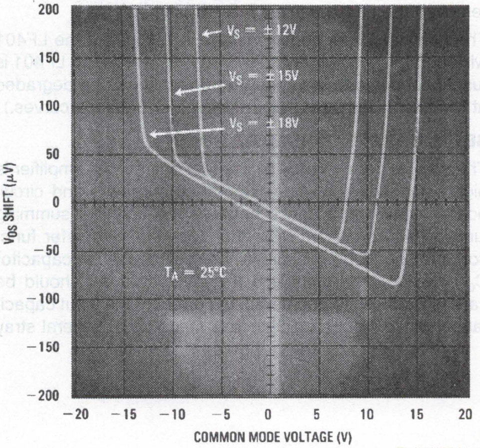
TL/H/8839-12

### Voltage Transfer Characteristic



TL/H/8839-13

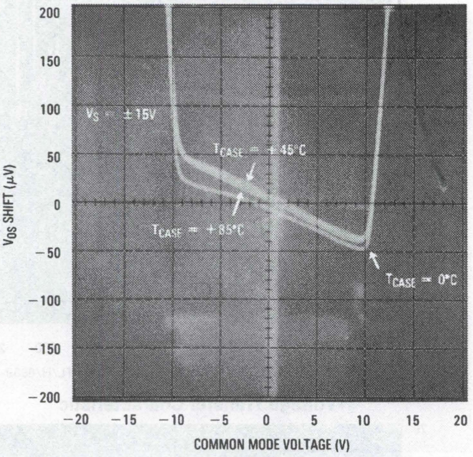
### Common Mode Voltage Transfer Characteristic



TL/H/8839-14

## Typical Performance Characteristics (Continued)

Common Mode Voltage Transfer Characteristic



TL/H/8839-15

## Application Hints

The LF401 is a high-speed, low offset, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. Input offset voltage at room temperature is less than 200 μV for LF401A. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the positive common-mode input range will not damage the device as long as the Absolute Maximum ratings are not violated, but if both inputs exceed the positive common-mode range the output voltage will go high. Latching will not occur, however, and when the offending signal is removed the LF401 will recover quickly.

The nominal power supply voltage is ±15V, but the LF401 will operate satisfactorily from ±10V to ±16V. The LF401 is functional down to ±5V, but performance will be degraded at low supply voltages. (See Typical Performance curves.)

### SETTLING TIME CONSIDERATIONS

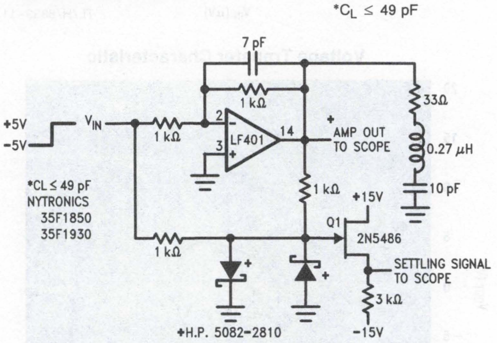
The settling performance of any fast operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor $C_C$ between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF401 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF401's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time — Positive Output Swing" and "Settling Time — Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than 1/2 mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF401's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for settling time testing must be able to drive 50Ω with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

### OUTPUT COMPENSATION

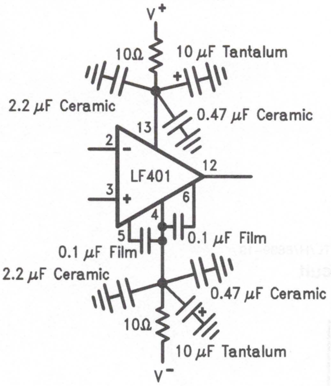
When operating at very low temperatures, a compensation network should be connected to the LF401's "raw" output pin. The 100Ω/22 pF network shown on the first page of this data sheet should be connected to pin 14 in applications where the junction temperature might go as low as 25°C (roughly 0°C ambient when the LF401 is "warmed up"). In applications where the device will be operating with a junction temperature down to 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.



TL/H/8839-16

**FIGURE 1. Simplified Settling Time Test Circuit (See Text)**

## Application Hints (Continued)



TL/H/8839–17

**FIGURE 2. Power Supply Bypassing (See Text)**

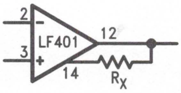
### SUPPLY BYPASSING

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 μF tanatalum, a 2.2 μF ceramic, and a 0.47 μF ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.

Pins 5 through 10 are used to trim the LF401's input offset voltage during the manufacturing process. Always leave pins 7 through 10 open, as signals applied to these pins will affect the amplifier output and can permanently degrade $V_{OS}$. For fastest settling time to 0.01%, pins 5 and 6 should be bypassed to pin 4 with 0.1 μF capacitors; otherwise, the LF401 may take an additional 600 ns to settle. The bypass capacitors should be low-leakage film types; otherwise the offset voltage can be increased. Settling time to 0.1% will be unaffected by bypassing these pins, so they may be left unconnected in applications requiring less precision.

### OUTPUT DRIVE AND CURRENT LIMIT

The LF401 can drive heavier resistive loads than most operational amplifiers. The output at pin 12 is internally current-limited when the voltage drop across the 25Ω output resistor reaches about 0.55V ($I_{out}$ = 22 mA). When more output current is needed, pin 14 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 12 to pin 14, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 12 and 14 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF401, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.



TL/H/8839–18

**FIGURE 3. Increasing the current limit using pin 14. Current limit is now determined by $R_X$ in parallel with the internal 25Ω sense resistor.**

The effective load impedance (including feedback resistance) should be kept above 500Ω for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1k to 2 kΩ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

### $V_{OS}$ ADJUSTMENT

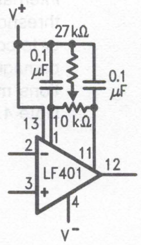
Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 11 as shown in *Figure 4a*. Bypassing the $V_{OS}$ adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 11 can often be left open, but to minimize the possibility of noise pickup the unused $V_{OS}$ trim pins should be connected to ground or V−.

In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF401 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

### INPUT BIAS CURRENT

The JFET input stage of the LF401 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF401. "Slide on" heat sinks such as the AAVID 5602B can reduce the junction temperature by about 10°C.

## Application Hints (Continued)


V+
27 kΩ
0.1 μF
0.1 μF
13
10 kΩ
1
2
11
LF401
12
3
4
V−

TL/H/8839-19

**FIGURE 4a. $V_{OS}$ Adjust Circuit**

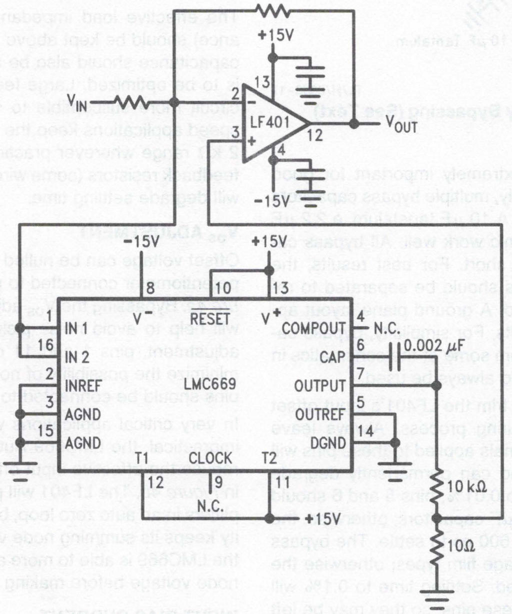

+15V
13
2
V_IN
LF401
V_OUT
3
12
4
−15V
−15V
+15V
8
10
13
1
IN 1
RESET
V−
V+
COMPOUT
4
N.C.
16
IN 2
6
CAP
0.002 μF
2
INREF
LMC669
7
OUTPUT
3
AGND
5
OUTREF
15
AGND
14
DGND
T1
CLOCK
T2
12
9
11
N.C.
10 kΩ
+15V
10Ω

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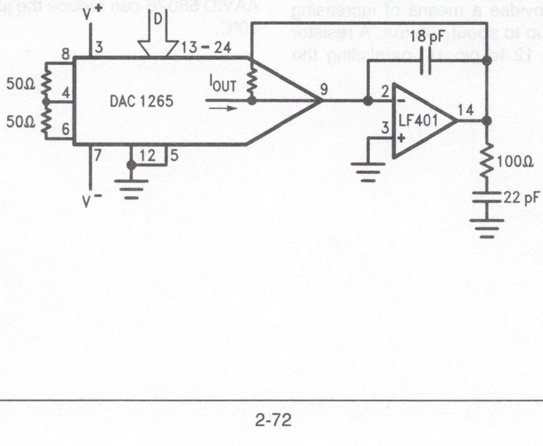
**FIGURE 4b. Automatic Offset Adjustment Using LMC669**

# Typical Applications

**High-Speed DAC with Voltage Output (See *Figure 2* for Recommended Bypass Components)**


V+
D
13 – 24
3
8
18 pF
50Ω
4
I_OUT
9
2
DAC 1265
14
50Ω
6
LF401
3
7
12
5
100Ω
22 pF
V−

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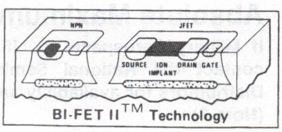
**National Semiconductor Corporation**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

## General Description

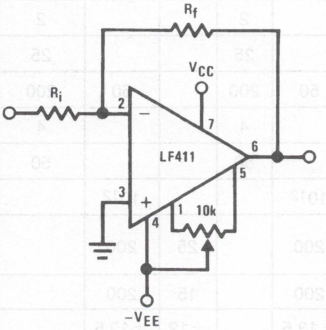
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

## Features

- Internally trimmed offset voltage 0.5 mV(max)
- Input offset voltage drift 10 μV/°C(max)
- Low input bias current 50 pA
- Low input noise current 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth 3 MHz(min)
- High slew rate 10V/μs(min)
- Low supply current 1.8 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz − 20 kHz <0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

## Typical Connection


R_f
V_CC
R_i
2
−
7
6
LF411
5
3
+
4
1
10k
−V_EE

TL/H/5655-1

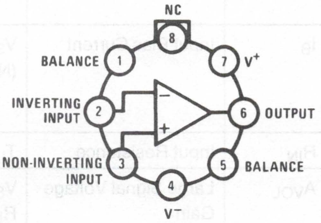
## Ordering Information

**LF411XYZ**

| | |
|---|---|
| X | indicates electrical grade |
| Y | indicates temperature range<br>"M" for military<br>"C" for commercial |
| Z | indicates package type<br>"H" or "N" |

## Connection Diagrams

**Metal Can Package**


NC
8
BALANCE
1
7
V+
INVERTING INPUT
2
−
+
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE
4
V−

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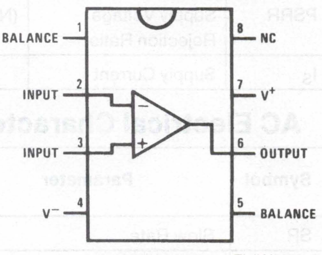
**Top View**

**Note:** Pin 4 connected to case.

**Order Number LF411AMH, LF411MH, LF411ACH or LF411CH**
**See NS Package Number H08B**

**Dual-In-Line Package**

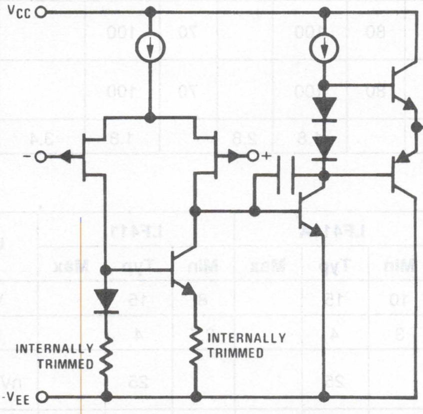

BALANCE
1
8
NC
INPUT
2
7
V+
INPUT
3
−
+
6
OUTPUT
V−
4
5
BALANCE

TL/H/5655-7

**Top View**

**Order Number**
**LF411ACN or LF411CN**
**See NS Package Number N08E**

## Simplified Schematic


V_CC
V_O
−
+
INTERNALLY TRIMMED
INTERNALLY TRIMMED
-V_EE

TL/H/5655-6

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 8)**

| | **LF411A** | **LF411** |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous |

| | **H Package** | **N Package** |
|---|---|---|
| Power Dissipation (Notes 2 and 9) | 670 mW | 670 mW |
| $T_j$max | 150°C | 115°C |
| $\theta_jA$ | 225°C/W (Still Air)<br>160°C/W (400 LF/min Air Flow) | 120°C/W |
| $\theta_jC$ | 25°C/W | |
| Operating Temp. Range | (Note 3) | (Note 3) |
| Storage Temp. Range | $-65°C \le T_A \le 150°C$ | $-65°C \le T_A \le 150°C$ |
| Lead Temp. (Soldering, 10 sec.) | 260°C | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | | LF411A Min | LF411A Typ | LF411A Max | LF411 Min | LF411 Typ | LF411 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega$, $T_A = 25°C$ | | | 0.3 | 0.5 | | 0.8 | 2.0 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ (Note 5) | | | 7 | 10 | | 7 | 20 (Note 5) | μV/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 4, 6) | $T_j = 25°C$ | | 25 | 100 | | 25 | 100 | pA |
| | | | $T_j = 70°C$ | | | 2 | | | 2 | nA |
| | | | $T_j = 125°C$ | | | 25 | | | 25 | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 4, 6) | $T_j = 25°C$ | | 50 | 200 | | 50 | 200 | pA |
| | | | $T_j = 70°C$ | | | 4 | | | 4 | nA |
| | | | $T_j = 125°C$ | | | 50 | | | 50 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$ | | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | | 25 | 200 | | 15 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$ | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | | −16.5 | | | −11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10k$ | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | | 80 | 100 | | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | | 1.8 | 2.8 | | 1.8 | 3.4 | mA |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF411A Min | LF411A Typ | LF411A Max | LF411 Min | LF411 Typ | LF411 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | 10 | 15 | | 8 | 15 | | V/μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | 3 | 4 | | 2.7 | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$, $f = 1\ kHz$ | | 25 | | | 25 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, $f = 1\ kHz$ | | 0.01 | | | 0.01 | | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_jA$.

**Note 3:** These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

**Note 4:** Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 5:** The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

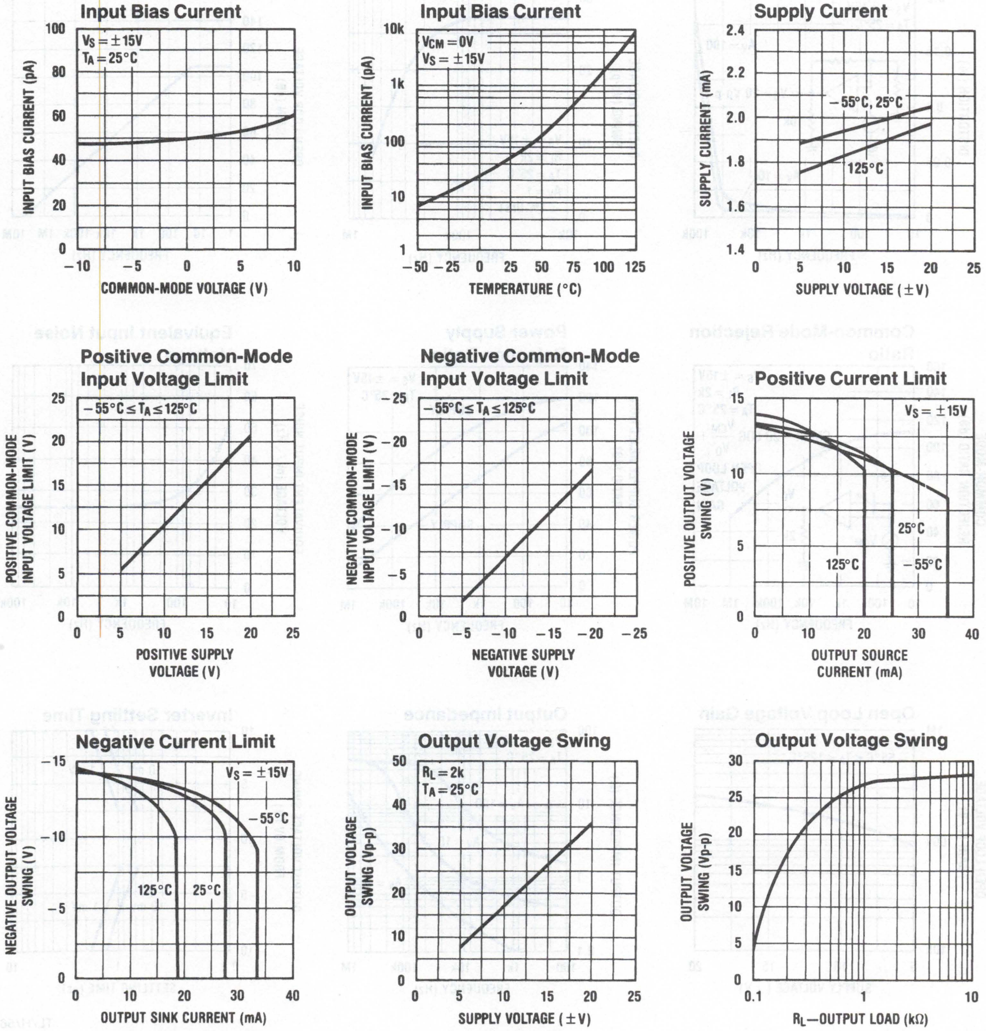
**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

**Note 8:** Refer to RETS 411AX for LF411AMH military specifications and to RETS 411X for LF411MH military specifications.

**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

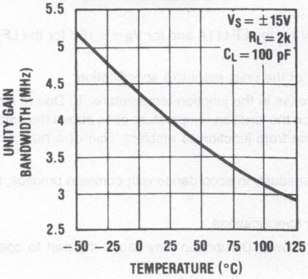
## Typical Performance Characteristics



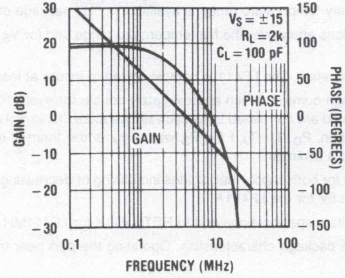
TL/H/5655-2

## Typical Performance Characteristics (Continued)

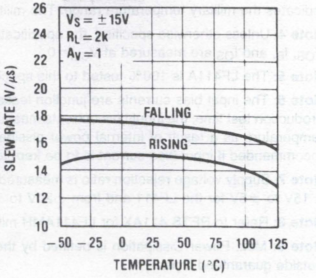
**Gain Bandwidth**



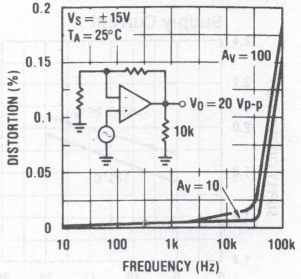
**Bode Plot**



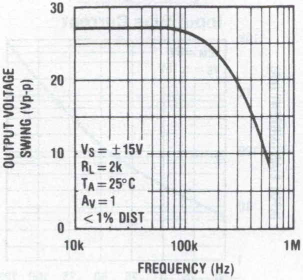
**Slew Rate**



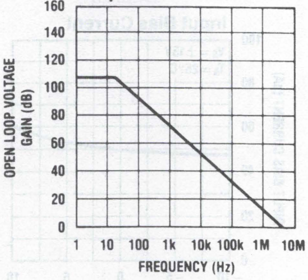
**Distortion vs Frequency**



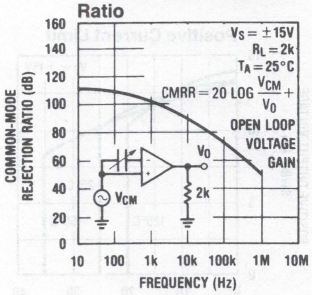
**Undistorted Output Voltage Swing**



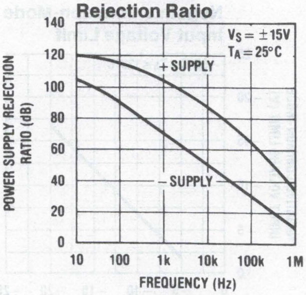
**Open Loop Frequency Response**



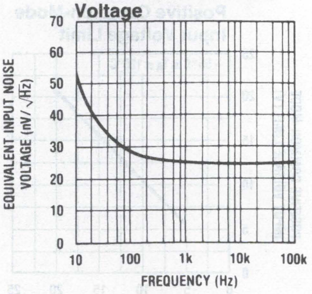
**Common-Mode Rejection Ratio**



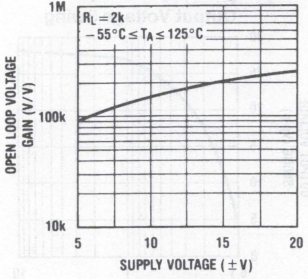
**Power Supply Rejection Ratio**



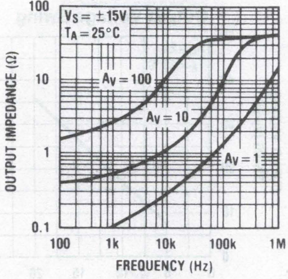
**Equivalent Input Noise Voltage**



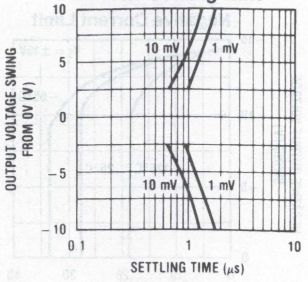
**Open Loop Voltage Gain**



**Output Impedance**



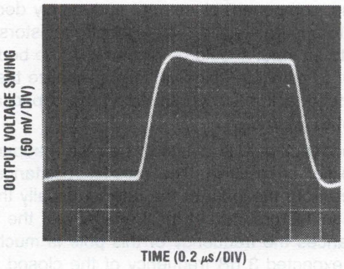
**Inverter Settling Time**



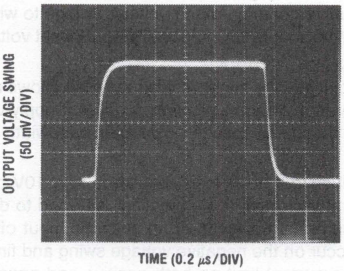
TL/H/5655–3

## Pulse Response $R_L = 2\ k\Omega$, $C_L 10\ pF$

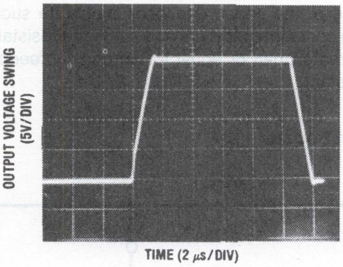
Small Signal Inverting



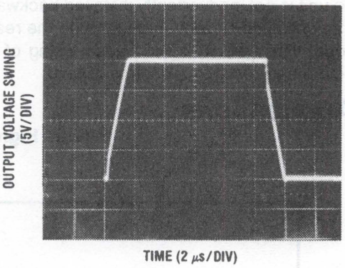
Small Signal Non-Inverting



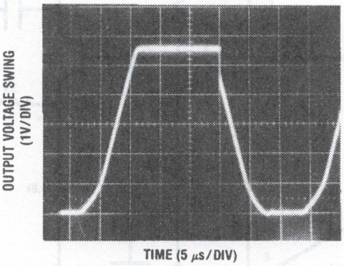
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655-4

## Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

## Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

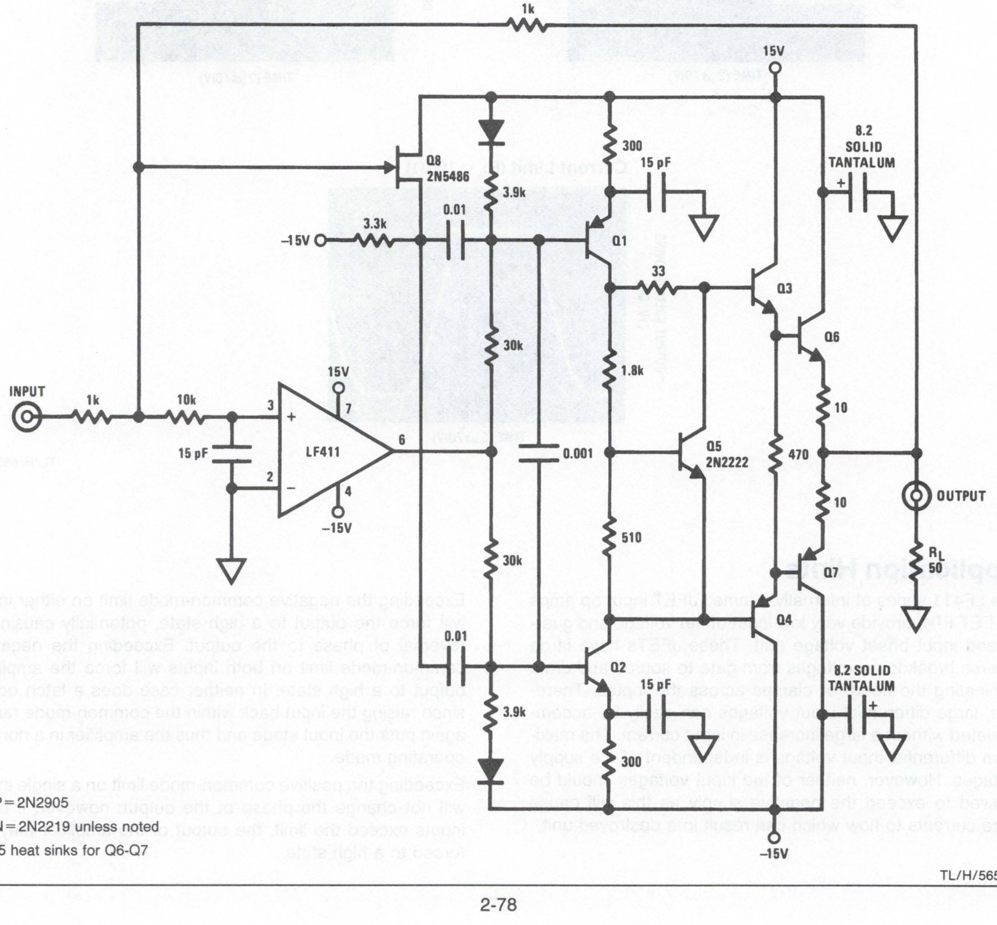
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Applications

### Ultra High Speed Current Booster



PNP = 2N2905

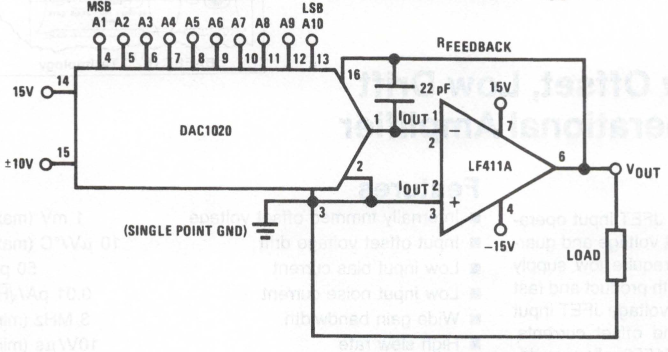
NPN = 2N2219 unless noted

TO-5 heat sinks for Q6-Q7

TL/H/5655-9

## Typical Applications (Continued)

**10-Bit Linear DAC with No $V_{OS}$ Adjust**


MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
15V
14
DAC1020
±10V
15
16
$R_{FEEDBACK}$
22 pF
15V
$I_{OUT}$ 1
2
7
LF411A
6
$V_{OUT}$
$\overline{I_{OUT}}$ 2
3
4
3
−15V
(SINGLE POINT GND)
LOAD

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\cdots\frac{A10}{1024}\right)$$

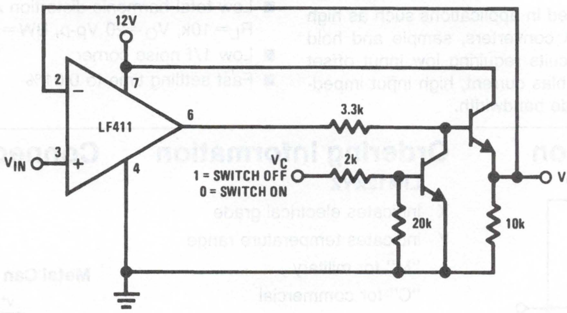
$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le \frac{1023}{1024} V_{REF}$$

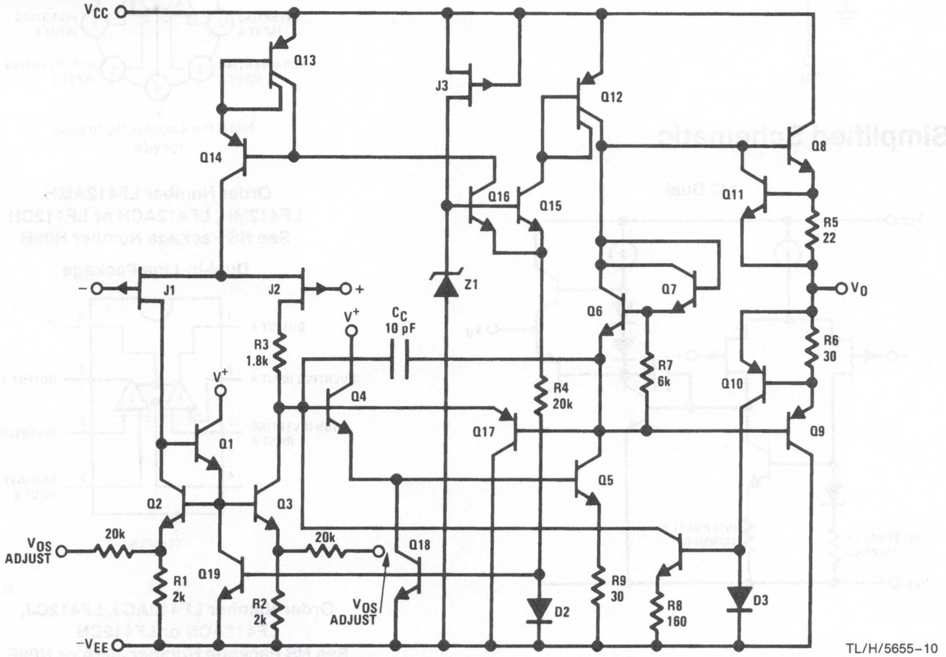
where $A_N = 1$ if the $A_N$ digital input is high

$A_N = 0$ if the $A_N$ digital input is low

**Single Supply Analog Switch with Buffered Output**

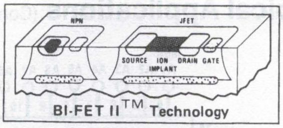

12V
2
7
LF411
6
3
$V_{IN}$
4
3.3k
2k
$V_C$
1 = SWITCH OFF
0 = SWITCH ON
$V_O$
20k
10k

## Detailed Schematic


$V_{CC}$
Q13
J3
Q12
Q14
Q8
Q16
Q15
Q11
R5
22
Z1
Q7
$V_O$
J1
J2
+
$V^+$
$C_C$
10 pF
Q6
R3
1.8k
R6
30
R7
6k
$V^+$
Q4
Q10
R4
20k
Q17
Q9
Q1
Q5
Q2
Q3
20k
20k
Q18
$V_{OS}$
ADJUST
R1
2k
Q19
R9
30
R8
160
D3
R2
2k
$V_{OS}$
ADJUST
D2
$-V_{EE}$

TL/H/5655–10

**National Semiconductor Corporation**


NPN
JFET
SOURCE ION IMPLANT DRAIN GATE
BI-FET II™ Technology

# LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

## General Description

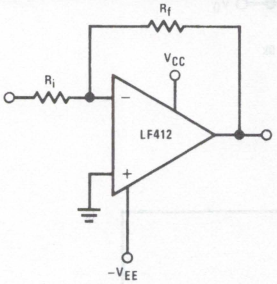
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

## Features

| | |
|---|---|
| ■ Internally trimmed offset voltage | 1 mV (max) |
| ■ Input offset voltage drift | 10 μV/°C (max) |
| ■ Low input bias current | 50 pA |
| ■ Low input noise current | 0.01 pA/$\sqrt{\text{Hz}}$ |
| ■ Wide gain bandwidth | 3 MHz (min) |
| ■ High slew rate | 10V/μs (min) |
| ■ Low supply current | 1.8 mA/Amplifier |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz | ≤0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 μs |

## Typical Connection


$R_f$
$V_{CC}$
$R_i$
−
+
LF412
$-V_{EE}$

## Ordering Information

**LF412XYZ**

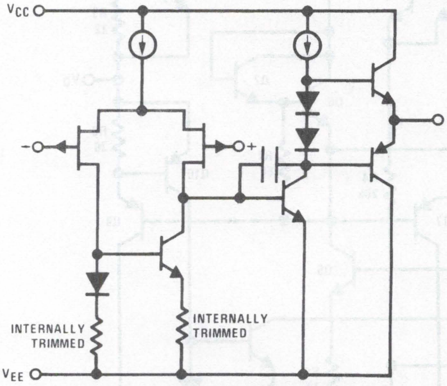
**X** indicates electrical grade

**Y** indicates temperature range
"M" for military
"C" for commercial

**Z** indicates package type
"H" or "N"

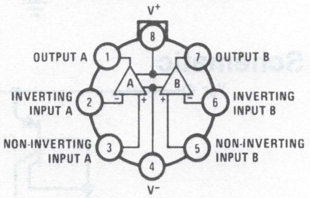
## Simplified Schematic

**1/2 Dual**


$V_{CC}$
−
+
$V_O$
INTERNALLY TRIMMED
INTERNALLY TRIMMED
$V_{EE}$

## Connection Diagrams

**Metal Can Package**

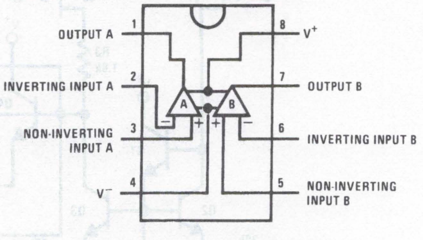

V+
8
OUTPUT A
1
7
OUTPUT B
INVERTING INPUT A
2
A
B
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V−

Note. Pin 4 connected to case.

TOP VIEW

**Order Number LF412AMH, LF412MH, LF412ACH or LF412CH See NS Package Number H08B**

**Dual-In-Line Package**


OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V−
4
5
NON-INVERTING INPUT B

TOP VIEW

TL/H/5656–1

**Order Number LF412ACJ, LF412CJ, LF412ACN or LF412CN See NS Package Number J08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 9)**

| | LF412A | LF412 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |

| | H Package | N Package |
|---|---|---|
| Power Dissipation (Note 10) | (Note 3) | 670 mW |
| $T_j$ max | 150°C | 115°C |
| $\theta_{jA}$ (Typical) | 195°C/W | 115°C/W |
| Operating Temp. Range | (Note 4) | (Note 4) |
| Storage Temp. Range | $-65°C \le T_A \le 150°C$ | $-65°C \le T_A \le 150°C$ |
| Lead Temp. (Soldering, 10 sec.) | 260°C | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | | LF412A | | | LF412 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega$, $T_A = 25°C$ | | | 0.5 | 1.0 | | 1.0 | 3.0 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ (Note 6) | | | 7 | 10 | | 7 | 20 (Note 6) | $\mu$V/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 5 and 7) | $T_j = 25°C$ | | 25 | 100 | | 25 | 100 | pA |
| | | | $T_j = 70°C$ | | | 2 | | | 2 | nA |
| | | | $T_j = 125°C$ | | | 25 | | | 25 | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 5 and 7) | $T_j = 25°C$ | | 50 | 200 | | 50 | 200 | pA |
| | | | $T_j = 70°C$ | | | 4 | | | 4 | nA |
| | | | $T_j = 125°C$ | | | 50 | | | 50 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$ | | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | | 25 | 200 | | 15 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10k$ | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | | −16.5 | | | −11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10k$ | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 8) | | 80 | 100 | | 70 | 100 | | dB |
| $I_S$ | Supply Current | $V_O = 0V$, $R_L = \infty$ | | | 3.6 | 5.6 | | 3.6 | 6.5 | mA |

## AC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF412A | | | LF412 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred) | | −120 | | | −120 | | dB |
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | 10 | 15 | | 8 | 15 | | V/$\mu$s |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | 3 | 4 | | 2.7 | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz | | 25 | | | 25 | | nV/$\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, f = 1 kHz | | 0.01 | | | 0.01 | | pA/$\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{jA}$.

**Note 4:** These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature $T_j$ max.

**Note 5:** Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 6:** The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

**Note 7:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

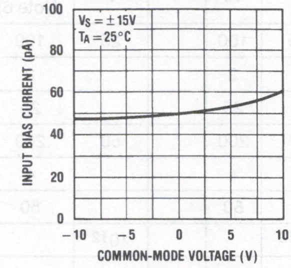
**Note 8:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

**Note 9:** Refer to RETS412AX for LF412AMH military specifications and to RETS412X for LF412MH military specifications.

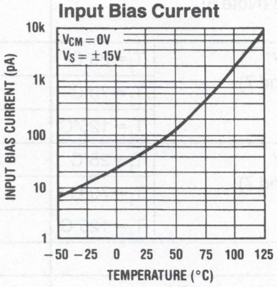
**Note 10:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

## Typical Performance Characteristics

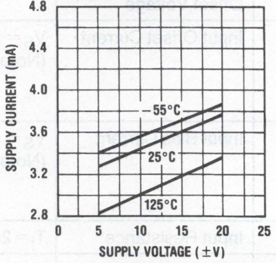
**Input Bias Current**



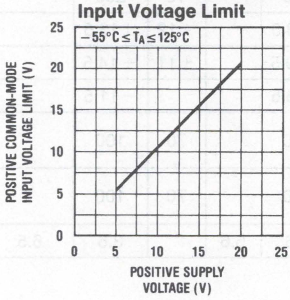
**Input Bias Current**



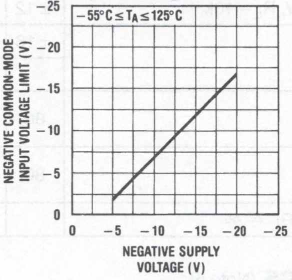
**Supply Current**



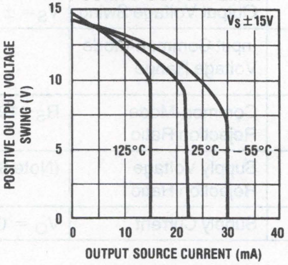
**Positive Common-Mode Input Voltage Limit**



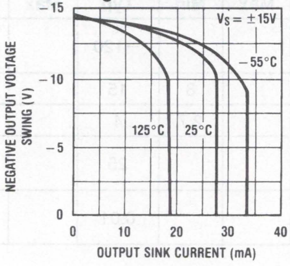
**Negative Common-Mode Input Voltage Limit**



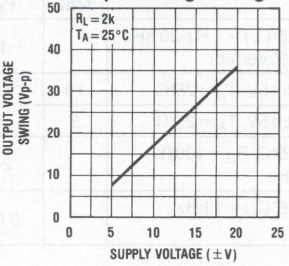
**Positive Current Limit**



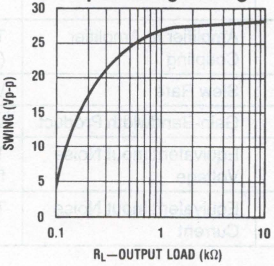
**Negative Current Limit**



**Output Voltage Swing**



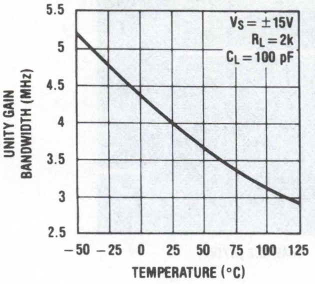
**Output Voltage Swing**



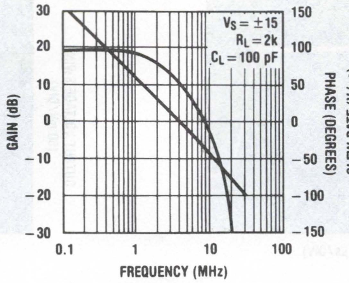
TL/H/5656–2

## Typical Performance Characteristics (Continued)

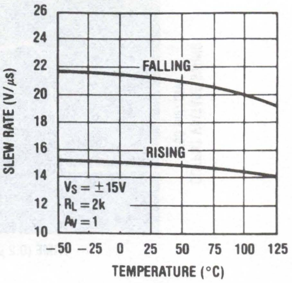
### Gain Bandwidth



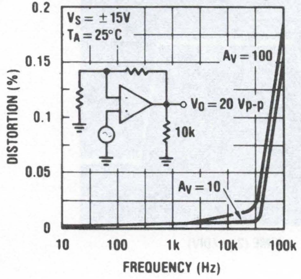
### Bode Plot



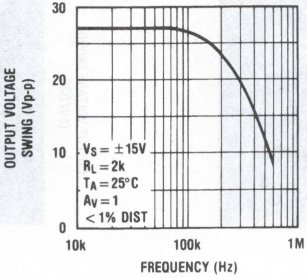
### Slew Rate



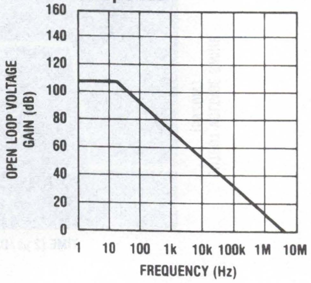
### Distortion vs Frequency



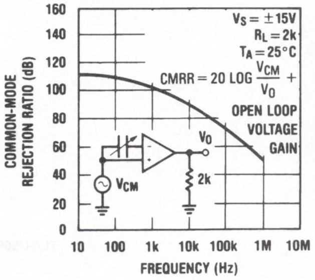
### Undistorted Output Voltage Swing



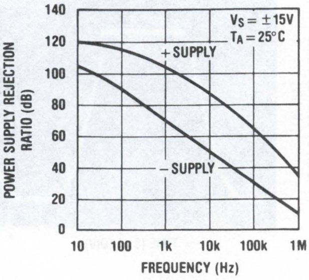
### Open Loop Frequency Response



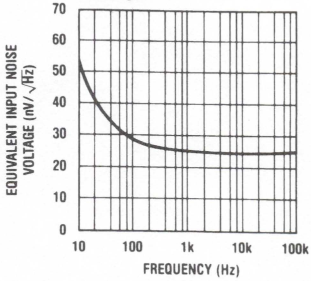
### Common-Mode Rejection Ratio



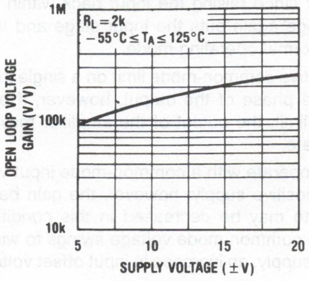
### Power Supply Rejection Ratio



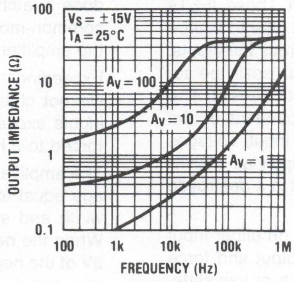
### Equivalent Input Noise Voltage



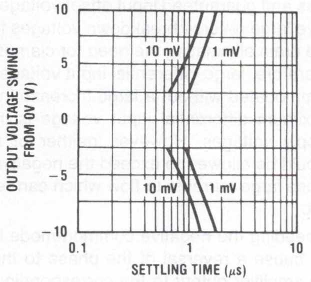
### Open Loop Voltage Gain



### Output Impedance



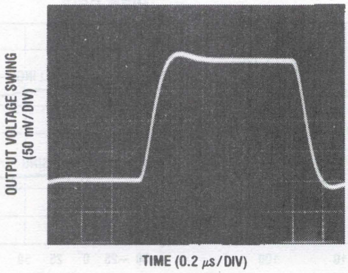
### Inverter Settling Time



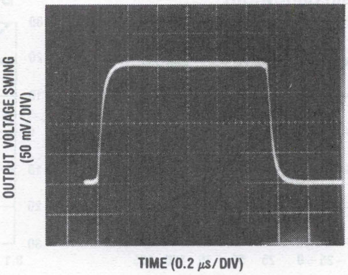
TL/H/5656-3

## Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

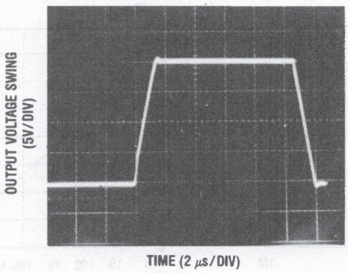
Small Signal Inverting



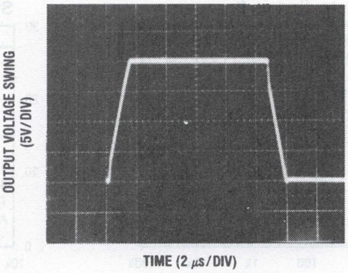
Small Signal Non-Inverting



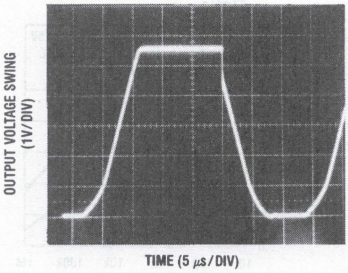
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5656-4

## Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

## Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

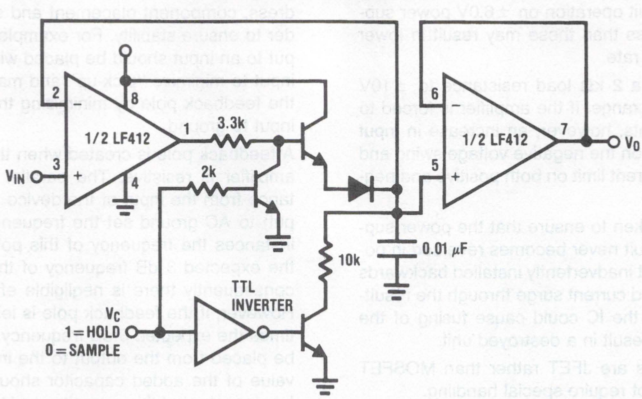
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

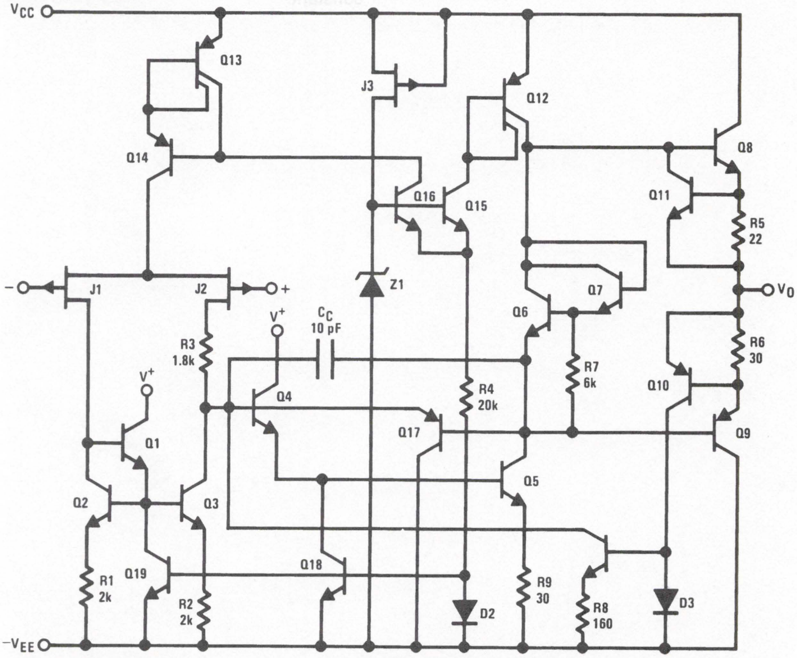
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Application

### Single Supply Sample and Hold

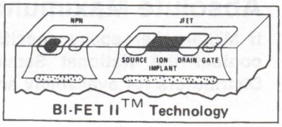

2
8
3
4
1
1/2 LF412
$V_{IN}$
+
3.3k
2k
10k
0.01 µF
6
5
7
–
+
1/2 LF412
$V_O$
TTL
INVERTER
$V_C$
1 = HOLD
0 = SAMPLE

## Detailed Schematic


$V_{CC}$
Q13
J3
Q12
Q8
Q14
Q16
Q15
Q11
R5
22
–
J1
J2
+
Z1
Q7
$V_O$
Q6
$V^+$
$C_C$
10 pF
R3
1.8k
R7
6k
R6
30
$V^+$
Q4
R4
20k
Q10
Q1
Q17
Q9
Q5
Q2
Q3
Q19
Q18
R1
2k
R2
2k
R9
30
R8
160
D2
D3
$-V_{EE}$

TL/H/5656–9

**National Semiconductor Corporation**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# LF441A/LF441 Low Power JFET Input Operational Amplifier

## General Description

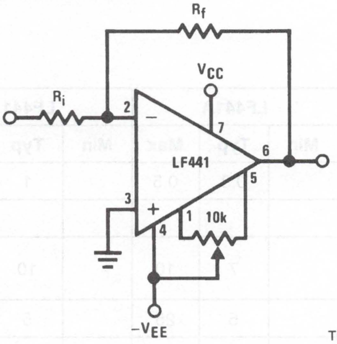
The LF441A/441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441A/441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441A/441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441A/441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441A/441 should be used where low power dissipation and good electrical characteristics are the major considerations.

## Features

| | |
|---|---|
| ■ 1/10 supply current of a LM741 | 200 μA (max) |
| ■ Low input bias current | 50 pA (max) |
| ■ Low input offset voltage | 0.5 mV (max) |
| ■ Low input offset voltage drift | 10 μV/°C (max) |
| ■ High gain bandwidth | 1 MHz |
| ■ High slew rate | 1 V/μs |
| ■ Low noise voltage for low power | 35 nV/√Hz |
| ■ Low input noise current | 0.01 pA/√Hz |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ High gain $V_O = \pm 10V$, $R_L = 10k$ | 50k (min) |

## Typical Connection


$R_f$
$V_{CC}$
$R_i$
2
7
6
LF441
5
3
1
10k
4
$-V_{EE}$

TL/H/9297–1

## Ordering Information

**LF441XYZ**

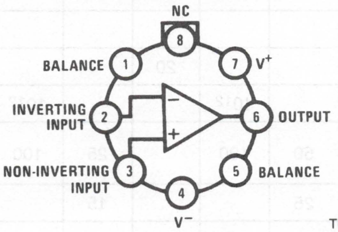
**X** indicates electrical grade

**Y** indicates temperature range
"M" for military,
"C" for commercial

**Z** indicates package type
"H" or "N"

## Connection Diagrams

**Metal Can Package**


NC
8
BALANCE
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE
4
V−

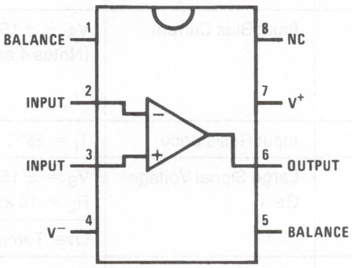
TL/H/9297–2

**Top View**

**Note:** Pin 4 connected to case.

**Order Number LF441AMH or LF441CH**
**See NS Package Number H08B**

**Dual-In-Line Package**


BALANCE
1
8
NC
INPUT
2
7
V+
INPUT
3
6
OUTPUT
V−
4
5
BALANCE

TL/H/9297–4

**Top View**

**Order Number LF441ACN, LF441CJ, LF441CM or LF441CN**
**See NS Package Number J08A, M08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | LF441A | LF441 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous |

| | H Package | J Package | N Package | M Package |
|---|---|---|---|---|
| Power Dissipation (Notes 2 and 9) | 670 mW | | 670 mW | |
| $T_{j\,max}$ | 150°C | | 115°C | |
| $\theta_{jA}$(Typical) | | | 130°C/W | 185°C/W |
| Board Mount in still air | 225°C/W | | | |
| Board Mount in 400 LF/ min air flow | 90°C/W | | | |
| $\theta_{jC}$ | 25°C/W | | | |
| Operating Temp. Range | (Note 3) | | (Note 3) | |
| Storage Temp. Range | $-65°C \le T_A \le 150°C$ | | $-65°C \le T_A \le 150°C$ | |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 300°C | 260°C | |
| $\theta_{jC}$ | 25°C | | | |

| | LF441A | LF441 |
|---|---|---|
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 sec.) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 sec.) | 215°C | 215°C |
| Infrared (15 sec.) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | | LF441A | | | LF441 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\,k\Omega, T_A = 25°C$ | | | 0.3 | 0.5 | | 1 | 5 | mV |
| | | Over Temperature | | | | | | | 7.5 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\,k\Omega$ (Note 5) | | | 7 | 10 | | 10 | | μV/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 4 and 6) | $T_j = 25°C$ | | 5 | 25 | | 5 | 50 | pA |
| | | | $T_j = 70°C$ | | | 1.5 | | | 1.5 | nA |
| | | | $T_j = 125°C$ | | | 10 | | | | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 4 and 6) | $T_j = 25°C$ | | 10 | 50 | | 10 | 100 | pA |
| | | | $T_j = 70°C$ | | | 3 | | | 3 | nA |
| | | | $T_j = 125°C$ | | | 20 | | | | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V, V_O = \pm 10V,$<br>$R_L = 10\,k\Omega, T_A = 25°C$ | | 50 | 100 | | 25 | 100 | | V/mV |
| | | Over Temperature | | 25 | | | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V, R_L = 10\,k\Omega$ | | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +18, −17 | | ±11 | +14, −12 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10\,k\Omega$ | | 80 | 100 | | 70 | 95 | | dB |

## DC Electrical Characteristics (Note 4) (Continued)

| Symbol | Parameter | Conditions | LF441A |  |  | LF441 |  |  | Units |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 |  | 70 | 90 |  | dB |
| $I_S$ | Supply Current |  |  | 150 | 200 |  | 150 | 250 | $\mu A$ |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF441A |  |  | LF441 |  |  | Units |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| SR | Slew Rate | $V_S = \pm 15V, T_A = 25°C$ | 0.8 | 1 |  | 0.6 | 1 |  | $V/\mu s$ |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V, T_A = 25°C$ | 0.8 | 1 |  | 0.6 | 1 |  | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C, R_S = 100\Omega$, f = 1 kHz |  | 35 |  |  | 35 |  | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, f = 1 kHz |  | 0.01 |  |  | 0.01 |  | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{jA}$.

**Note 3:** The LF441A is available in both the commercial temperature range 0°C $\leq T_A \leq$ 70°C and the military temperature range −55°C $\leq T_A \leq$ 125°C. The LF441A/441 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

**Note 4:** Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF441A and for $V_S = \pm 15V$ for the LF441. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 5:** The LF441A is 100% tested to this specification.

**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

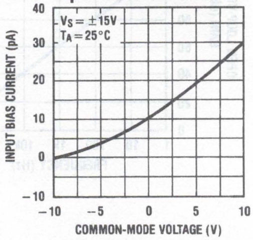
**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

**Note 8:** Refer to RETS441AX for LF441AMH military specifications.

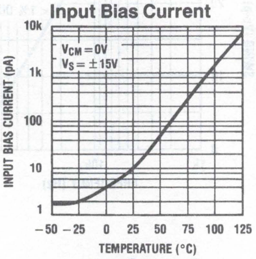
**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

## Typical Performance Characteristics

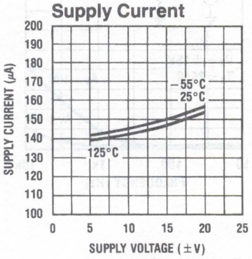
**Input Bias Current**



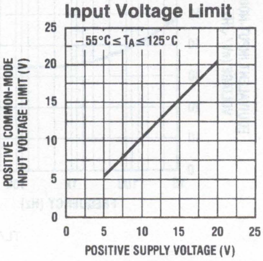
**Input Bias Current**



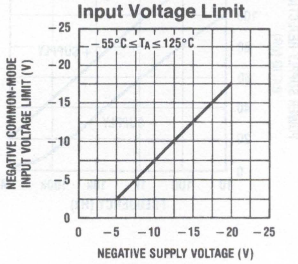
**Supply Current**



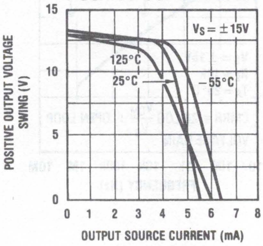
**Positive Common-Mode Input Voltage Limit**



**Negative Common-Mode Input Voltage Limit**

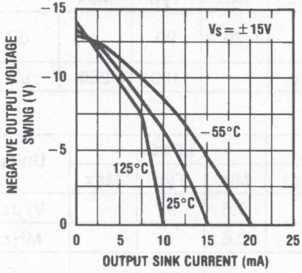


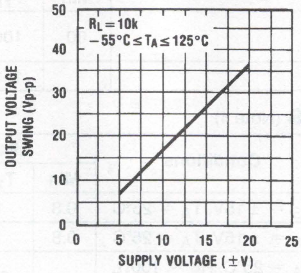
**Positive Current Limit**

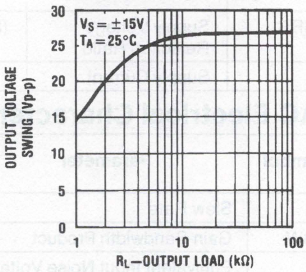


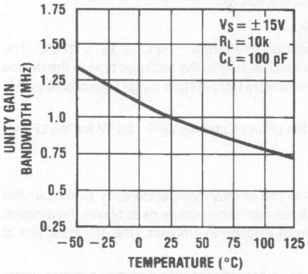
TL/H/9297–5

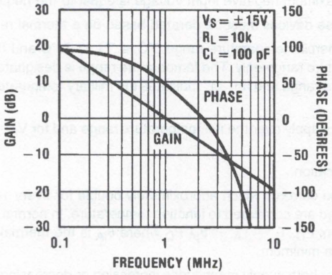
## Typical Performance Characteristics (Continued)

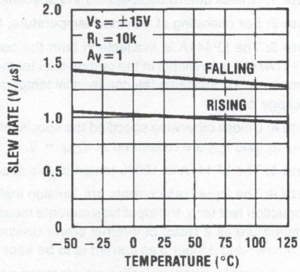

Negative Current Limit

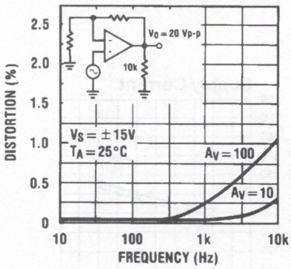

Output Voltage Swing

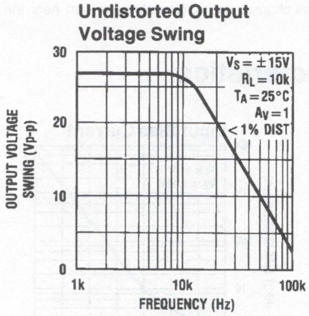

Output Voltage Swing

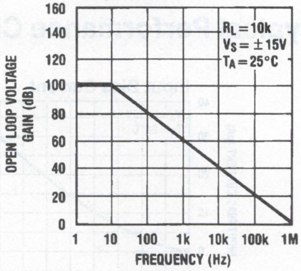

Gain Bandwidth

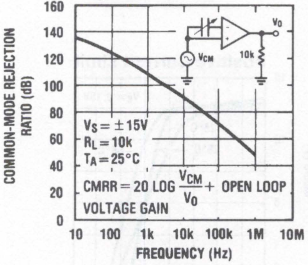

Bode Plot

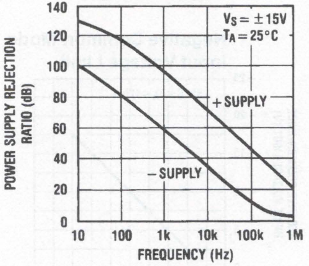

Slew Rate

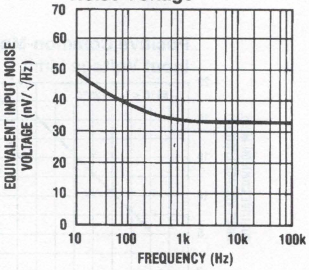

Distortion vs Frequency


Undistorted Output Voltage Swing


Open Loop Frequency Response

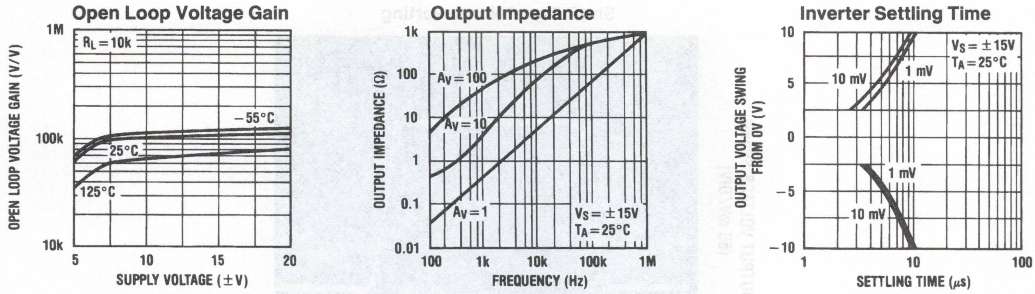

Common-Mode Rejection Ratio


Power Supply Rejection Ratio


Equivalent Input Noise Voltage

TL/H/9297-6

## Typical Performance Characteristics (Continued)

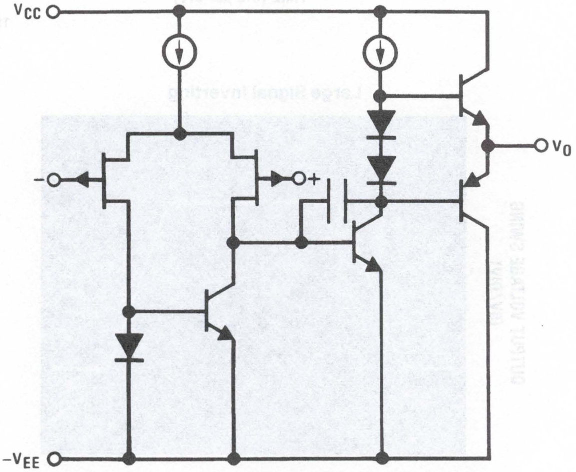

Open Loop Voltage Gain

Output Impedance

Inverter Settling Time

TL/H/9297-7

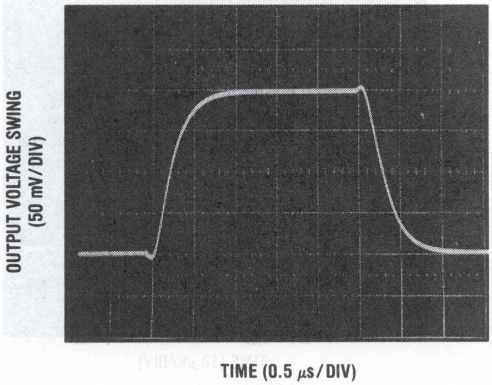
## Simplified Schematic



TL/H/9297-3

## Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

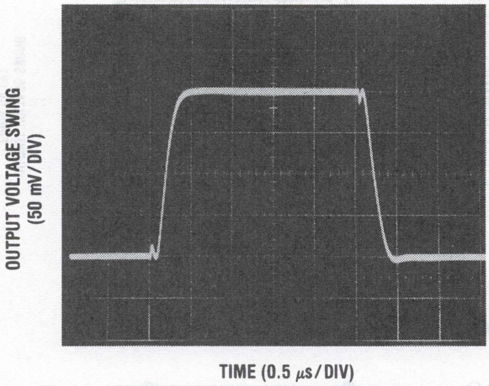
Small Signal Inverting



TL/H/9297-8

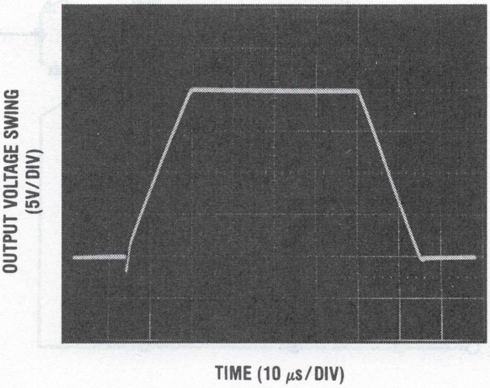
## **Pulse Response** $R_L = 10\ k\Omega$, $C_L = 10\ pF$ (Continued)

**Small Signal Non-Inverting**



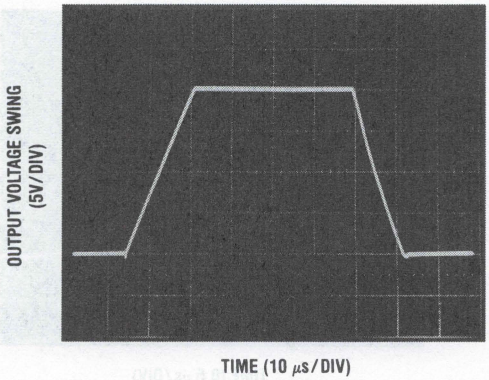
TL/H/9297–9

**Large Signal Inverting**



TL/H/9297–10

**Large Signal Non-Inverting**



TL/H/9297–11

## Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of ±3V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifier will drive a 10 kΩ load resistance to ±10V over the full temperature range.

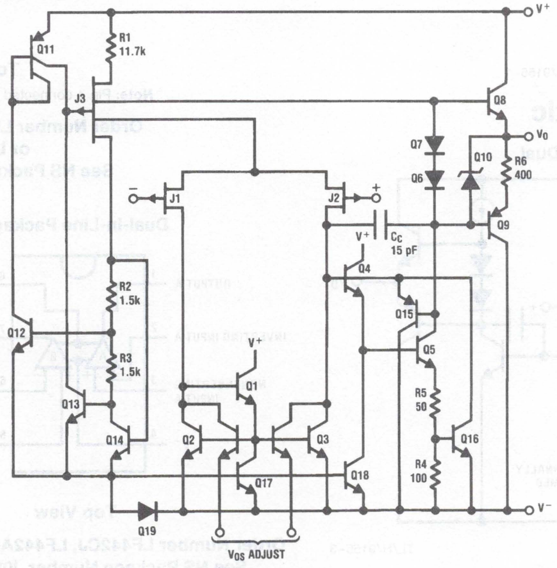
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because this amplifier is a JFET rather than MOSFET input op amp it does not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

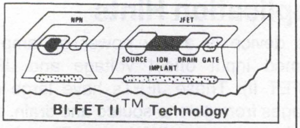
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Detailed Schematic



TL/H/9297–13

**National Semiconductor Corporation**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

## General Description

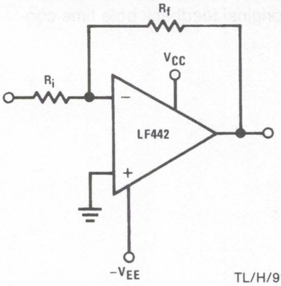
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

## Features

| | |
|---|---|
| ■ 1/10 supply current of a LM1458 | 400 μA (max) |
| ■ Low input bias current | 50 pA (max) |
| ■ Low input offset voltage | 1 mV (max) |
| ■ Low input offset voltage drift | 10 μV/°C (max) |
| ■ High gain bandwidth | 1 MHz |
| ■ High slew rate | 1 V/μs |
| ■ Low noise voltage for low power | 35 nV/$\sqrt{Hz}$ |
| ■ Low input noise current | 0.01 pA/$\sqrt{Hz}$ |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ High gain $V_O = \pm 10V$, $R_L = 10k$ | 50k (min) |

## Typical Connection


$R_f$
$V_{CC}$
$R_i$
−
+
LF442
$-V_{EE}$

TL/H/9155–1

## Ordering Information

**LF442XYZ**

X indicates electrical grade

Y indicates temperature range

"M" for military

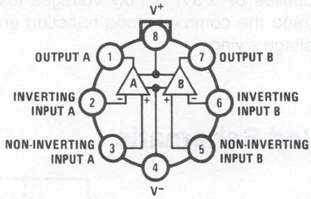
"C" for commercial

Z indicates package type

"H" or "N"

## Connection Diagrams

### Metal Can Package


V+
8
OUTPUT A
1
7
OUTPUT B
A
B
INVERTING INPUT A
2
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
5
NON-INVERTING INPUT B
4
V−

TL/H/9155–2

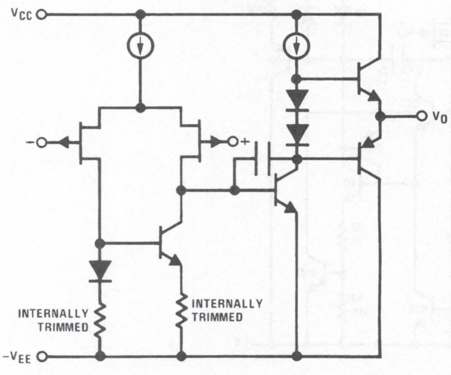
Top View

**Note:** Pin 4 connected to case

**Order Number LF442AMH, LF442ACH or LF442CH**
**See NS Package Number H08B**

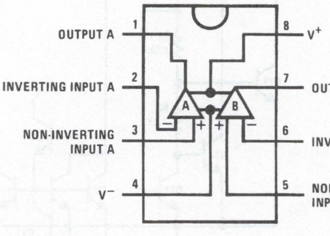
## Simplified Schematic

**½ Dual**


$V_{CC}$
−
+
$V_O$
INTERNALLY TRIMMED
INTERNALLY TRIMMED
$-V_{EE}$

TL/H/9155–3

### Dual-In-Line Package


OUTPUT A
1
8
V+
INVERTING INPUT A
2
7
OUTPUT B
A
B
NON-INVERTING INPUT A
3
6
INVERTING INPUT B
V−
4
5
NON-INVERTING INPUT B

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Top View

**Order Number LF442CJ, LF442ACN or LF442CN**
**See NS Package Number J08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 9)**

| | LF442A | LF442 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |

| | H Package | N Package |
|---|---|---|
| $T_j$ max | 150°C | 115°C |
| $\theta_{JA}$ (Typical) | | |
| (Note 3) | 83°C/W | 114°C/W |
| (Note 4) | 217°C/W | 152°C/W |
| $\theta_{JC}$ (Typical) | 21°C/W | |
| Operating Temperature Range | (Note 4) | (Note 4) |
| Storage Temperature Range | $-65°C \leq T_A \leq 150°C$ | $-65°C \leq T_A \leq 150°C$ |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 6)

| Symbol | Parameter | Conditions | | LF442A | | | LF442 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega, T_A = 25°C$ | | | 0.5 | 1.0 | | 1.0 | 5.0 | mV |
| | | Over Temperature | | | | | | | 7.5 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | | 7 | 10 | | 7 | | $\mu V/°C$ |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 6 and 7) | $T_j = 25°C$ | | 5 | 25 | | 5 | 50 | pA |
| | | | $T_j = 70°C$ | | | 1.5 | | | 1.5 | nA |
| | | | $T_j = 125°C$ | | | 10 | | | | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 6 and 7) | $T_j = 25°C$ | | 10 | 50 | | 10 | 100 | pA |
| | | | $T_j = 70°C$ | | | 3 | | | 3 | nA |
| | | | $T_j = 125°C$ | | | 20 | | | | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | $\Omega$ |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V, V_O = \pm 10V, R_L = 10\ k\Omega, T_A = 25°C$ | | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | | 25 | 200 | | 15 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V, R_L = 10\ k\Omega$ | | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +18<br>−17 | | ±11 | +14<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\ k\Omega$ | | 80 | 100 | | 70 | 95 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 8) | | 80 | 100 | | 70 | 90 | | dB |
| $I_S$ | Supply Current | | | | 300 | 400 | | 400 | 500 | $\mu A$ |

## AC Electrical Characteristics (Note 6)

| Symbol | Parameter | Conditions | LF442A | | | LF442 | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred) | | −120 | | | −120 | | dB |
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | 0.8 | 1 | | 0.6 | 1 | | V/µs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | 0.8 | 1 | | 0.6 | 1 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz | | 35 | | | 35 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, f = 1 kHz | | 0.01 | | | 0.01 | | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** The value given is in 400 linear feet/min air flow.

**Note 4:** The value given is in static air.

**Note 5:** These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

**Note 6:** Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

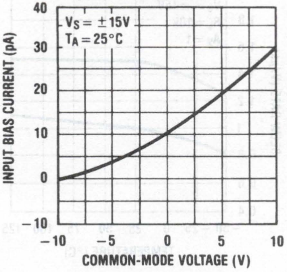
**Note 7:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 8:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

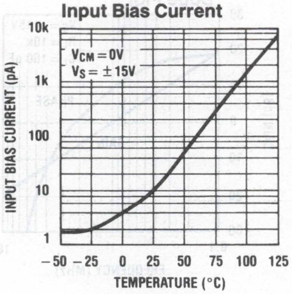
**Note 9:** Refer to RETS442AX for LF442AMH military specifications and to RETS442X for LF442MH military specifications.

## Typical Performance Characteristics

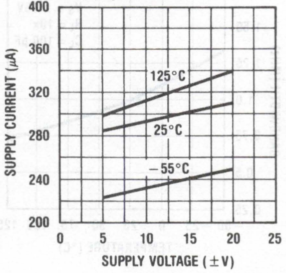
Input Bias Current



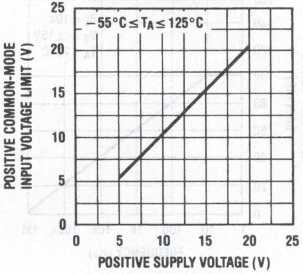
Input Bias Current



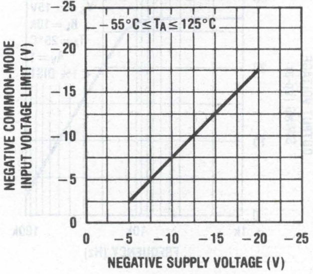
Supply Current



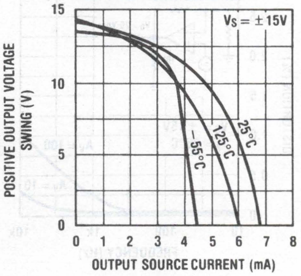
Positive Common-Mode Input Voltage Limit



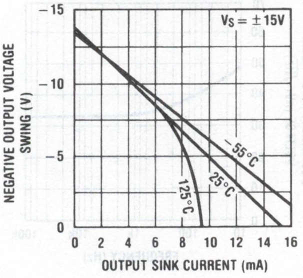
Negative Common-Mode Input Voltage Limit



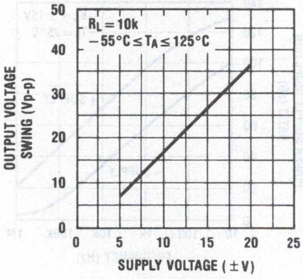
Positive Current Limit



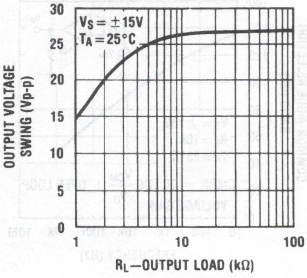
Negative Current Limit



Output Voltage Swing



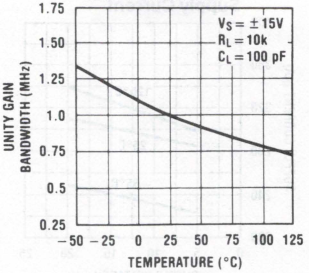
Output Voltage Swing



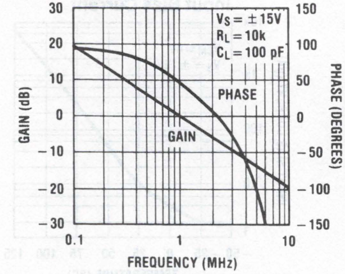
TL/H/9155–5

## Typical Performance Characteristics (Continued)

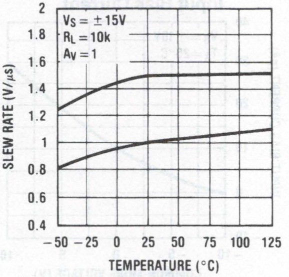
**Gain Bandwidth**



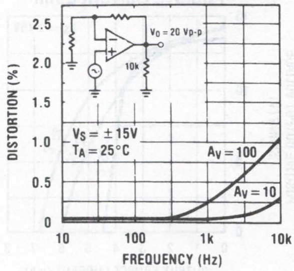
**Bode Plot**



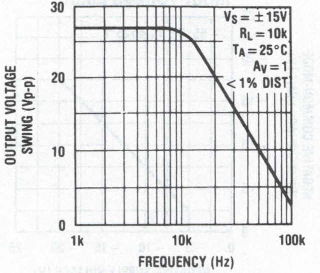
**Slew Rate**



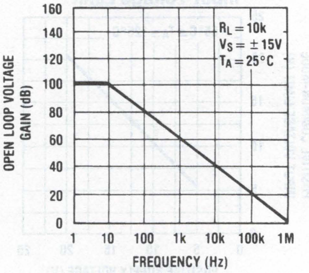
**Distortion vs Frequency**



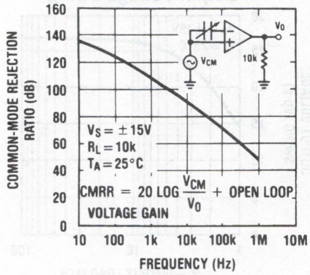
**Undistorted Output Voltage Swing**



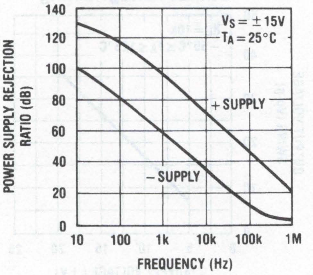
**Open Loop Frequency Response**



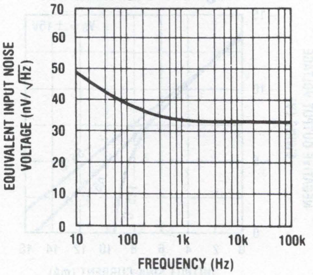
**Common-Mode Rejection Ratio**



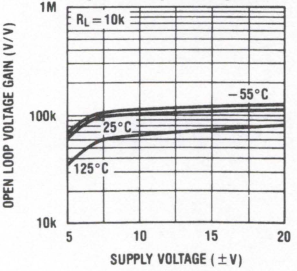
**Power Supply Rejection Ratio**



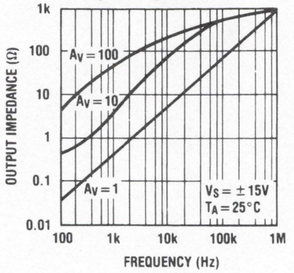
**Equivalent Input Noise Voltage**



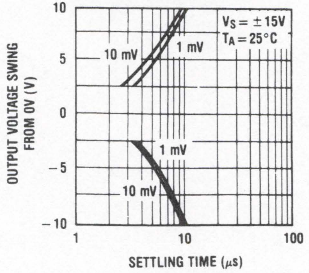
**Open Loop Voltage Gain**



**Output Impedance**



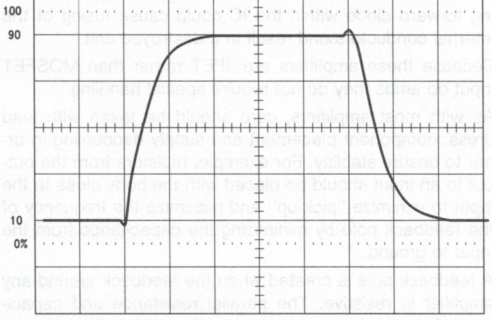
**Inverter Settling Time**



TL/H/9155–6

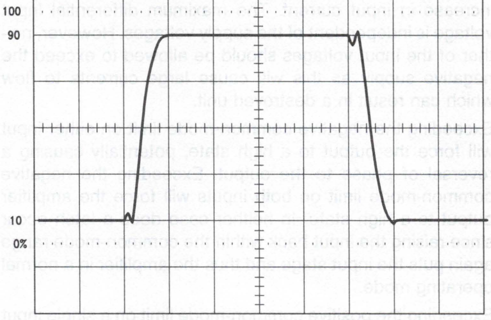
## Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

### Small Signal Inverting



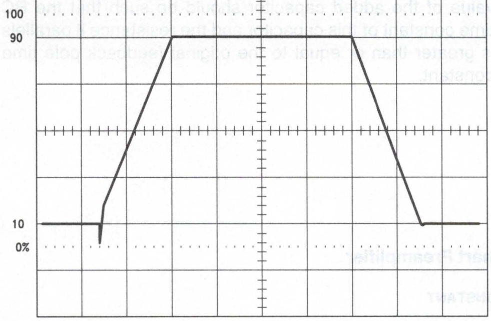
TL/H/9155–7

### Small Signal Non-Inverting



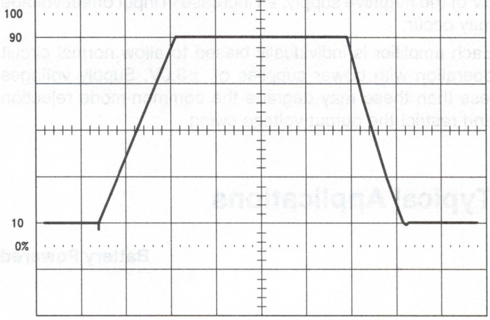
TL/H/9155–8

### Large Signal Inverting



TL/H/9155–9

### Large Signal Non-Inverting



TL/H/9155–10

# Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

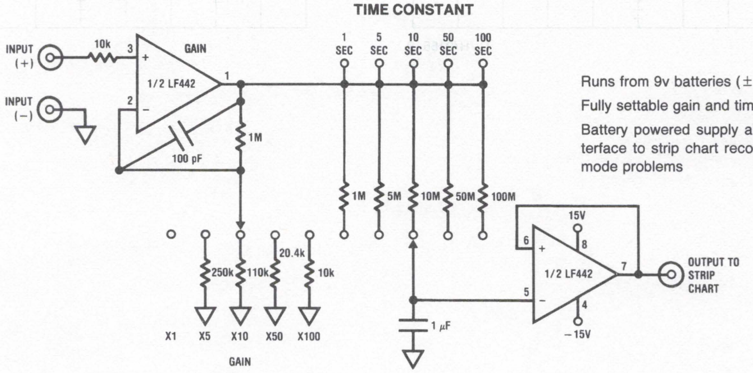
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

# Typical Applications

**Battery Powered Strip Chart Preamplifier**



Runs from 9v batteries (±9V supplies)

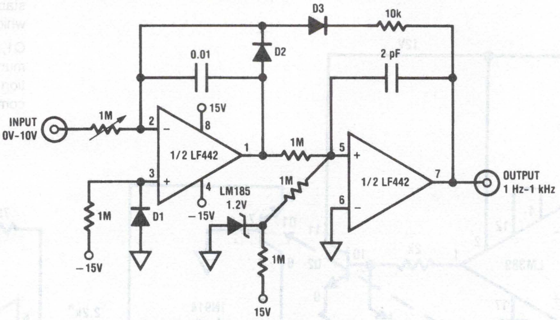
Fully settable gain and time constant

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

TL/H/9155-11

## Typical Applications (Continued)

### "No FET" Low Power V → F Converter


D3
10k
D2
0.01
2 pF
15V
8
INPUT
0V-10V
1M
2
1/2 LF442
1
1M
5
3
4
LM185
1.2V
1M
1/2 LF442
7
OUTPUT
1 Hz-1 kHz
6
1M
D1
−15V
−15V
1M
15V

Trim 1M pot for 1 kHz full-scale output

15 mW power drain

No integrator reset FET required

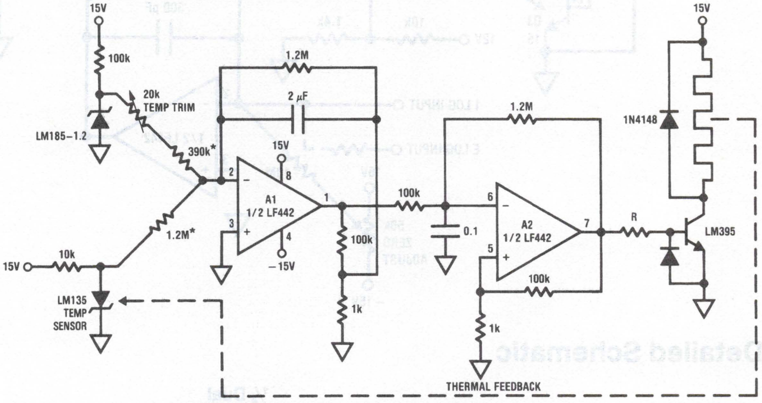
Mount D1 and D2 in close proximity

1% linearity to 1 kHz

TL/H/9155-12

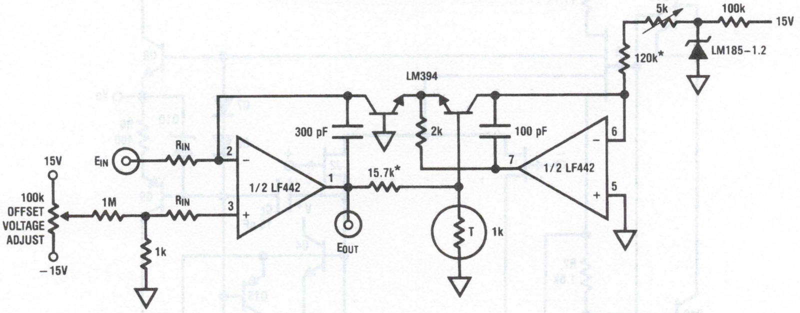
### High Efficiency Crystal Oven Controller

- $T_{control}$ = 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor


15V
100k
1.2M
20k
TEMP TRIM
2 µF
LM185-1.2
390k*
15V
2
8
A1
1/2 LF442
1
3
4
−15V
1.2M*
15V
10k
LM135
TEMP
SENSOR
100k
100k
1k
0.1
1.2M
6
A2
1/2 LF442
7
5
100k
1k
THERMAL FEEDBACK
R
15V
1N4148
LM395

TL/H/9155-13

### Conventional Log Amplifier


5k
100k
15V
LM185-1.2
120k*
LM394
300 pF
2k
100 pF
RIN
2
1/2 LF442
1
15.7k*
7
1/2 LF442
6
5
EIN
15V
100k
OFFSET
VOLTAGE
ADJUST
1M
RIN
3
−15V
1k
EOUT
T
1k

TL/H/9155-14

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

$R_T$ = Tel Labs type Q81

Trim 5k for 10 µA through the 5k–120k combination

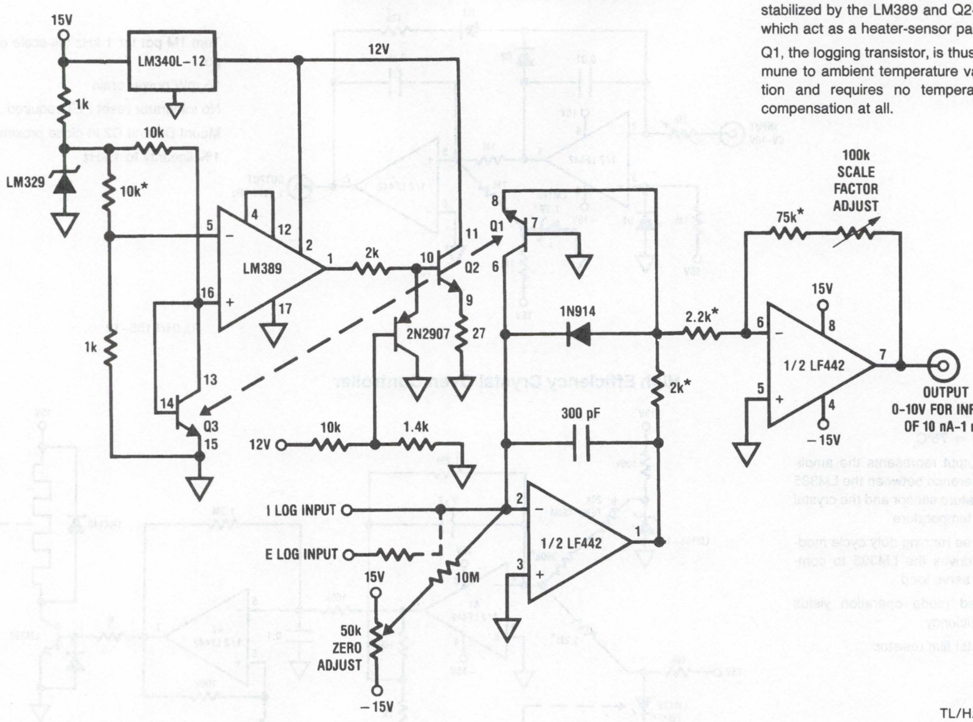
*1% film resistor

# Typical Applications (Continued)

## Unconventional Log Amplifier

Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.

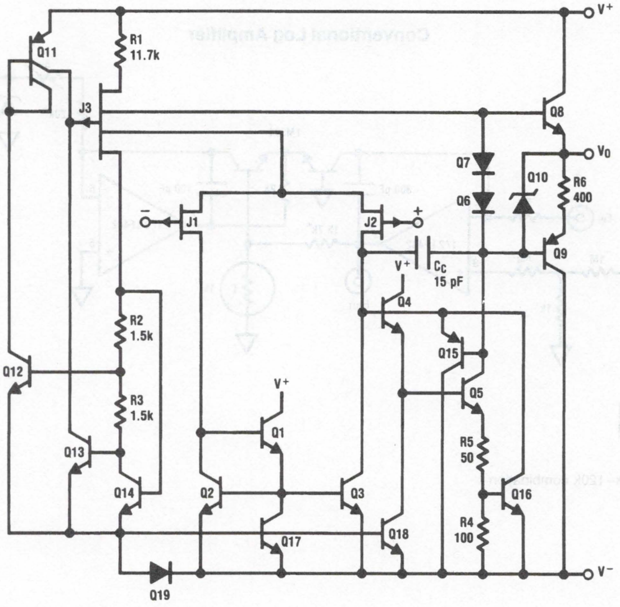
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.


15V
LM340L-12
12V
1k
10k
LM329
10k*
LM389
4
12
5
2
1
2k
10
11
Q1
Q2
6
8
7
16
17
9
2N2907
27
1k
13
14
Q3
15
10k
1.4k
12V
1N914
2.2k*
2k*
300 pF
100k SCALE FACTOR ADJUST
75k*
15V
6
8
1/2 LF442
7
5
4
−15V
OUTPUT 0-10V FOR INPUTS OF 10 nA-1 mA
I LOG INPUT
E LOG INPUT
2
1
3
1/2 LF442
10M
15V
50k ZERO ADJUST
−15V

TL/H/9155-15

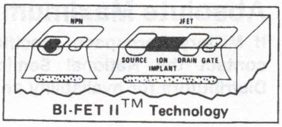
# Detailed Schematic

## ½ Dual


V+
Q11
R1 11.7k
J3
Q8
Vo
Q7
Q6
Q10
R6 400
J1
J2
Cc 15 pF
V+
Q9
Q4
R2 1.5k
Q15
Q12
Q5
R3 1.5k
V+
Q1
Q13
R5 50
Q14
Q2
Q3
Q16
Q17
Q18
R4 100
Q19
V−

TL/H/9155-16

**National Semiconductor Corporation**



# LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

## General Description

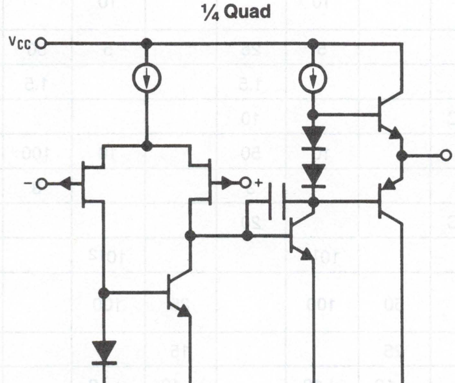
The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

## Features

| | |
|---|---|
| ■ ¼ supply current of a LM148 | 200 μA/Amplifier (max) |
| ■ Low input bias current | 50 pA (max) |
| ■ High gain bandwidth | 1 MHz |
| ■ High slew rate | 1 V/μs |
| ■ Low noise voltage for low power | 35 nV/$\sqrt{\text{Hz}}$ |
| ■ Low input noise current | 0.01 pA/$\sqrt{\text{Hz}}$ |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ High gain $V_O = \pm 10V$, $R_L = 10k$ | 50k (min) |

## Simplified Schematic

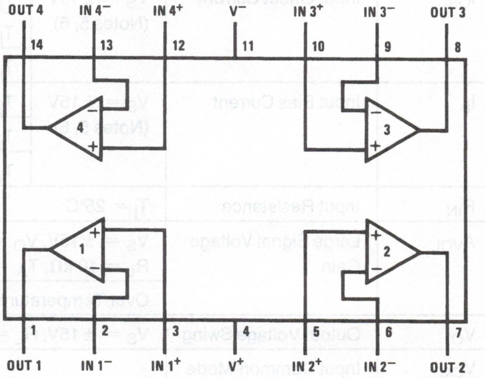


TL/H/9156-1

## Connection Diagram

**LF444AMD/LF444CD/LF444ACN/LF444CN**

**Dual-In-Line Package**



TL/H/9156-2

**Top View**

**Order Number LF444AMD, LF444CD, LF444CJ, LF444CM, LF444CWM, LF444ACN or LF444CN**

**See NS Package Number D14E, J14A, M14A, M14B or N14A**

## Ordering Information

**LF444XYZ**

**X** indicates electrical grade

**Y** indicates temperature range

"M" for military, "C" for commercial

**Z** indicates package type "D", "M" or "N"

2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | LF444A | LF444 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |

| | D Package | N Package |
|---|---|---|
| Power Dissipation (Notes 3 and 9) | 900 mW | 670 mW |
| $T_j$ max | 150°C | 115°C |
| $\theta_{jA}$ (Typical) | 100°C/W | 85°C/W |

| | D Package | N Package |
|---|---|---|
| Operating Temperature Range | (Note 4) | (Note 4) |
| Storage Temperature Range | $-65°C \le T_A \le 150°C$ | |
| Lead Temperature DIP (Soldering, 10 sec.) | 260°C | 260°C |

ESD rating to be determined.

| Soldering Information | | |
|---|---|---|
| Dual-In-Line Package (Soldering, 10 sec.) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 sec.) | 215°C | 215°C |
| Infrared (15 sec.) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | | LF444A | | | LF444 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10k$, $T_A = 25°C$ | | | 2 | 5 | | 3 | 10 | mV |
| | | $0°C \le T_A \le +70°C$ | | | | 6.5 | | | 12 | mV |
| | | $-55°C \le T_A \le +125°C$ | | | | 8 | | | | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | | 10 | | | 10 | | μV/°C |
| $I_{OS}$ | Input Offset Current | $V_S = \pm 15V$ (Notes 5, 6) | $T_j = 25°C$ | | 5 | 25 | | 5 | 50 | pA |
| | | | $T_j = 70°C$ | | | 1.5 | | | 1.5 | nA |
| | | | $T_j = 125°C$ | | | 10 | | | | nA |
| $I_B$ | Input Bias Current | $V_S = \pm 15V$ (Notes 5, 6) | $T_j = 25°C$ | | 10 | 50 | | 10 | 100 | pA |
| | | | $T_j = 70°C$ | | | 3 | | | 3 | nA |
| | | | $T_j = 125°C$ | | | 20 | | | | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $V_O = \pm 10V$<br>$R_L = 10\ k\Omega$, $T_A = 25°C$ | | 50 | 100 | | 25 | 100 | | V/mV |
| | | Over Temperature | | 25 | | | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | | ±12 | ±13 | | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | ±16 | +18<br>−17 | | ±11 | +14<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10\ k\Omega$ | | 80 | 100 | | 70 | 95 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | | 80 | 100 | | 70 | 90 | | dB |
| $I_S$ | Supply Current | | | | 0.6 | 0.8 | | 0.8 | 1.0 | mA |

## AC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF444A |  |  | LF444 |  |  | Units |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
|  | Amplifier-to-Amplifier Coupling |  |  | −120 |  |  | −120 |  | dB |
| SR | Slew Rate | $V_S = \pm 15V, T_A = 25°C$ |  | 1 |  |  | 1 |  | V/µs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V, T_A = 25°C$ |  | 1 |  |  | 1 |  | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C, R_S = 100\Omega$, f = 1 kHz |  | 35 |  |  | 35 |  | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_A = 25°C$, f = 1 kHz |  | 0.01 |  |  | 0.01 |  | $pA/\sqrt{Hz}$ |

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_{jA}$.

**Note 4:** The LF444A is available in both the commercial temperature range 0°C ≤ $T_A$ ≤ 70°C and the military temperature range −55°C ≤ $T_A$ ≤ 125°C. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

**Note 5:** Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

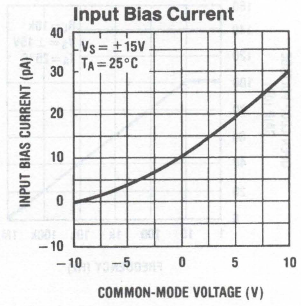
**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA}P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

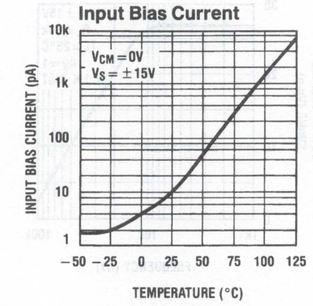
**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

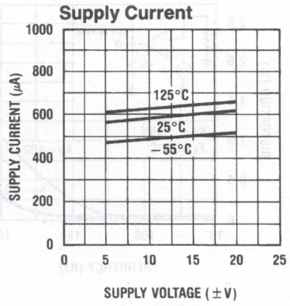
**Note 8:** Refer to RETS444AX for LF444AMD military specifications.

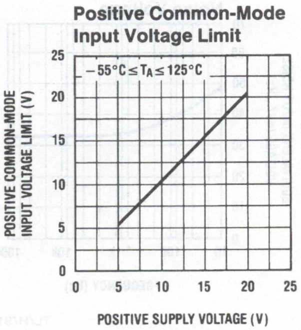
**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

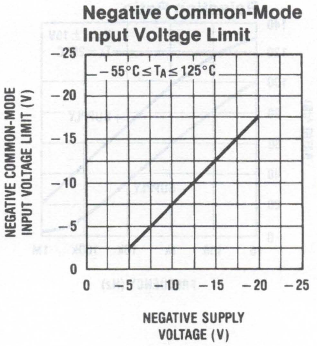
## Typical Performance Characteristics

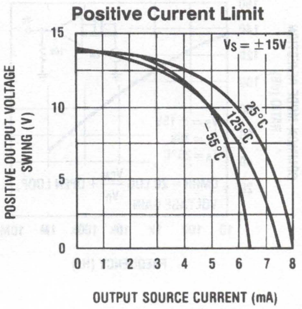

Input Bias Current


Input Bias Current


Supply Current


Positive Common-Mode Input Voltage Limit

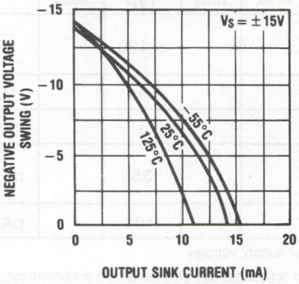

Negative Common-Mode Input Voltage Limit


Positive Current Limit

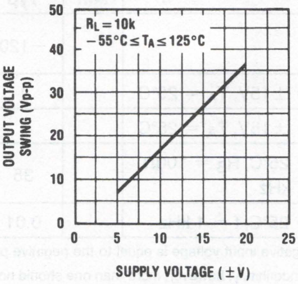
TL/H/9156–3

## Typical Performance Characteristics (Continued)

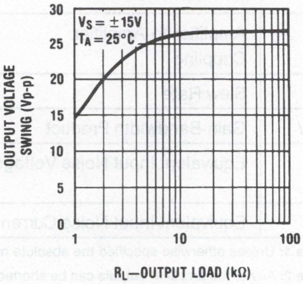
### Negative Current Limit



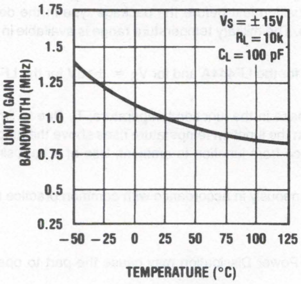
### Output Voltage Swing



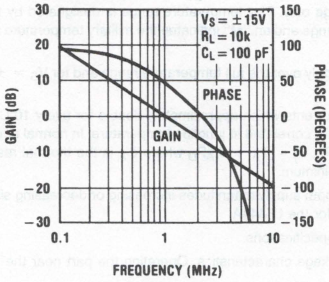
### Output Voltage Swing



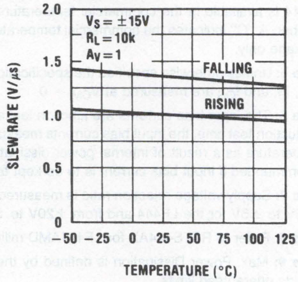
### Gain Bandwidth



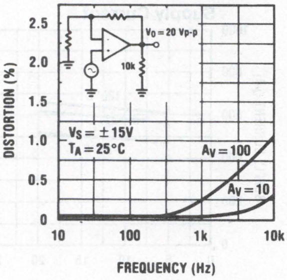
### Bode Plot



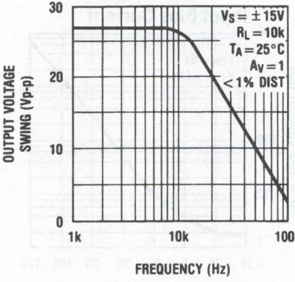
### Slew Rate



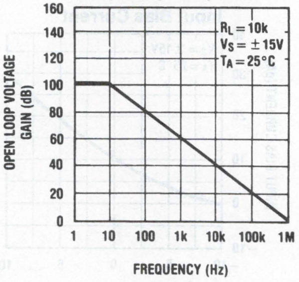
### Distortion vs Frequency



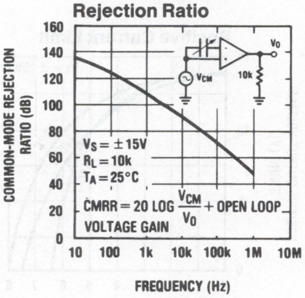
### Undistorted Output Voltage Swing



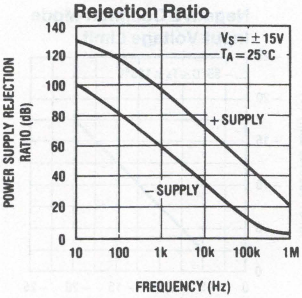
### Open Loop Frequency Response



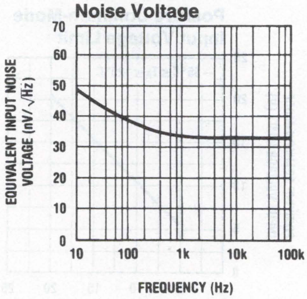
### Common-Mode Rejection Ratio



### Power Supply Rejection Ratio

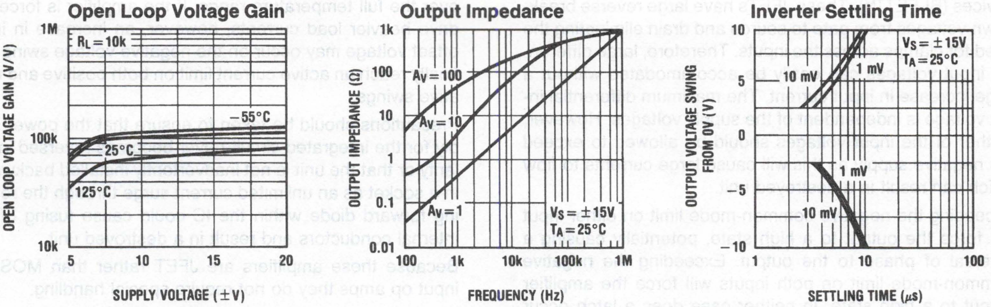


### Equivalent Input Noise Voltage



TL/H/9156–4

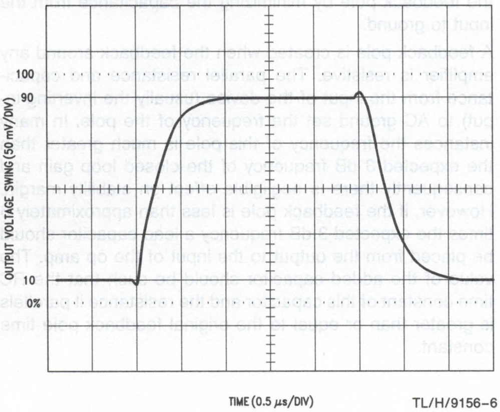
## Typical Performance Characteristics (Continued)



TL/H/9156–5

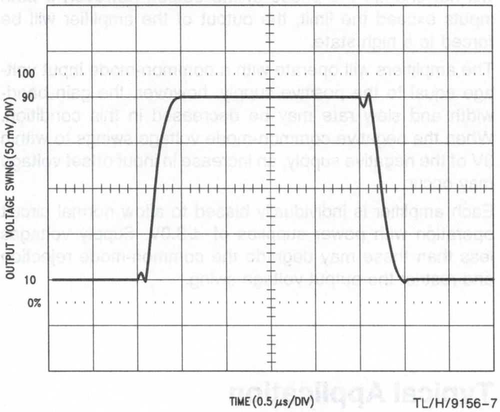
## Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

### Small Signal Inverting



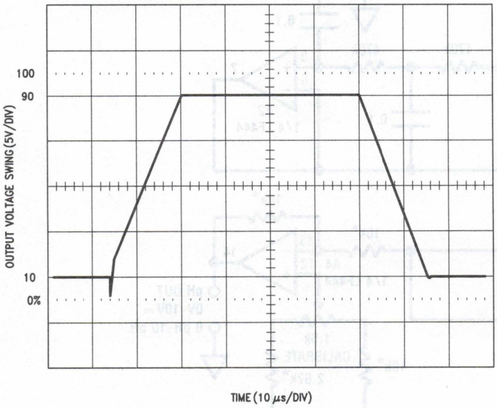
TL/H/9156–6

### Small Signal Non-Inverting



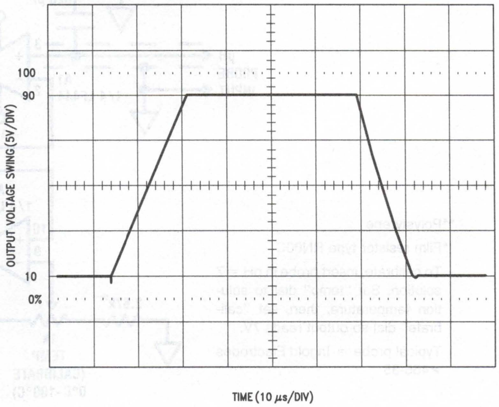
TL/H/9156–7

### Large Signal Inverting



TL/H/9156–8

### Large Signal Non-Inverting



TL/H/9156–9

## Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

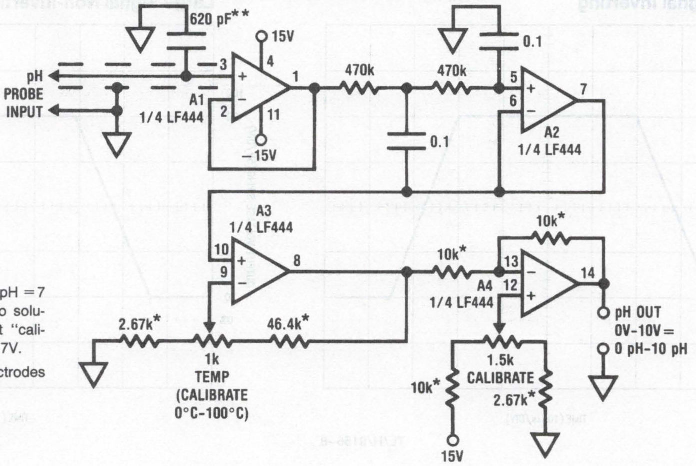
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Application

**pH Probe Amplifier/Temperature Compensator**



**Polystyrene

*Film resistor type RN60C

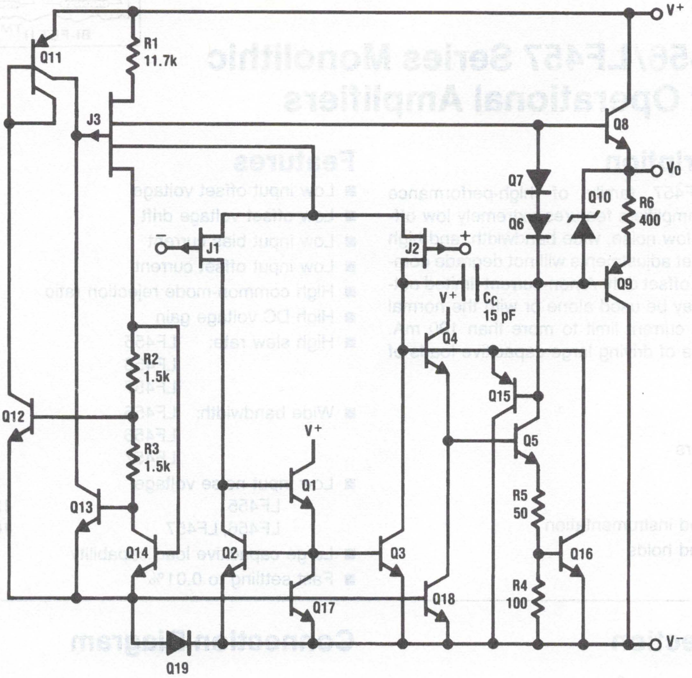
To calibrate, insert probe in pH = 7 solution. Set "temp" dial to solution temperature, then, set "calibrate" dial so output reads 7V.

Typical probe = Ingold Electrodes #465-35

TL/H/9156–10

## Detailed Schematic

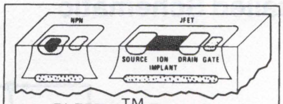
¼ Quad


V+
R1
11.7k
Q11
J3
Q8
V0
Q7
Q10
R6
400
Q6
−
J1
J2
+
V+
Cc
15 pF
Q9
Q4
R2
1.5k
Q15
Q12
V+
Q5
R3
1.5k
Q1
R5
50
Q13
Q14
Q2
Q3
Q16
R4
100
Q18
Q17
Q19
V−

TL/H/9156–11

National
Semiconductor
Corporation

**ADVANCED INFORMATION**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE

BI-FET II™ Technology

# LF455/LF456/LF457 Series Monolithic JFET Input Operational Amplifiers

## General Description

The LF455/LF456/LF457 family of high-performance Bi-FET™ operational amplifiers features extremely low offset voltage, high gain, low noise, wide bandwidth, and high slew rate. External offset adjustments will not degrade common-mode rejection or offset drift. A non-current-limited output is provided, and may be used alone or with the normal output to increase the current limit to more than 100 mA. Either output is capable of driving large capacitive loads of up to 10,000 pF.

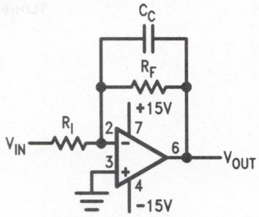
## Applications

- DAC output amplifiers
- Precision Buffers
- Fast Integrators
- Precision, high speed instrumentation
- Precision sample and holds

## Features

| | | |
|---|---|---|
| ■ Low input offset voltage | | 250 μV |
| ■ Low offset voltage drift | | 3 μV/°C |
| ■ Low input bias current | | 50 pA |
| ■ Low input offset current | | 10 pA |
| ■ High common-mode rejection ratio | | 100 dB |
| ■ High DC voltage gain | | 106 dB |
| ■ High slew rate: | LF455 | 5V/μs |
| | LF456 | 12V/μs |
| | LF457 | 50V/μs |
| ■ Wide bandwidth: | LF455 | 3 MHz |
| | LF456 | 5 MHz |
| | LF457 | 20 MHz |
| ■ Low input noise voltage: | | |
| LF455 | | 12nV/√Hz @ 1kHz |
| LF456, LF457 | | 10nV/√Hz @ 1kHz |
| ■ Large capacitive load capability | | 10,000 pF |
| ■ Fast settling to 0.01% | | 1.5 μs |

## Typical Connection


$C_C$
$R_F$
+15V
$R_I$
2
7
6
3
4
$V_{IN}$
$V_{OUT}$
−15V

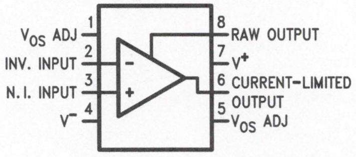
TL/H/9225–1

$\frac{R_f}{R_i}$ must be greater than 4 for the LF457.

LF455 and LF456 are unity gain stable.

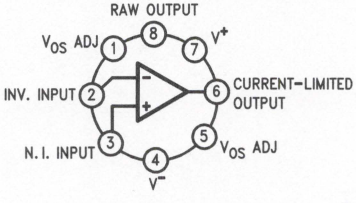
## Connection Diagram

**Dual-In-Line Package (N)**


$V_{OS}$ ADJ
INV. INPUT
N. I. INPUT
$V^-$
1
2
3
4
8
7
6
5
RAW OUTPUT
$V^+$
CURRENT–LIMITED OUTPUT
$V_{OS}$ ADJ

TL/H/9225–2

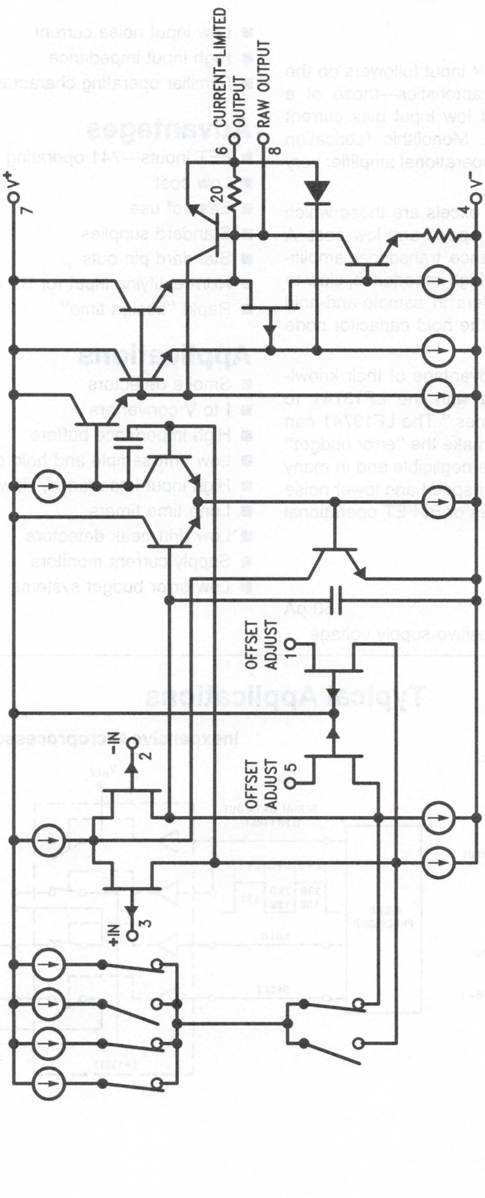
**Metal Can Package (H)**


RAW OUTPUT
8
$V^+$
7
$V_{OS}$ ADJ
1
INV. INPUT
2
CURRENT–LIMITED OUTPUT
6
N. I. INPUT
3
4
$V^-$
5
$V_{OS}$ ADJ

TL/H/9225–3

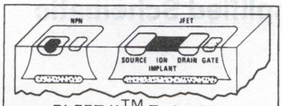
**Order Number LF455/LF456/LF457**
**See NS Package H08A or N08E**

## Simplified Schematic


V+
7
6
CURRENT-LIMITED OUTPUT
8
RAW OUTPUT
20
V−
4
OFFSET ADJUST
1
OFFSET ADJUST
5
−IN
2
+IN
3

TL/H/9225-4

**National Semiconductor Corporation**



BI-FET II™ Technology

# LF13741
# Monolithic JFET Input Operational Amplifier

## General Description

The LF13741 is a 741 with BI-FET™ input followers on the same die. Familiar operating characteristics—those of a 741—with the added advantage of low input bias current make the LF13741 easy to use. Monolithic fabrication makes this "drop-in-replacement" operational amplifier very economical.

Applications in which the LF13741 excels are those which require low bias current, moderate speed and low cost. A few examples include high impedance transducer amplifiers, photocell amplifiers, buffers for high impedance, slow to moderate speed sources and buffers in sample-and-hold type systems where leakage from the hold capacitor node must be kept to a minimum.

Systems designers can take full advantage of their knowledge of the 741 when designing with the LF13741 to achieve extremely rapid "design times." The LF13741 can also be used in existing sockets to make the "error budget" for input bias and/or offset currents negligible and in many cases eliminate trimming. For higher speed and lower noise use the LF155, LF156, LF157 series of BI-FET operational amplifiers.

## Features

| | |
|---|---|
| ■ Low input bias current | 50 pA |
| ■ Input common-mode range to positive supply voltage | |
| ■ Low input noise current | 0.01 pA/$\sqrt{\text{Hz}}$ |
| ■ High input impedance | $5 \times 10^{11}\Omega$ |
| ■ Familiar operating characteristics | |

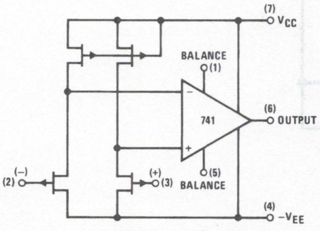
## Advantages

- FET inputs—741 operating characteristics
- Low cost
- Ease of use
- Standard supplies
- Standard pin outs
- Non-rectifying input for RF environment
- Rapid "design time"

## Applications

- Smoke detectors
- I to V converters
- High impedance buffers
- Low drift sample and hold circuits
- High input impedance, slow comparators
- Long time timers
- Low drift peak detectors
- Supply current monitors
- Low error budget systems

## Simplified Schematic

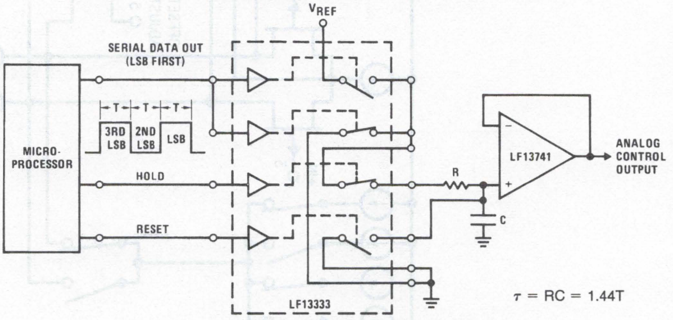


All on one die.

TL/H/9296-1

## Typical Applications

**Inexpensive Microprocessor D/A**



TL/H/9296-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Operating Temperature Range | 0°C to +70°C |
| $T_{j(MAX)}$ | 100°C |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 3) | ±16V |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |

| | H Package | N Package |
|---|---|---|
| $\theta_{jA}$ (Typical) | | |
| (Note 1) | 88°C/W | 163°C/W |
| (Note 2) | 232°C/W | 218°C/W |
| $\theta_{jC}$ (Typical) | 25°C/W | |
| Metal Package Lead Temperature (Soldering, 10 sec.) | | 300°C |
| Plastic Package (Soldering, 4 sec.) | | 260°C |
| ESD rating to be determined. | | |

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega$, $T_A = 25°C$ | | 5 | 15 | mV |
| | | Over Temperature | | | 20 | |
| | Voltage Offset Adjustment Range | | 10 | | | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | 10 | | $\mu V/°C$ |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$ (Notes 4, 5) | | 10 | 50 | pA |
| | | $T_j \le 70°C$ | | | 2 | nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$ (Notes 4, 5) | | 50 | 200 | pA |
| | | $T_j \le 70°C$ | | 1.6 | 8 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $5 \times 10^{11}$ | | $\Omega$ |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 2\ k\Omega$ | 25 | 100 | | V/mV |
| | | Over Temperature | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | ±12 | ±13 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15.1<br>−12 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10\ k\Omega$ | 70 | 90 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 77 | 96 | | dB |
| $I_S$ | Supply Current | | | 2 | 4 | mA |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | $V_S = \pm15V, T_A = 25°C$ | | 0.5 | | V/μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm15V, T_A = 25°C$ | | 1.0 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C, R_S = 100\Omega$<br>f = 100 Hz<br>f = 1000 Hz | | <br>50<br>37 | | <br>$nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_j = 25°C$<br>f = 100 Hz<br>f = 1000 Hz | | <br>0.01<br>0.01 | | <br>$pA/\sqrt{Hz}$<br>$pA/\sqrt{Hz}$ |

**Note 1:** The value given is in 400 Linear Feet/Min air flow.

**Note 2:** The value given is in static air.

**Note 3:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

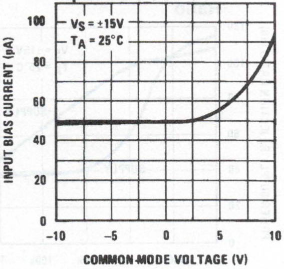
**Note 4:** These specifications apply for $V_S = \pm15V$ and $0°C \leq T_A \leq +70°C$. $V_{OS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

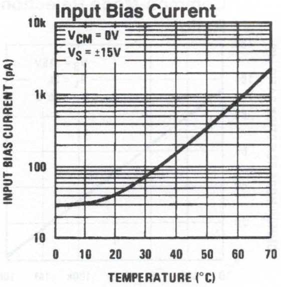
**Note 6:** Supply Voltage Rejection Ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm10V$ to $\pm15V$.

# Typical Performance Characteristics

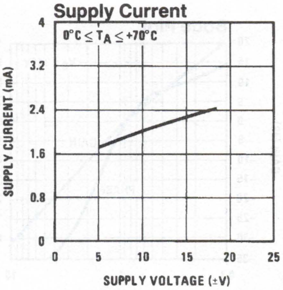
### Input Bias Current



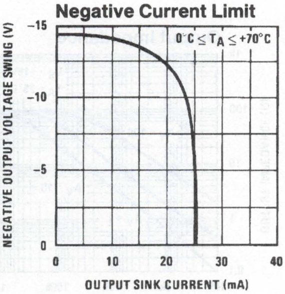
### Input Bias Current



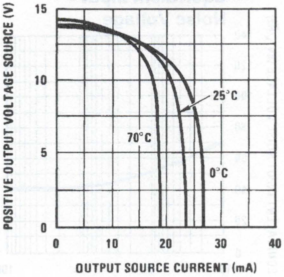
### Supply Current



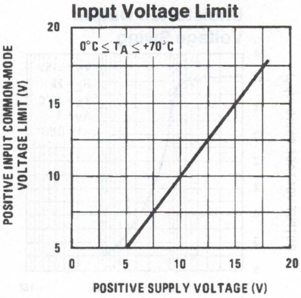
### Negative Current Limit



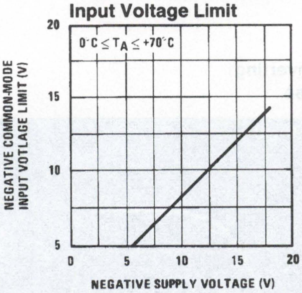
### Positive Current Limit



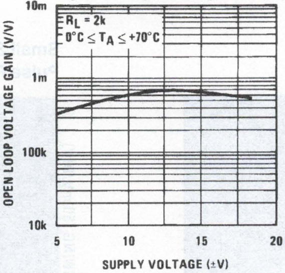
### Positive Common-Mode Input Voltage Limit



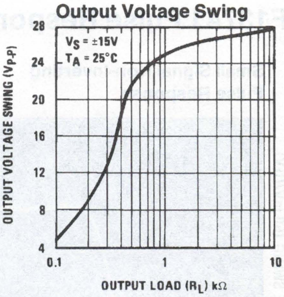
### Negative Common-Mode Input Voltage Limit



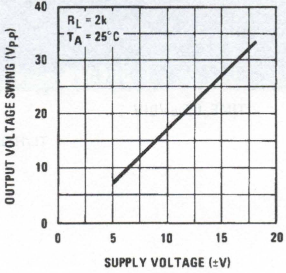
### Open Loop Voltage Gain (V/V)



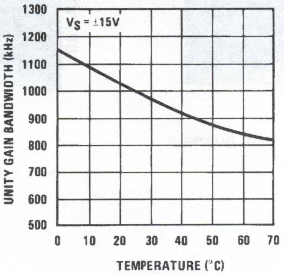
### Output Voltage Swing



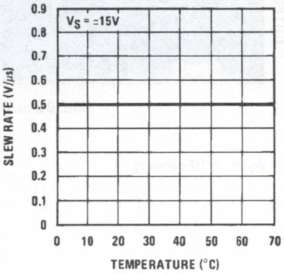
### Voltage Swing



### Gain Bandwidth



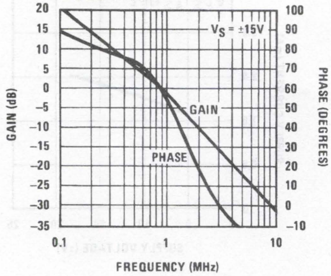
### Slew Rate



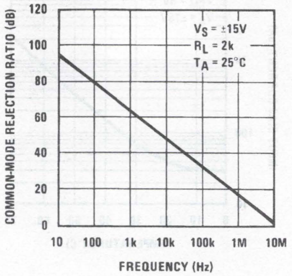
TL/H/9296–3

## Typical Performance Characteristics (Continued)

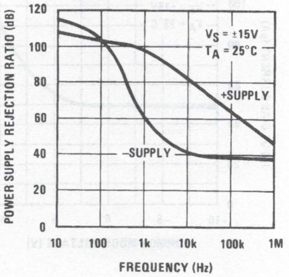
### Bode Plot



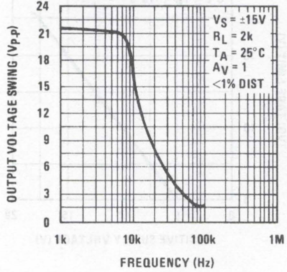
### Common-Mode Rejection Ratio



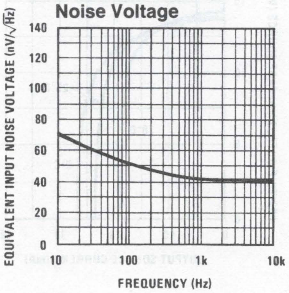
### Power Supply Rejection Ratio



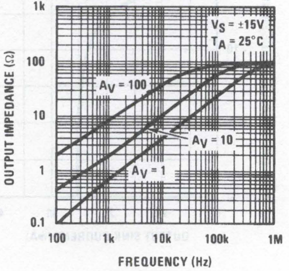
### Undistorted Output Voltage Swing



### Equivalent Input Noise Voltage



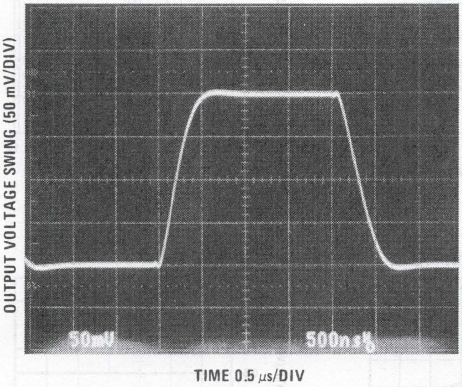
### Output Impedance



TL/H/9296–4

## LF13741 Pulse Responses

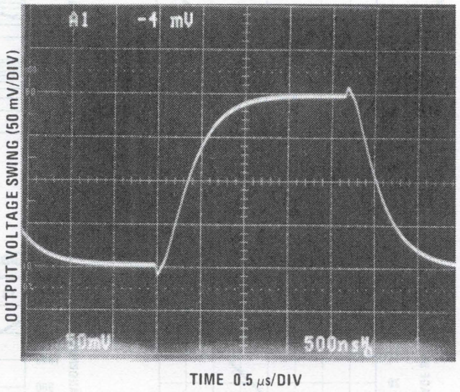
### Small Signal Non-Inverting Pulse Response



TL/H/9296–5

$A_V$ = +1(Follower)

### Small Signal Inverting Pulse Response



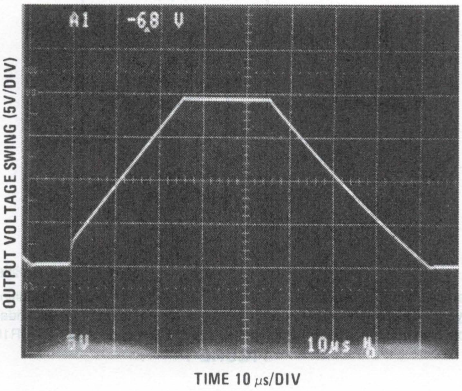
TL/H/9296–6

$A_V$ = −1(Inverter)

## Typical Performance Characteristics (Continued)

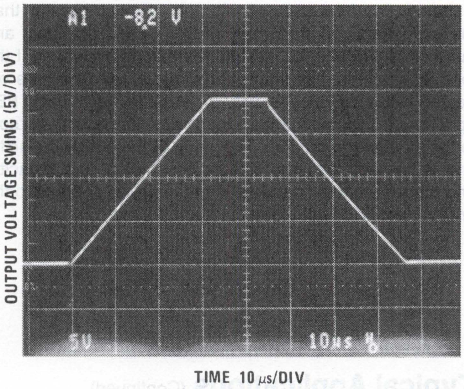
## LF13741 Pulse Responses (Continued)

**Large Signal Non-Inverting Pulse Response**



TL/H/9296-7

**Large Signal Inverting Pulse Response**



TL/H/9296-8

Vertical: Output Voltage Swing
Horizontal = Time

## Application Hints

### GENERAL CHARACTERISTICS

The LF13741 makes the job of converting from a bipolar to an FET input op amp easy. As a systems designer you are probably very familiar with the operating characteristics of a 741 op amp. In fact, many of you have used 741s with FET input followers—that's just what the LF13741 is, but it's all on a single die.

When you need a low cost, reliable, well known op amp with low input currents and moderate speed, use an LF13741.

### DIFFERENTIAL INPUTS

You don't have to use clamps across the inputs for differential input voltages of less than 40V. The input JFETs of the LF13741, in addition to being well matched, have large reverse breakdown voltages from gate to source and drain.

### POSITIVE INPUT COMMON-MODE VOLTAGE LIMIT

With the LF13741 (unlike the normal 741) you can take both inputs above the positive supply voltage by more than 0.1V before the amplifier ceases to function. This feature enables you to use the LF13741 to monitor and/or limit the current from the same supply used to power it (see typical applications).

If you exceed the positive common-mode voltage limit on only one input, the output phase will remain correct. When you exceed the limit on both inputs, the output phase is unpredictable.

### NEGATIVE INPUT COMMON-MODE VOLTAGE LIMIT

There are two negative input voltage ranges of interest:

1. The range between the negative common-mode voltage limit and the negative supply voltage.
2. Voltages which are more negative than the negative supply voltage.

If you take only one of the inputs of the LF13741 into the first range, the output phase will remain correct. When you take both inputs into this range the output will go toward the positive supply voltage.

If you force either or both of the inputs into the second range, an internal diode will be turned "ON." Unless you externally limit the diode current to about 1 mA, the device will be destroyed. In either case, limited or unlimited input current, you cannot predict the output.

### HANDLING

You do not have to take any special precautions in handling the LF13741. It has JFET, as opposed to fragile MOSFET, inputs.

### APPLYING POWER

You should never: reverse the power supplies to the LF13741; plug a part in backwards in a powered socket or board; make the negative supply voltage more positive than an input voltage.

Any one of these supply conditions will forward bias an internal diode. If you have not externally limited the resulting current, the device will be destroyed.

### LAYOUT

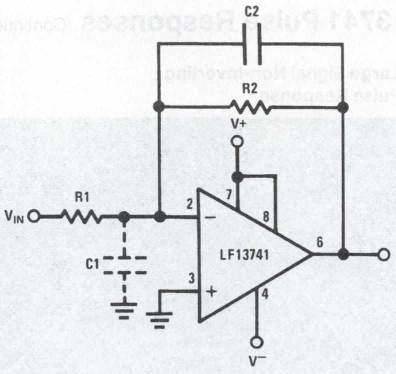
To ensure stability of response you should take care with lead dress, component placement and power supply decoupling. For example, the body of feedback resistors (from output to input pins) should be placed close to the inverting input pin. Noise "pickup" and capacitance to ground from the input pin will be minimized—effects which are usually desirable.

Because of the very low input bias currents of the LF13741, special care should be taken in printed circuit board layouts to prevent unnecessary leakage from the input nodes, (see Typical Applications).

## Application Hints (Continued)

### FEEDBACK POLE

You create a feedback pole when you place resistive feedback around an amplifier. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency (a distinct possibility when using FET op amps), you should place a lead capacitor from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant *(Figure 1)*.



TL/H/9296-9

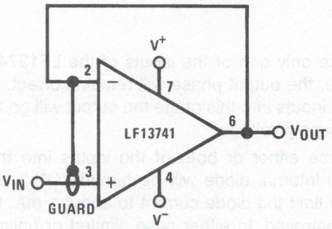
Parasitic input capacitance C1 ≅ (3 pF for LF13741 plus any additional layout capacitance ) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

**FIGURE 1**

## Typical Applications (Continued)

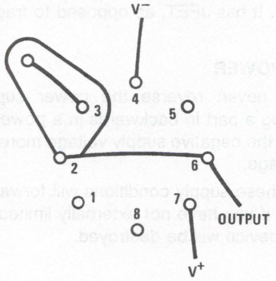
### Circuits Using Guard Rings to Prevent Leakage Currents Between Inputs and V−

**Guarded Voltage Follower**



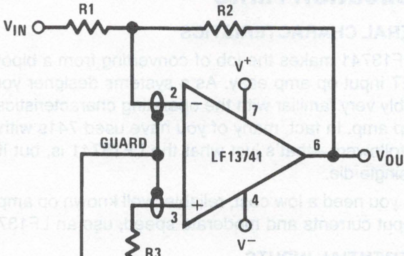
TL/H/9296-10

**PC Layout**



TL/H/9296-12

**Guarded Inverting Amplifier**

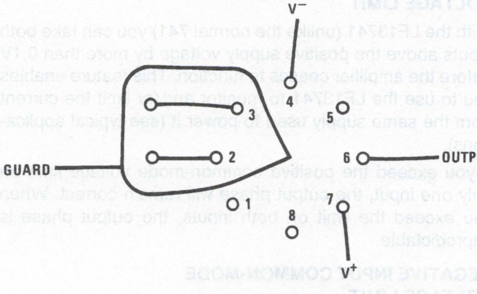


$$A_V = -\frac{R2}{R1}$$

$$R3 = R1||R2$$

TL/H/9296-11

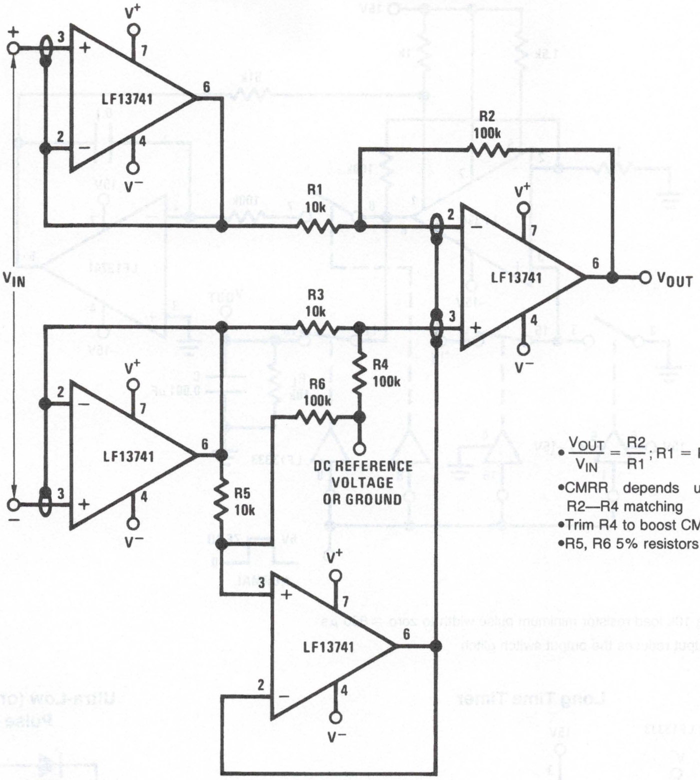
**PC Layout**



TL/H/9296-13

## Typical Applications (Continued)

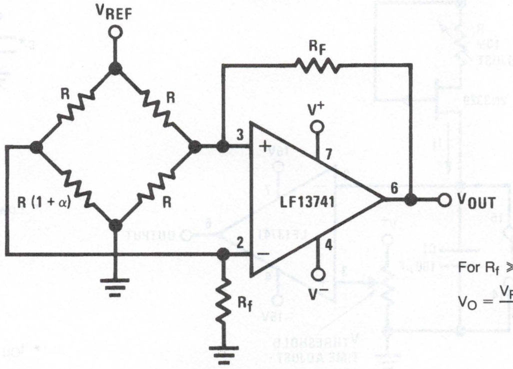
### Guarded Instrumentation Amplifier


+
−
VIN
V+
V−
LF13741
3
2
7
4
6
R1
10k
R2
100k
R3
10k
R4
100k
R5
10k
R6
100k
DC REFERENCE
VOLTAGE
OR GROUND
VOUT

- $\frac{V_{OUT}}{V_{IN}} = \frac{R2}{R1}$; R1 = R3, R2 = R4
- CMRR depends upon R1—R3, R2—R4 matching
- Trim R4 to boost CMRR
- R5, R6 5% resistors

TL/H/9296-14

### Bridge Amplifier


VREF
R
R
R (1 + α)
R
RF
Rf
V+
V−
LF13741
3
2
7
4
6
VOUT

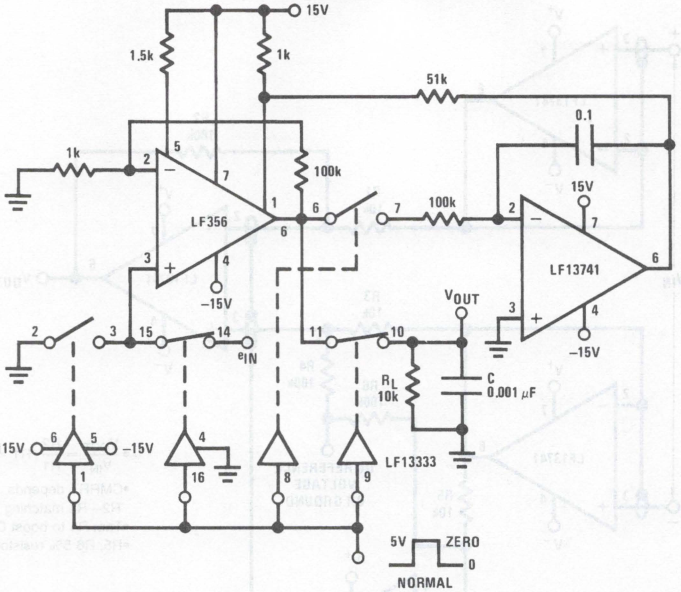
For $R_f \gg R$

$$V_O = \frac{V_{REF}}{2}\left(\frac{R_F}{R}\right)\left(\frac{\alpha}{1+\alpha}\right)$$

TL/H/9296-15

## Typical Applications (Continued)

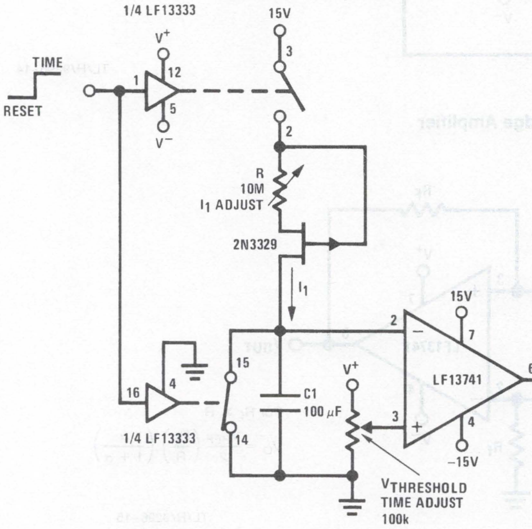
### Auto Zero Circuit for LF356


15V
1.5k
1k
51k
0.1
1k
100k
LF356
2
5
7
1
6
3
4
−15V
6
7
100k
2
15V
7
LF13741
6
3
4
−15V
VOUT
2
3
15
14
eIN
11
10
RL 10k
C 0.001 µF
15V
6
5
−15V
1
4
16
8
9
LF13333
5V
ZERO
NORMAL
0

TL/H/9296-16

- With the output having a 10k load resistor minimum pulse width to zero ≈800 µs
- The capacitor on the output reduces the output switch glitch

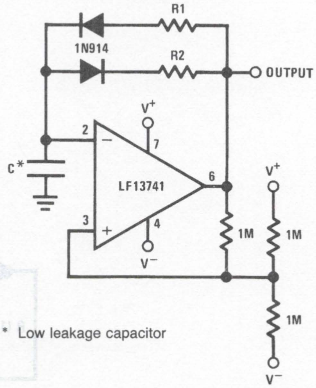
### Long Time Timer


1/4 LF13333
V+
TIME
RESET
1
12
5
V−
15V
3
2
R 10M
I1 ADJUST
2N3329
I1
15V
2
7
LF13741
6
OUTPUT
3
4
−15V
16
4
15
14
1/4 LF13333
C1 100 µF
V+
VTHRESHOLD TIME ADJUST 100k

TL/H/9296-17

- Time $= \frac{C1}{I_1} V_{THRESHOLD}$
- Output goes high on time out
- Reverse op amp inputs for output low on time out
- C1 low leakage capacitor

### Ultra-Low (or High) Duty Cycle Pulse Generator


R1
1N914
R2
OUTPUT
V+
2
7
C*
LF13741
6
3
4
V−
1M
V+
1M
1M
V−

* Low leakage capacitor

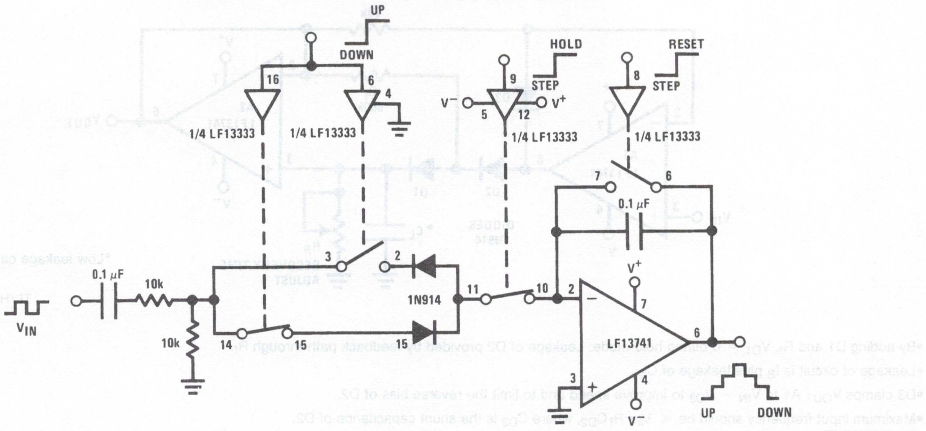
TL/H/9296-18

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

  where $V_S = V^+ + |V^-|$

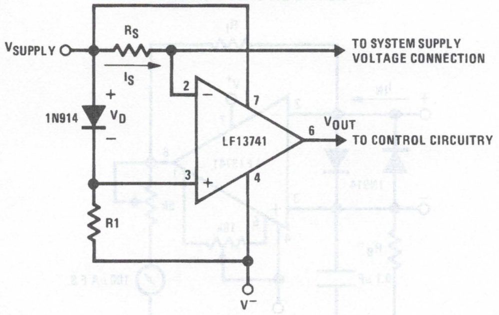
## Typical Applications (Continued)

### Up/Down Staircase Generator/Step and Hold


UP
DOWN
HOLD
STEP
RESET
STEP
16
6
4
1/4 LF13333
1/4 LF13333
V⁻
9
5
12
V⁺
1/4 LF13333
8
1/4 LF13333
7
6
0.1 μF
3
2
0.1 μF
10k
V_IN
10k
14
15
15
1N914
11
10
2
V⁺
7
LF13741
6
3
4
V⁻
UP
DOWN

TL/H/9296-19

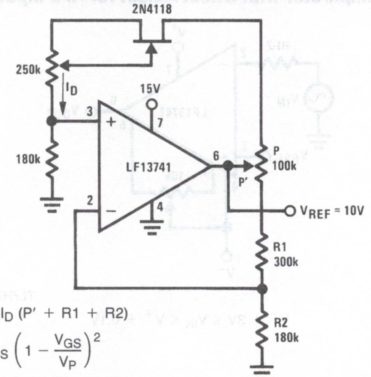
### Supply Current Indicator/Limiter


V_SUPPLY
R_S
I_S
TO SYSTEM SUPPLY VOLTAGE CONNECTION
+
1N914
V_D
−
2
7
LF13741
6
V_OUT
TO CONTROL CIRCUITRY
3
4
R1
V⁻

TL/H/9296-20

- $V_{OUT}$ switches high when $R_S I_S > V_D$

### Low Drift Adjustable Voltage Reference


2N4118
250k
I_D
15V
3
7
180k
LF13741
6
P
100k
P′
2
4
V_REF = 10V
R1
300k
R2
180k

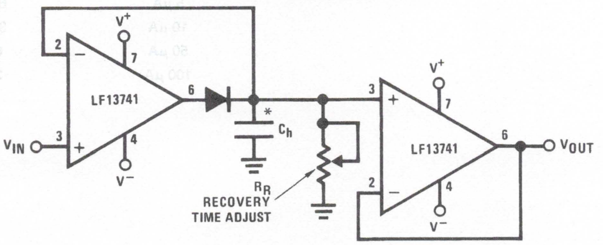
- $V_{REF} = I_D (P' + R1 + R2)$

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- Trim 250k potentiometer for drift adjust
- Trim 100k potentiometer for $V_{REF}$ adjust

TL/H/9296-21

### Low Drift Peak Detector

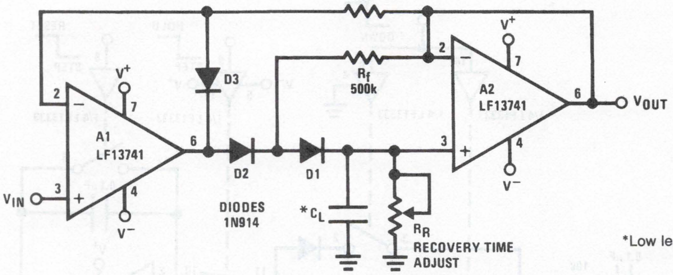

V⁺
2
7
LF13741
6
V_IN
3
4
V⁻
*
C_h
R_R
RECOVERY TIME ADJUST
V⁺
3
7
LF13741
6
V_OUT
2
4
V⁻

TL/H/9296-23

*Low leakage capacitor

## Typical Applications (Continued)

### Ultra-Low Drift Peak Detector

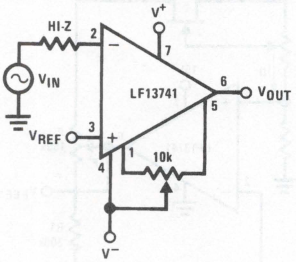

20k
V+
7
2
−
A1
LF13741
6
3
+
4
V−
VIN
D3
D2
D1
DIODES
1N914
*CL
Rf
500k
RR
RECOVERY TIME
ADJUST
V+
7
2
−
A2
LF13741
6
3
+
4
V−
VOUT

*Low leakage capacitor

TL/H/9296-24

- By adding D1 and $R_f$, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through $R_f$.
- Leakage of circuit is $I_B$ plus leakage of $C_h$.
- D3 clamps $V_{OUT}$ A1 to $V_{IN} - V_{D3}$ to improve speed and to limit the reverse bias of D2.
- Maximum input frequency should be $\ll \frac{1}{2}\pi R_f C_{D2}$, where $C_{D2}$ is the shunt capacitance of D2.

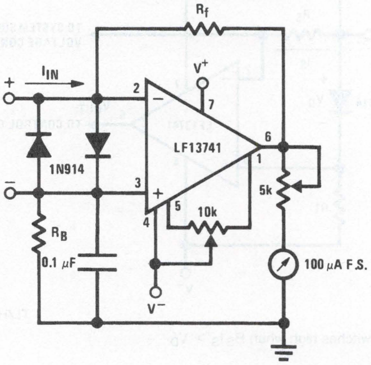
### Comparator with Offset Adjust for Hi-Z Inputs


HI-Z
VIN
2
−
V+
7
LF13741
6
VOUT
5
3
+
VREF
1
10k
4
V−

TL/H/9296-25

$V^- + 3V \le V_{IN} \le V^+ + 0.1V$

### Low Current Ammeter

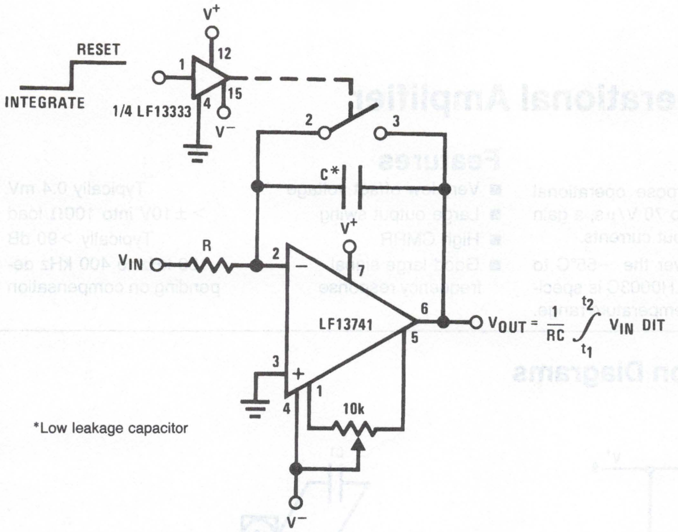

Rf
+
IIN
2
−
V+
7
1N914
LF13741
6
1
5k
−
3
+
5
10k
4
RB
0.1 μF
V−
100 μA F.S.

TL/H/9296-26

| $I_{FULL\ SCALE}$ | $R_F$ | $R_B$ |
|---|---|---|
| 100 nA | 1.5M | 1.5M |
| 500 nA | 300k | 300k |
| 1 μA | 300k | 0 |
| 5 μA | 60k | 0 |
| 10 μA | 30k | 0 |
| 50 μA | 6k | 0 |
| 100 μA | 3k | 0 |

## Typical Applications (Continued)

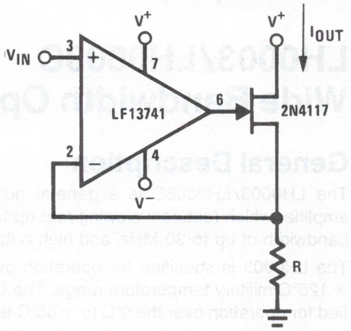
### Long Time Integrator


RESET
INTEGRATE
V+
12
1
1/4 LF13333
4
15
V−
2
3
C*
V+
7
R
VIN
2
LF13741
6
5
3
1
4
10k
V−
VOUT = 1/RC ∫ t1 t2 VIN DIT

*Low leakage capacitor

TL/H/9296-27

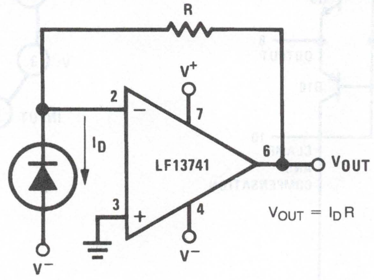
### Precision Current Sink


V+
V+
IOUT
VIN
3
7
LF13741
6
2N4117
2
4
V−
R

TL/H/9296-28

$I_{OUT} = \frac{V_{IN}}{R}$, where $I_{OUT} \leq I_{DSS}$

### Photo Cell Amplifier (I to V Converter)

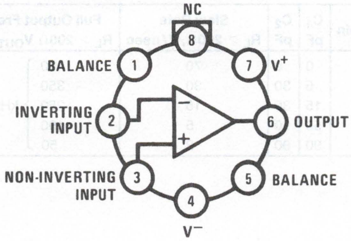

R
V+
2
7
ID
LF13741
6
VOUT
3
4
V−
V−

$V_{OUT} = I_D R$

TL/H/9296-29

## Connection Diagrams (Top Views)

### TO-99 Metal Can Package

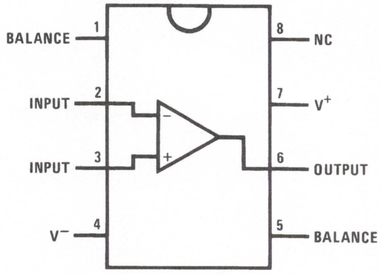

NC
8
BALANCE 1
7 V+
INVERTING INPUT 2
6 OUTPUT
NON-INVERTING INPUT 3
5 BALANCE
4
V−

TL/H/9296-30

**Note:** Pin 4 connected to case.

**Order Number LF13741H**
**See NS Package Number H08C**

### Dual-In-Line Package


BALANCE 1
INPUT 2
INPUT 3
V− 4
8 NC
7 V+
6 OUTPUT
5 BALANCE

TL/H/9296-31

**Order Number LF13741N**
**See NS Package Number N08E**

National Semiconductor Corporation

PRELIMINARY

# LH0003/LH0003C Wide Bandwidth Operational Amplifier

## General Description

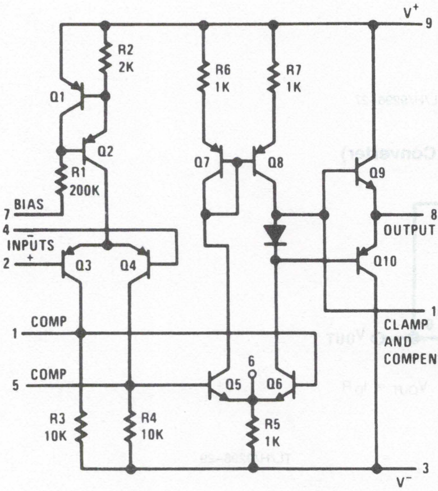
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 V/µs, a gain bandwidth of up to 30 MHz, and high output currents.

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

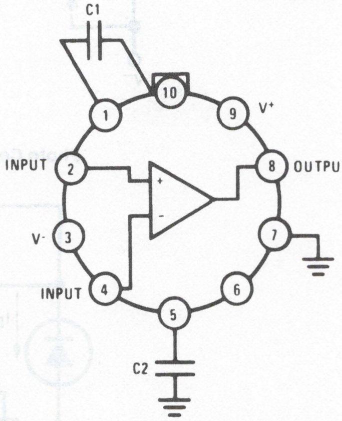
## Features

| | |
|---|---|
| ■ Very low offset voltage | Typically 0.4 mV |
| ■ Large output swing | > ±10V into 100Ω load |
| ■ High CMRR | Typically >90 dB |
| ■ Good large signal frequency response | 50 kHz to 400 kHz depending on compensation |

## Schematic and Connection Diagrams


V+
9
R2
2K
R6
1K
R7
1K
Q1
Q2
R1
200K
Q7
Q8
Q9
BIAS
7
4
INPUTS
2
−
+
Q3
Q4
8
OUTPUT
Q10
10
CLAMP
AND
COMPENSATION
COMP
1
COMP
5
6
Q5
Q6
R3
10K
R4
10K
R5
1K
3
V−

TL/H/5561–1


C1
10
1
9
V+
INPUT
2
8
OUTPUT
+
−
V-
3
7
INPUT
4
6
5
C2

TL/H/5561–2

**Top View**

**Order Number LH0003H or LH0003CH**
**See NS Package Number H10G**

**Typical Compensation**

| Circuit Gain | $C_1$ pF | $C_2$ pF | Slew Rate $R_L > 200\Omega$, V/µsec | Full Output Frequency $R_L > 200\Omega$ $V_{OUT} = \pm 10V$ |
|---|---|---|---|---|
| ≥40 | 0 | 0 | 70 | 400 |
| ≥10 | 5 | 30 | 30 | 350 |
| ≥ 5 | 15 | 30 | 15 | 250 kHz |
| ≥ 2 | 50 | 50 | 5 | 100 |
| ≥ 1 | 90 | 90 | 2 | 50 |

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation | See Curve |
| Differential Input Voltage | ±7V |
| Input Voltage | Equal to Supply |
| Load Current | 120 mA |
| Operating Temperature Range | |
| LH0003 | −55°C to +125°C |
| LH0003C | 0°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Notes 1 & 2)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $R_S < 100\Omega$ | | 0.4 | 3.0 | mV |
| Input Offset Current | | | 0.02 | 0.2 | μA |
| Input Bias Current | | | 0.4 | 2.0 | μA |
| Supply Current | $V_S = \pm 20V$ | | 1.2 | 3 | mA |
| Voltage Gain | $R_L = 100k, V_S = \pm 15V, V_{OUT} = \pm 10V$ | 20 | 70 | | V/mV |
| | $R_L = 2k, V_S = \pm 15V, V_{OUT} = \pm 10V$ | 15 | 40 | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V, R_L = 100\Omega$ | ±10 | ±12 | | V |
| Input Resistance | | | 100 | | kΩ |
| Average Temperature Coefficient of Offset Voltage | $R_S \leq 100\Omega$ | | 4 | | μV/°C |
| Average Temperature Coefficient of Bias Current | | | 8 | | nA/°C |
| CMRR | $R_S < 100\Omega, V_S = \pm 15V, V_{IN} = \pm 10V$ | 70 | 90 | | dB |
| PSRR | $R_S < 100\Omega, V_S = \pm 15V, \Delta V = 5V$ to $20V$ | 70 | 90 | | dB |
| Equivalent Input Noise Voltage | $R_S = 100\Omega$, f = 10 kHz to 100 kHz<br>$V_S = \pm 15V$ dc | | 1.8 | | μVrms |

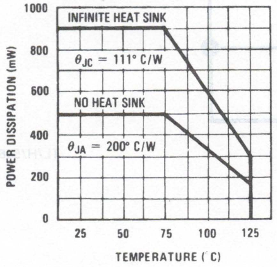
**Note 1:** These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1$ = 90 pF from Pin 1 to Pin 10 and $C_2$ = 90 pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

**Note 2:** Typical values are for $T_A = 25°C$ unless otherwise specified.

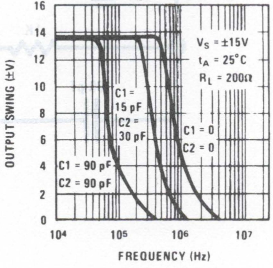
**Note 3:** Refer to RETS0003X for LH0003H military specifications.

## Typical Performance Characteristics

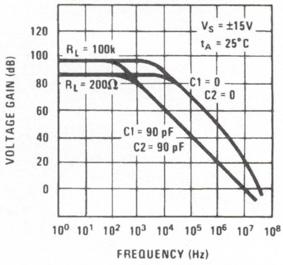
**Maximum Power Dissipation**



**Large Signal Frequency Response**



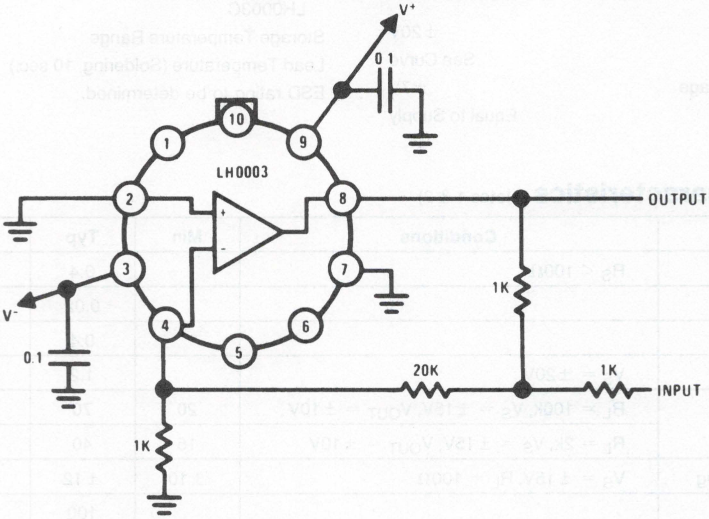
**Open Loop Frequency Response**



TL/H/5561–5

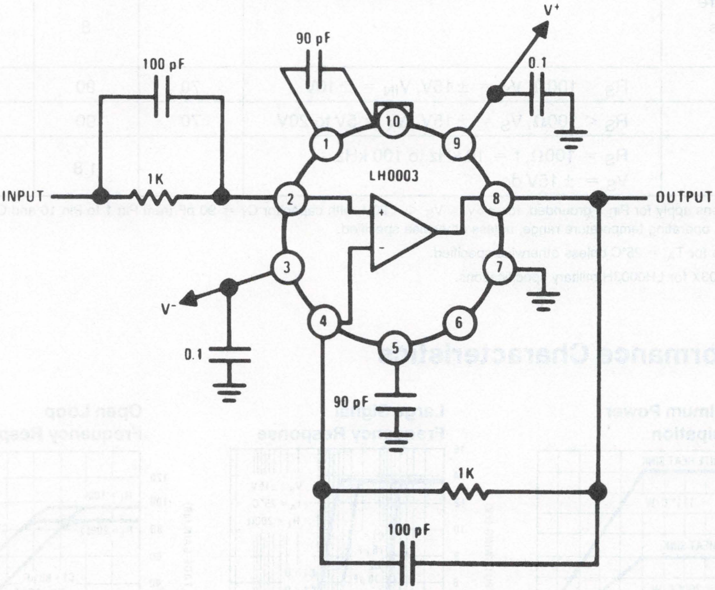
## Typical Applications

### High Slew Rate Unity Gain Inverting Amplifier


V+
0.1
10
1
9
LH0003
2
8
OUTPUT
+
-
3
7
1K
V-
4
6
5
0.1
20K
1K
INPUT
1K

TL/H/5561–3

### Unity Gain Follower


V+
90 pF
0.1
100 pF
10
1
9
1K
LH0003
INPUT
2
8
OUTPUT
+
-
3
7
V-
4
6
5
0.1
90 pF
1K
100 pF

TL/H/5561–4

**National Semiconductor Corporation**

# LH0004/LH0004C High Voltage Operational Amplifier

## General Description

The LH0004/LH0004C is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and $V_S$ = ±40V.

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

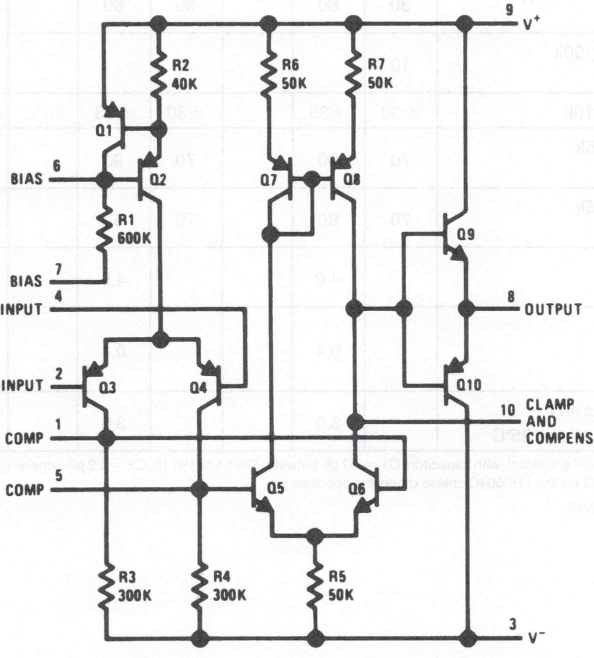
## Features

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 kΩ load with ±40V supplies
- Low input offset current typically 20 nA for the LH0004 and 45 nA for the LH0004C
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

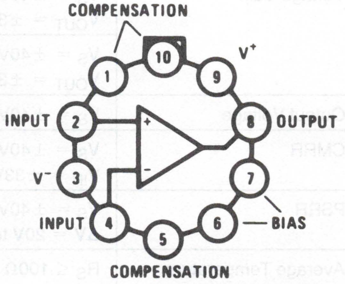
## Applications

- Precision high voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

## Schematic and Connection Diagrams


9 V+
R2 40K
R6 50K
R7 50K
Q1
6 BIAS
Q2
Q7
Q8
R1 600K
Q9
7 BIAS
4 -INPUT
8 OUTPUT
2 +INPUT
Q3
Q4
Q10
10 CLAMP AND COMPENSATION
1 COMP
5 COMP
Q5
Q6
R3 300K
R4 300K
R5 50K
3 V−

TL/H/5559–1


COMPENSATION
10
V+
1
9
INPUT 2
+
8 OUTPUT
V− 3
−
7
INPUT 4
6 — BIAS
5
COMPENSATION

TL/H/5559–2

**Note:** Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 kΩ per volt of potential between Pin 3 and Pin 9.

**Order Number LH0004H or LH0004CH**
**See NS Package Number H10G**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)**

| | |
|---|---|
| Supply Voltage, Continuous | ±45V |
| Power Dissipation (see Curve) | 400 mW |
| Differential Input Voltage | ±7V |
| Input Voltage | Equal to Supply |
| Short Circuit Duration | 3 sec |
| Operating Temperature Range | |
| LH0004 | −55°C to +125°C |
| LH0004C | 0°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

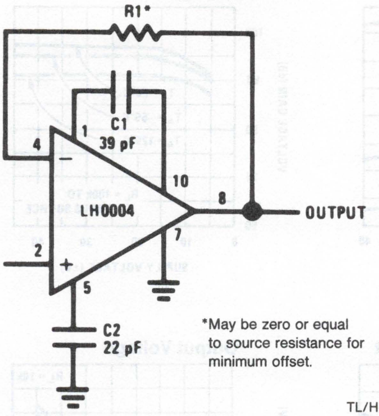
| Parameter | Conditions | LH0004 | | | LH0004C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 100\Omega$, $T_A = 25°C$ | | 0.3 | 1.0 | | 0.3 | 1.5 | mV |
| | $R_S \leq 100\Omega$ | | | 2.0 | | | 3.0 | |
| Input Bias Current | $T_A = 25°C$ | | 20 | 100 | | 30 | 120 | nA |
| | | | | 300 | | | 300 | |
| Input Offset Current | $T_A = 25°C$ | | 3 | 20 | | 10 | 45 | nA |
| | | | | 100 | | | 150 | |
| Positive Supply Current | $V_S = \pm 40V$, $T_A = 25°C$ | | 110 | 150 | | 110 | 150 | μA |
| | $V_S = \pm 40V$ | | | 175 | | | 175 | |
| Negative Supply Current | $V_S = \pm 40V$, $T_A = 25°C$ | | 80 | 100 | | 80 | 100 | μA |
| | $V_S = \pm 40V$ | | | 135 | | | 135 | |
| Voltage Gain | $V_S = \pm 40V$, $R_L = 100k$, $T_A = 25°C$<br>$V_{OUT} = \pm 30V$ | 30 | 60 | | 30 | 60 | | V/mV |
| | $V_S = \pm 40V$, $R_L = 100k$<br>$V_{OUT} = \pm 30V$ | 10 | | | 10 | | | V/mV |
| Output Voltage | $V_S = \pm 40V$, $R_L = 10k$ | ±30 | ±35 | | ±30 | ±33 | | V |
| CMRR | $V_S = \pm 40V$, $R_S \leq 5k$<br>$V_{IN} = \pm 33V$ | 70 | 90 | | 70 | 90 | | dB |
| PSRR | $V_S = \pm 40V$, $R_S \leq 5k$<br>$\Delta V = 20V$ to $40V$ | 70 | 90 | | 70 | 90 | | dB |
| Average Temperature Coefficient Offset Voltage | $R_S \leq 100\Omega$ | | 4.0 | | | 4.0 | | μV/°C |
| Average Temperature Coefficient of Offset Current | | | 0.4 | | | 0.4 | | nA/°C |
| Equivalent Input Noise Voltage | $R_S = 100\Omega$, $V_S = \pm 40V$<br>f = 500 Hz to 5 kHz, $T_A = 25°C$ | | 3.0 | | | 3.0 | | μVrms |

**Note 1:** These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

**Note 2:** Refer to RETS0004X for LH0004H military specifications.

## Typical Applications

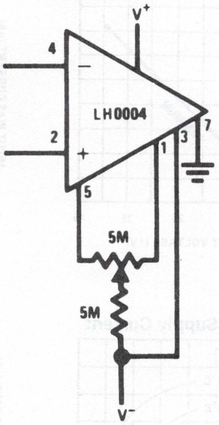
### Voltage Follower


R1*
C1
39 pF
4
1
10
8
OUTPUT
LH0004
7
2
5
C2
22 pF

*May be zero or equal to source resistance for minimum offset.

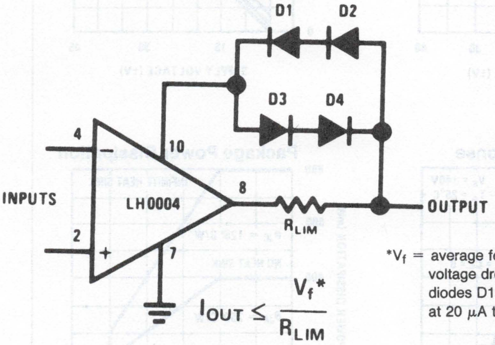
TL/H/5559-3

### Input Offset Voltage Adjust


V+
4
LH0004
2
3
7
1
5
5M
5M
V−

TL/H/5559-4

### External Current Limiting Method

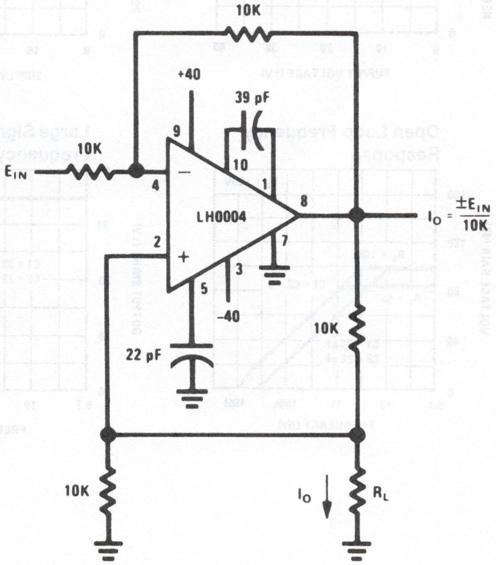

D1
D2
D3
D4
4
10
INPUTS
LH0004
8
2
7
RLIM
OUTPUT

$$I_{OUT} \leq \frac{V_f^*}{R_{LIM}}$$

*$V_f$ = average forward voltage drop of diodes D1 to D4 at 20 µA to 50 µA.

TL/H/5559-5

### High Compliance Current Source

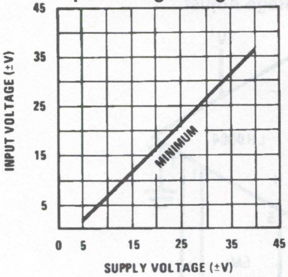

10K
+40
39 pF
9
10K
EIN
10
4
1
LH0004
8
2
7
3
5
−40
22 pF
10K
10K
IO
RL

$$I_O = \frac{\pm E_{IN}}{10K}$$

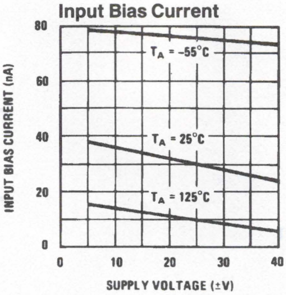
TL/H/5559-6

## Typical Performance Characteristics

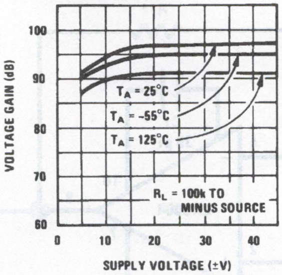
Input Voltage Range



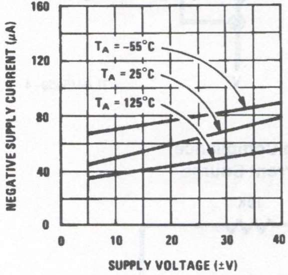
Input Bias Current



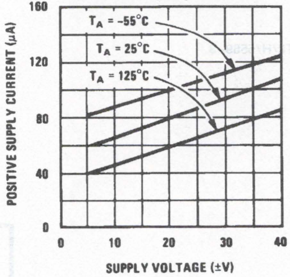
Voltage Gain



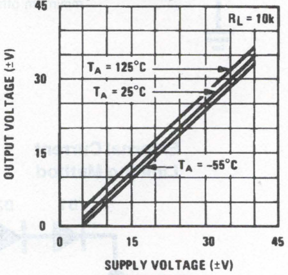
Negative Supply Current



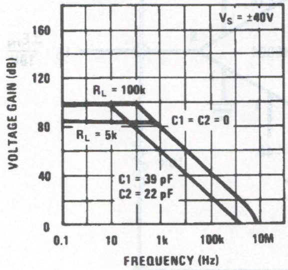
Positive Supply Current



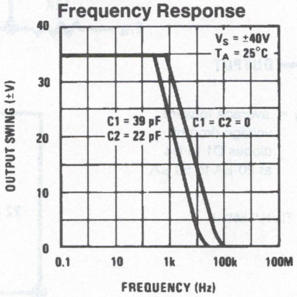
Output Voltage



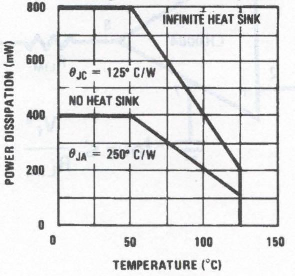
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



TL/H/5559–7

**National Semiconductor Corporation**

# LH0020/LH0020C High Gain Operational Amplifier

## General Description

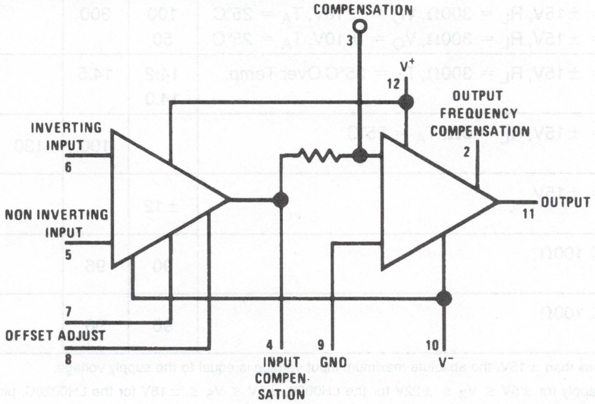
The LH0020/LH0020C is a general purpose operational amplifier designed to source and sink 50 mA output currents. In addition to its high output capability, the LH0020/LH0020C exhibits excellent open loop gain, typically in excess of 100 dB. The parameters of the LH0020 are guaranteed over the temperature range of −55°C to +125°C and $\pm 5V \leq V_S \leq \pm 22V$, while those of the LH0020C are guaranteed over the temperature range of 0°C to +85°C and $\pm 5V \leq V_S \leq \pm 18V$.

Output current capability, excellent input characteristics, and large open loop gain make the LH0020/LH0020C suitable for application in a wide variety of applications from precision DC power supplies to precision medium power comparator.

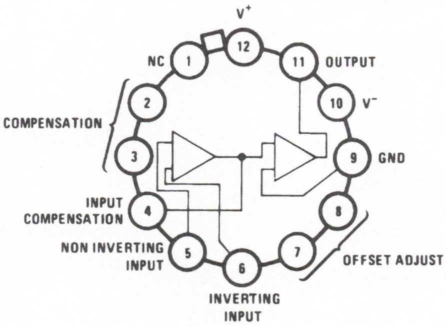
## Features

- Low offset voltage typically 1.0 mV at 25°C over the entire common-mode voltage range
- Low offset current typically 10 nA at 25°C for the LH0020 and 30 nA for the LH0020C
- Offset voltage is adjustable to zero with a single potentiometer
- ±14V, 50 mA output capability

## Schematic and Connection Diagrams


COMPENSATION
3
V+
12
OUTPUT FREQUENCY COMPENSATION
2
INVERTING INPUT
6
NON INVERTING INPUT
5
OUTPUT
11
7
OFFSET ADJUST
8
4
INPUT COMPEN-SATION
9
GND
10
V−

TL/H/5554–1


V+
NC
1
12
11
OUTPUT
2
10
V−
COMPENSATION
3
9
GND
INPUT COMPENSATION
4
8
NON INVERTING INPUT
5
6
7
OFFSET ADJUST
INVERTING INPUT

TL/H/5554–2

**Top View**

**Order Number LH0020G or LH0020CG**
**See NS Package Number G12B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 3)**

| | |
|---|---|
| Supply Voltage | ±22V |
| Power Dissipation | 1.5W |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 1) | ±15V |
| Output Short Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0020 | −55°C to +125°C |
| LH0020C | 0°C to +85°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 2) $T_{min} \le T_A \le T_{max}$ unless otherwise specified

| Parameter | Conditions | LH0020 | | | LH0020C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \le 100\Omega$, $T_A = 25°C$<br>Over Temp. | | 1.0<br>2.0 | 2.5<br>4.0 | | 1.0<br>3.0 | 6.0<br>7.5 | mV<br>mV |
| Input Offset Current | $T_A = 25°C$<br>Over Temp. | | 10 | 50<br>100 | | 30 | 200<br>300 | nA<br>nA |
| Input Bias Current | $T_A = 25°C$<br>Over Temp. | | 60 | 250<br>500 | | 200 | 500<br>800 | nA<br>nA |
| Supply Current | $V_S = \pm 15V$, $T_A = 25°C$ | | 3.5 | 5.0 | | 3.6 | 6.0 | mA |
| Input Resistance | $T_A = 25°C$ | 0.6 | 1.0 | | 0.3 | 1.0 | | MΩ |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$, $T_A = 25°C$<br>$V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$, $T_A = 25°C$ | 100<br>50 | 300 | | 50<br>30 | 150 | | V/mV<br>V/mV |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 300\Omega$, $T_A = 25°C$<br>Over Temp. | 14.2<br>14.0 | 14.5 | | 14.0<br>13.5 | 14.2 | | V<br>V |
| Output Short Circuit Current | $V_S = \pm 15V$, $R_L = 0\Omega$, $T_A = 25°C$ | | 100 | 130 | 25 | 120 | 140 | mA |
| Input Voltage Range | $V_S = \pm 15V$ | ±12 | | | ±12 | | | V |
| Common-Mode Rejection Ratio | $R_S \le 100\Omega$ | 90 | 96 | | 90 | 96 | | dB |
| Power Supply Rejection Ratio | $R_S \le 100\Omega$ | 90 | 96 | | 90 | 96 | | dB |

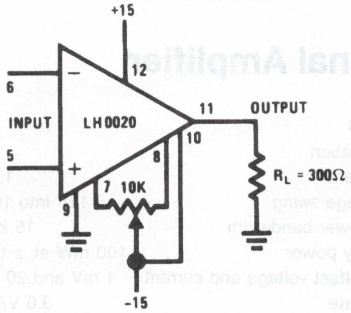
**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** These specifications apply for $\pm 5V \le V_S \le \pm 22V$ for the LH0020, $\pm 5V \le V_S \le \pm 18V$ for the LH0020C, pin 9 grounded, and a 5000 pF capacitor between pins 2 and 3, unless otherwise specified.

**Note 3:** Refer to RETS0020G for LH0020G militiary specifications.

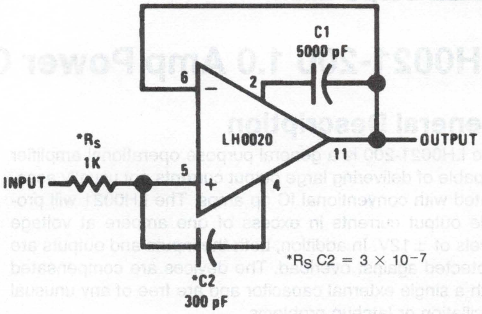
## Typical Applications

### Offset Adjustment


+15
12
−
6
INPUT
LH0020
11
OUTPUT
10
5
+
8
7
10K
9
$R_L$ = 300Ω
−15

TL/H/5554-3

### Unity Gain Frequency Compensation


C1
5000 pF
6
−
2
*$R_S$
1K
LH0020
OUTPUT
INPUT
5
+
11
4
*C2
300 pF

$*R_S\ C2 = 3 \times 10^{-7}$

TL/H/5554-4

**National Semiconductor Corporation**

# LH0021-200 1.0 Amp Power Operational Amplifier

## General Description

The LH0021-200 is a general purpose operational amplifier capable of delivering large output currents not usually associated with conventional IC op amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latchup problems.

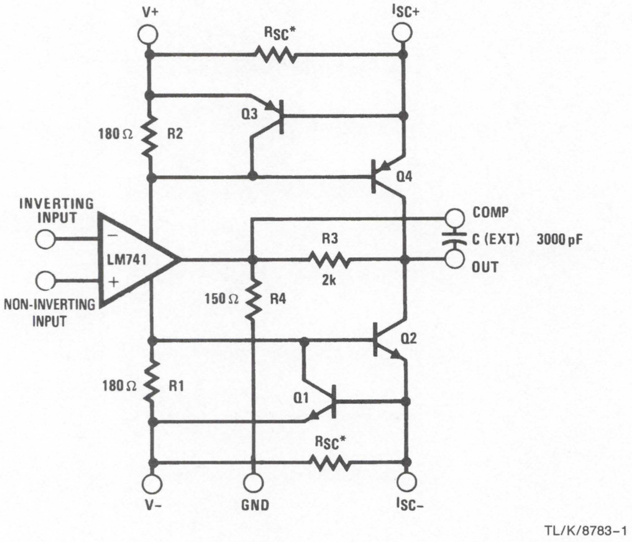
The excellent input characteristics and high output capability of the LH0021-200 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

The LH0021-200 is supplied in an 8-pin TO-3 package rated at 20W with a suitable heatsink. Also, the LH0021-200 is guaranteed over the temperature range of −55°C to +200°C.

## Features

| | |
|---|---|
| ■ 200°C Operation | |
| ■ Output current | 1.0A |
| ■ Output voltage swing | ±12V into 10Ω |
| ■ Wide full power bandwidth | 15 kHz |
| ■ Low standby power | 100 mW at ±15V |
| ■ Low input offset voltage and current | 1 mV and 20 nA |
| ■ High slew rate | 3.0 V/μs |
| ■ High open loop gain | 100 dB |
| ■ Expected life in operation | 160 Hours |

## Schematic and Connection Diagrams


V+
ISC+
RSC*
Q3
180Ω
R2
Q4
INVERTING INPUT
LM741
NON-INVERTING INPUT
COMP
C (EXT)
3000 pF
OUT
R3
2k
150Ω
R4
Q2
180Ω
R1
Q1
RSC*
V−
GND
ISC−

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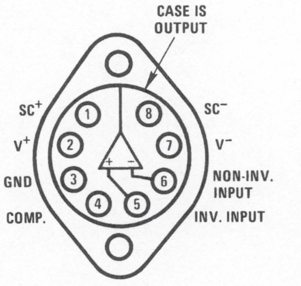
*RSC external on "K" package


CASE IS OUTPUT
SC+
SC−
V+
V−
GND
NON-INV. INPUT
COMP.
INV. INPUT
1
2
3
4
5
6
7
8

TL/K/8783-2

**Top View**

**Order Number LH0021K-200**
**See NS Package Number K08A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation | See curves |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 1) | ±15V |
| Peak Output Current LH0021-200 (Note 2) | 2.0A |
| Output Short Circuit Duration (Note 3) | Continuous |
| Operating Temperature Range | |
| LH0021-200 | −55°C to +200°C |
| Storage Temperature Range | −65°C to +225°C |
| Lead Temperature (Soldering, 10 sec.) | +260°C |
| Expected Operating Life at 200°C | 160 Hrs. |

ESD rating is to be determined.

## DC Electrical Characteristics for LH0021-200 (Notes 4, 5 & 6)

| Symbol | Parameter | Conditions | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | Input Offset Voltage | $R_S \leq 100\Omega$ | | | 15 | mV |
| | Input Offset Current | | | | 500 | nA |
| | Input Bias Current | | | | 2.0 | $\mu$A |
| | Input Resistance | $T_C = 25°C$ | | 1.0 | | MΩ |
| | Common Mode Rejection Ratio | $R_S \leq 100\Omega, \Delta V_{CM} = \pm 10V$ | 60 | 90 | | dB |
| | Input Voltage Range | $V_S = \pm 15V$ | ±12 | | | V |
| | Power Supply Rejection Ratio | $R_S \leq 100\Omega, \Delta V_S = \pm 10V$ | 60 | 96 | | dB |
| | Voltage Gain | $V_S = \pm 15V, V_O = \pm 10V$<br>$R_L = 100\Omega$ | 70 | | | dB |
| | Output Voltage Swing | $V_S = \pm 15V, R_L = 100\Omega$ | ±10 | ±14 | | V |
| | Power Supply Current | $V_S = \pm 15V, V_{OUT} = 0$ | | 2.5 | 5.0 | mA |

## AC Electrical Characteristics for LH0021-200 ($T_A = 25°C, V_S = \pm 15V, C_C = 3000$ pF)

| Symbol | Parameter | Conditions | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | Slew Rate | $A_V = +1, R_L = 100\Omega$ | | 3.0 | | V/$\mu$s |
| | Power Bandwidth | $R_L = 100\Omega$ | | 20 | | kHz |

**Note 1:** Rating applies for supply voltages greater than ±15V. For supplies less than ±15V, rating is equal to supply voltages.

**Note 2:** Rating applies for LH0021K-200 with $R_{SC} = 0\Omega$.

**Note 3:** Rating applies as long as package rating is not exceeded.

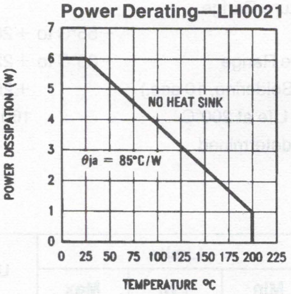
**Note 4:** Test conditions are $V_S = \pm 15V$, $R_S = 100\Omega$, $C_C = 3000$ pF and apply for $-55°C \leq T_A \leq 200°C$ unless otherwise specified.

**Note 5:** For further information, see the LH0021/LH0021C Datasheet.

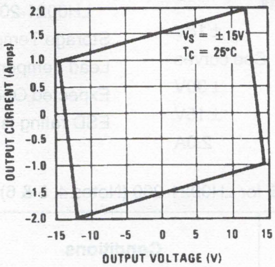
**Note 6:** In order to limit maximum junction temperature to +225°C it may be necessary to operate with $V_S < \pm 15V$ when $T_A$ or $T_C$ exceeds specific values depending on the $P_D$ within the device package. Total $P_D$ is the sum of quiescent and load-related dissipation.

# Typical Performance Characteristics

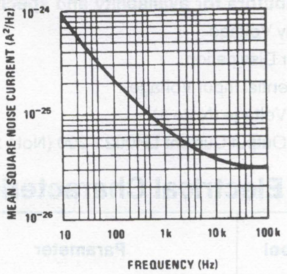
### Power Derating—LH0021



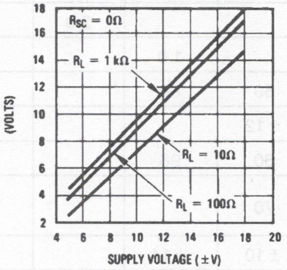
### Safe Operating Area—LH0021



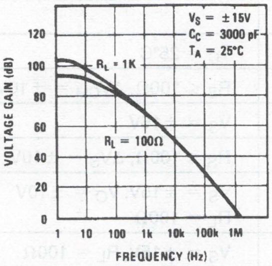
### Input Noise Current



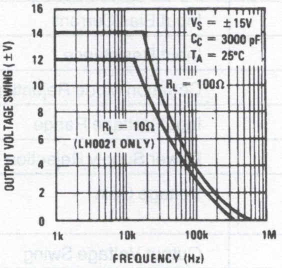
### Output Voltage Swing



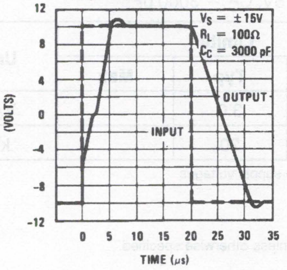
### Open Loop Frequency Response



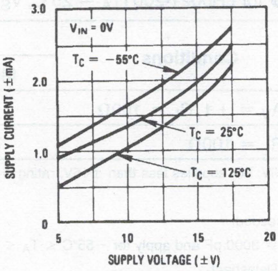
### Large Signal Frequency Response



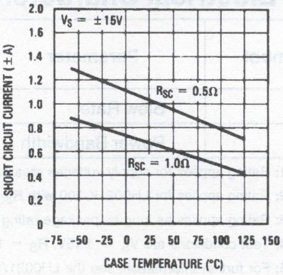
### Voltage Follower Pulse Response



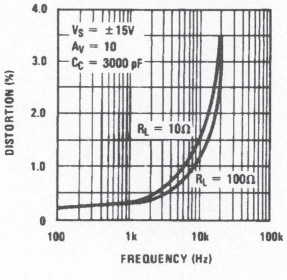
### No Load Supply Current



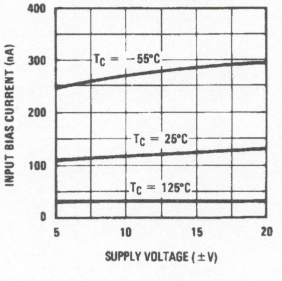
### Short Circuit Current vs Temperature LH0021/LH0021C



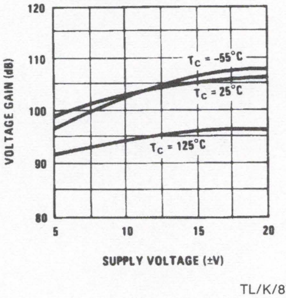
### Distortion vs Frequency



### Input Bias Current

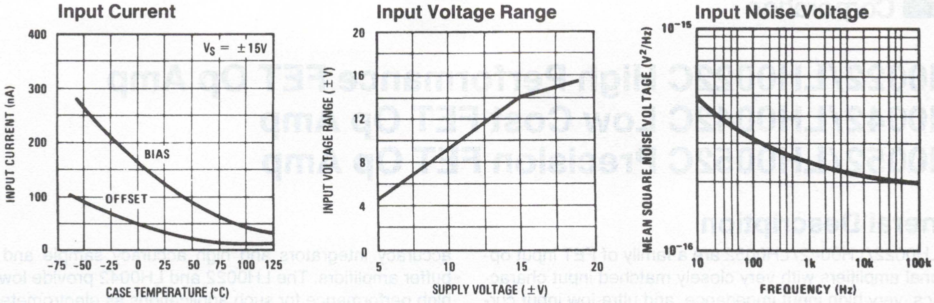


### Voltage Gain



TL/K/8783-3

## Typical Performance Characteristics (Continued)


Input Current

Input Voltage Range

Input Noise Voltage

TL/K/8783-4

For further applications information see the LH0021/LH0041 Datasheet.

National
Semiconductor
Corporation

# LH0022/LH0022C High Performance FET Op Amp
# LH0042/LH0042C Low Cost FET Op Amp
# LH0052/LH0052C Precision FET Op Amp

## General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 μV maximum offset and 2 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with negligible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection is available on special request.

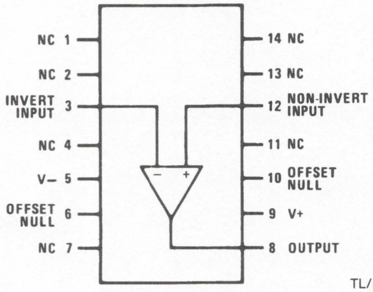
For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

## Features

- Low input offset current—500 femtoamps max (LH0052)
- Low input offset drift—2 μV/°C typ (LH0052)
- Low input offset voltage—100 μV typ
- High open loop gain—100 dB typ
- Excellent slew rate—3.0 V/μs typ
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

## Connection Diagrams

**Dual-In-Line Package**

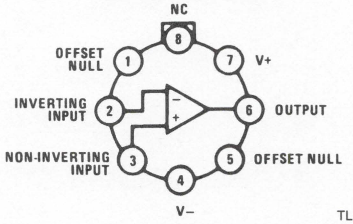


TL/K/5557–2

**Top View**

**Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD**
**See NS Package Number D14E**

**Metal Can Package**

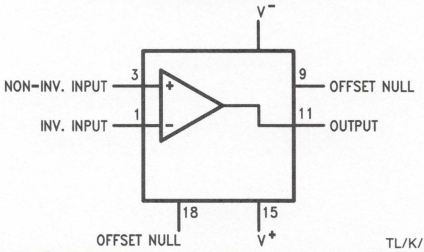


TL/K/5557–3

**Top View**

**Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH**
**See NS Package Number H08D**

**Leadless Chip Carrier**



TL/K/5557–4

**Order Number LH0042E**
**See NS Package Number E20A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±22V |
| Power Dissipation (see Graph) | 500 mW |
| Input Voltage (Note 1) | ±15V |
| Differential Input Voltage (Note 2) | ±30V |
| Voltage Between Offset Null and $V^-$ | ±0.5V |
| Short Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0022, LH0042, LH0052 | −55°C to +125°C |
| LH0022C, LH0042C, LH0052C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## DC Electrical Characteristics for LH0022/LH0022C (Note 3) $T_A = T_J(\text{Max})$

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0022 | | | LH0022C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \le 100\ k\Omega$, $T_A = 25°C$<br>$V_S = \pm 15V$ | | 2.0 | 4.0 | | 3.5 | 6.0 | mV |
| | $R_S \le 100\ k\Omega$, $V_S = \pm 15V$ | | | 5.0 | | | 7.0 | mV |
| Temperature Coefficient of Input Offset Voltage | $R_S \le 100\ k\Omega$ | | 10 | | | 15 | | µV/°C |
| Offset Voltage Drift with Time | | | 3 | | | 4 | | µV/week |
| Input Offset Current | (Note 4) | | 0.2 | 2.0 | | 1.0 | 5.0 | pA |
| | | | | 2.0 | | | 0.5 | nA |
| Temperature Coefficient of Input Offset Current | | | Doubles Every 10°C | | | Doubles Every 10°C | | |
| Offset Current Drift with Time | | | 0.1 | | | 0.1 | | pA/week |
| Input Bias Current | (Note 4) | | 5 | 10 | | 10 | 25 | pA |
| | | | | 10 | | | 2.5 | nA |
| Temperature Coefficient of Input Bias Current | | | Doubles Every 10°C | | | Doubles Every 10°C | | |
| Differential Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Common Mode Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Input Capacitance | | | 4.0 | | | 4.0 | | pF |
| Input Voltage Range | $V_S = \pm 15V$ | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| Common Mode Rejection Ratio | $R_S \le 10\ k\Omega$, $V_{IN} = \pm 10V$ | 80 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \le 10\ k\Omega$, $\pm 5V \le V_S \le \pm 15V$ | 80 | 90 | | 70 | 90 | | dB |
| Large Signal Voltage Gain | $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$<br>$T_A = 25°C$, $V_S = \pm 15V$ | 100 | 200 | | 75 | 160 | | V/mV |
| | $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$<br>$V_S = \pm 15V$ | 50 | | | 50 | | | V/mV |
| Output Voltage Swing | $R_L = 1\ k\Omega$, $T_A = 25°C$<br>$V_S = \pm 15V$ | ±10 | ±12.5 | | ±10 | ±12 | | V |
| | $R_L = 2\ k\Omega$, $V_S = \pm 15V$ | ±10 | | | ±10 | | | V |
| Output Current Swing | $V_{OUT} = \pm 10V$, $T_A = 25°C$ | ±10 | ±15 | | ±10 | ±15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | | | 25 | | | 25 | | mA |
| Supply Current | $V_S = \pm 15V$ | | 2.0 | 2.5 | | 2.4 | 2.8 | mA |
| Power Consumption | $V_S = \pm 15V$ | | | 75 | | | 85 | mW |

## DC Electrical Characteristics for LH0042/LH0042C (Note 3)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0042 | | | LH0042C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 100\ k\Omega$ | | 5.0 | 20 | | 6.0 | 20 | mV |
| Temperature Coefficient of Input Offset Voltage | $R_S \leq 100\ k\Omega$ | | 10 | | | 15 | | μV/°C |
| Offset Voltage Drift with Time | | | 7.0 | | | 10 | | μV/week |
| Input Offset Current | (Note 4) | | 1.0 | 5.0 | | 2.0 | 10 | pA |
| Temperature Coefficient of Input Offset Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Offset Current Drift with Time | | | 0.1 | | | 0.1 | | pA/week |
| Input Bias Current | (Note 4) | | 10 | 25 | | 15 | 50 | pA |
| Temperature Coefficient of Input Bias Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Differential Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Common Mode Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Input Capacitance | | | 4.0 | | | 4.0 | | pF |
| Input Voltage Range | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| Common Mode Rejection Ratio | $R_S \leq 10\ k\Omega,\ V_{IN} = \pm 10V$ | 70 | 86 | | 70 | 80 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10\ k\Omega,\ \pm 5V \leq V_S \leq \pm 15V$ | 70 | 86 | | 70 | 86 | | dB |
| Large Signal Voltage Gain | $R_S \leq 2\ k\Omega,\ V_{OUT} = \pm 10V$ | 50 | 150 | | 25 | 100 | | V/mV |
| Output Voltage Swing | $R_L = 1\ k\Omega,\ T_A = 25°C$ | ±10 | ±12.5 | | ±10 | ±12 | | V |
| | $R_L = 2\ k\Omega$ | ±10 | | | ±10 | | | V |
| Output Current Swing | $V_{OUT} = \pm 10V$ | ±10 | ±15 | | ±10 | ±15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | | | 20 | | | 20 | | mA |
| Supply Current | | | 2.5 | 3.5 | | 2.8 | 4.0 | mA |
| Power Consumption | | | | 105 | | | 120 | mW |

## DC Electrical Characteristics for LH0052/LH0052C (Note 3)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0052 | | | LH0052C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S < 100\ k\Omega,\ V_S = +15V$<br>$T_A = 25°C$ | | 0.1 | 1.0 | | 0.4 | 2.0 | mV |
| | $R_S < 100\ k\Omega,\ V_S = \pm 15V$ | | | 2.0 | | | 3.0 | mV |
| Temperature Coefficient of Input Offset Voltage | $V_S = 100\ k\Omega,\ V_S = \pm 15V$ | | 2.0 | | | 5.0 | | μV/°C |
| Offset Voltage Drift with Time | | | 2.0 | | | 4.0 | | μV/week |
| Input Offset Current | (Note 4) | | 0.01 | 5.0 | | 0.02 | 1.0 | pA |
| | | | | 500 | | | 100 | pA |
| Temperature Coefficient of Input Offset Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Offset Current Drift with Time | | | 0.1 | | | 0.1 | | pA/week |

## DC Electrical Characteristics for LH0052/LH0052C (Note 3) (Continued)

| Parameter | Conditions | LH0052 Min | LH0052 Typ | LH0052 Max | LH0052C Min | LH0052C Typ | LH0052C Max | Units |
|---|---|---|---|---|---|---|---|---|
| Input Bias Current | (Note 4) | | 0.5 | 2.5 | | 1.0 | 5.0 | pA |
| | | | | 2.5 | | | 0.5 | nA |
| Temperature Coefficient of Input Bias Current | | | Doubles Every 10°C | | | Doubles Every 10°C | | |
| Differential Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Common Mode Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Input Capacitance | | | 4.0 | | | 4.0 | | pF |
| Input Voltage Range | $V_S = \pm 15V$ | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| Common Mode Rejection Ratio | $R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$ | 74 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$ | 74 | 90 | | 70 | 90 | | dB |
| Large Signal Voltage Gain | $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$<br>$V_S = \pm 15V$, $T_A = 25°C$ | 100 | 200 | | 75 | 160 | | V/mV |
| | $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$<br>$V_S = \pm 15V$ | 50 | | | 50 | | | V/mV |
| Output Voltage Swing | $R_L = 1\ k\Omega$, $T_A = 25°C$<br>$V_S = \pm 15V$ | ±10 | ±12.5 | | ±10 | ±12 | | V |
| | $R_L = 2\ k\Omega$, $V_S = \pm 15V$ | ±10 | | | ±10 | | | V |
| Output Current Swing | $V_{OUT} = \pm 10V$, $T_A = 25°C$ | ±10 | ±15 | | ±10 | ±15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | | | 25 | | | 25 | | mA |
| Supply Current | $V_S = \pm 15V$ | | 3.0 | 3.5 | | 3.0 | 3.8 | mA |
| Power Consumption | $V_S = \pm 15V$ | | | 105 | | | 114 | mW |

## AC Electrical Characteristics for all amplifiers ($T_A = 25°C$, $V_S = \pm 15V$)

| Parameter | Conditions | LH0022/42/52 Min | LH0022/42/52 Typ | LH0022/42/52 Max | LH0022C/42C/52C Min | LH0022C/42C/52C Typ | LH0022C/42C/52C Max | Units |
|---|---|---|---|---|---|---|---|---|
| Slew Rate | Voltage Follower | 1.5 | 3.0 | | 1.0 | 3.0 | | V/μs |
| Large Signal Bandwidth | Voltage Follower | | 40 | | | 40 | | kHz |
| Small Signal Bandwidth | | | 1.0 | | | 1.0 | | MHz |
| Rise Time | | | 0.3 | 1.5 | | 0.3 | 1.5 | μs |
| Overshoot | | | 10 | 30 | | 15 | 40 | % |
| Settling Time (0.1%) | $\Delta V_{IN} = 10V$ | | 4.5 | | | 4.5 | | μs |
| Overload Recovery | | | 4.0 | | | 4.0 | | μs |

## AC Electrical Characteristics for all amplifiers ($T_A$ = 25°C, $V_S$ = ±15V) (Continued)

| Parameter | Conditions | LH0022/42/52 Min | LH0022/42/52 Typ | LH0022/42/52 Max | LH0022C/42C/52C Min | LH0022C/42C/52C Typ | LH0022C/42C/52C Max | Units |
|---|---|---|---|---|---|---|---|---|
| Input Noise Voltage | $R_S$ = 10 kΩ, $f_o$ = 10 Hz | | 150 | | | 150 | | nV/√Hz |
| | $R_S$ = 10 kΩ, $f_o$ = 100 Hz | | 55 | | | 55 | | nV/√Hz |
| | $R_S$ = 10 kΩ, $f_o$ = 1 kHz | | 35 | | | 35 | | nV/√Hz |
| | $R_S$ = 10 kΩ, $f_o$ = 10 kHz | | 30 | | | 30 | | nV/√Hz |
| | BW = 10 Hz to 10kHz, $R_S$ = 10 kΩ | | 12 | | | 12 | | μVrms |
| Input Noise Current | BW = 10 Hz to 10kHz | | <0.1 | | | <0.1 | | pArms |

**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

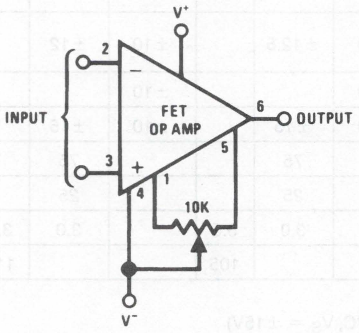
**Note 2:** Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

**Note 3:** Unless otherwise specified, these specifications apply for $\pm 5V \le V_S \le +20V$ and $-55°C \le T_A \le +125°C$ for the LH0022/42/52 and $-25°C \le T_A \le +85°C$ for the LH0022C/42C/52C. Typical values are given for $T_A$ = 25°C.

**Note 4:** Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature $T_j$ = 25°C. Self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

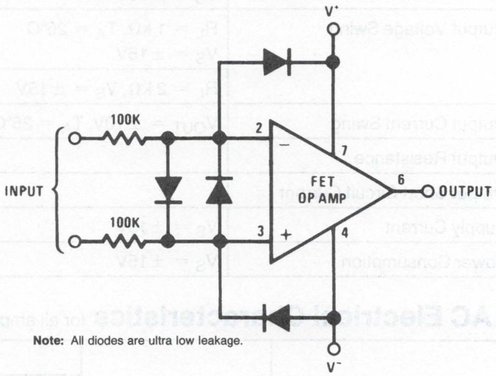
## Auxiliary Circuits (Shown for TO-5 pin out)

**Offset Null**



TL/K/5557-5

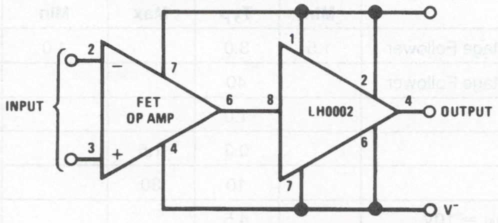
**Protecting Inputs from ±150V Transients**



**Note:** All diodes are ultra low leakage.

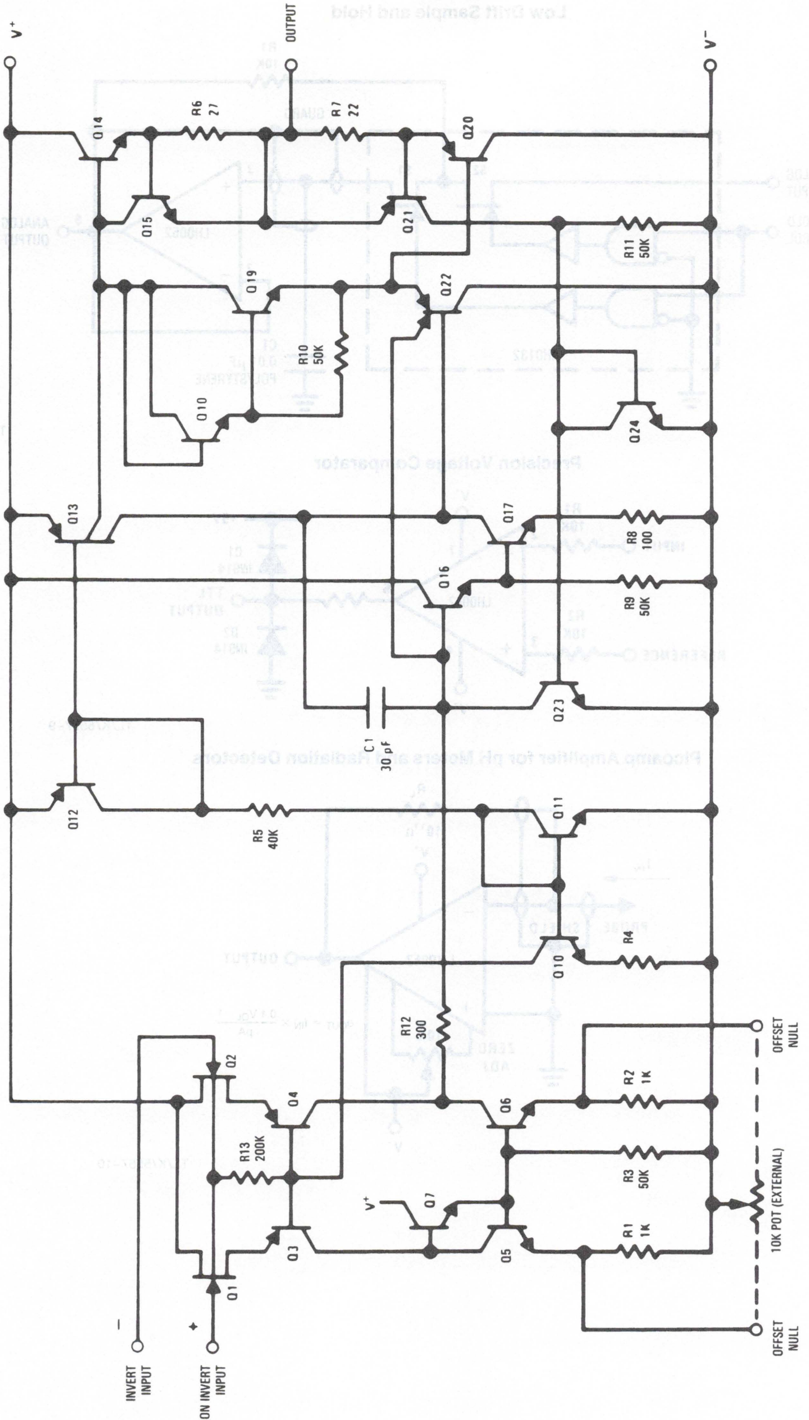
TL/K/5557-6

**Boosting Output Drive to ±100 mA**



TL/K/5557-7

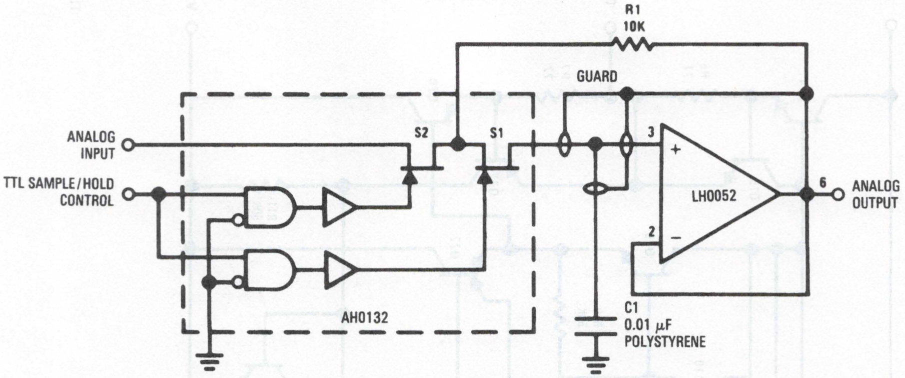
## Schematic Diagram


V+
OUTPUT
V−
Q14
R6 27
R7 22
Q20
Q15
Q21
R11 50K
Q19
Q22
R10 50K
Q10
Q24
Q13
Q17
R8 100
Q16
R9 50K
Q23
C1 30 pF
Q12
R5 40K
Q11
Q10
R4
R12 300
Q2
Q4
Q6
R2 1K
OFFSET NULL
R13 200K
R3 50K
V+
Q7
10K POT (EXTERNAL)
Q3
Q5
R1 1K
Q1
−
+
INVERT INPUT
NON INVERT INPUT
OFFSET NULL

TL/K/5557–1

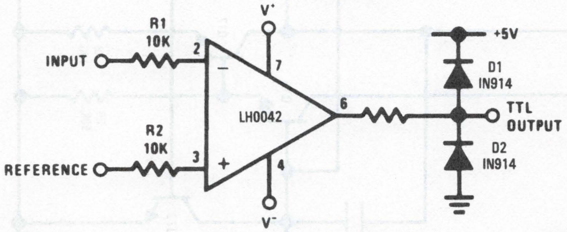
## Typical Applications

### Low Drift Sample and Hold


R1
10K
GUARD
ANALOG INPUT
S2
S1
3
TTL SAMPLE/HOLD CONTROL
LH0052
6
ANALOG OUTPUT
2
AH0132
C1
0.01 µF
POLYSTYRENE

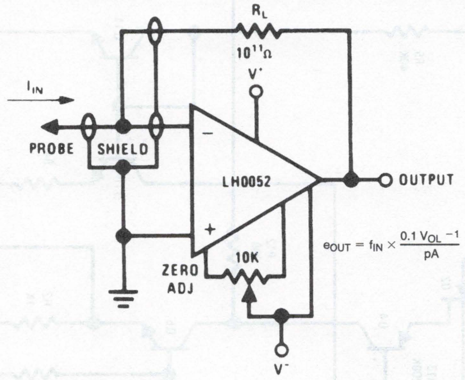
TL/K/5557-8

### Precision Voltage Comparator


V+
R1
10K
INPUT
2
7
+5V
D1
IN914
LH0042
6
TTL
OUTPUT
R2
10K
3
REFERENCE
4
D2
IN914
V-

TL/K/5557-9

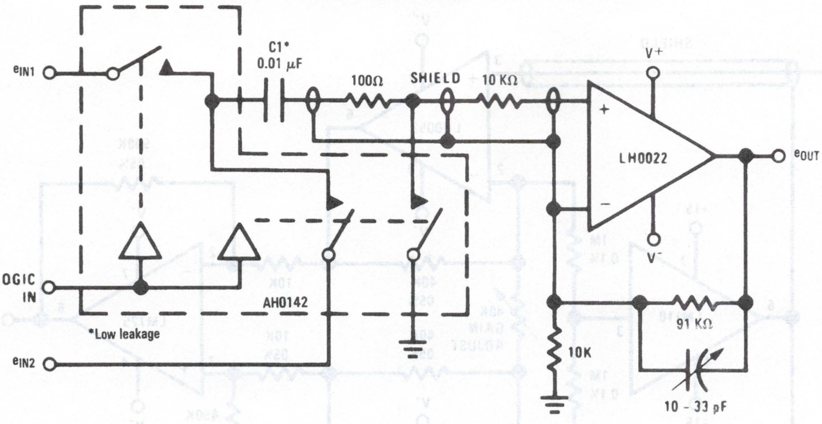
### Picoamp Amplifier for pH Meters and Radiation Detectors


R_L
10¹¹Ω
I_IN
V+
PROBE
SHIELD
LH0052
OUTPUT
e_OUT = f_IN × 0.1 V_OL^-1 / pA
10K
ZERO
ADJ
V-

TL/K/5557-10

## Typical Applications (Continued)

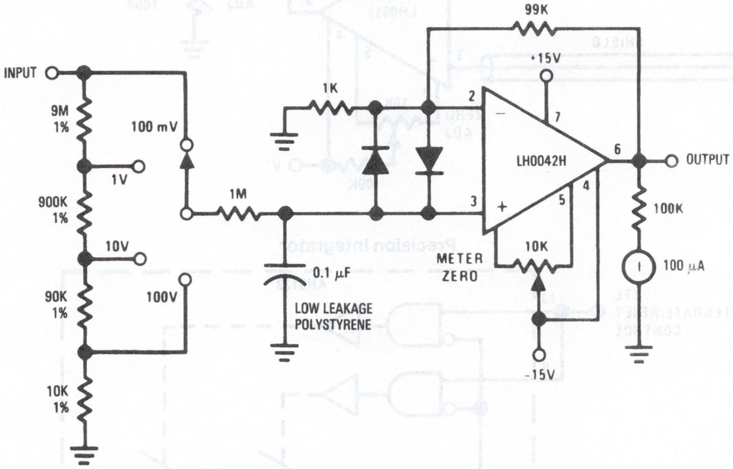
### Precision Subtractor for Automatic Test Gear


eIN1
C1*
0.01 μF
100Ω
SHIELD
10 KΩ
V+
+
−
LH0022
eOUT
V−
LOGIC IN
AH0142
*Low leakage
eIN2
91 KΩ
10K
10 - 33 pF

$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

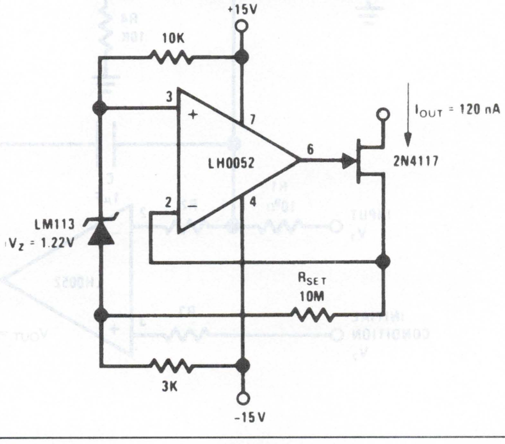
TL/K/5557-11

### Sensitive Low Cost "VTVM"


INPUT
9M 1%
100 mV
1V
900K 1%
10V
90K 1%
100V
10K 1%
1K
1M
0.1 μF
LOW LEAKAGE POLYSTYRENE
99K
+15V
2
7
3
6
4
5
LH0042H
OUTPUT
100K
100 μA
METER ZERO
10K
-15V

TL/K/5777-12

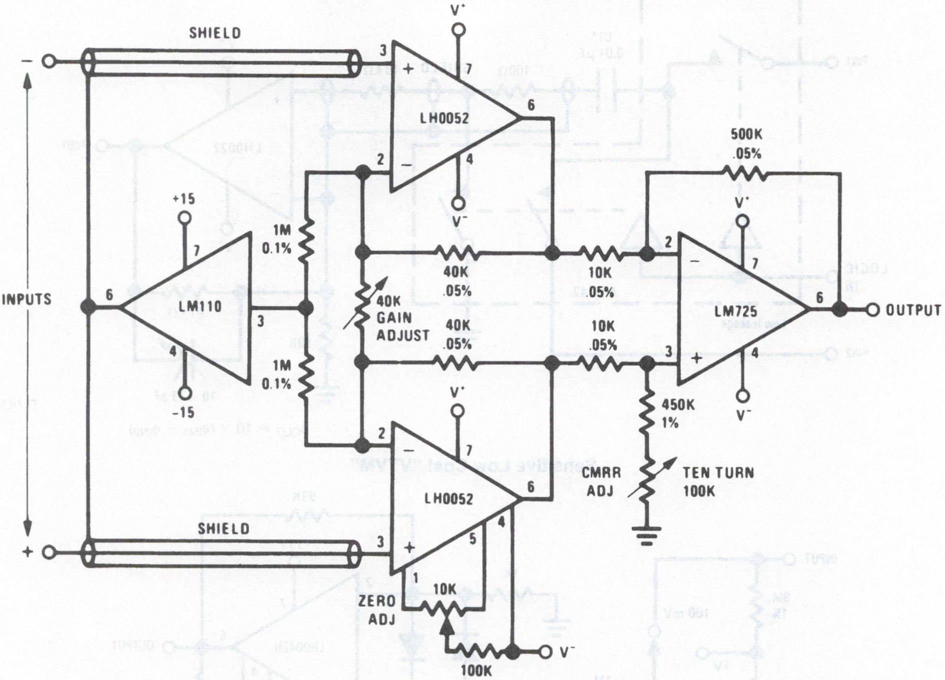
### Ultra Low Level Current Source


+15V
10K
3
+
7
LH0052
6
2
4
IOUT = 120 nA
2N4117
LM113
VZ = 1.22V
RSET
10M
3K
-15V

TL/K/5557-13

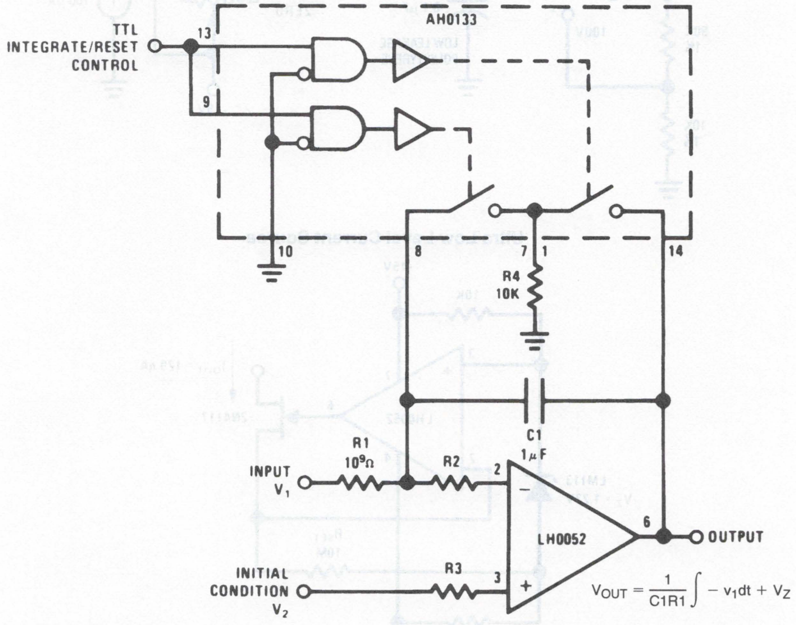
## Typical Applications (Continued)

### True Instrumentation Amplifier


V⁺
SHIELD
−
3
+
7
LH0052
6
2
−
4
V⁻
+15
7
1M
0.1%
INPUTS
6
LM110
3
4
−15
40K
GAIN
ADJUST
40K
.05%
40K
.05%
10K
.05%
10K
.05%
500K
.05%
V⁺
2
−
7
LM725
6
OUTPUT
3
+
4
V⁻
1M
0.1%
450K
1%
CMRR
ADJ
TEN TURN
100K
V⁺
2
−
7
LH0052
6
4
5
SHIELD
+
3
+
1
10K
ZERO
ADJ
100K
V⁻

TL/K/5557-14

### Precision Integrator

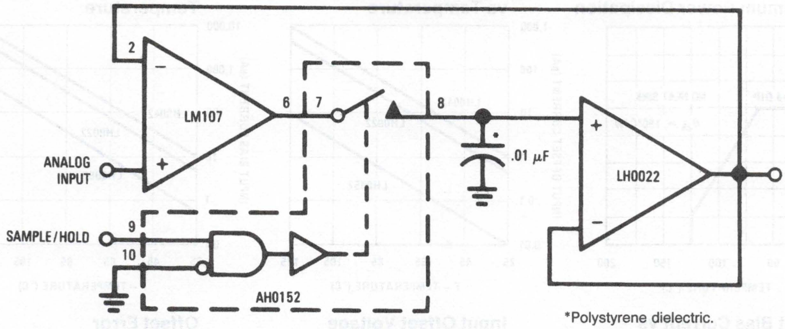

AH0133
TTL
INTEGRATE/RESET
CONTROL
13
9
10
8
7
1
14
R4
10K
C1
1 μF
R1
$10^9\Omega$
R2
INPUT
$V_1$
2
−
LH0052
6
OUTPUT
INITIAL
CONDITION
$V_2$
R3
3
+

$V_{OUT} = \frac{1}{C1R1}\int - v_1 dt + V_Z$

TL/K/5557-15

## Typical Applications (Continued)

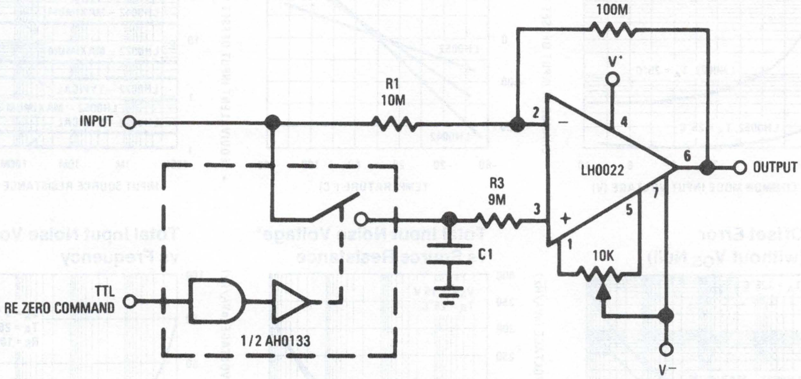
### Precision Sample and Hold


2
LM107
6
7
8
ANALOG INPUT
+
−
.01 μF
*
LH0022
+
−
OUTPUT
SAMPLE/HOLD
9
10
AH0152

*Polystyrene dielectric.

TL/K/5557-16

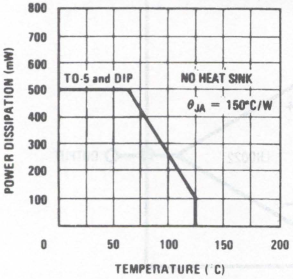
### Re-Zeroing Amplifier

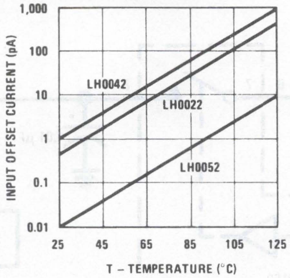

R2
100M
V+
R1
10M
INPUT
2
−
4
LH0022
6
OUTPUT
R3
9M
3
+
7
5
1
C1
10K
TTL
RE ZERO COMMAND
1/2 AH0133
V−

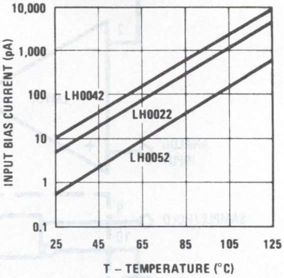
C1—0.01 μF polystyrene.

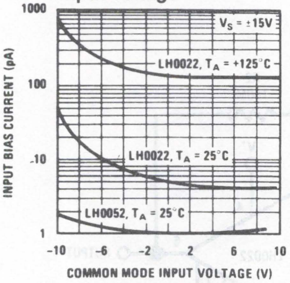
TL/K/5557-17

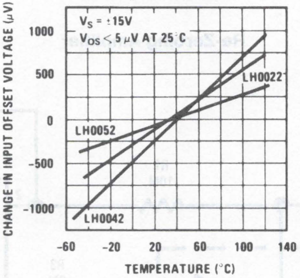
## Typical Performance Characteristics

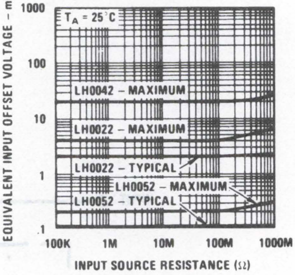

Maximum Power Dissipation

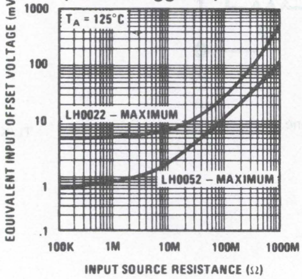

Input Offset Current vs Temperature

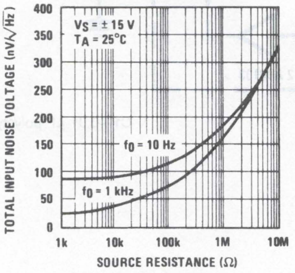

Input Bias Current vs Temperature

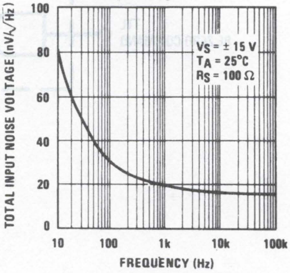

Input Bias Current vs Input Voltage

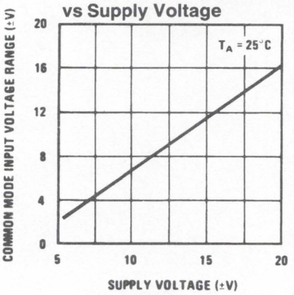

Input Offset Voltage vs Temperature

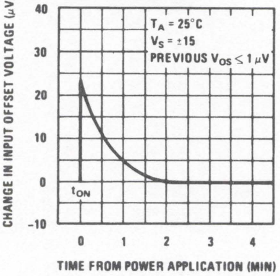

Offset Error (without $V_{OS}$ Null)

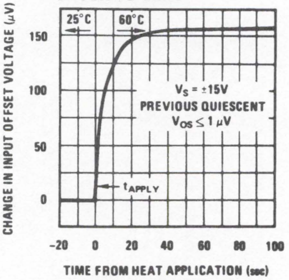

Offset Error (without $V_{OS}$ Null)


Total Input Noise Voltage* vs Source Resistance


Total Input Noise Voltage* vs Frequency


Common Mode Input Voltage vs Supply Voltage


Stabilization Time of Input Offset Voltage from Power Turn-On

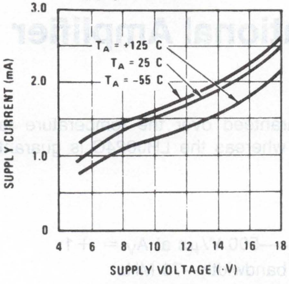

Change in Input Offset Voltage Due to Thermal Shock vs Time

TL/K/5557–18

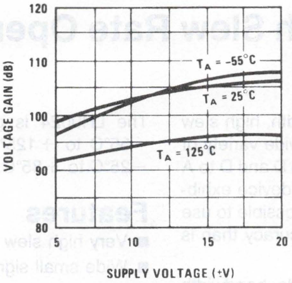
*Noise voltage includes contribution from source resistance.

## Typical Performance Characteristics (Continued)

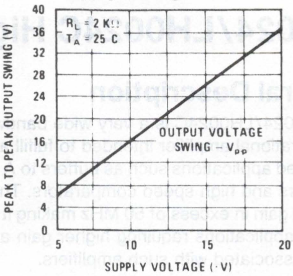
### Supply Voltage vs Supply Current



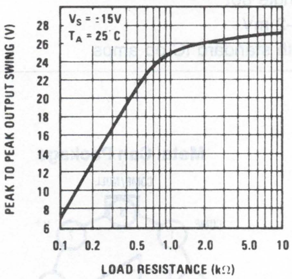
### Voltage Gain



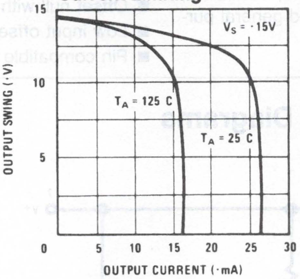
### Output Swing vs Supply Voltage



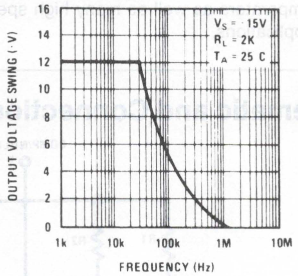
### Output Voltage Swing vs Load Resistance



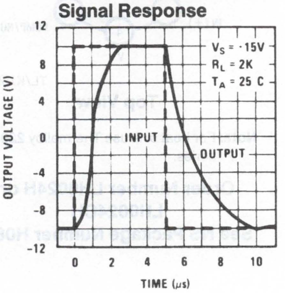
### Current Limiting



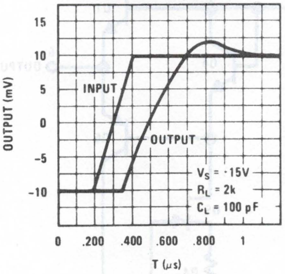
### Output Voltage Swing vs Frequency



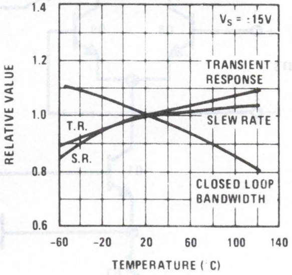
### Voltage Follower Large Signal Response



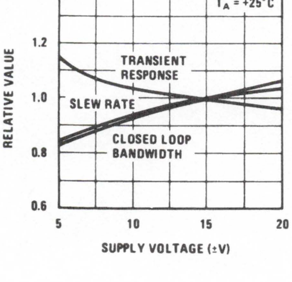
### Transient Response



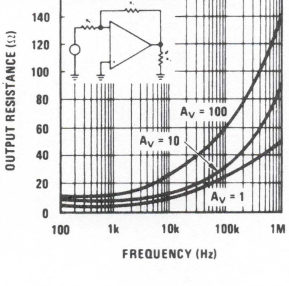
### Frequency Characteristics vs Ambient Temperature



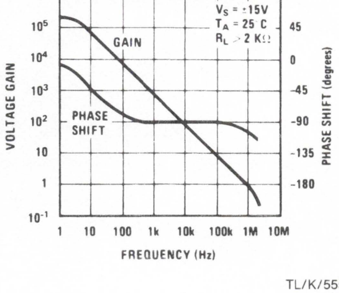
### Frequency Characteristics vs Supply Voltage



### Output Resistance vs Frequency



### Open Loop Transfer Characteristics vs Frequency



TL/K/5557-19

**National Semiconductor Corporation**

# LH0024/LH0024C High Slew Rate Operational Amplifier

## General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

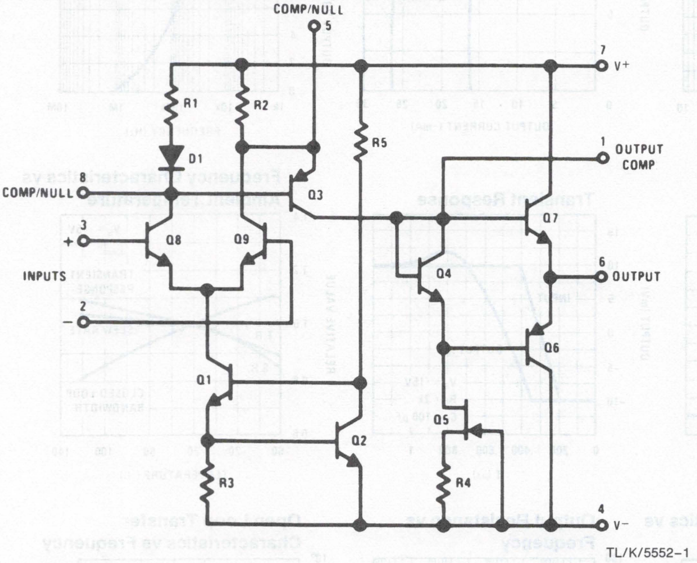
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range −55°C to +125°C, whereas the LH0024C is guaranteed −25°C to +85°C.

## Features

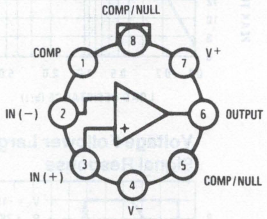
- Very high slew rate—500 V/µs at $A_V = +1$
- Wide small signal bandwidth—70 MHz
- Wide large signal bandwidth—15 MHz
- High output swing—±12V into 1k
- Offset null with single pot
- Low input offset—2 mV
- Pin compatible with standard IC op amps

## Schematic and Connection Diagrams



TL/K/5552-1

**Metal Can Package**



TL/K/5552-2

**Top View**

**Note:** For heat sink use Thermalloy 2230-5 series.

**Order Number LH0024H or LH0024CH**
**See NS Package Number H08B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 2)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage | Equal to Supply |
| Differential Input Voltage | ±5V |
| Power Dissipation | 600 mW |
| Operating Temperature Range | |
| LH0024 | −55°C to +125°C |
| LH0024C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 1)

| Parameter | Conditions | LH0024 | | | LH0024C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25°C$<br>$R_S = 50\Omega$ | | 2.0 | 4.0<br>6.0 | | 5.0 | 8.0<br>10.0 | mV<br>mV |
| Average Temperature Coefficient of Input Offset Voltage | $V_S = \pm 15V$, $R_S = 50\Omega$<br>−55°C to 125°C | | −20 | | | −25 | | μV/°C |
| Input Offset Current | $T_A = 25°C$ | | 2.0 | 5.0<br>10.0 | | 4.0 | 15.0<br>20.0 | μA<br>μA |
| Input Bias Current | $T_A = 25°C$ | | 15 | 30<br>40 | | 18 | 40<br>50 | μA<br>μA |
| Supply Current | | | 12.5 | 15 | | 12.5 | 15 | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$<br>$V_S = \pm 15V$, $R_L = 1k$ | 4<br>3 | 5 | | 3<br>2.5 | 4 | | V/mV<br>V/mV |
| Input Voltage Range | $V_S = \pm 15V$ | ±12 | ±13 | | ±12 | ±13 | | V |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$<br>$V_S = \pm 15V$, $R_L = 1k$ | ±12<br>±10 | ±13 | | ±10<br>±10 | ±13 | | V<br>V |
| Slew Rate | $V_S = \pm 15V$, $R_L = 1k$,<br>$C_1 = C_2 = 30$ pF,<br>$A_V = +1$, $T_A = 25°C$ | 400 | 500 | | 250 | 400 | | V/μs |
| Common-Mode Rejection Ratio | $V_S = \pm 15V$, $\Delta V_{IN} = \pm 10V$,<br>$R_S = 50\Omega$ | | 60 | | | 60 | | dB |
| Power Supply Rejection Ratio | $\pm 5V \leq V_S \leq \pm 18V$,<br>$R_S = 50\Omega$ | | 60 | | | 60 | | dB |

**Note 1:** These specifications apply for $V_S = \pm 15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

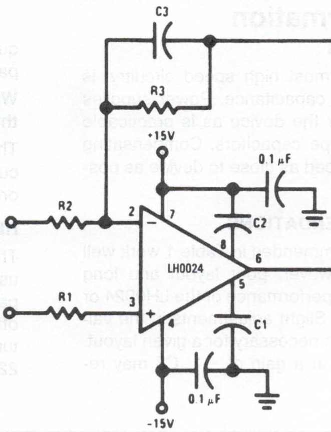
**Note 2:** Refer to RETS0024H for LH0024H military specifications.

## Frequency Compensation

**TABLE I**

| Closed Loop Gain | $C_1$ | $C_2$ | $C_3$ |
|---|---|---|---|
| 100 | 0 | 0 | 0 |
| 20 | 0 | 0 | 0 |
| 10 | 0 | 20 pF | 1 pF |
| 1 | 30 pF | 30 pF | 3 pF |

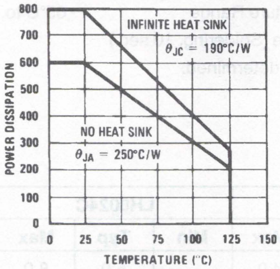
**Frequency Compensation Circuit**



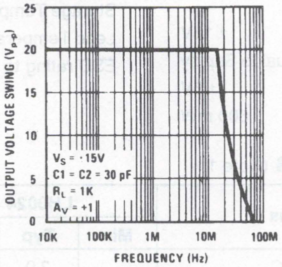
TL/K/5552–6

## Typical Performance Characteristics

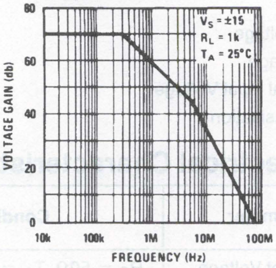
Maximum Power Dissipation



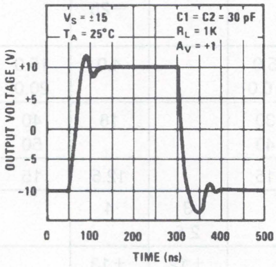
Large Signal Frequency Response



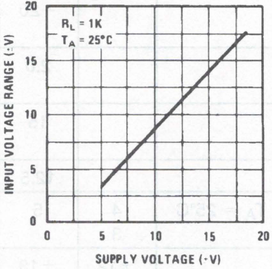
Open Loop Frequency Response



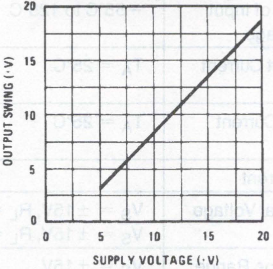
Voltage Follower Pulse Response



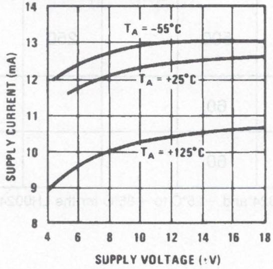
Input Voltage vs Supply Voltage



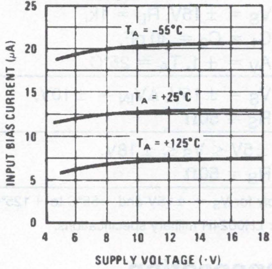
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



TL/K/5552-7

## Applications Information

### LAYOUT CONSIDERATIONS

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least 0.01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

### COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

**When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1 kΩ.**

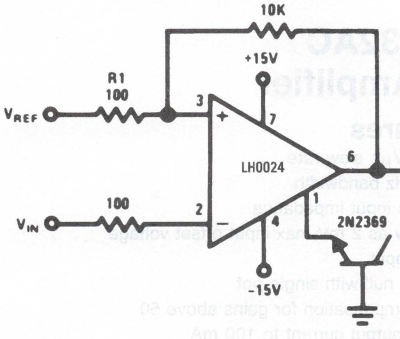
The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

### HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

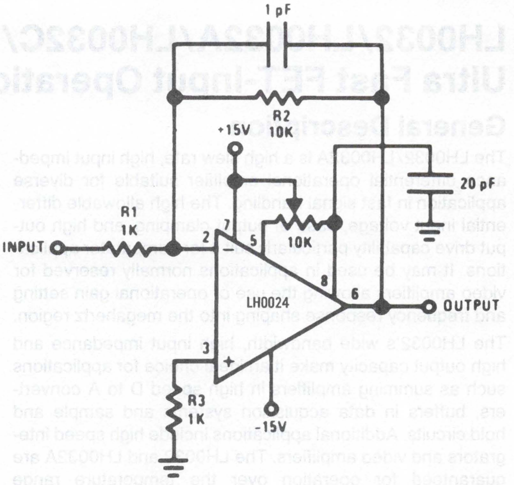
## Typical Applications

### TTL Compatible Comparator


10K
+15V
R1
100
V_REF
3
+
7
LH0024
6
1
100
V_IN
2
−
4
2N2369
−15V

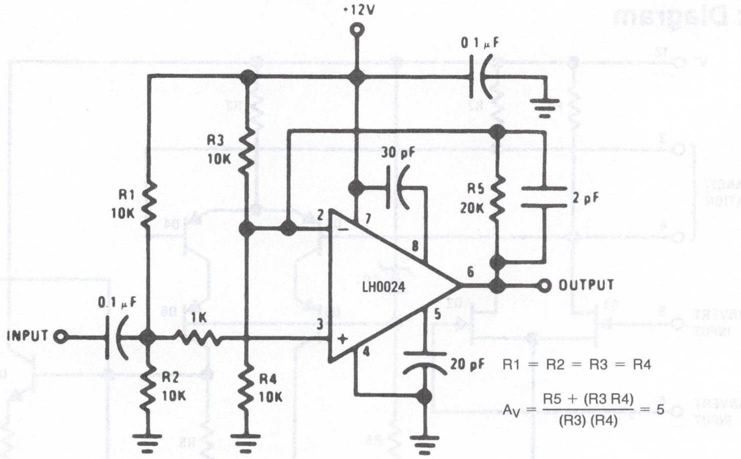
TL/K/5552-3

### Offset Null


1 pF
R2
10K
+15V
20 pF
R1
1K
INPUT
2
7
5
10K
−
8
LH0024
6
OUTPUT
3
+
R3
1K
−15V

TL/K/5552-4

### Video Amplifier


+12V
0.1 µF
R3
10K
30 pF
R5
20K
2 pF
R1
10K
2
−
7
8
6
OUTPUT
LH0024
0.1 µF
INPUT
1K
3
+
5
4
20 pF
R2
10K
R4
10K

R1 = R2 = R3 = R4

$$A_V = \frac{R5 + (R3\ R4)}{(R3)\ (R4)} = 5$$

TL/K/5552-5

**National Semiconductor Corporation**

**PRELIMINARY**

# LH0032/LH0032A/LH0032C/LH0032AC Ultra Fast FET-Input Operational Amplifier

## General Description

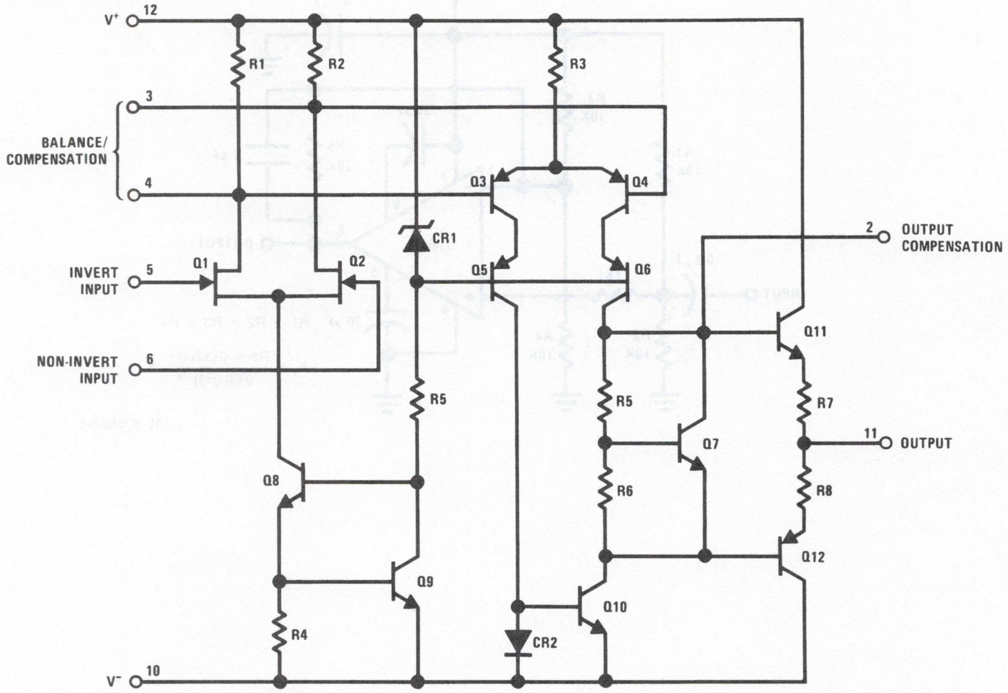
The LH0032/LH0032A is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 and LH0032A are guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C and LH0032AC are guaranteed for −25°C to +85°C.

## Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

## Block Diagram


V+
12
R1
R2
R3
3
BALANCE/
COMPENSATION
4
Q3
Q4
CR1
2
OUTPUT
COMPENSATION
INVERT
INPUT
5
Q1
Q2
Q5
Q6
Q11
NON-INVERT
INPUT
6
R5
R5
R7
11
OUTPUT
Q7
Q8
R6
R8
Q12
Q9
Q10
R4
CR2
V-
10

TL/K/5265-1

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_S$ | ±18V |
| Input Voltage, $V_{IN}$ | $\pm V_S$ |
| Differential Input Voltage | ±30V or $\pm 2V_S$ |
| Power Dissipation, $P_D$ | |
| $T_A = 25°C$ | 1.5W, derate 100°C/W to 125°C (Note 1) |
| $T_C = 25°C$ | 2.2W, derate 70°C/W to 125°C (Note 1) |
| Operating Temperature Range, $T_A$ | |
| LH0032G/AG/E | −55°C to +125°C |
| LH0032CG/ACG | −25°C to +85°C |
| Operating Junction Temperature, $T_J$ | 175°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

## DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_j$)

| Symbol | Parameter | Test Conditions | | LH0032A | | | LH0032AC | | | LH0032 | | | LH0032C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $V_{IN} = 0$ | $T_A = T_J = 25°C$ (Note 3) | | 1 | 2<br>5 | | 2 | 5<br>7 | | 2 | 5<br>10 | | 2 | 15<br>20 | mV |
| $\Delta V_{OS}/\Delta T$ | Average Offset Voltage Drift | | (Note 4) | | 15 | 30 | | 15 | 30 | | 15 | 50 | | 15 | 50 | μV/°C |
| $I_{OS}$ | Input Offset Current | | $T_J = 25°C$ (Note 3)<br>$T_A = 25°C$ (Note 5) | | | 10<br>250<br>10 | | | 30<br>500<br>3 | | | 25<br>250<br>25 | | | 50<br>500<br>5 | pA<br>pA<br>nA |
| $I_B$ | Input Bias Current | | $T_J = 25°C$ (Note 3)<br>$T_A = 25°C$ (Note 5) | | | 50<br>1<br>25 | | | 150<br>5<br>10 | | | 100<br>1<br>50 | | | 500<br>5<br>15 | pA<br>nA<br>nA |
| *$V_{INCM}$ | Input Voltage Range | | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | V |
| CMRR | Common Mode Rejection Ratio | $\Delta V_{IN} = \pm 10V$ | | 50 | 60 | | 50 | 60 | | 50 | 60 | | 50 | 60 | | dB |
| $A_{VOL}$ | Open-Loop Voltage Gain | $V_O = \pm 10V$, f = 1 kHz $R_L = 1\ k\Omega$ (Note 6) | $T_J = 25°C$ | 60 | 70 | | 60 | 70 | | 60 | 70 | | 60 | 70 | | dB |
| | | | | 57 | | | 57 | | | 57 | | | 57 | | | |
| $V_O$ | Output Voltage Swing | $R_L = 1\ k\Omega$ | | ±10 | ±13.5 | | ±10 | ±13 | | ±10 | ±13.5 | | ±10 | ±13 | | V |
| $I_S$ | Power Supply Current | $T_A = 25°C$, $I_O = 0$ (Note 5) | | | 18 | 20 | | 20 | 22 | | 18 | 20 | | 20 | 22 | mA |
| PSRR | Power Supply Rejection Ratio | $\Delta V_S = 10V$ (±5 to ±15V) | | 50 | 60 | | 50 | 60 | | 50 | 60 | | 50 | 60 | | dB |

## AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$ (Note 7)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $S_R$ | Slew Rate | $A_V = +1$ | $\Delta V_{IN} = 20V$ | 350 | 500 | | V/μs |
| $t_s$ | Settling Time to 1% of Final Value | $A_V = -1$, | | | 100 | | ns |
| $t_s$ | Settling Time to 0.1% of Final Value | | | | 300 | | |
| $t_R$ | Small Signal Rise Time | $A_V = +1$, $\Delta V_{IN} = 1V$ | | | 8 | 20 | |
| $t_D$ | Small Signal Delay Time | | | | 10 | 25 | |

**Note 1.** In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when $T_A$ or $T_C$ exceeds specific values depending on the $P_D$ within the device package. Total $P_D$ is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

**Note 2.** LH0032AG/G are 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032ACG/CG are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

**Note 3.** Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25$ C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, $V_{OS}$ may change one to several mV, and $I_B$ and $I_{OS}$ will change significantly during warm-up. Refer to $I_B$ and $I_{OS}$ vs. temperature graph for expected values.

**Note 4.** LH0032AG/G are 100% production tested for this parameter. LH0032ACG/CG are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and $T_{MAX}$.

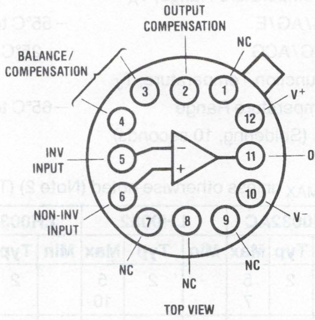
**Note 5.** Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

**Note 6.** Guaranteed thru correlated automatic pulse testing at $T_J = 25°C$.

**Note 7.** Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

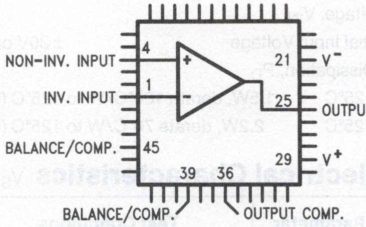
*Guaranteed by CMRR test condition.

## Connection Diagrams


OUTPUT COMPENSATION
BALANCE/ COMPENSATION
NC
$V^+$
3
2
1
4
12
INV INPUT
5
11
OUT
6
10
NON-INV INPUT
7
8
9
$V^-$
NC
NC
NC
TOP VIEW

TL/K/5265-23

**Order Number LH0032G, LH0032AG, LH0032CG or LH0032ACG**
**See NS Package Number G12B**

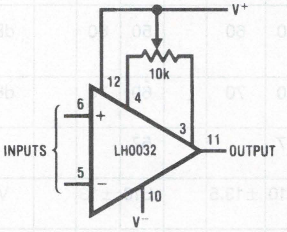

NON-INV. INPUT
4
INV. INPUT
1
BALANCE/COMP.
45
21
$V^-$
25
OUTPUT
29
$V^+$
39
36
BALANCE/COMP.
OUTPUT COMP.

TL/K/5265-25

**Order Number LH0032E**
**See NS Package Number E48B**

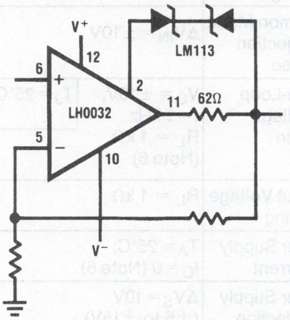
## Auxiliary Circuits

**Offset Null**


$V^+$
10k
12
4
6
3
11
OUTPUT
INPUTS
LH0032
5
10
$V^-$

TL/K/5265-15

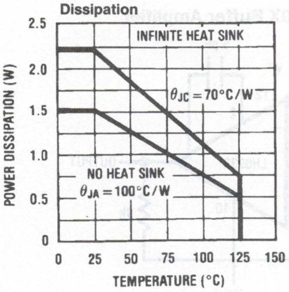
**Output Short Circuit Protection**


$V^+$
LM113
12
6
2
11
62Ω
LH0032
5
10
$V^-$

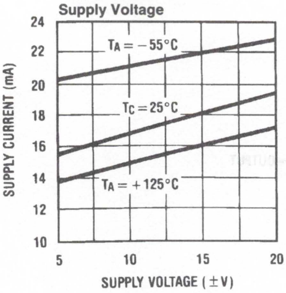
TL/K/5265-16

## Typical Performance Characteristics

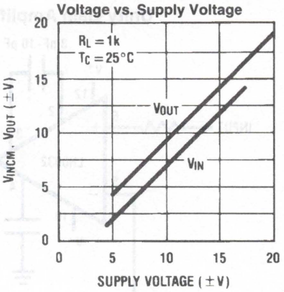
**Maximum Power Dissipation**



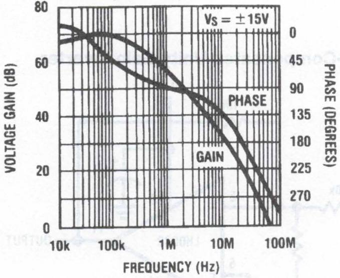
**Supply Current vs. Supply Voltage**



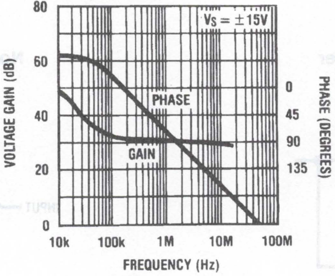
**Input Voltage Range and Output Voltage vs. Supply Voltage**



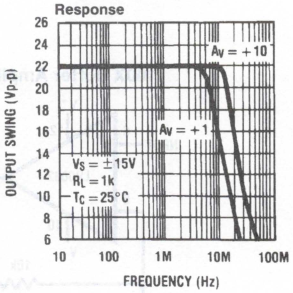
**Bode Plot (Uncompensated)**



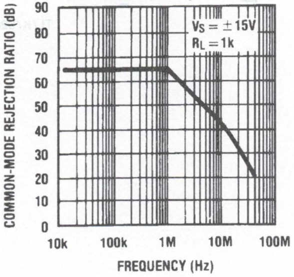
**Bode Plot (Unity Gain Compensation)**



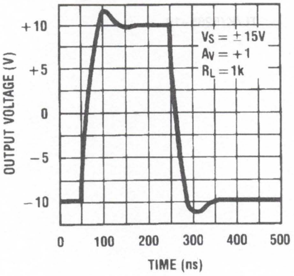
**Large Signal Frequency Response**



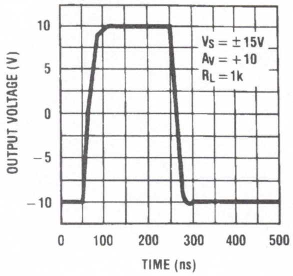
**Common Mode Rejection Ratio vs. Frequency**



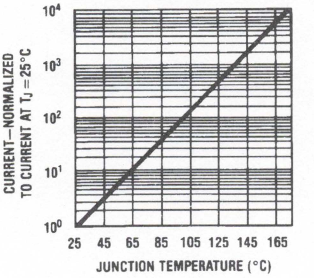
**Large Signal Pulse Response**



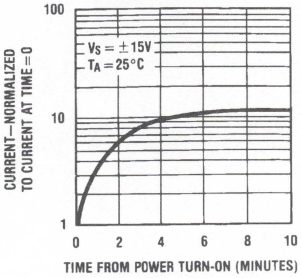
**Large Signal Pulse Response**



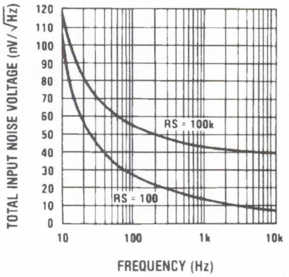
**Normalized Input Bias and Offset Current vs. Junction Temperature**



**Normalized Input Bias Current During Warm-Up**



**Total Input Noise Voltage vs. Frequency***

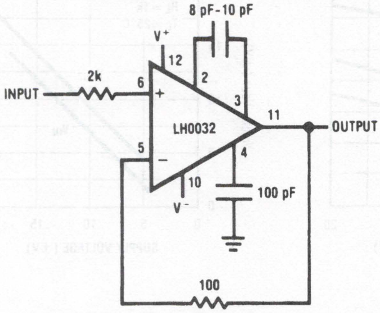


TL/K/5265-2

*Noise voltage includes contribution from source resistance.

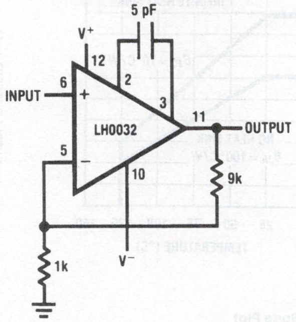
# Typical Applications

**Unity Gain Amplifier**


8 pF-10 pF
V+
12
2
INPUT
2k
6
+
3
11
OUTPUT
LH0032
5
−
4
10
100 pF
V−
100

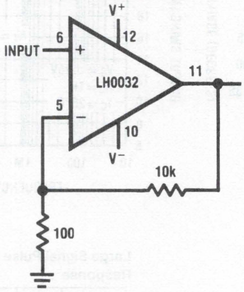
TL/K/5265-17

**10X Buffer Amplifier**


5 pF
V+
12
2
INPUT
6
+
3
11
OUTPUT
LH0032
5
−
10
9k
1k
V−

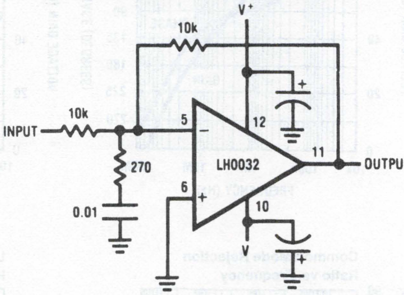
TL/K/5265-18

**100X Buffer Amplifier**


V+
12
INPUT
6
+
LH0032
11
5
−
10
V−
10k
100

TL/K/5265-19

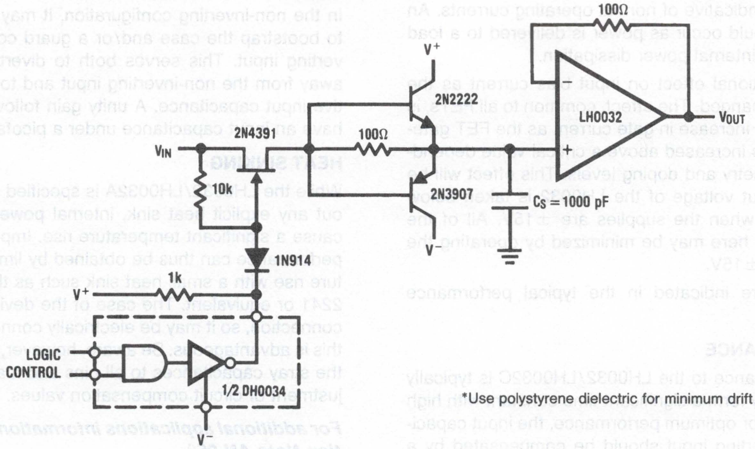
**Non-Compensated Unity Gain Inverter**


V+
10k
+
10k
INPUT
5
−
12
270
LH0032
11
OUTPUT
6
+
0.01
10
V
+

TL/K/5265-20

## Typical Applications (Continued)

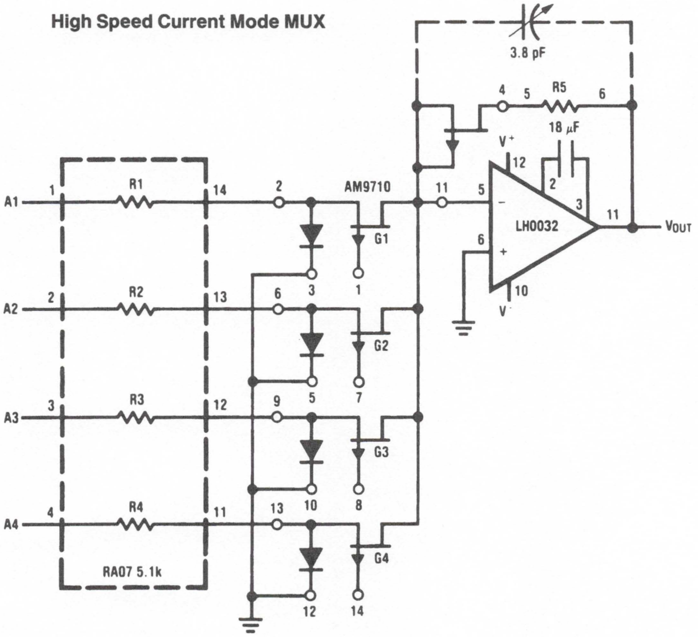
**High Speed Sample and Hold**


V+
100Ω
2N2222
LH0032
VOUT
2N4391
100Ω
VIN
−
+
10k
2N3907
CS = 1000 pF
V−
1N914
1k
V+
LOGIC
CONTROL
1/2 DH0034
V−

*Use polystyrene dielectric for minimum drift

TL/K/5265-21

**High Speed Current Mode MUX**


3.8 pF
4
5
R5
6
18 µF
V+
12
2
3
AM9710
11
5
LH0032
11
VOUT
6
10
V−
A1
1
R1
14
2
G1
1
3
A2
2
R2
13
6
G2
5
7
A3
3
R3
12
9
G3
10
8
A4
4
R4
11
13
G4
12
14
RA07 5.1k

TL/K/5265-22

## Applications Information

### POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 µF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

### INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

## Applications Information (Continued)

vice temperature will stabilize within 5-10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

### INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

### HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

***For additional applications information request Application Note AN-253.***

**National Semiconductor Corporation**

# LH0044 Series Precision Low Noise Operational Amplifiers

## General Description

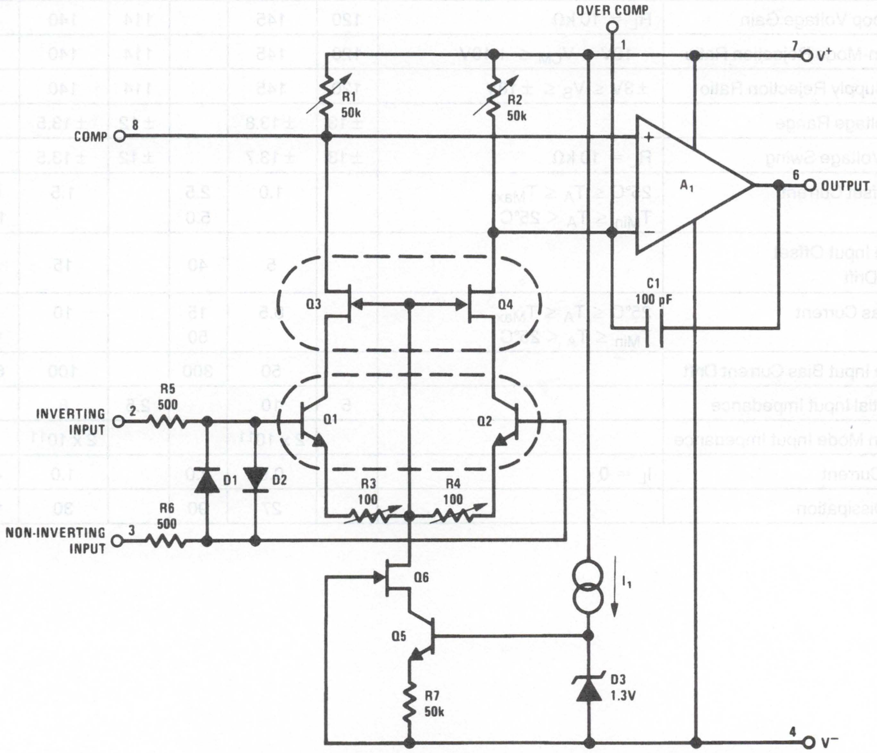
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 is guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

## Features

| | |
|---|---|
| ■ Low input offset voltage | 25μV max |
| ■ Excellent long-term stability | ±1μV/month max |
| ■ Low offset drift | 0.5μV/°C max |
| ■ Very low noise | 0.7μVp-p max 0.1 Hz to 10 Hz |
| ■ High CMRR and PSRR | 120 dB min |
| ■ High open loop gain | 120 dB min |
| ■ Wide common-mode range | ±13V min |
| ■ Wide supply voltage range | ±2V to ±20V |

## Equivalent Circuit



TL/K/5551–1

# Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation | 600 mW |
| Differential Input Voltage (Note 4) | ±1V |
| Input Voltage (Note 5) | ±15V |
| Output Short-Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0044 | −55°C to +125°C |
| LH0044AC, LH0044B, LH0044C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

# DC Electrical Characteristics (Note 1)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0044AC | | | LH0044/ LH0044B/LH0044C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$, $R_S = 50\Omega$, $V_{CM} = 0V$<br>LH0044C Only | | 8 | 25 | | 12 | 50<br>100 | µV<br>µV |
| Input Offset Voltage | $R_S = 50\Omega$, $V_{CM} = 0V$<br>LH0044A and LH0044B Only | | | 55<br>75 | | | 180<br>80 | µV<br>µV |
| Average Input Offset Voltage Drift | $T_{Min} \le T_A \le T_{Max}$<br>LH0044B Only | | 0.1 | 0.5 | | 0.2 | 1.3<br>0.5 | µV/°C<br>µV/°C |
| Long-Term Stability | (Note 2) | | 0.2 | 1 | | 0.3 | 2 | µV/month |
| Input Noise Voltage (Note 3) | BW = 0.1 Hz to 10 Hz, $R_S = 50\Omega$<br>$R_S = 10\ k\Omega$ Imbalance | | 0.35<br>0.50 | 0.7<br>0.9 | | 0.35<br>0.50 | 0.8<br>1.0 | µVp-p<br>µVp-p |
| Thermal Feedback Coefficient | | | 0.005 | | | 0.005 | | µV/mW |
| Open Loop Voltage Gain | $R_L = 10\ k\Omega$ | 120 | 145 | | 114 | 140 | | dB |
| Common-Mode Rejection Ratio | $-10V \le V_{CM} \le +10V$ | 120 | 145 | | 114 | 140 | | dB |
| Power Supply Rejection Ratio | $\pm 3V \le V_S \le \pm 18V$ | 120 | 145 | | 114 | 140 | | dB |
| Input Voltage Range | | ±13 | ±13.8 | | ±12 | ±13.5 | | V |
| Output Voltage Swing | $R_L = 10\ k\Omega$ | ±13 | ±13.7 | | ±12 | ±13.5 | | V |
| Input Offset Current | $25°C \le T_A \le T_{Max}$<br>$T_{Min} \le T_A < 25°C$ | | 1.0 | 2.5<br>5.0 | | 1.5 | 5.0<br>10.0 | nA<br>nA |
| Average Input Offset Current Drift | | | 5 | 40 | | 15 | 80 | pA/°C |
| Input Bias Current | $25°C \le T_A \le T_{Max}$<br>$T_{Min} \le T_A < 25°C$ | | 8.5 | 15<br>50 | | 10 | 30<br>100 | nA<br>nA |
| Average Input Bias Current Drift | | | 50 | 300 | | 100 | 600 | pA/°C |
| Differential Input Impedance | | 5 | 10 | | 2.5 | 8 | | MΩ |
| Common Mode Input Impedance | | | $2 \times 10^{11}$ | | | $2 \times 10^{11}$ | | Ω |
| Supply Current | $I_L = 0$ | | 0.9 | 3.0 | | 1.0 | 4.0 | mA |
| Power Dissipation | | | 27 | 90 | | 30 | 120 | mW |

## AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

| Parameter | Conditions | Typ | Units |
|---|---|---|---|
| Input Noise Voltage | $R_S = 1\ k\Omega, f_O = 10\ Hz$<br>$R_S = 1\ k\Omega, f_O = 1\ kHz$ | 11<br>9 | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| Slew Rate | $A_V = +1, R_L = 10\ k\Omega, V_{IN} = \pm 10V$ | 0.06 | $V/\mu s$ |
| Large Signal Bandwidth | $A_V = +1, R_L = 10\ k\Omega, V_{IN} = \pm 10V$ | 1 | kHz |
| Overload Recovery Time | $A_V = +100, V_{IN} = -100\ mV, \Delta V_{IN} = 200\ mV$ | 5 | $\mu s$ |
| Small Signal Bandwidth | $A_V = +1, R_L = 10\ k\Omega$ | 400 | kHz |
| Small Signal Rise Time | $A_V = +1, R_L = 10\ k\Omega, V_{IN} = 10\ mV$ | 2.5 | $\mu s$ |
| Overshoot | $A_V = +1, R_L = 10\ k\Omega, V_{IN} = 10\ mV, C_L = 100\ pF$ | 10 | % |

**Note 1:** All specifications apply for all device grades, at $V_S = \pm 15V$, and from $T_{Min}$ to $T_{Max}$ unless otherwise specified. $T_{Min}$ is $-55°C$ and $T_{Max}$ is $+125°C$ for the LH0044. $T_{Min}$ is $-25°C$ and $T_{Max}$ is $+85°C$ for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

**Note 2:** This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

**Note 3:** Noise is 100% tested on the LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

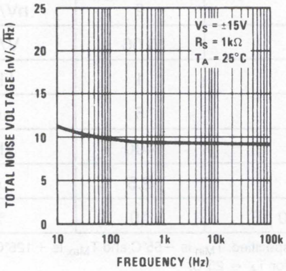
**Note 4:** The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

**Note 5:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

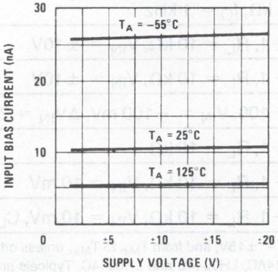
**Note 6:** Refer to RETS0044AH for LH0044AH military specifications and RETS0044H for LH0044H military specfications.

## Typical Performance Characteristics

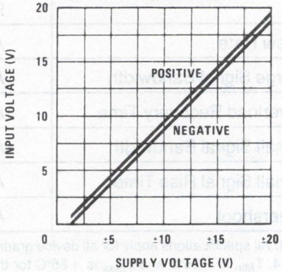
### Total Input Noise Voltage vs Frequency



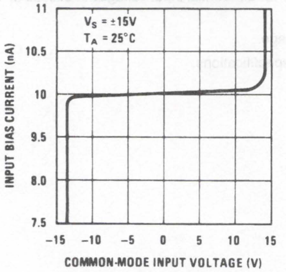
### Input Bias Current



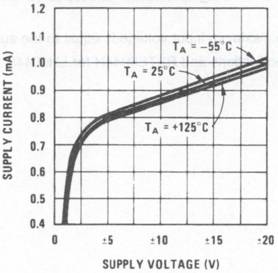
### Input Voltage Range



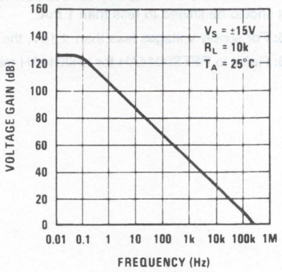
### Input Bias Current vs Common-Mode Input Voltage



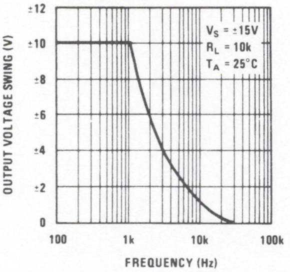
### Supply Current vs Supply Voltage



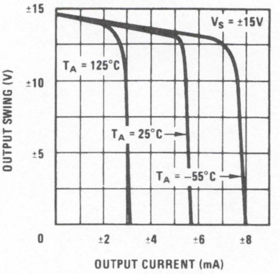
### Open Loop Frequency Response



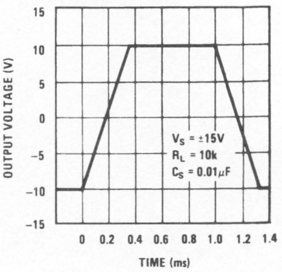
### Large Signal Voltage Response



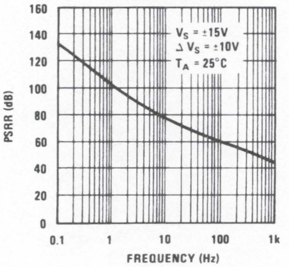
### Output Swing



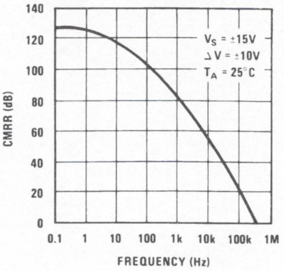
### Large Signal Pulse Response



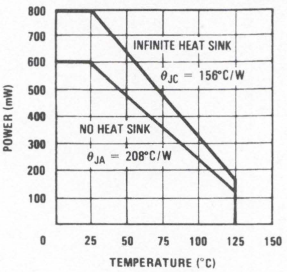
### Power Supply Rejection Ratio vs Frequency



### CMRR vs Frequency



### Maximum Power Dissipation



TL/K/5551–3

# Applications Information

## LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

## OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\text{ pF} + C_{ext}\text{ pF}}\ \text{(Hz)}$$

## COMPENSATION

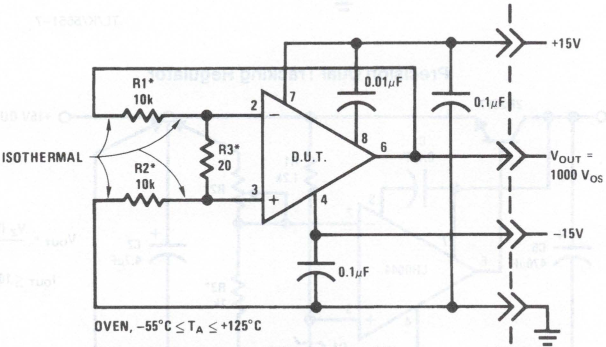
For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01 $\mu$F disc capacitor is recommended between pin 7 ($V^+$) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01 $\mu$F capacitor.

## OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to $V^+$. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

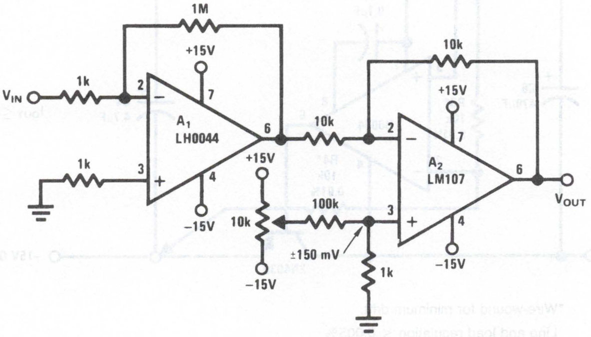
The recommended technique for offset nulling the LH0044 is shown in *Figure 2*. Null is accomplished in $A_2$ and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to the use of $A_2$ is less than 1 $\mu$V/V for $V^+$ and $V^-$ changes and 0.01 $\mu$V/°C drift for the values shown in *Figure 2*.



*Wire-wound construction (TCR ≤ 10 ppp/°C)

TL/K/5551–4

FIGURE 1. LH0044 Temperature Test Circuit

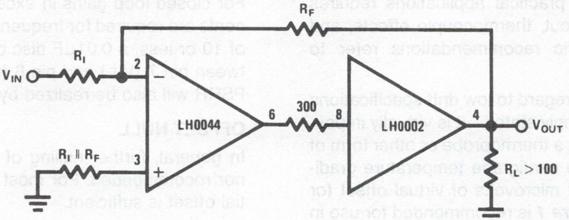


TL/K/5551–5

FIGURE 2. LH0044 Null Technique

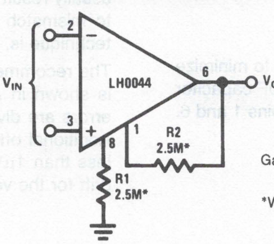
## Typical Applications

### Buffered Output for Heavy Loads


R<sub>F</sub>
R<sub>I</sub>
V<sub>IN</sub>
2
−
LH0044
3
+
R<sub>I</sub> ‖ R<sub>F</sub>
6
300
8
LH0002
4
V<sub>OUT</sub>
R<sub>L</sub> > 100

TL/K/5551-6

### X1000 Instrumentation Amp


2
−
V<sub>IN</sub>
LH0044
3
+
6
V<sub>OUT</sub>
1
8
R2
2.5M*
R1
2.5M*

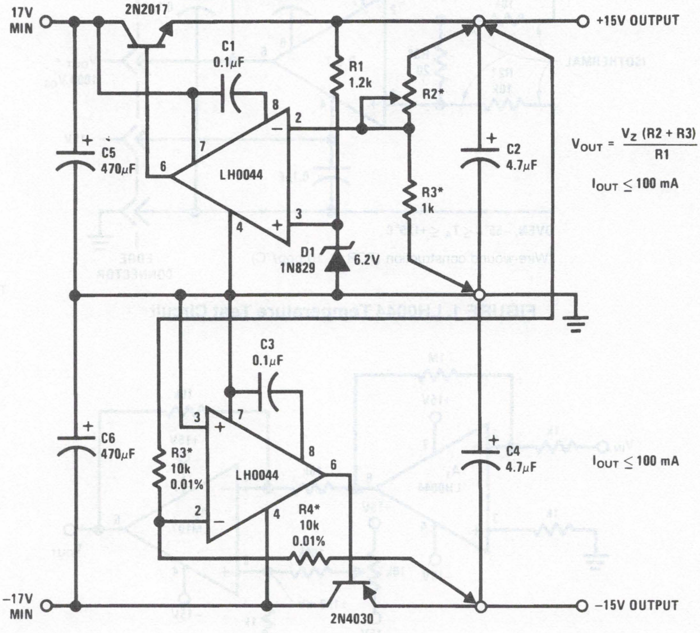
Gain = $g_m R_L$

$\geq 0.2 \times 10^3$ (R1 + R2) for $V_{IN} \leq 10$ mV

*Wire-wound resistors

TL/K/5551-7

### Precision Dual Tracking Regulator


17V
MIN
2N2017
C1
0.1μF
8
2
−
R1
1.2k
R2*
+15V OUTPUT
+
C5
470μF
7
6
LH0044
3
+
4
C2
4.7μF
R3*
1k
D1
1N829
6.2V
C3
0.1μF
3
+
7
+
C6
470μF
R3*
10k
0.01%
LH0044
8
6
2
−
4
R4*
10k
0.01%
+
C4
4.7μF
−17V
MIN
2N4030
−15V OUTPUT

$V_{OUT} = \dfrac{V_Z\,(R2 + R3)}{R1}$

$I_{OUT} \leq 100$ mA

$I_{OUT} \leq 100$ mA

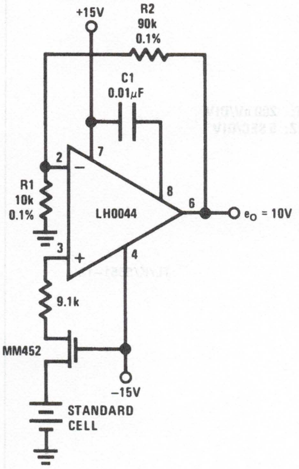
TL/K/5551-8

*Wire-wound for minimum drift.

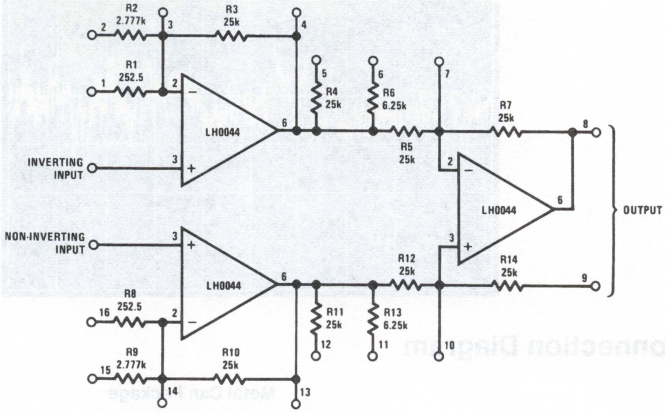
Line and load regulation ≤ 0.005%

## Typical Applications (Continued)

### 10V Reference Supply


+15V
R2
90k
0.1%
C1
0.01μF
7
2
R1
10k
0.1%
LH0044
8
6
$e_O$ = 10V
3
4
9.1k
1/4 MM452
−15V
STANDARD
CELL

TL/K/5551-9

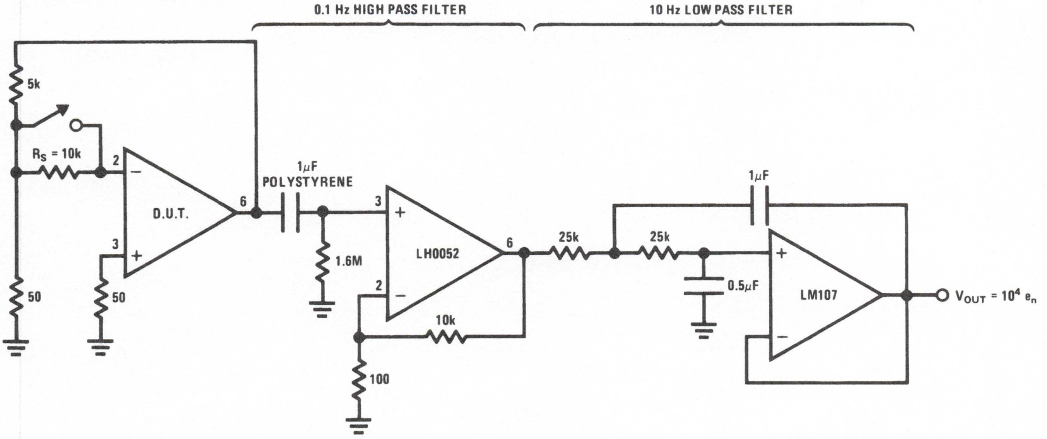

R2
2.777k
2
3
R3
25k
4
R1
252.5
1
2
5
R4
25k
6
R6
6.25k
7
LH0044
6
R5
25k
R7
25k
8
INVERTING
INPUT
3
2
LH0044
6
OUTPUT
NON-INVERTING
INPUT
3
3
LH0044
6
R12
25k
R14
25k
9
R8
252.5
16
2
R11
25k
R13
6.25k
12
11
10
R9
2.777k
15
14
R10
25k
13

TL/K/5551-10

### Precision Instrumentation Amplifier

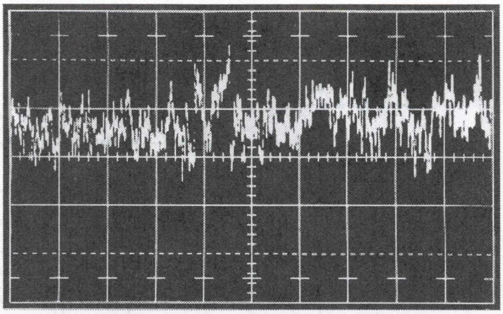
| Overall Gain | Input Stage Gain | Output Stage Gain |
|---|---|---|
| X1 | X1 | X1 |
| X2 | X1 | X2 |
| X5 | X1 | X5 |
| X10 | X10 | X1 |
| X20 | X10 | X2 |
| X50 | X10 | X5 |
| X100 | X100 | X1 |
| X200 | X100 | X2 |
| X500 | X100 | X5 |
| X995 | X199 | X5 |

## Noise Test Circuit


0.1 Hz HIGH PASS FILTER
10 Hz LOW PASS FILTER
5k
$R_S$ = 10k
2
D.U.T.
6
3
50
50
1μF
POLYSTYRENE
1.6M
3
LH0052
6
2
10k
100
25k
25k
1μF
0.5μF
LM107
$V_{OUT} = 10^4 e_n$

TL/K/5551-11

## Noise Test Circuit (Continued)

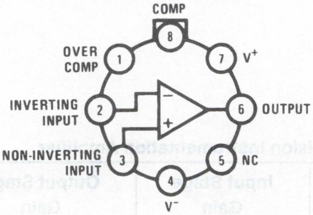


VERT: 200 nV/DIV
HORIZ: 5 SEC/DIV

TL/K/5551–12

## Connection Diagram

**Metal Can Package**


COMP
8
OVER
COMP
1
7
V+
INVERTING
INPUT
2
6
OUTPUT
NON-INVERTING
INPUT
3
5
NC
4
V−

TL/K/5551–2

**Top View**

Case is electrically isolated

**Note:** Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

**Order Number LH0044H, LH0044CH,**
**LH0044ACH or LH0044BH**
**See NS Package Number H08B**

**National Semiconductor Corporation**

# LH0045/LH0045C Two Wire Transmitter

## General Description

The LH0045/LH0045C Two Wire Transmitters are linear integrated circuits designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 and LH0045C contain an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0 mA to 20 mA or 10 mA to 50 mA.

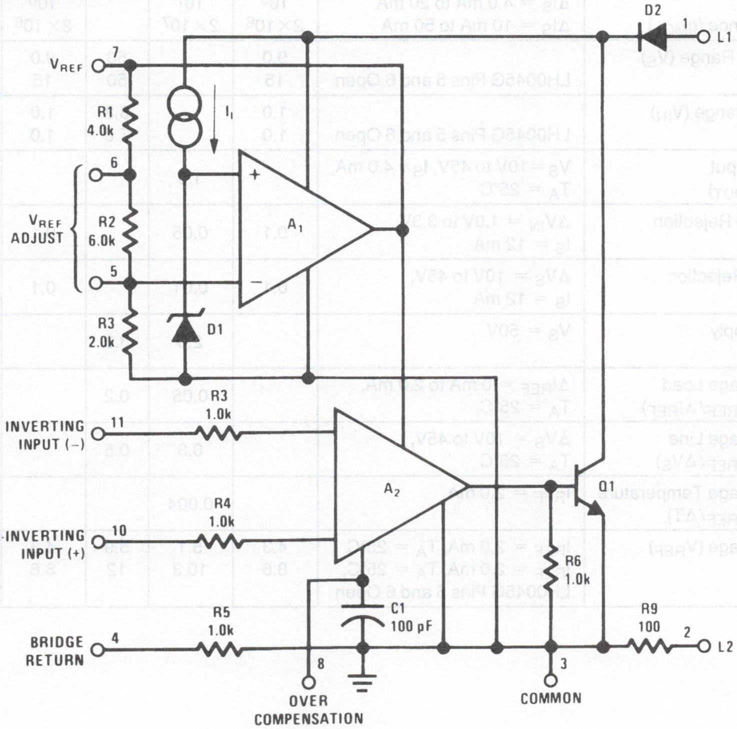
Designed for use with various sensors, the LH0045/LH0045C will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

The LH0045/LH0045C is intended to fulfill a wide variety of process control, instrumentation, and data acquisition applications. The LH0045 is guaranteed over the temperature range of −55°C to +125°C; whereas the LH0045C is guaranteed from −25°C to +85°C.

## Features

| | |
|---|---|
| ■ High sensitivity | ≥10 μA/μV |
| ■ Low input offset voltage | 1.0 mV |
| ■ Low input bias current | 2.0 nA |
| ■ Single supply operation | 10V to 50V |
| ■ Programmable bridge reference (LH0045G) | 5.0V to 30V |
| ■ Non-interactive span and null adjust | |
| ■ Over compensation capability | |
| ■ Supply reversal protection | |

## Equivalent Schematic


D2
1
L1
$V_{REF}$
7
R1
4.0k
$I_1$
6
$V_{REF}$ ADJUST
R2
6.0k
5
+
−
$A_1$
R3
2.0k
D1
R3
1.0k
INVERTING INPUT (−)
11
$A_2$
Q1
R4
1.0k
NON-INVERTING INPUT (+)
10
R6
1.0k
C1
100 pF
R5
1.0k
BRIDGE RETURN
4
8
OVER COMPENSATION
3
COMMON
R9
100
2
L2

***Note:** Pins shown are for the 12 pin to 8 ("G") package.

TL/K/5556–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)**

| | |
|---|---|
| Supply Voltage (L1 to common) | +50V |
| Input Current | +20 mA |
| Input Voltage (Either Input to Common) | 0V to $V_{REF}$ |
| Differential Input Voltage | ±20V |
| Output Current (Either L1 or L2) | 50 mA |
| Reference Output Current | 5.0 mA |
| Power Dissipation | |
| LH0045G | 1.5W |
| Operating Temperature Range | |
| LH0045 | −55°C to +125°C |
| LH0045C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +260°C |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0045 | | | LH0045C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($V_{OS}$) | $I_S$ = 4.0 mA, $T_A$ = 25°C | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| | $I_S$ = 4.0 mA | | | 3.0 | | | 10 | mV |
| Offset Voltage Temperature Coefficient ($\Delta V_{OS}/\Delta T$) | $I_S$ = 4.0 mA | | 3.0 | | | 6.0 | | μV/°C |
| Input Bias Current ($I_B$) | $T_A$ = 25°C | | 0.8 | 2.0 | | 1.5 | 7.0 | nA |
| | | | | 3.0 | | | 10 | nA |
| Input Offset Current ($I_{OS}$) | $T_A$ = 25°C | | 0.05 | 0.2 | | 0.2 | 1.0 | nA |
| | | | | 0.4 | | | 1.5 | nA |
| Open Loop Transconductance ($g_{MOL}$) | $\Delta I_S$ = 4.0 mA to 20 mA | $10^6$ | $10^7$ | | $10^6$ | $10^7$ | | μΩ |
| | $\Delta I_S$ = 10 mA to 50 mA | $2\times10^6$ | $2\times10^7$ | | $2\times10^6$ | $2\times10^7$ | | μΩ |
| Supply Voltage Range ($V_S$) | | 9.0 | | 50 | 9.0 | | 50 | V |
| | LH0045G Pins 5 and 6 Open | 15 | | 50 | 15 | | 50 | V |
| Input Voltage Range ($V_{IN}$) | | 1.0 | | 3.3 | 1.0 | | 3.3 | V |
| | LH0045G Pins 5 and 6 Open | 1.0 | | 7.6 | 1.0 | | 7.6 | V |
| Open Loop Output Impedance ($R_{OUT}$) | $V_S$ = 10V to 45V, $I_S$ = 4.0 mA, $T_A$ = 25°C | | 1.0 | | | 1.0 | | MΩ |
| Common Mode Rejection Ratio (CMRR) | $\Delta V_{IN}$ = 1.0V to 3.3V, $I_S$ = 12 mA | 0.1 | 0.05 | | 0.1 | 0.05 | | mV/V |
| Power Supply Rejection Ratio (PSRR) | $\Delta V_S$ = 10V to 45V, $I_S$ = 12 mA | 0.1 | 0.01 | | 0.1 | 0.01 | | mV/V |
| Open Loop Supply Current ($I_{SOL}$) | $V_S$ = 50V | | 2.0 | 3.0 | | 2.0 | 3.0 | mA |
| Reference Voltage Load Regulation ($\Delta V_{REF}/\Delta I_{REF}$) | $\Delta I_{REF}$ = 0 mA to 2.0 mA, $T_A$ = 25°C, | | 0.05 | 0.2 | | 0.05 | 0.2 | % |
| Reference Voltage Line Regulation ($\Delta V_{REF}/\Delta V_S$) | $\Delta V_S$ = 10V to 45V, $T_A$ = 25°C | | 0.3 | 0.5 | | 0.3 | 0.7 | mV/V |
| Reference Voltage Temperature Coefficient ($\Delta V_{REF}/\Delta T$) | $I_{REF}$ = 2.0 mA | | 0.004 | | | 0.004 | | %/°C |
| Reference Voltage ($V_{REF}$) | $I_{REF}$ = 2.0 mA, $T_A$ = 25°C | 4.3 | 5.1 | 5.9 | 4.3 | 5.1 | 5.9 | V |
| | $I_{REF}$ = 2.0 mA, $T_A$ = 25°C, LH0045G Pins 5 and 6 Open | 8.6 | 10.3 | 12 | 8.6 | 10.3 | 12 | V |

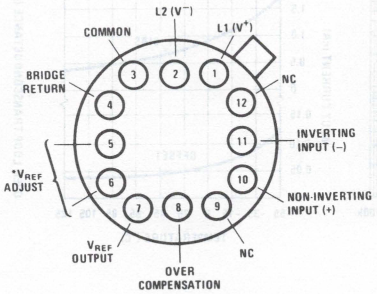
## Electrical Characteristics (Note 1) (Continued)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0045 | | | LH0045C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Resistor R9 | $I_S = 12$ mA, $T_A = 25°C$ | 95 | 100 | 105 | 95 | 100 | 105 | Ω |
| Average Temperature Coefficient of R9 ($TCR_9$) | $I_S = 12$ mA | | 50 | 300 | | 50 | 300 | PPM/°C |
| Resistor R5 | $I_S = 1.0$ mA, $T_A = 25°C$ | 950 | 1000 | 1050 | 950 | 1000 | 1050 | Ω |
| Average Temperature Coefficient of R5 ($TCR_5$) | $I_S = 1.0$ mA | | 50 | 300 | | 50 | 300 | PPM/°C |
| Input Resistance ($R_{IN}$) | $T_A = 25°C$ | | 50 | | | 50 | | MΩ |

**Note 1:** Unless otherwise specified, these specifications apply for $+10V \leq V_S \leq +50V$, pin 5 shorted to pin 6 on the LH0045G, over the temperature range −55°C to +125°C for the LH0045 and −25°C to +85°C for the LH0045C.

**Note 2:** Refer to RETS 0045G for LH0045G military specifications.

## Connection Diagram


L2 (V−)
COMMON
L1 (V+)
NC
BRIDGE RETURN
INVERTING INPUT (−)
*VREF ADJUST
NON-INVERTING INPUT (+)
VREF OUTPUT
NC
OVER COMPENSATION
1
2
3
4
5
6
7
8
9
10
11
12

TL/K/5556–2

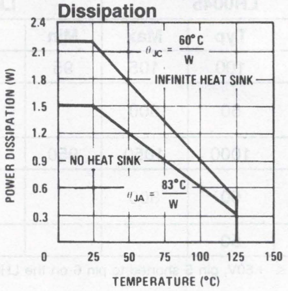
**Top View**

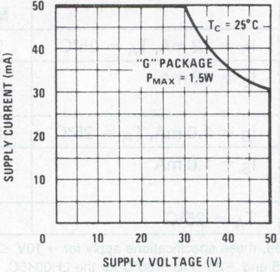
***Note:** Pin 5 is shorted to Pin 6 to obtain a Nominal +5.1V, $V_{REF}$. Left open $V_{REF} = +10V$.

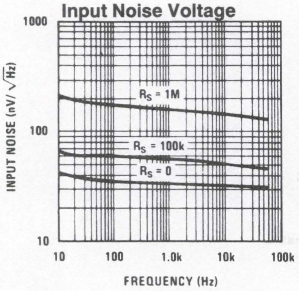
The case is isolated from the circuit for both to 3 and to 8.

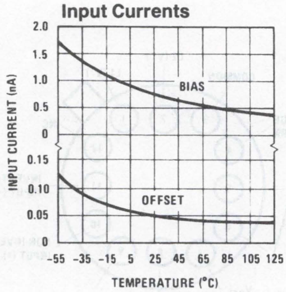
**Order Number LH0045G or LH0045CG**
**See NS Package Number G12B**

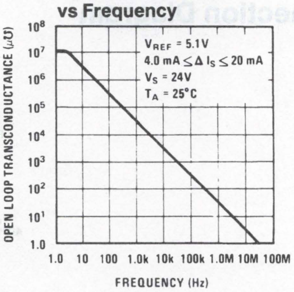
## Typical Performance Characteristics

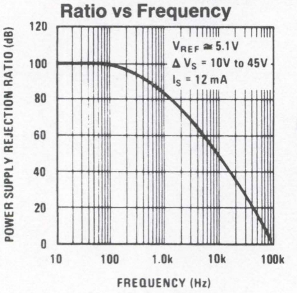

LH0045G Maximum Power Dissipation

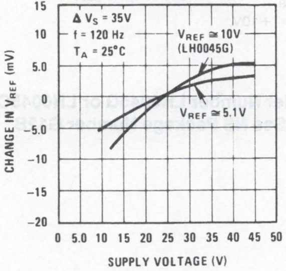

Safe Operating Area

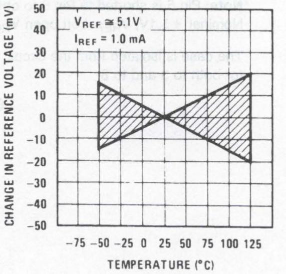

Input Noise Voltage

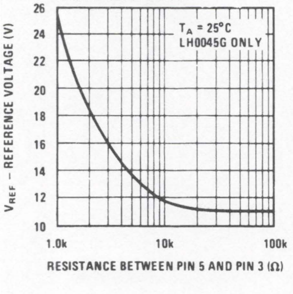

Input Currents

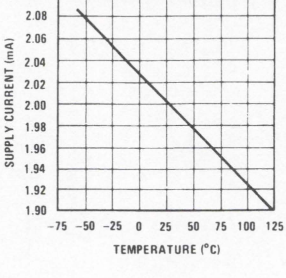

Open Loop Transconductance vs Frequency

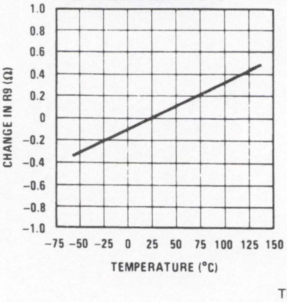

Power Supply Rejection Ratio vs Frequency


$V_{REF}$ Line Regulation


Variation of $V_{REF}$ with Temperature Normalized to 25°C


$V_{REF}$ vs Resistance Between Pin 5 and Pin 3

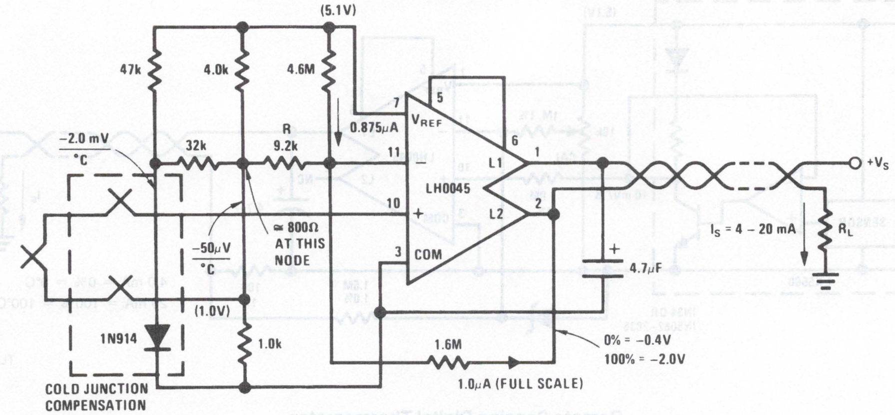

Open Loop Supply Current vs Temperature


Change in R9 with Temperature Normalized to 25°C

TL/K/5556–3

## Typical Applications

### Thermocouple Input Transmitter


(5.1V)
47k
4.0k
4.6M
0.875μA
7
5
VREF
R
9.2k
32k
−2.0 mV/°C
11
−
6
1
L1
LH0045
10
+
L2
2
+VS
IS = 4 − 20 mA
RL
≅ 800Ω AT THIS NODE
−50μV/°C
3
COM
4.7μF
(1.0V)
1N914
1.0k
1.6M
0% = −0.4V
100% = −2.0V
1.0μA (FULL SCALE)
COLD JUNCTION COMPENSATION

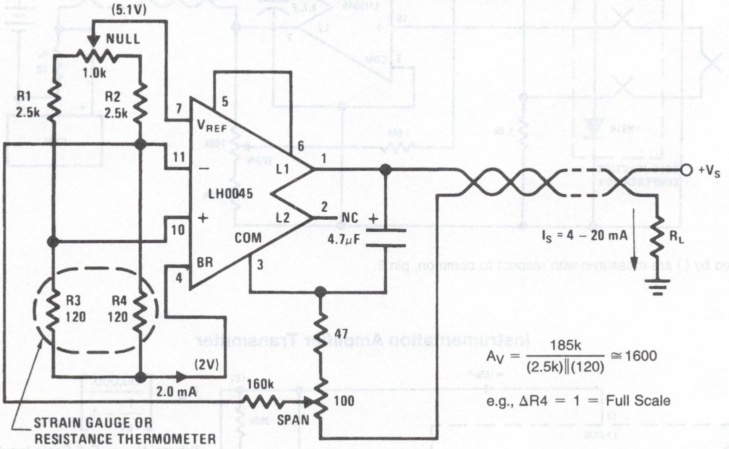
TL/K/5556–4

For 1 μA Full Scale, $R_{IN} = V_{IN}/1\ \mu A$ = Source Impedance @ Pin 11

e.g., $V_{IN}$ (Full Scale) = 10 mV, $R_{IN}$ = 10k

Bridge Impedance = 0.8k, R = 10k − 0.8k = 9.2k

### Resistance Bridge Input Transmitter


(5.1V)
NULL
1.0k
R1
2.5k
R2
2.5k
7
5
VREF
11
−
6
1
L1
LH0045
2
NC
L2
+
10
+
COM
4.7μF
BR
3
4
+VS
IS = 4 − 20 mA
RL
R3
120
R4
120
(2V)
47
2.0 mA
160k
100
SPAN
STRAIN GAUGE OR RESISTANCE THERMOMETER

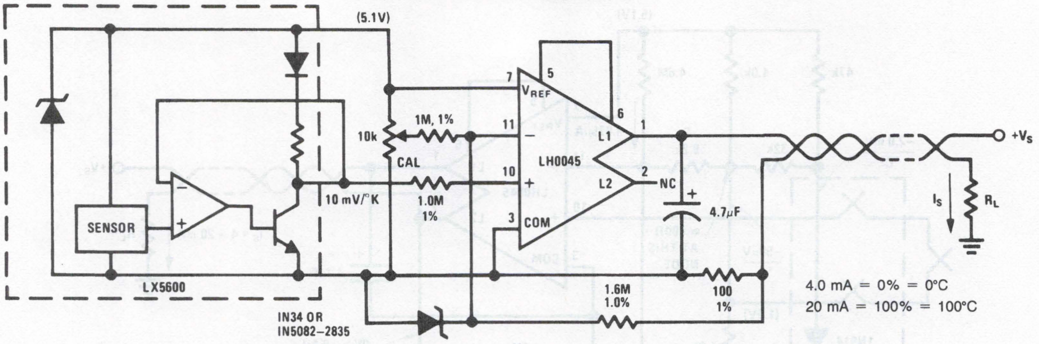
$$A_V = \frac{185k}{(2.5k)\|(120)} \cong 1600$$

e.g., ΔR4 = 1 = Full Scale

TL/K/5556–5

## Typical Applications (Continued)

### Electronic Temperature Sensor


(5.1V)
SENSOR
LX5600
10k
CAL
1M, 1%
1.0M
1%
10 mV/°K
IN34 OR
IN5082–2835
7
5
V_REF
11
6
L1
1
10
LH0045
L2
2
NC
3
COM
4.7µF
1.6M
1.0%
100
1%
+V_S
I_S
R_L
4.0 mA = 0% = 0°C
20 mA = 100% = 100°C

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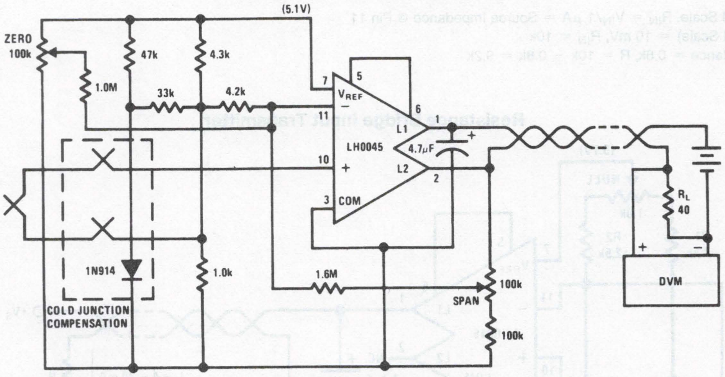
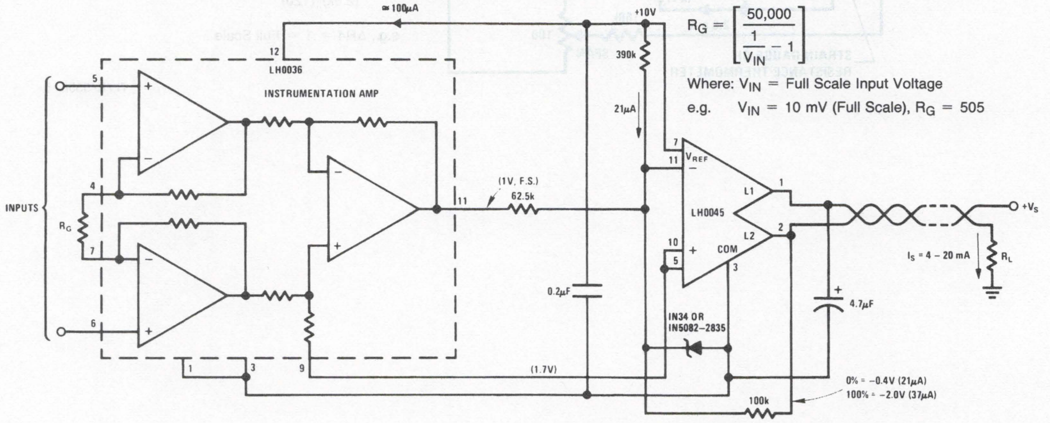
### Remote Sensing Digital Thermometer


(5.1V)
ZERO
100k
1.0M
47k
4.3k
33k
4.2k
7
5
V_REF
11
6
L1
1
LH0045
4.7µF
10
L2
2
3
COM
1N914
1.0k
COLD JUNCTION
COMPENSATION
1.6M
SPAN
100k
100k
R_L
40
DVM

TL/K/5556–7

*All voltages indicated by ( ) are measured with respect to common, pin 3.

### Instrumentation Amplifier Transmitter


≈ 100µA
12
LH0036
INSTRUMENTATION AMP
INPUTS
5
4
R_G
7
6
11
1
3
9
(1V, F.S.)
62.5k
(1.7V)
0.2µF
+10V
390k
21µA
7
V_REF
11
L1
1
LH0045
L2
2
10
5
COM
3
IN34 OR
IN5082–2835
4.7µF
+V_S
I_S = 4 – 20 mA
R_L
100k
0% = –0.4V (21µA)
100% = –2.0V (37µA)

$$R_G = \left[\frac{50{,}000}{\frac{1}{V_{IN}} - 1}\right]$$

Where: $V_{IN}$ = Full Scale Input Voltage

e.g. $V_{IN}$ = 10 mV (Full Scale), $R_G$ = 505

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*All voltages indicated by ( ) are measured with respect to common, pin 3.

## Applications Information

### CIRCUIT DESCRIPTION AND OPERATION

A simplified schematic of the LH0045/LH0045C is shown in *Figure 1.* Differential amplifier, $A_2$ converts very low level signals to an output current via transistor Q1. Reference voltage diode D1 is used to supply voltage for operation of $A_2$ and to bias an external bridge. Current source $I_1$ minimizes fluctuation in the bridge reference voltage due to changes in $V_S$.

In normal operation, the LH0045/LH0045C is used in conjunction with an external bridge comprised of $R_{B1}$ through $R_{B4}$. The bridge resistors in conjunction with bridge return resistor, R5, bias $A_2$ in its linear region and sense the input signal; e.g. $R_{B4}$ might be a strain sensitive resistor in a strain gauge bridge. $R_T$ is adjusted to purposely unbalance the bridge for 4.0 mA output (null) for zero signal input. This is accomplished by forcing 2.5 $\mu$A more through $R_{B3}$ than $R_{B4}$.

The 2.5 $\mu$A imbalance causes a voltage rise of (2.5 $\mu$A) × (100Ω) or 250 $\mu$V at the top of $R_{B3}$. Terminal L2 may be viewed as the output of an op amp whose closed loop gain is approximately $R_F/R_{B3} = 1600$.

The 250 $\mu$V rise at the top of $R_{B3}$ causes a voltage drop of (1600) × (250 $\mu$V) or −0.4V across R9. An output current, $I_S$, equal to 0.4V/R9 or 4.0 mA is thus established in Q1. If $R_{B4}$ is now decreased by 1.0Ω (due to application of a strain force), a −1.0 mV change in input voltage will result. This causes L2 to drop to −2.0V. The output current would then be 2.0V/100Ω or 20 mA (Full Scale). If $R_{B3}$ is a resistor of the same material as $R_{B4}$ but not subjected to the strain, temperature drift effects will be equal in the two legs and will cancel.

In actual practice the loading effects of $R_{B2}$ on the gain (span) and $R_F$ on output current must be taken into account.

### THERMAL CONSIDERATIONS

The power output transistor of the LH0045 is thermally isolated from the signal amplifier, $A_2$. Nevertheless, a change in the power dissipation will cause a change in the temperature of the package and thus may cause amplifier drift. These temperature excursions may be minimized by careful heat sinking to hold the case temperature equal to the ambient. With the TO-8 (G) package this is best accomplished by a clip-on heat sink such as the Thermalloy #2240A or the Wakefield #215-CB. The case is electrically isolated from the circuit.

In addition, the power change can be minimized by operating the device from relatively high supply voltages in series with a relatively high load resistance. When the signal forces the supply current higher, the voltage across the device will be reduced and the internal power dissipation kept nearly equal to the low current, high voltage condition.

For example, take the case of a 4.0 mA to 20 mA transmitter with a 24V supply and a 100Ω load resistance. The power at 4.0 mA is (23.6V) × (4.0 mA) = 94.4 mW while at full scale the power is (22V) × (20 mA) = 440 mW. The net change in power is 345 mW. This change in power will cause a change in temperature and thus a change in offset voltage of $A_2$.

If the optimum load resistance of 800Ω (from *Figure 2*) is used, the power at null is [24V − (4.0 mA) × (800Ω)] (4.0 mA) = 83 mW. The power at full scale is [24V − (20 mA) × (800Ω)] (20 mA) = 160 mW. The net change is 77 mW. This change is significantly less than without the resistor.

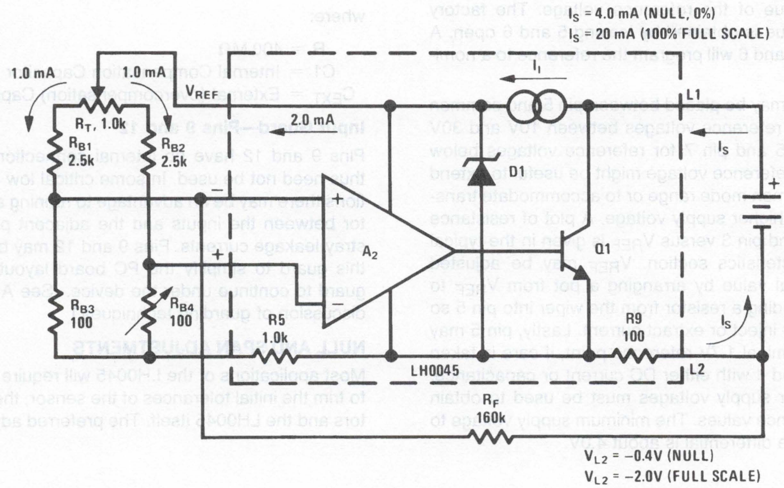

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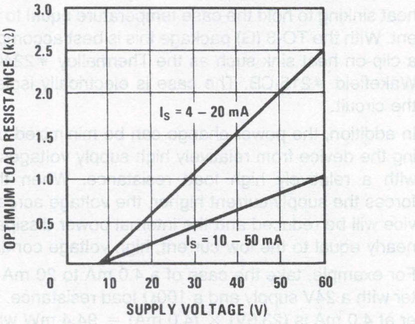
FIGURE 1. LH0045 Simplified Schematic

## Applications Information (Continued)

If the supply voltage is increased to 48V and the load resistance chosen to be the optimum value from *Figure 2* (1.95k), then the power at null is [48V − (4.0 mA) × (1.95k)] (4.0 mA) = 160.8 mW and the power at full scale is [48 − (20) × (1.95k)] (20 mA) = 180 mW for a net change of 19.2 mW.



TL/K/5556–10

**FIGURE 2. Optimum Load Resistance vs Supply Voltage**

Note that the optimized load resistance is actually the sum of the line resistance, receiver resistances and added external load resistance. However, in many applications the line resistance and receiver resistances are negligible compared to the added external load resistance and thus may be omitted in calculations.

### AUXILIARY PINS

The LH0045 has several auxiliary pins designed to provide the user with enhanced flexibility and performance. The following is a discussion of possible uses for these pins.

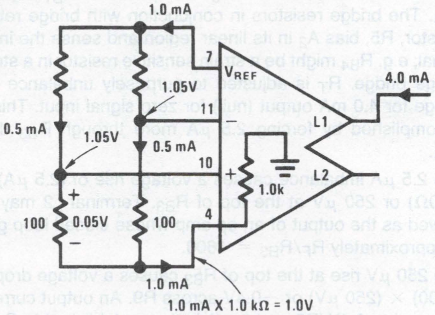
#### Programmable $V_{REF}$—Pins 5 and 6

The LH0045G provides pins 5 and 6 to allow the user to program the value of the reference voltage. The factory trimmed 10V value is obtained by leaving 5 and 6 open. A short between 5 and 6 will program the reference to a nominal 5.1V.

A resistor or pot may be placed between pin 5 and common (pin 3) to obtain reference voltages between 10V and 30V or between pin 5 and pin 7 for reference voltages below 10V. Increased reference voltage might be useful to extend the positive common mode range or to accommodate transducers requiring higher supply voltage. A plot of resistance between pin 5 and pin 3 versus $V_{REF}$ is given in the typical electrical characteristics section. $V_{REF}$ may be adjusted about its nominal value by arranging a pot from $V_{REF}$ to common and feeding a resistor from the wiper into pin 5 so that it may either inject or extract current. Lastly, pin 5 may be used as a nominal 1.7V reference point, if care is taken not to unduly load it with either DC current or capacitance. Obviously, higher supply voltages must be used to obtain the higher reference values. The minimum supply voltage to reference voltage differential is about 4.0V.

#### Bridge Return

An applications resistor is provided in the LH0045 with a nominal value of 1.0 kΩ. The primary application for the resistor is to maintain the minimum common mode input voltage (1.0V) required by the signal amplifier, $A_2$. A typical input application might utilize a strain gauge or thermistor bridge where the resistance of the sensor is 100Ω. Since only 1.0 mA may be drawn from $V_{REF}$, the 1.0 kΩ bridge return resistor is used to bias $A_2$ in its linear region as shown in *Figure 3*.



TL/K/5556–11

**FIGURE 3. Use of Bridge Return**

#### Over Compensation—Pin 8

Over compensation of the signal amplifier, $A_2$, may be desirable in DC applications where the noise-bandwidth must be minimized. A capacitor should be placed between pin 8 and pin 3, common.

Typically,

$$f_{3\,db} = \frac{1}{2\pi R (C_1 + C_{EXT})}$$

where:

R = 400 MΩ
C1 = Internal Compensation Capacitor = 100 pF
$C_{EXT}$ = External (overcompensation) Capacitor

#### Input Guard—Pins 9 and 12

Pins 9 and 12 have no internal connection whatever and thus need not be used. In some critical low current applications there may be an advantage to running a guard conductor between the inputs and the adjacent pins to intercept stray leakage currents. Pins 9 and 12 may be connected to this guard to simplify the PC board layout and allow the guard to continue under the device. (See AN-63 for further discussion of guarding techniques.)

### NULL AND SPAN ADJUSTMENTS

Most applications of the LH0045 will require potentiometers to trim the initial tolerances of the sensor, the external resistors and the LH0045 itself. The preferred adjustment proce-

## Applications Information (Continued)

dure is to stimulate the sensor, alternating between two known values, such as zero and full scale. The span and null are adjusted by monitoring the output current on a chart recorder, meter, or oscilloscope. A full scale stimulus is applied to the sensor and the span potentiometer adjusted for the desired full scale. Then, to adjust the null, apply a zero percent signal to the sensor and adjust the null potentiometer for the desired zero percent current indication.

If it is impractical to cycle the sensor during the calibration procedure, the signal may be simulated electrically with two cautions: 1) the calibration signal must be floating and 2) the calibration thus achieved does not account for sensor inaccuracies and/or errors in the signal generator.

### SENSOR SELECTION

Generally it is easiest to use an insulated sensor. If it is necessary to use a grounded sensor, the power supply must be isolated from chassis ground to avoid extraneous circulating currents.

### DESIGN EXAMPLE

There are numerous circuit configurations that may be utilized with the LH0045. The following is intended as a general design example which may be extended to specific cases.

**Circuit Requirements**

Output Characteristics

a. 0% = 4.0 mA (NULL)

b. 100% = 20 mA (SPAN = 16 mA)

c. Supply Voltage = 24V

Input (Sensor) Characteristics

a. $V_{IN} = 100$ mV (Full Scale)

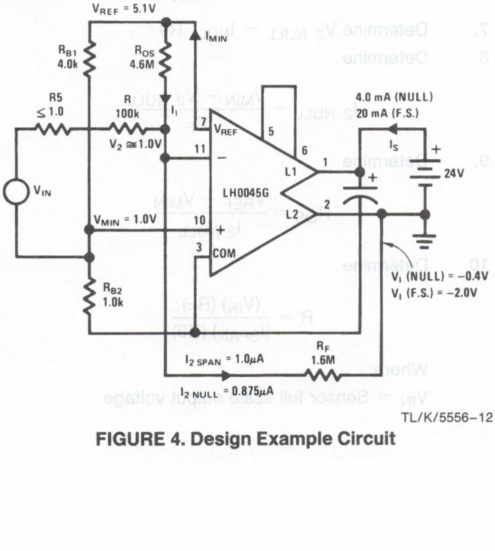
b. $V_{IN} = 0$ mV (Zero Scale)

c. Source Impedance $\leq 1.0\Omega$

General Characteristics

a. $0°C \leq T_A \leq +75°C$

b. Overall Accuracy $\leq 0.5\%$



TL/K/5556–12

**FIGURE 4. Design Example Circuit**

**Selection of $R_F$**

Input bias current to the LH0045C is guaranteed less than 10 nA. Furthermore, the change in $I_B$ over the temperature range of interest is typically under 1.0 nA. If $I_{2\ SPAN}$ is selected to be 1.0 μA (1000 $\Delta I_B$) errors due to $\Delta I_B/\Delta T$ will be less than 0.1%. For SPAN = 16 mA.

$$V_{SPAN} = \Delta V_1 = -(16\text{ mA})(R9) = -1.6V$$

where R9 = Internal Current Set Resistor = 100Ω.

For $I_{2\ SPAN} = 1.0\ \mu A$,

$$R_F = \frac{V_{SPAN}}{I_{2\ SPAN}} = \frac{-1.6V}{1.0\ \mu A} = 1.6M$$

$$R_F = 1.6\ M\Omega$$

**Note:** For applications with DC gain (ratio of feedback and input resistance) less than 8, it is recommended that a Schottky barrier diode be connected between pin 11 (cathode) and pin 3 (anode). This prevents the possibility of latch up resulting from the inverting input being forced beyond the amplifier supply voltage during power up.

**Selection of $R_{B1}$ and $R_{B2}$**

The minimum input common mode voltage, $V_{MIN}$ required at the pin 10 input of $A_2$ is 1.0V. Furthermore, the maximum open loop supply current ($I_{SOL}$) drawn by the LH0045 is 3.0 mA. That leaves $I_{MIN} = 4.0\text{ mA} - 3.0\text{ mA} = 1.0$ mA left to bias the bridge at null. Hence:

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}} = \frac{1.0V}{1.0\text{ mA}} = 1.0\ k\Omega$$

And,

$$\frac{V_{REF}\, R_{B2}}{R_{B1} + R_{B2}} = 1.0V$$

$$R_{B1} = R_{B2}\frac{V_{REF} - 1.0V}{1.0V}$$

$$= 1.0k\ (5.1 - 1.0)$$

$$R_{B1} \cong 4.0\ k\Omega$$

Alternatively, an LM113, 1.22V reference diode, or an op amp such as the LM108 may be used to bias the signal amplifier, $A_2$, as shown in *Figure 5.* These techniques have the advantage of lowering the impedance seen at pin 10.

**Selection of $R_{OS}$**

$R_{OS}$ is selected to provide the null current of 4.0 mA, $V_{1\ NULL} = 4.0\text{ mA} \times 100\Omega = 0.4V$. From previous calculations we know that $V_{MIN} = 1.0V$. The voltage pin 11, $V_2$ is:

$$V_2 = V_{MIN} + V_{OS} \cong V_{MIN}$$

for $V_{IN} = 0V$

Hence, the current required to generate the null voltage, $I_{2\ NULL}$ is:

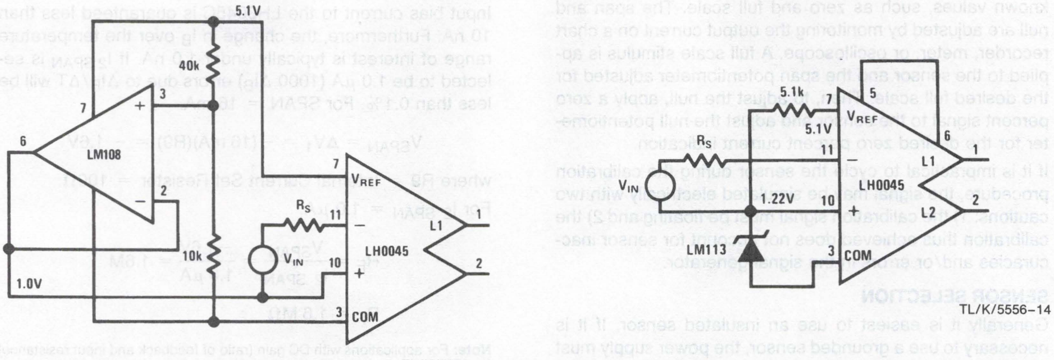
$$I_{2\ NULL} = \frac{V_{MIN} - V_{1\ NULL}}{R_F}$$

$$= \frac{1.0V - (-0.4V)}{1.6\ M\Omega} = 0.875\ \mu A$$

This current must be provided by $R_{OS}$ from $V_{REF}$; hence:

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

## Applications Information (Continued)



TL/K/5556-13

TL/K/5556-14

**FIGURE 5. Alternate Biasing Techniques**

The nominal value for $V_{REF}$ is 5.1V, therefore the nominal value for $R_{OS}$ is:

$$\frac{5.1V - 1.0V}{0.875\ \mu A} \text{ or}$$

$$R_{OS} = 4.6\ M\Omega$$

It should be noted however, that the variation of $V_{REF}$ may be as high as 5.9V or as low as 4.3V. Furthermore, the tolerances of R9 (100Ω), $R_{B1}$. $R_{B2}$, and the input $V_{OS}$ of $A_2$ would predict values for $R_{OS}$ as low as 3.98M and as high as 5.43M. The implication is that in the specific case, $R_{OS}$ should be implemented with a pot, of appropriate value, in order to accommodate the tolerances of $V_{REF}$, R9, $V_{OS}$, $R_{B1}$, $R_{B2}$, etc.

**Selection of R**

SPAN is required to be 16 mA. From feedback theory and the gain equation we know:

$$I_{SPAN} = V_{IN} \frac{R_F}{R} \times \frac{1}{R9}$$

where:

R = Total impedance in signal path between pin 10 and pin 11

R9 = Current setting resistor = 100Ω

$V_{IN}$ = Full scale input voltage = 100 mV

$$\therefore R = \frac{(V_{IN})\ (R_F)}{(I_{SPAN}\ (R9)}$$

$$R = \frac{(100\ mV)\ (1.6\ M\Omega)}{(16\ mA)\ (100\Omega)}$$

$$R = 100\ k\Omega$$

As before, uncertainties in device parameters might dictate that $R_F$ be made a pot of appropriate value.

**Summary of the Steps to Determine External Resistor Values**

1. Select $I_{FULL\ SCALE} = I_{NULL} + I_{SPAN}$ for the desired application. ($I_{NULL}$ is frequently 4.0 mA and $I_{FULL\ SCALE}$ is frequently 20 mA.)
2. Select $I_{2\ SPAN}$ so that it is large compared to $\Delta I_B$. $1000\ \Delta I_B$ is a good value.
3. Determine $V_{SPAN} = \Delta V_2 = (I_{SPAN})\ (R9)$.
4. Determine $R_F = (V_{SPAN}/I_{2\ SPAN})$
5. Select

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}}$$

$$R_{B2} \geq \frac{1V}{I_{NULL} - I_{SOL}}$$

Where:

$V_{MIN}$ = minimum common mode input voltage

$I_{MIN}$ = minimum available bridge current

$I_{SOL}$ = maximum open loop supply current

6. Determine

$$R_{B1} = R_{B2} \frac{V_{REF} - V_{MIN}}{V_{MIN}}$$

7. Determine $V_{2\ NULL} = I_{NULL}\ R9$
8. Determine

$$I_{2\ NULL} = \frac{V_{MIN} - V_{2\ NULL}}{R_F}$$

9. Determine

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

10. Determine

$$R = \frac{(V_{IN})\ (R_F)}{(I_{SPAN})\ (R9)}$$

Where:

$V_{IN}$ = Sensor full scale output voltage

## Applications Information (Continued)

### ERROR BUDGET ANALYSIS

**Errors Due to Change in $V_{REF}$ ($\Delta V_{REF}$)**

There are several factors which could cause a change in $V_{REF}$. First, as the ambient temperature changes, a $V_{REF}$ drift of ±0.2 mV/°C might be expected. Secondly, supply voltage variations could cause a 0.5 mV/V change in $V_{REF}$. Lastly, self-heating due to power dissipation variations can cause drift of the reference.

An overall expression for change in $V_{REF}$ is:

$$\Delta V_{REF} = \underbrace{[(\theta)(\Delta P_{DISS}) + \Delta T_A]\frac{\Delta V_{REF}}{\Delta T}}_{\text{Thermal Effects}}$$

$$+ \underbrace{\frac{\Delta V_{REF}}{\Delta V_S}(\Delta V_S)}_{\text{Supply Voltage Effects}}$$

Where:

$\theta$ = Thermal resistance, either junction-to-ambient or junction-to-case

$\Delta P_{DISS}$ = Change in avg. power dissipation

$\Delta T_A$ = Change in ambient temperature

$\frac{\Delta V_{REF}}{\Delta T}$ = Reference voltage drift (in mV/°C)

$\frac{\Delta V_{REF}}{\Delta V_S}$ = Line regulation of $V_{REF}$

Several steps may be taken to minimize the bracketed terms in the equation above. For example, operating the LH0045G with a heat sink reduces the thermal resistance from $\theta_{jA}$ = 83°C/W to $\theta_{jC}$ = 60°C/W. The $\Delta P_{DISS}$ term may be significantly reduced using the power minimization technique described under "Thermal Considerations". For the design example, $\Delta P_{DISS}$ is reduced from 384 mW to 77 mW ($R_L$ = 800Ω). Evaluating the LH0045G with a heat sink and $R_L$ = 800Ω yields.

$$\Delta V_{REF} = \left(\frac{60°C}{W}(0.077W) + 75°C\right)\left(\frac{0.2\ mV}{°C}\right)$$

$$+ \frac{0.5\ mV}{V}(16V)$$

$$\Delta V_{REF} = 24\ mV$$

An expression for error in the output current due to $\Delta V_{REF}$ is:

$$\frac{\Delta I_S}{I_{SPAN}}(\%) = 100\frac{(K)(R_{OS})(\Delta V_{REF}) - (1-K)(\Delta V_{REF})(RF)}{(R9)\ (R_{OS})\ (I_{SPAN}}$$

Where:

$\Delta V_{REF}$ = Total change in $V_{REF}$

$K = \frac{R_{B2}}{R_{B1} + R_{B2}}$

R9 = Current set resistor

$I_{SPAN}$ = Change in output current from 0% to 100%

For example, $\Delta V_{REF}$ = 24 mV, K = 0.2, R9 = 100Ω, $I_{SPAN}$ = 16 mA. Hence, a 0.12% worst case error might be expected in output currents due to $\Delta V_{REF}$ effects.

**Error Due to $V_{OS}$ Drift**

One of the primary causes of error in $I_S$ is caused by $V_{OS}$ drift. Drift may be induced either by self heating of the device or ambient temperature changes. The input offset voltage drift, $\Delta V_{OS}/\Delta T$, is nominally 3.3 μV/°C per millivolt of initial offset. An expression for the total temperature dependent drift is:

$$\Delta V_{OS} = [(\theta)(\Delta P_{DISS}) + \Delta T_A]\frac{\Delta V_{OS}}{\Delta T}$$

Where:

$\theta$ = Thermal resistance either junction-to-ambient or junction-to-case

$\Delta P_{DISS}$ = Change in average power dissipation

$\Delta T_A$ = Change in ambient temperature

The bracketed term may be minimized by heat sinking and using the power minimization technique described under "Thermal Considerations". For the LH0045G design example, $\Delta V_{OS}$ = 0.352 mV under ambient conditions and 0.263 mV using a heat sink and $R_L$ = 800Ω.

The error in output current due to $\Delta V_{OS}$ is:

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in } \%) = 100 \times \frac{\Delta V_{OS}}{V_{IN}\ (\text{FULL SCALE})}$$

$$= 100 \times \frac{R_F}{(R)\ (R9)\ (I_{SPAN})}$$

For the design example, $\Delta V_{OS}$ = 0.263 mV, $V_{IN}$ (Full Scale) = 100 mV. Hence, 0.26 mV ÷ 100 mV or 0.26% worst case error could be expected in output current effects.

**Errors Due to Changes in R9**

The temperature coefficient of R9 (TCR) will produce errors in the output current. Changes in R9 may be caused by self-heating of the device or by ambient temperature changes.

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in } \%) = 100\frac{\Delta R9}{\Delta T}(\theta\ P_{DISS} + \Delta T_A)$$

Where:

$\theta$ = Thermal resistance either from junction-to-ambient or junction-to-case

$\Delta P_{DISS}$ = Change in average power dissipation

## Applications Information (Continued)

$\Delta T_A$ = Change in ambient temperature

$\frac{\Delta R9}{\Delta T}$ = TCR of R9

Using the LH0045G design example, $\Delta R9/\Delta T = 0.03\%/°C$, hence a 3.2% worst case error in output current might be expected for operation without a heat sink over the temperature range.

Heat sinking the device and using $R_L = 800\Omega$, reduces $\Delta I_S/I_{SPAN}$ to 2.3%.

The error analysis indicates that the internal current set resistor, R9, is inadequate to satisfy high accuracy design criterion. In these instances, an external 100Ω resistor should be substituted for R9.

Obviously, the TCR of the resistor should be low. Metal film or wire-wound resistors are the best choice offering TCR's less than 10 ppm/°C versus 50 ppm/°C typical drift for R9.

**External Causes of Error**

The components external to the LH0045 are also critical in determining errors. Specifically, the composition of resistors $R_{B1}$, $R_{OS}$, $R_F$, R, etc. in the design example will influence both drift and long term stability.

In particular, resistors and potentiometers of wire wound construction are recommended. Also, metal-film resistors with low TCR ($\leq$ 10 ppm/°C) may be used for fixed resistor applications.

**Error Analysis Summary**

The overall errors attributable to the LH0045 may be minimized using heat sinking, and utilization of an external load resistor. Although $R_L$ reduces the compliance of the circuit, its use is generally advisable in precision applications. External components should be selected for low TCR and long term stability.

The design example errors, using an external 100Ω wire wound resistor for R9 equal:

$$\frac{\Delta I_S}{I_{SPAN}} = \underbrace{0.12\%}_{\Delta V_{REF}} + \underbrace{0.26\%}_{\Delta V_{OS}} + \underbrace{0.08\%}_{\Delta R9} = 0.46\%$$

### SOCKETS AND HEAT SINKS

Mounting sockets, test sockets and heat sinks are available for the G package.

The following or their equivalents are recommended:

**Sockets:**

G — 12-Lead TO-8: Barnes Corp. #MGX-12
Textool #212-100-323

**Heat Sinks:**

G — 12-Lead TO-8: Thermalloy #2240A
Wakefield #215-CB

## Definition of Terms

**Input Offset Voltage, $V_{OS}$:** The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

**Input Bias Current, $I_B$:** The average of the two input currents.

**Input Offset Current, $I_{OS}$:** The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

**Input Resistance, $R_{IN}$:** The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 $V_{DC}$.

**Open Loop Transconductance, $g_{MOL}$:** The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

**Open Loop Output Resistance, $R_{OUT}$:** The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

**Common Mode Rejection Ratio, CMRR:** The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

**Power Supply Rejection Ratio, PSRR:** The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

**Input Voltage Range, $V_{IN}$:** The range of voltages on the input terminals for which the device operates within specifications.

**Open Loop Supply Current, $I_S$:** The supply current required with the signal amplifier $A_2$ biased off (inverting input positive, non-inverting input negative) and no load on the $V_{REF}$ terminal.

This represents a measure of the minimum low end signal current.

**Reference Voltage Line Regulation, $\Delta V_{REF}/\Delta V_S$:** The ratio of the change in $V_{REF}$ to the peak-to-peak change in supply (output) voltage producing it.

**Reference Voltage Load Regulaion, $\Delta V_{REF}/\Delta I_{REF}$:** The change in $V_{REF}$ for a stipulated change in $I_{REF}$.

**National Semiconductor Corporation**

# LH0061/LH0061C 0.5 Amp Wide Band Operational Amplifier

## General Description

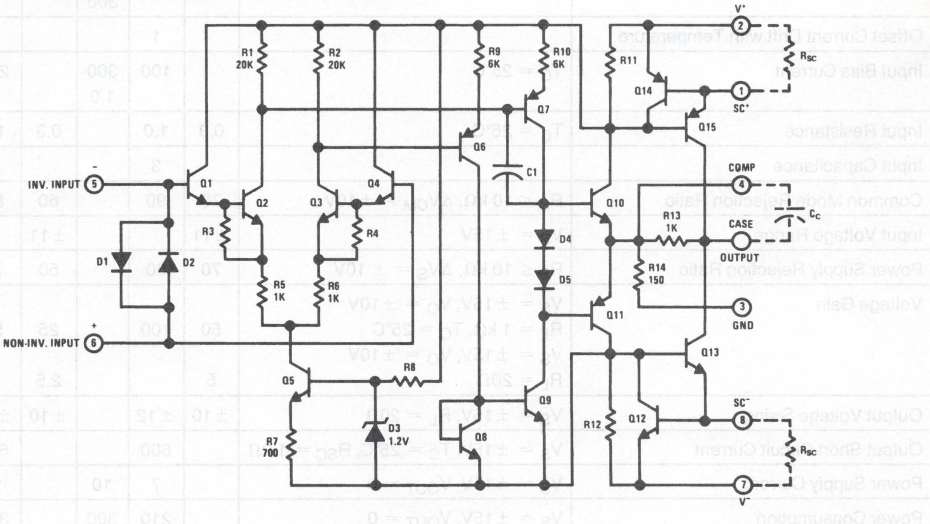
The LH0061/LH0061C is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5 ampere at voltage levels of ±12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20W.

The wide bandwidth and high output power capabilities of the LH0061/LH0061C make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers. The LH0061 is guaranteed over the temperature range −55°C to +125°C; whereas, the LH0061C is guaranteed from −25°C to +85°C.

## Features

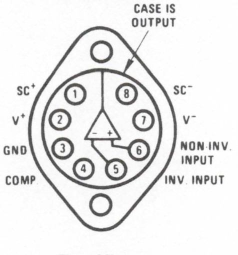
| | |
|---|---|
| ■ Output current | 0.5A |
| ■ Wide large signal bandwidth | 1 MHz |
| ■ High slew rate | 70V/μs |
| ■ Low standby power | 240 mW |
| ■ Low input current | 300 nA Max |

## Schematic and Connection Diagrams


V+
2
R1 20K
R2 20K
R9 6K
R10 6K
R11
RSC
Q14
1
SC+
Q7
Q15
Q6
C1
COMP
4
INV. INPUT
5
Q1
Q2
Q3
Q4
Q10
CC
R3
R4
D4
R13 1K
CASE
OUTPUT
D1
D2
D5
R14 150
R5 1K
R6 1K
Q11
3
GND
NON-INV. INPUT
6
Q13
R8
Q5
Q9
D3 1.2V
SC−
8
R12
Q12
R7 700
Q8
RSC
7
V−

TL/K/6861-1

**TO-3 Package**


CASE IS OUTPUT
SC+
1
8
SC−
V+
2
7
V−
GND
3
6
NON-INV. INPUT
COMP
4
5
INV. INPUT
−
+

TL/K/6861-2

**Top View**

**Order Number LH0061CK**
**See NS Package Number K08A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation | See Curve |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Peak Output Current | 2A |
| Output Short Circuit Duration (Note 4) | Continuous |
| Operating Temperature Range | |
| LH0061 | −55°C to +125°C |
| LH0061C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 1)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0061 | | | LH0061C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \le 10\ k\Omega$, $T_C = 25°C$, $V_S = \pm 15V$ | | 1.0 | 4.0 | | 3.0 | 10 | mV |
| | $R_S \le 10\ k\Omega$, $V_S = \pm 15V$ | | | 6.0 | | | 15 | mV |
| Voltage Drift with Temperature | $R_S \le 10\ k\Omega$ | | 5 | | | 5 | | $\mu V/°C$ |
| Offset Voltage Change with Output Power | | | 5 | | | 5 | | $\mu V$/watt |
| Input Offset Current | $T_C = 25°C$ | | 30 | 100 | | 50 | 200 | nA |
| | | | | 300 | | | 500 | nA |
| Offset Current Drift with Temperature | | | 1 | | | 1 | | nA/°C |
| Input Bias Current | $T_C = 25°C$ | | 100 | 300 | | 200 | 500 | nA |
| | | | | 1.0 | | | 1.0 | $\mu A$ |
| Input Resistance | $T_C = 25°C$ | 0.3 | 1.0 | | 0.3 | 1.0 | | MΩ |
| Input Capacitance | | | 3 | | | 3 | | pF |
| Common Mode Rejection Ratio | $R_S \le 10\ k\Omega$, $\Delta V_{CM} = \pm 10V$ | 70 | 90 | | 60 | 80 | | dB |
| Input Voltage Range | $V_S = \pm 15V$ | ±11 | | | ±11 | | | V |
| Power Supply Rejection Ratio | $R_S \le 10\ k\Omega$, $\Delta V_S = \pm 10V$ | 70 | 80 | | 50 | 70 | | dB |
| Voltage Gain | $V_S = \pm 15V$, $V_O = \pm 10V$<br>$R_L = 1\ k\Omega$, $T_C = 25°C$ | 50 | 100 | | 25 | 50 | | V/mV |
| | $V_S = \pm 15V$, $V_O = \pm 10V$<br>$R_L = 20\Omega$ | 5 | | | 2.5 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 20\Omega$ | ±10 | ±12 | | ±10 | ±12 | | V |
| Output Short Circuit Current | $V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 1.0\Omega$ | | 600 | | | 600 | | mA |
| Power Supply Current | $V_S = \pm 15V$, $V_{OUT} = 0$ | | 7 | 10 | | 10 | 15 | mA |
| Power Consumption | $V_S = \pm 15V$, $V_{OUT} = 0$ | | 210 | 300 | | 300 | 450 | mW |

## AC Electrical Characteristics ($T_C = 25°C, V_S = \pm 15V, C_C = 3000\ pF$)

| Parameter | Conditions | Limits |  |  |  |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | LH0061 |  |  | LH0061C |  |  |  |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Slew Rate | $A_V = +1, R_L = 100\Omega$ | 25 | 70 |  | 25 | 70 |  | V/µs |
| Power Bandwidth | $R_L = 100\Omega$ |  | 1 |  |  | 1 |  | MHz |
| Small Signal Transient Response |  |  | 30 |  |  | 30 |  | ns |
| Small Signal Overshoot |  |  | 5 | 20 |  | 10 | 30 | % |
| Settling Time (0.1%) | $\Delta V_{IN} = 10V, A_V = +1$ |  | 0.8 |  |  | 0.8 |  | µs |
| Overload Recovery Time |  |  | 1 |  |  | 1 |  | µs |
| Harmonic Distortion | $f = 1\ kHz, P_O = 0.5W$ |  | 0.2 |  |  | 0.2 |  | % |

**Note 1:** Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$, $C_C = 3000$ pF, and $-55°C \leq T_C \leq +125°C$ for the LH0061K and $-25°C \leq T_C \leq +85°C$ for the LH0061CK. Typical values are for $T_C = 25°C$.

**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.

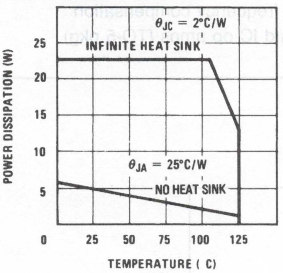
**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** Rating applies as long as package power rating is not exceeded.

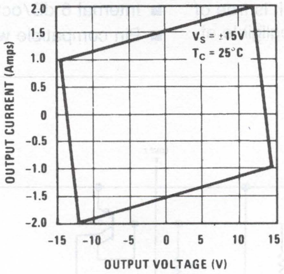
**Note 5:** Refer to RETS0061K for LH0061K military specifications.

## Typical Performance Characteristics

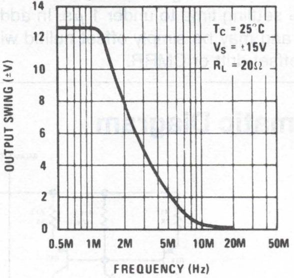
### Power Derating



### Safe Operating Area



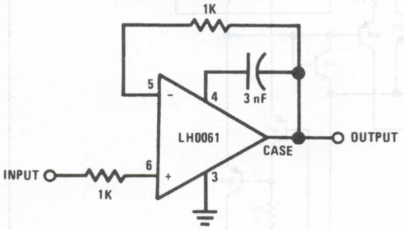
### Large Signal Frequency Response



TL/K/6861–3

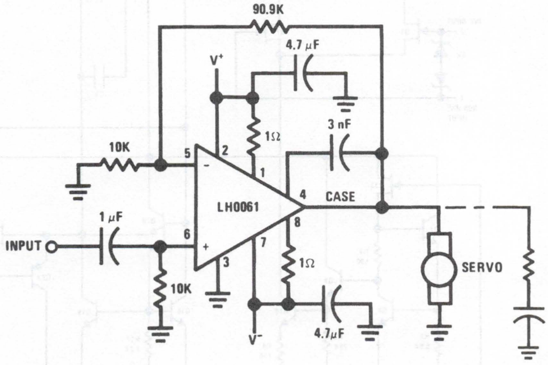
## Typical Applications

### Unity Gain Driver



TL/K/6861–4

### AC Servo Amplifier



TL/K/6861–5

**National Semiconductor Corporation**

# LH0062/LH0062C High Speed FET Operational Amplifier

## General Description

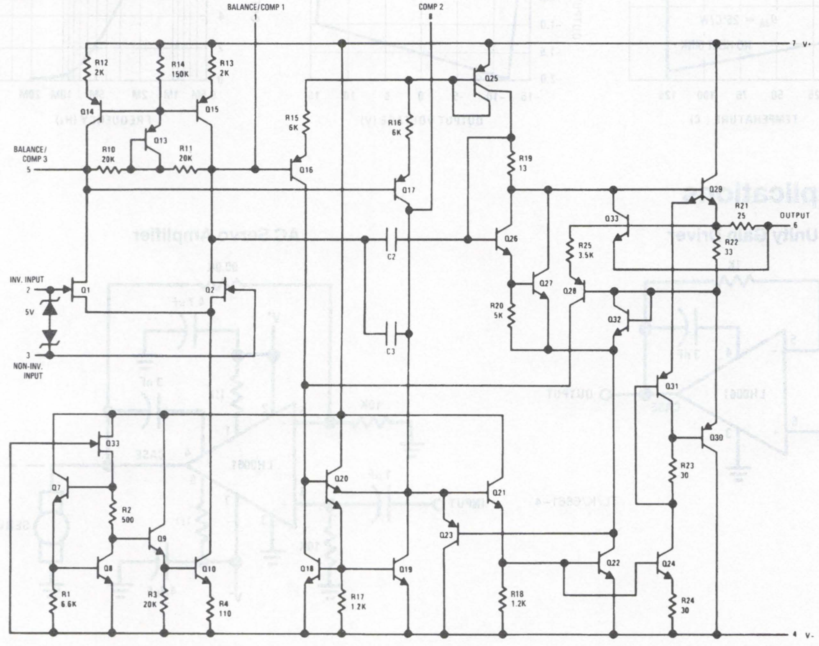
The LH0062/LH0062C is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 120 V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques). Over-compensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs. In addition it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system. The LH0062 is specified for the full military temperature range of −55° to +125°C while the LH0062C is specified to operate over a −25°C to +85°C temperature range.

## Features

| | |
|---|---|
| ■ High slew rate | 70 V/μs |
| ■ Wide bandwidth | 15 MHz |
| ■ Settling time (0.1%) | 1 μs |
| ■ Low input offset voltage | 2 mV |
| ■ Low input offset current | 1 pA |
| ■ Wide supply range | ±5V to ±20V |
| ■ Internal 6 dB/octave frequency compensation | |
| ■ Pin compatible with std IC op amps (TO-5 pkg) | |

## Schematic Diagram


BALANCE/COMP 1
1
COMP 2
8
V+
R12 2K
R14 150K
R13 2K
Q14
Q15
Q13
BALANCE/COMP 3
5
R10 20K
R11 20K
R15 6K
Q16
R16 6K
Q17
Q25
R19 13
Q29
R21 25
OUTPUT
6
Q33
R22 33
R25 3.5K
Q26
C2
Q27
Q28
R20 5K
Q32
C3
INV. INPUT
2
Q1
Q2
5V
3
NON-INV. INPUT
Q31
Q30
Q33
Q7
R2 500
Q9
Q8
Q10
R1 6.6K
R3 20K
R4 110
Q20
Q21
Q23
R23 30
Q18
Q19
Q22
Q24
R17 1.2K
R18 1.2K
R24 30
4 V-

TL/K/6862–1

*Pin Numbers Shown for TO-5 Package

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (see graph) | 500 mW |
| Input Voltage (Note 1) | ±5V |
| Differential Input Voltage (Note 2) | ±30V |

| | |
|---|---|
| Short Circuit Duration | Continuous |
| Operating Temperature | |
| LH0062 | −55°C to +125°C |
| LH0062C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH0062 | | | LH0062C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \le 100\ k\Omega$, $T_A = 25°C$,<br>$R_S \le 100\ k\Omega$ | | 2 | 5<br>7 | | 10 | 15<br>20 | mV<br>mV |
| Temperature Coefficient of Input Offset Voltage | $R_S \le 100\ k\Omega$ | | 25 | | | 25 | | μV/°C |
| Offset Voltage Drift with Time | | | 4 | | | 5 | | μV/week |
| Input Offset Current | $T_A = 25°C$ | | 0.2 | 2<br>2 | | 1 | 5<br>0.2 | pA<br>nA |
| Temperature Coefficient of Input Offset Current | | | Doubles every 10°C | | | Doubles every 10°C | | |
| Offset Current Drift with Time | | | 0.1 | | | 0.1 | | pA/week |
| Input Bias Current | $T_A = 25°C$<br>(Note 4) | | 5 | 10<br>10 | | 10 | 65<br>2 | pA<br>nA |
| Temperature Coefficient of Input Bias Current | | | Doubles every 10°C | | | Doubles every 10°C | | |
| Differential Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Common Mode Input Resistance | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| Input Capacitance | | | 4 | | | 4 | | pF |
| Input Voltage Range | $V_S = \pm 15V$ | ±10 | ±12 | | ±10 | ±12 | | V |
| Common Mode Rejection Ratio | $R_S \le 10\ k\Omega$, $V_{IN} = \pm 10V$ | 80 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \le 10\ k\Omega$, $\pm 5V \le V_S \le \pm 15V$ | 80 | 90 | | 70 | 90 | | dB |
| Large Signal Voltage Gain | $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$<br>$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$ | 50<br>25 | 200 | | 25<br>25 | 160 | | V/mV<br>V/mV |
| Output Voltage Swing | $R_L = 2\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$<br>$R_L = 2\ k\Omega$, $V_S = \pm 15V$ | ±12<br>±10 | ±13 | | ±12<br>±10 | 13 | | V<br>V |
| Output Current Swing | $V_{OUT} = \pm 10V$, $T_A = 25°C$ | ±10 | ±15 | | ±10 | ±15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | $T_A = 25°C$ | | 25 | | | 25 | | mA |
| Supply Current | $V_S = \pm 15V$ | | 5 | 8 | | 7 | 12 | mA |
| Power Consumption | $V_S = \pm 15V$ | | | 240 | | | 360 | mW |

## AC Electrical Characteristics ($T_A$ = 25°C, $V_S$ = ±15V)

| Parameter | Conditions | LH0062 Min | LH0062 Typ | LH0062 Max | LH0062C Min | LH0062C Typ | LH0062C Max | Units |
|---|---|---|---|---|---|---|---|---|
| Slew Rate | Voltage Follower | 50 | 70 | | 50 | 70 | | V/µs |
| Large Signal Bandwidth | Voltage Follower | | 2 | | | 2 | | MHz |
| Small Signal Bandwidth | | | 15 | | | 15 | | MHz |
| Rise Time | | | 25 | | | 25 | | ns |
| Overshoot | | | 10 | | | 15 | | % |
| Settling Time (0.1%) | $\Delta V_{IN}$ = 10V | | 1 | | | 1 | | µs |
| Overload Recovery | | | 0.9 | | | 0.9 | | µs |
| Input Noise Voltage | $R_S$ = 10 kΩ, $f_o$ = 10 Hz | | 150 | | | 150 | | nV/√Hz |
| Input Noise Voltage | $R_S$ = 10 kΩ, $f_o$ = 100 Hz | | 55 | | | 55 | | nV/√Hz |
| Input Noise Voltage | $R_S$ = 10 kΩ, $f_o$ = 1 kHz | | 35 | | | 35 | | nV/√Hz |
| Input Noise Voltage | $R_S$ = 10 kΩ, $f_o$ = 10 kHz | | 30 | | | 30 | | nV/√Hz |
| Input Noise Voltage | BW = 10 Hz to 10 kHz, $R_S$ = 10 kΩ | | 12 | | | 12 | | µVrms |
| Input Noise Current | BW = 10 Hz to 10 kHz | | <0.1 | | | <0.1 | | pArms |

**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** Inputs are protected from excessive voltages by back-to-back diodes. Input currents should be limited to 1 mA.

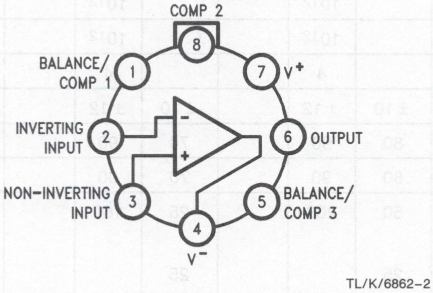
**Note 3:** Unless otherwise specified, these specifications apply for $\pm5V \le V_S \le \pm20V$ and $-55°C \le T_A \le +125°C$ for the LH0062 and $-25°C \le T_A \le +85°C$ for the LH0062C. Typical values are given for $T_A$ = 25°C. Power supplies should be bypassed with 0.1 µF ceramic capacitors.

**Note 4:** Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature T = 25°C, self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

**Note 5:** Refer to RETS0062X for LH0062D and LH0062H military specifications.

## Connection Diagrams

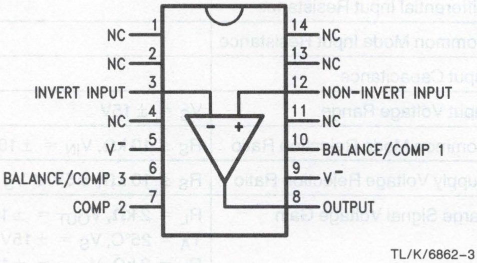
### Metal Can Package


COMP 2
8
BALANCE/COMP 1
1
7
V+
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE/COMP 3
4
V−
TL/K/6862-2

**Top View**

**Order Number LH0062H or LH0062CH**
**See NS Package Number H08D**

### Dual-In-Line Package

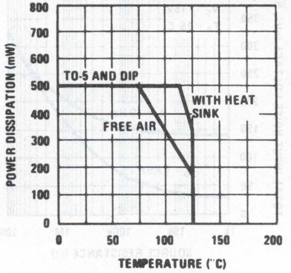

NC 1
NC 2
INVERT INPUT 3
NC 4
V+ 5
BALANCE/COMP 3 6
COMP 2 7
14 NC
13 NC
12 NON-INVERT INPUT
11 NC
10 BALANCE/COMP 1
9 V−
8 OUTPUT
TL/K/6862-3

**Top View**

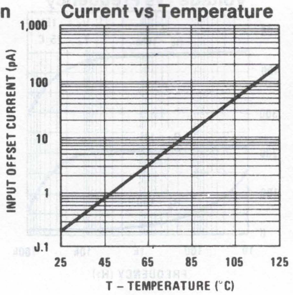
**Order Number LH0062D or LH0062CD**
**See NS Package Number D14E**

## Typical Performance Characteristics

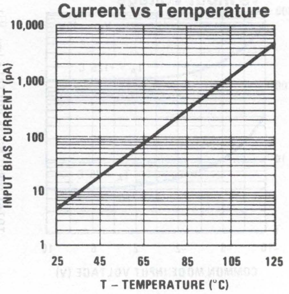
### Maximum Power Dissipation



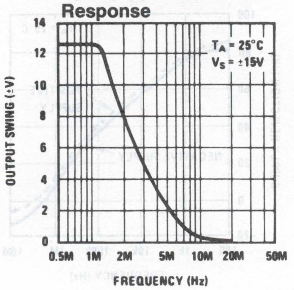
### Input Offset Current vs Temperature



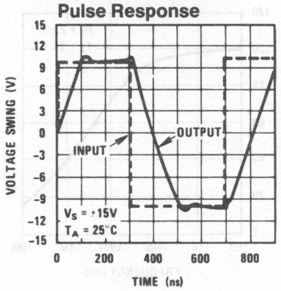
### Input Bias Current vs Temperature



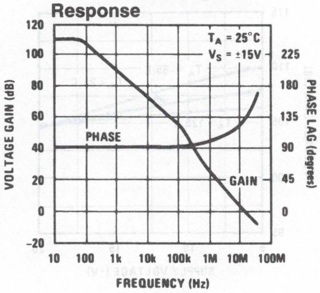
### Large Signal Frequency Response



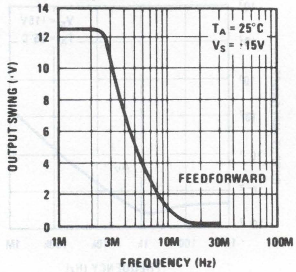
### Voltage Follower Pulse Response



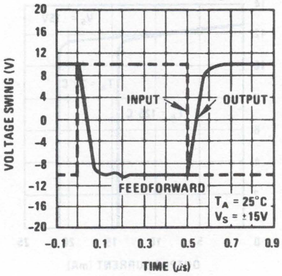
### Open Loop Frequency Response



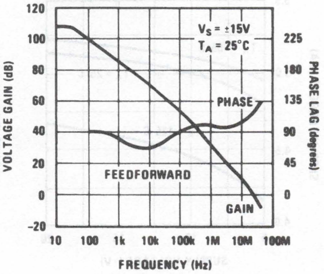
### Large Signal Frequency Response



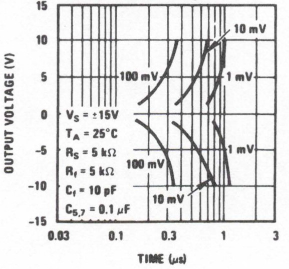
### Inverter Pulse Response



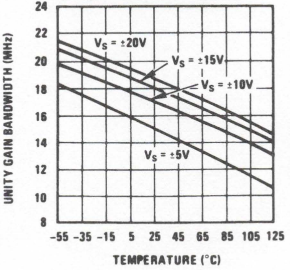
### Open Loop Frequency Response



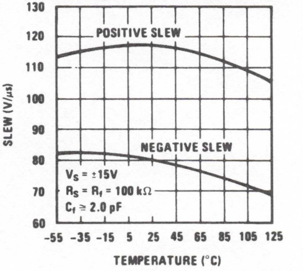
### Inverter Settling Time



### Unity Gain Bandwidth

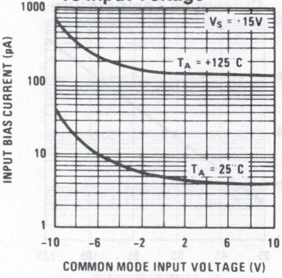


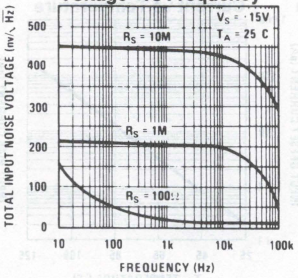
### Voltage Follower Slew Rate

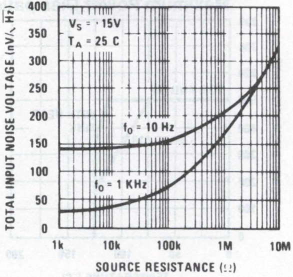


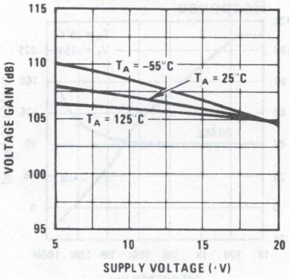
TL/K/6862-4

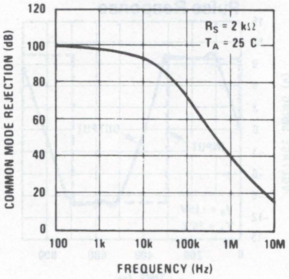
## Typical Performance Characteristics (Continued)

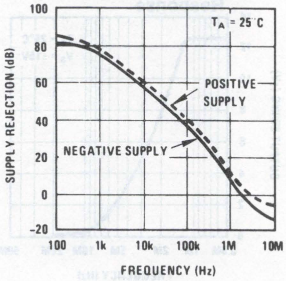

**Input Bias Current vs Input Voltage**

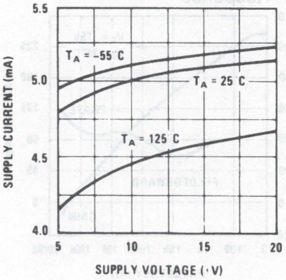

**Total Input Noise Voltage* vs Frequency**

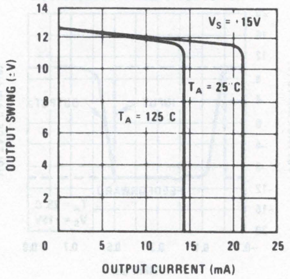

**Total Input Noise Voltage* vs Source Resistance**

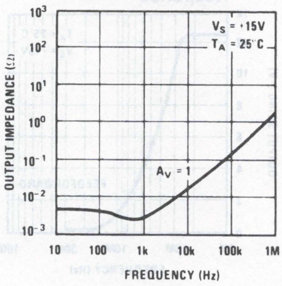

**Voltage Gain**


**Common Mode Rejection**


**Power Supply Rejection**


**Supply Current**


**Current Limiting**

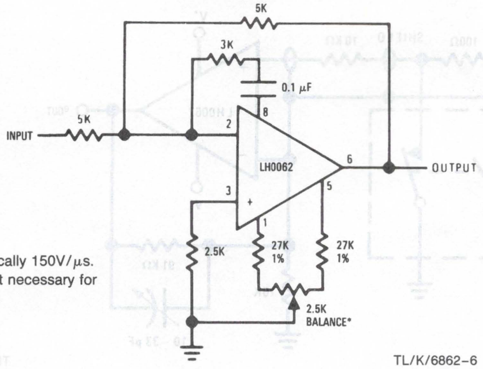

**Closed Loop Output Impedance**

TL/K/6862-5

*Noise Voltage Includes Contribution from Source Resistance

# Auxiliary Circuits

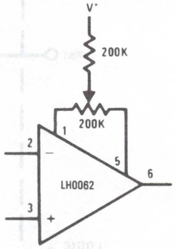
### Feedforward Compensation for Greater Inverting Slew Rate†


5K
3K
0.1 µF
8
2
INPUT
5K
LH0062
6
OUTPUT
3
+
5
1
2.5K
27K 1%
27K 1%
2.5K BALANCE*

†Slew rate typically 150V/µs.
*Balance circuit necessary for increased slew.

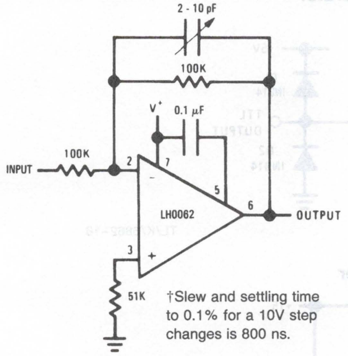
TL/K/6862-6

### Offset Balancing


V+
200K
200K
1
2
–
5
6
LH0062
3
+

TL/K/6862-7

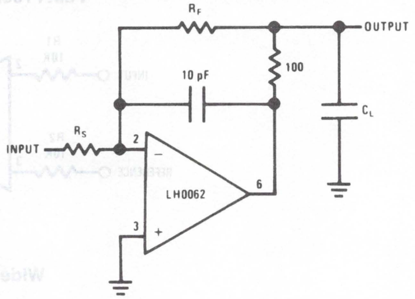
### Compensation for Minimum Settling† Time


2 - 10 pF
100K
V+
0.1 µF
INPUT
100K
2
7
–
5
LH0062
6
OUTPUT
3
+
51K

†Slew and settling time to 0.1% for a 10V step changes is 800 ns.

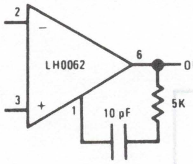
TL/K/6862-8

### Isolating Large Capacitive Loads


RF
OUTPUT
10 pF
100
CL
INPUT
RS
2
–
LH0062
6
3
+

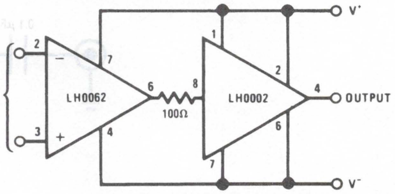
TL/K/6862-9

### Overcompensation


2
–
LH0062
6
OUTPUT
3
+
1
10 pF
5K

TL/K/6862-10

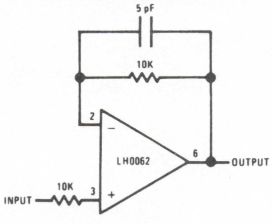
### Boosting Output Drive to ± 100 mA


V+
1
2
–
7
INPUT
LH0062
6
8
100Ω
LH0002
2
4
OUTPUT
3
+
4
6
7
V–

TL/K/6862-11

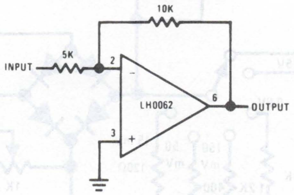
# Typical Applications*

### Fast Voltage Follower


5 pF
10K
2
–
LH0062
6
OUTPUT
10K
INPUT
3
+

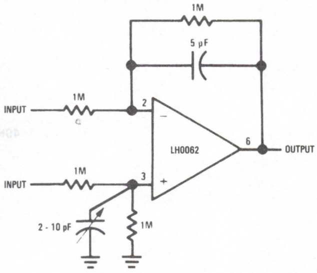
TL/K/6862-12

### Fast Summing Amplifier


10K
5K
INPUT
2
–
LH0062
6
OUTPUT
3
+

TL/K/6862-13

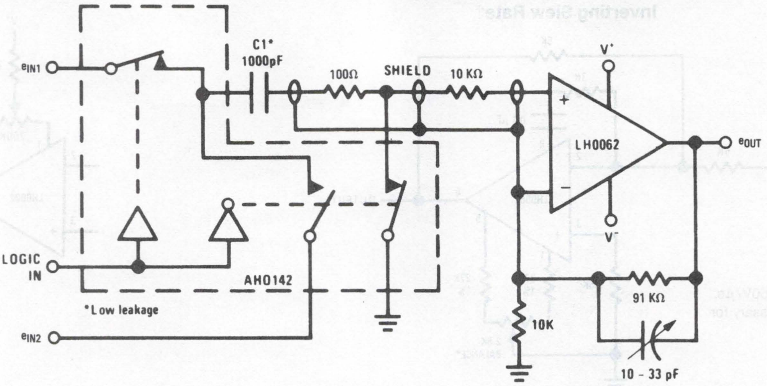
### Differential Amplifier


1M
5 pF
INPUT
1M
2
–
LH0062
6
OUTPUT
INPUT
1M
3
+
2 - 10 pF
1M

TL/K/6862-14

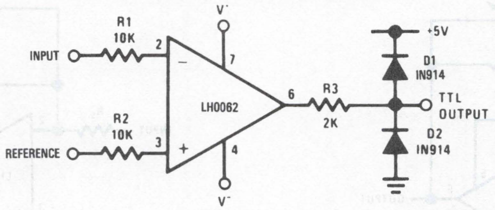
## Typical Applications* (Continued)

### High Speed Subtractor


eIN1
C1*
1000pF
100Ω
SHIELD
10 KΩ
V+
+
−
LH0062
eOUT
V−
LOGIC
IN
AH0142
*Low leakage
eIN2
10K
91 KΩ
10 - 33 pF

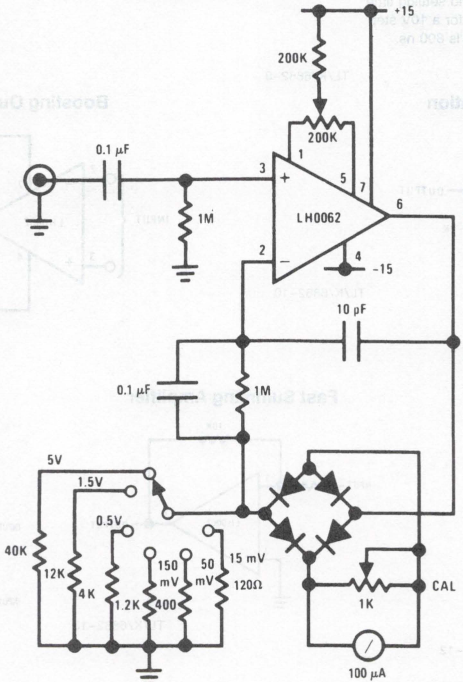
TL/K/6862-15

### Fast Precision Voltage Comparator


R1
10K
INPUT
2
−
V+
7
LH0062
6
R3
2K
+5V
D1
IN914
TTL
OUTPUT
D2
IN914
R2
10K
REFERENCE
3
+
4
V−

TL/K/6862-16

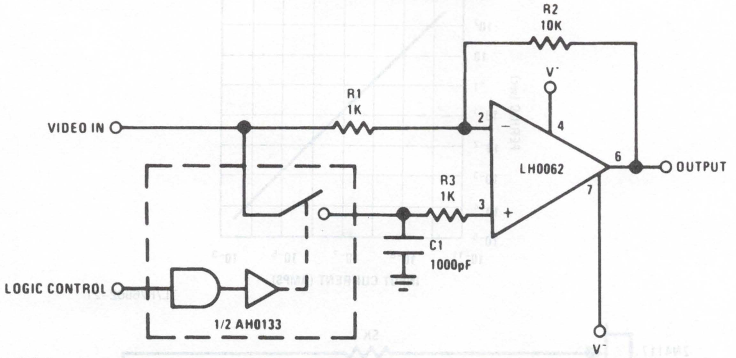
### Wide Range AC Voltmeter


+15
200K
200K
1
0.1 μF
3
+
5
7
6
LH0062
1M
2
−
4
−15
10 pF
0.1 μF
1M
5V
1.5V
0.5V
40K
12K
4K
1.2K
150
mV
400
50
mV
15 mV
120Ω
1K
CAL
100 μA

TL/K/6862-17

## Typical Applications* (Continued)

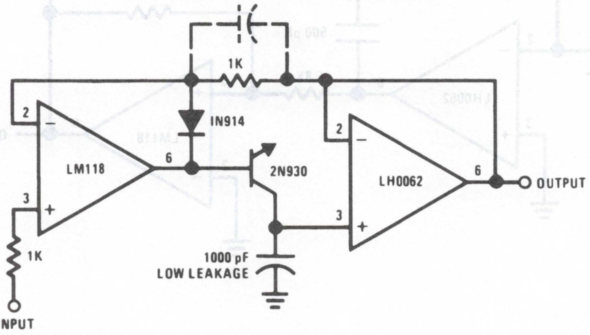
### Video DC Restoring Amplifier


R2
10K
V+
R1
1K
VIDEO IN
2
−
4
6
OUTPUT
LH0062
7
R3
1K
3
+
C1
1000pF
LOGIC CONTROL
1/2 AH0133
V−

*Pin numbers shown for TO-5 package

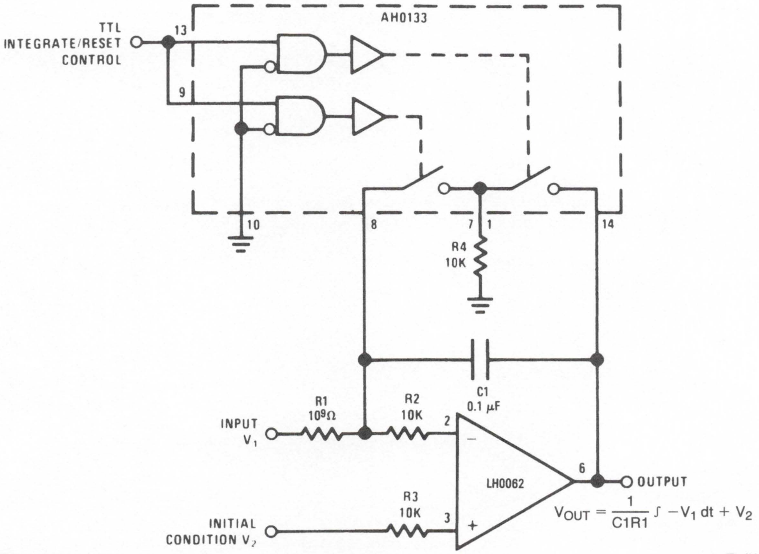
TL/K/6862–18

### High Speed Positive Peak Detector


1K
2
−
IN914
LM118
6
2N930
2
−
LH0062
6
OUTPUT
3
+
3
+
1K
1000 pF
LOW LEAKAGE
INPUT

TL/K/6862–19

### Precision Integrator


AH0133
TTL
INTEGRATE/RESET
CONTROL
13
9
10
8
7
1
14
R4
10K
C1
0.1 μF
R1
10⁹Ω
R2
10K
INPUT
V1
2
−
LH0062
6
OUTPUT
R3
10K
3
+
INITIAL
CONDITION V2

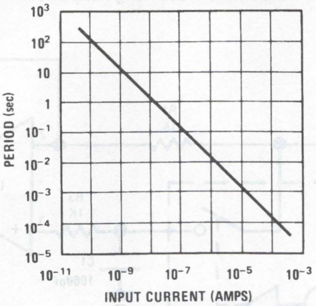
$$V_{OUT} = \frac{1}{C1R1} \int -V_1\,dt + V_2$$

*Pin numbers shown for TO-5 package

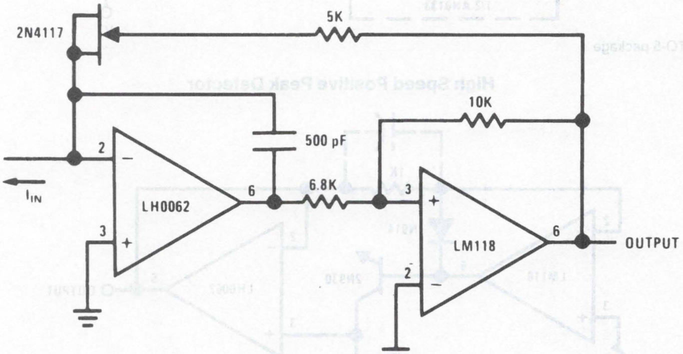
TL/K/6862–20

## Typical Applications* (Continued)

### Precision Wide Range Current to Period Converter



TL/K/6862-21


2N4117
5K
10K
500 pF
2
−
3
+
$I_{IN}$
LH0062
6
6.8K
3
+
2
−
LM118
6
OUTPUT

TL/K/6862-22

**National Semiconductor Corporation**

# LH0082 Optical Communication Receiver/Amplifier

## General Description

The LH0082 is a general purpose, low-noise, fiber-optic receiver, which may also be used as a fast current to voltage converter, or as a high speed voltage amplifier. The circuit includes a wide-bandwidth FET-input amplifier, a 2.4V reference, a comparator with hysteresis, and all the necessary resistors and capacitors for feedback and coupling, all integrated in a hermetic dual-in-line package. The large gain-bandwidth of the preamp enables fast response even with high capacitance photodiodes. A separate analog output permits the reception of analog signals to 20 MHz via a fiber-optic link. The internal comparator converts a low level analog signal to a CMOS/TTL compatible logic signal at data rates up to 5 Mbits/s NRZ. The LH0082 can be used with an external comparator at data rates to 40 Mbits/s.

## Features

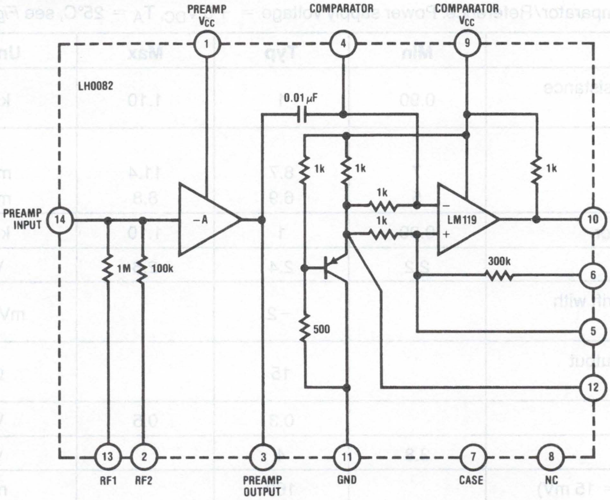
- Single 4.5V to 12V supply
- 600 MHz unity gain bandwidth
- Low noise
- Low edge jitter
- $<10^{-9}$ bit error rate
- Low input bias current
- Pin selectable sensitivity: −45 dBm/−35 dBm*
- CMOS/TTL compatibility
- Can be used with photodiodes, PIN photodiodes, phototransistors, avalanche photodiodes, and photomultipliers
- Hermetic dual-in-line metal package
- Highly versatile building block
- >21 dB dynamic range

## Applications

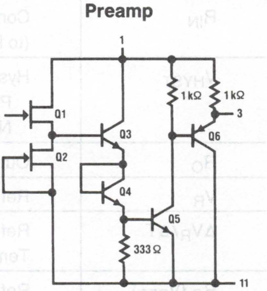
- Data terminals
- Secure communication
- Peripheral control/communication
- Video transmission
- Wideband amplifier
- High speed current to voltage converter
- Fiber-optic repeater
- Video amplifier
- Industrial machine control

*Assumes 0.5 A/W PIN diode input

## Schematic Diagrams


PREAMP V_CC
COMPARATOR
COMPARATOR V_CC
1
4
9
LH0082
0.01 µF
1k
1k
1k
1k
1k
−A
LM119
−
+
PREAMP INPUT
14
1M
100k
300k
500
10
COMPARATOR OUTPUT
6
HYSTERESIS
5
COMPARATOR +
12
REFERENCE
13
2
3
11
7
8
RF1
RF2
PREAMP OUTPUT
GND
CASE
NC

TL/H/9325-1


Preamp
1
14
Q1
Q2
Q3
Q4
Q5
Q6
1 kΩ
1 kΩ
3
333 Ω
11

TL/H/9325-3

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 1)**

| | |
|---|---|
| Supply Voltage | +15V |
| Power Dissipation, $T_A = 25°C$ | 0.5W |
| Junction Temperature | 150°C |
| Storage Temperature | −65°C to +150°C |
| Operating Temperature Range (Note 2) | |
| LH0082CD | −25°C to +85°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Input Current | ±10 mA |
| ESD Susceptibility | TBD |

## Electrical Characteristics Preamplifier: Power supply voltage = $+5\ V_{DC}$, $T_A = 25°C$, see *Figure 1*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_B$ | Input Bias Current | | 100 | 250 | pA |
| $C_{IN}$ | Input Capacitance | | | 5 | pF |
| $A_V$ | Voltage Gain | 50 | 90 | | V/V |
| $f_{3\ dB}$ | −3 dB Frequency | | 18 | | MHz |
| $V_Q$ | Output Quiescent Voltage | 1.9 | 2.1 | 2.6 | V |
| $\Delta V_Q/\Delta T$ | Output Quiescent Voltage Drift with Temperature | | −6 | | mV/°C |
| $Z_O$ | Open Loop Output Impedance at 1 MHz | | 30 | | Ω |
| | Output Noise (10 Hz to 10 MHz) | | 300 | | μV RMS |
| $V_O$ | Output Swing (No Load) | 3.5 | 4.0 | | $V_{P-P}$ |
| | Transimpedance: | | | | |
| | Low Sensitivity | 90 | 100 | 110 | kΩ |
| | High Sensitivity | 0.9 | 1 | 1.1 | MΩ |
| $I_S$ | Supply Current | | 22 | 30 | mA |

## Electrical Characteristics Comparator/Reference: Power supply voltage = $+5V_{DC}$, $T_A = 25°C$, see *Figure 2*

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $R_{IN}$ | Comparator Input Resistance (to Reference) | 0.90 | 1 | 1.10 | kΩ |
| $V_{HYST}$ | Hysteresis Voltage | | | | |
| | Positive | 7 | 8.7 | 11.4 | mV |
| | Negative | 5 | 6.9 | 8.8 | mV |
| $R_O$ | Output Pull-up Resistor | 0.90 | 1 | 1.10 | kΩ |
| $V_R$ | Reference Voltage | 2.2 | 2.4 | 2.6 | V |
| $\Delta V_R/\Delta T$ | Reference Voltage Drift with Temperature | | −2 | | mV/°C |
| $R_O$ ($V_{REF}$) | Reference Voltage Output Resistance | | 15 | | Ω |
| $V_{OL}$ | ($I_{OL} = 3.2$ mA) | | 0.3 | 0.5 | V |
| $V_{OH}$ | ($I_{OH} = -1$ mA) | 3.8 | 4 | | V |
| $T_{PD}$ | ($V_{IN} = 30$ mV, $V_{OD} = 15$ mV) | | 160 | | ns |
| $T_R$ | ($C_L = 3$ pF) | | 80 | | ns |
| $T_F$ | ($C_L = 3$ pF) | | 60 | | ns |
| $I_S$ | Supply Current: | | | | |
| | Output High | 4.5 | 8 | 17 | mA |
| | Output Low | 9.5 | 13 | 22 | mA |

## Electrical Characteristics

Fiber-Optic Receiver: Photodiode responsivity is assumed to be 0.5 A/W, capacitance of 10 pF at 2.5V reverse bias, $V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15 pF

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | High Sensitivity: $R_F$ = 1 MΩ,<br>(see *Figure 3*)<br>Input Power for $10^{-9}$ BER<br>(Bit Rate = 500 kbit NRZ) | | 200 | | nW |
| $t_r$, $t_f$ | Analog Output Rise or Fall Time<br>Maximum Data Rate, NRZ, Digital Output | | 1.5<br>650 | | μs<br>kbit/s |
| $P_N$ | Noise Equivalent Power | | 1 | | nW |
| $i_N$ | Equivalent Input Noise Current (10 Hz to 10 MHz) | | 300 | | pA RMS |
| | Low Sensitivity: $R_F$ = 100 kΩ,<br>(see *Figure 4*)<br>Input Power for $10^{-9}$ BER<br>(Bit Rate = 2 Mbit NRZ) | | 800 | | nW |
| $t_r$, $t_f$ | Analog Output Rise or Fall Time<br>Maximum Data Rate, NRZ, Digital Output | | 50<br>5 | | ns<br>Mbit/s |
| $P_N$ | Noise Equivalent Power | | 10 | | nW |
| $i_N$ | Equivalent Input Noise Current (10 Hz to 10 MHz) | | 3 | | nA RMS |
| $I_S$ | Total Supply Current (High or Low Sensitivity) | | 35 | | mA |

**Note 1:** Refer to RETS0082D for LH0082D/883 and LH0082D-MIL specifications.

**Note 2:** For military temperature range, see RETS0082D.

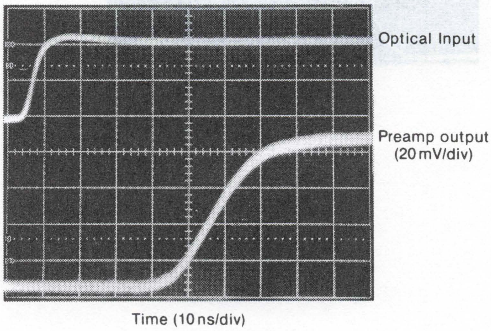
### DIGITAL EDGE JITTER

A potential problem in digital transmission systems is "edge jitter". Jitter is related to the system rise time and receiver noise and can be approximated by the following equation:

$$\text{RMS edge jitter} = \frac{\text{System rise time (10\%–90\%)}}{\text{(p/p signal voltage} \div \text{RMS noise voltage in receiver)}}$$

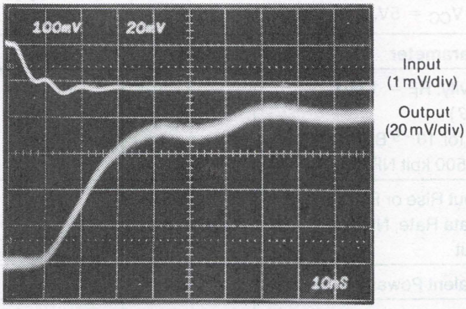
For a 5 Mbits/s NRZ operation using a 0.5 A/W PIN diode, the LH0082 requires a 2 μW peak optical power. This translates to 120 mV peak-to-peak signal voltage. Following through this equation the RMS edge jitter of the LH0082 is inconsequential at approximately 0.1 μs.

**Fiber-Optic Receiver Preamp Response**
$R_F$ = 100 kΩ
Photodiode capacitance = 10 pF, $V_{CC}$ = 5V



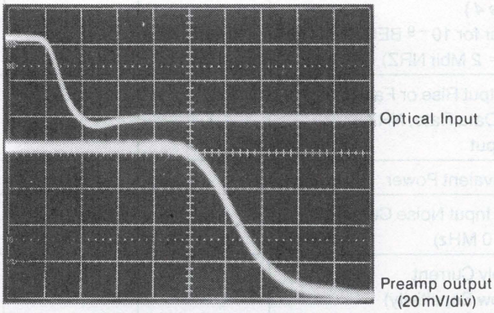
TL/H/9325–4

## Preamp Voltage Mode Pulse Response



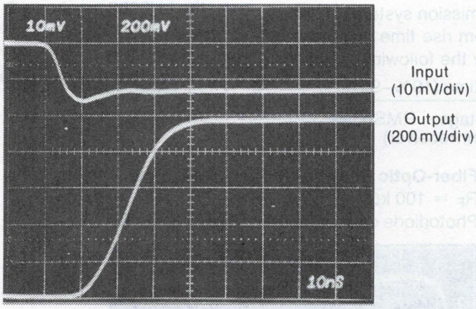
Small Signal

TL/H/9325-5



Time (10 ns/div)

TL/H/9325-6

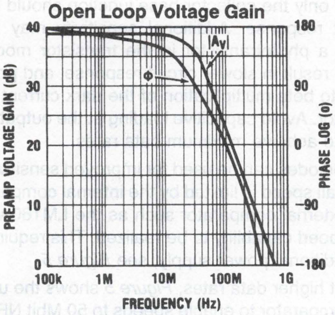


Large Signal

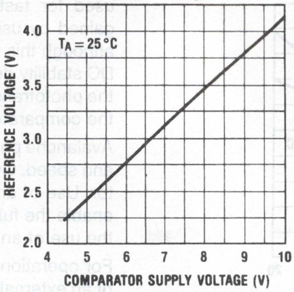
TL/H/9325-7

## Typical Performance Characteristics

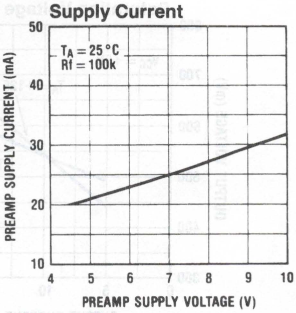
**Open Loop Voltage Gain**



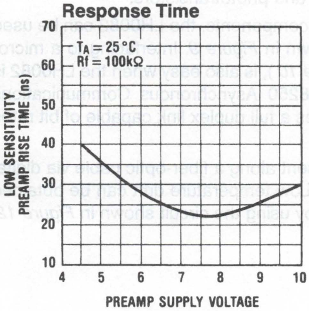
**Reference Voltage**



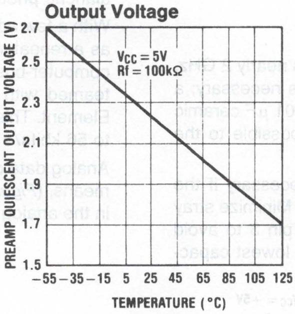
**Supply Current**



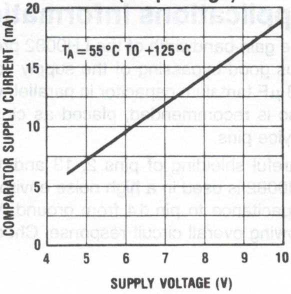
**Response Time**



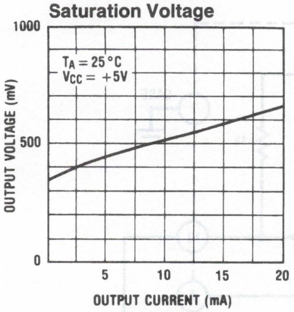
**Output Voltage**



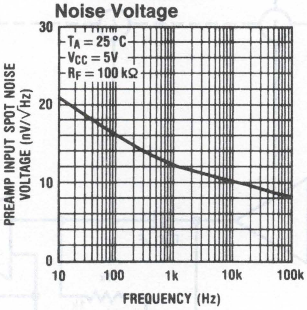
**Comparator Supply Current (Output High)**



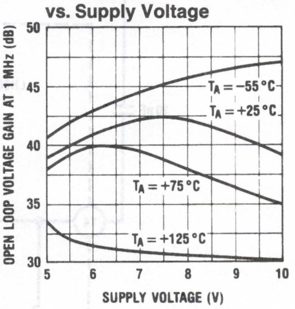
**Comparator Output Saturation Voltage**



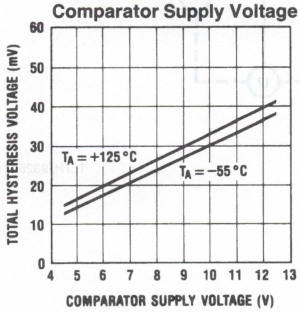
**Preamp Input Spot Noise Voltage**



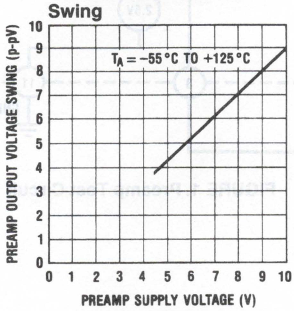
**Preamp Open Loop Voltage vs. Supply Voltage**



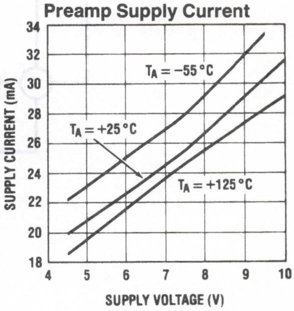
**Hysteresis Voltage vs. Comparator Supply Voltage**



**Preamp Output Voltage Swing**

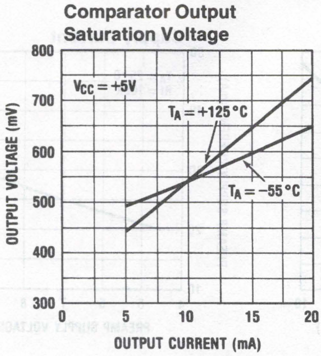


**Preamp Supply Current**



TL/H/9325-8

## Typical Performance Characteristics (Continued)



TL/H/9325-9

## Applications Information

The gain-bandwidth of the LH0082 preamp is nearly 2 GHz, thus good bypassing of the supply voltage is necessary; a 3.3 μF tantalum capacitor in parallel with a 0.01 μF ceramic disc is recommended, placed as close as possible to the device pins.

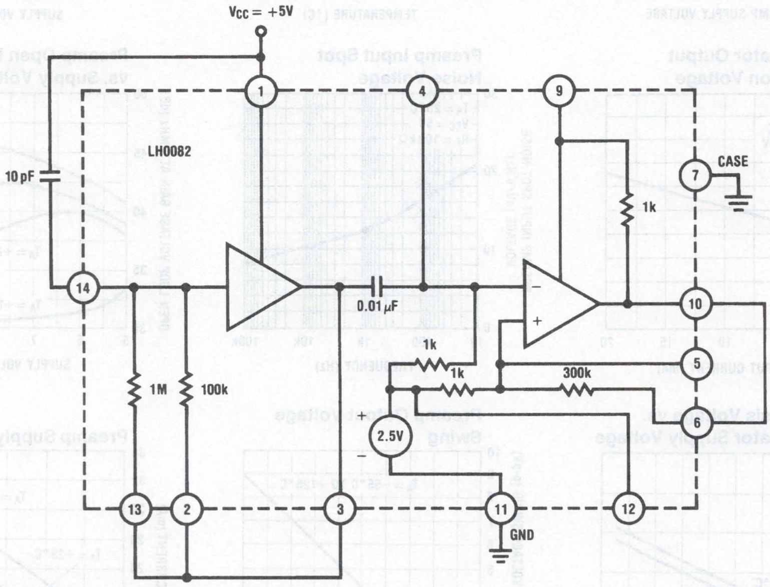
Careful shielding of pins 2, 13 and 14 is necessary if the LH0082 is used in a high noise environment. Minimize stray capacitance to pin 14 from ground, $V_{CC}$ or pin 3 to avoid slowing overall circuit response. Choose the lowest capacitance photodiode possible for the application. When using phototransistors, only the collector-base junction should be used for fastest response. Additional sensitivity may be gained by using a phototransistor in the transistor mode, although this will result in slower circuit response, and poor DC stability due to beta multiplication of the dark current of the phototransistor. Avoid capacitive loading at the output of the comparator to achieve maximum data rates.

Avalanche photodiodes can be used for improved sensitivity and speed. Overall speed is limited by the internal comparator. Use of an external comparator such as the LM160 will enable the full speed capability to be realized. This requires the use of an additional power supply, see *Figure 5*.

For operations at higher data rates, *Figure 5* shows the use of an external comparator to enable speeds to 50 Mbit NRZ. *Figure 6, 7* and *8* demonstrate interfacing techniques to avalanche photodiodes and phototransistors.

With a few additional components, the LH0082 can be used as a repeater as shown in *Figure 9*. Interfacing to a microcomputer-bus, (*Figure 10*), is also easy when the LH0082 is teamed with an INS8250 Asynchronous Communications Element. This provides a full duplex link capable of bit rates to 56 kbits/s NRZ.

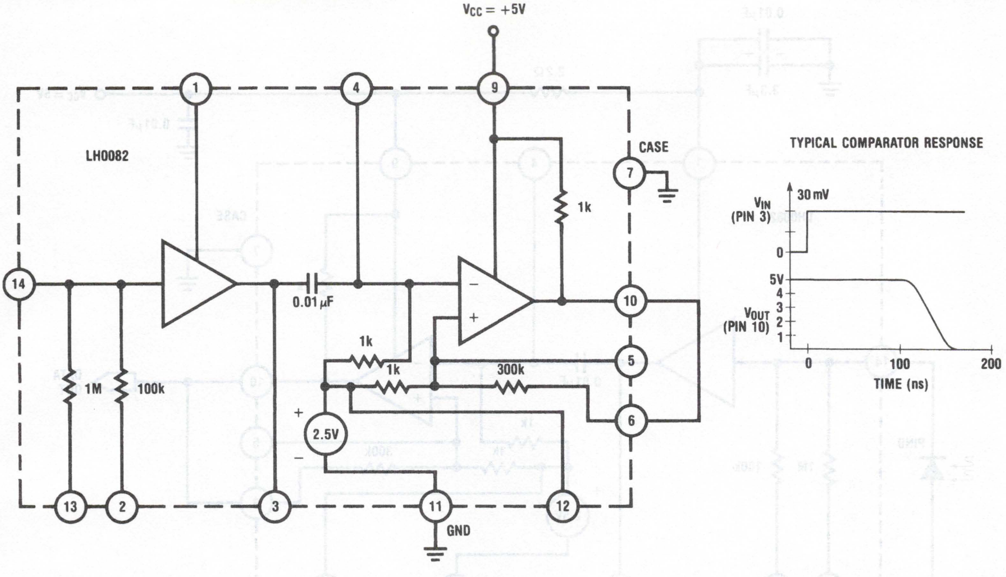
Analog data can be sent along a fiber-optic cable via digital means, (*Figure 11*). Low temperature drift can be obtained in the analog mode, by using the circuit shown in *Figure 12*.



TL/H/9325-10

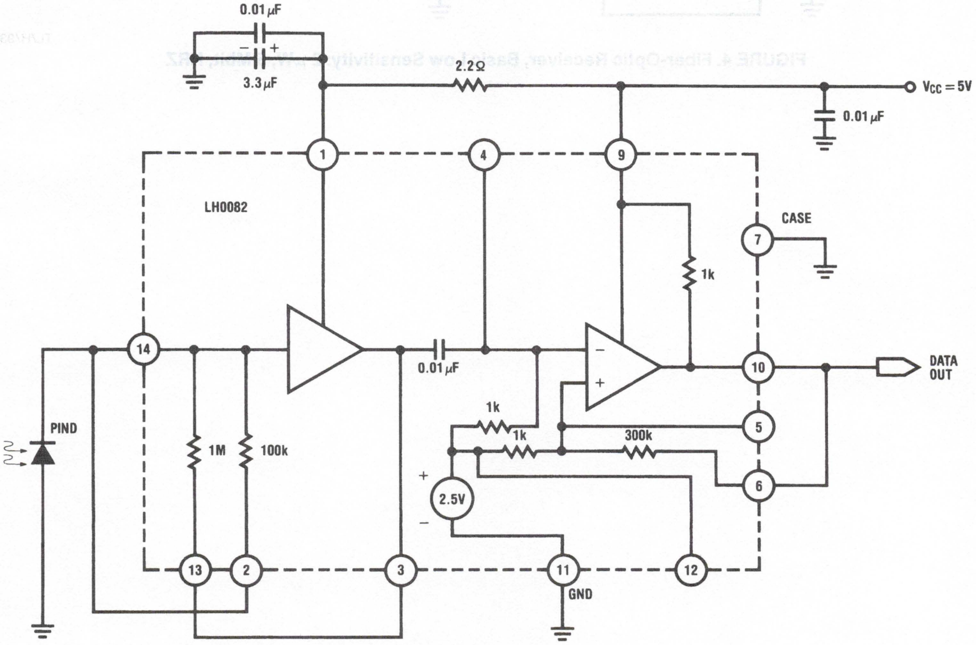
FIGURE 1. Preamp Test Circuit

# Applications Information (Continued)


VCC = +5V
LH0082
1
4
9
1k
CASE
7
14
0.01 µF
10
1k
1k
300k
5
6
+
2.5V
−
1M
100k
13
2
3
11
GND
12
TYPICAL COMPARATOR RESPONSE
VIN
(PIN 3)
30 mV
0
5V
4
3
2
1
VOUT
(PIN 10)
0
100
200
TIME (ns)

TL/H/9325-11

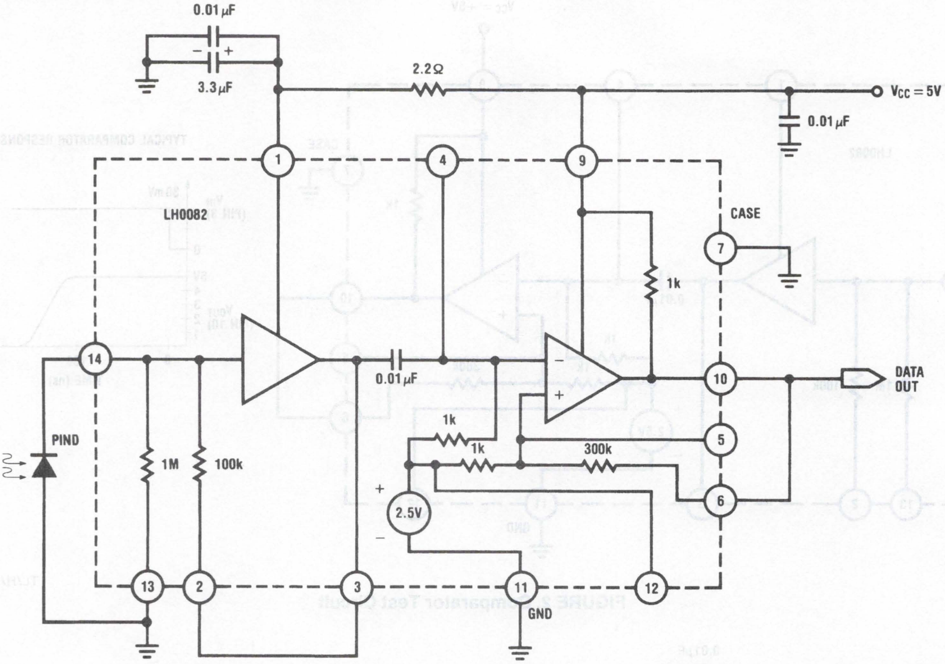
FIGURE 2. Comparator Test Circuit


0.01 µF
3.3 µF
2.2Ω
VCC = 5V
0.01 µF
1
4
9
LH0082
CASE
7
1k
14
0.01 µF
10
DATA OUT
PIND
1M
100k
1k
1k
300k
5
6
+
2.5V
−
13
2
3
11
GND
12

TL/H/9325-12

FIGURE 3. Fiber-Optic Receiver, Basic High Sensitivity: 150 nW, 400 kbps NRZ

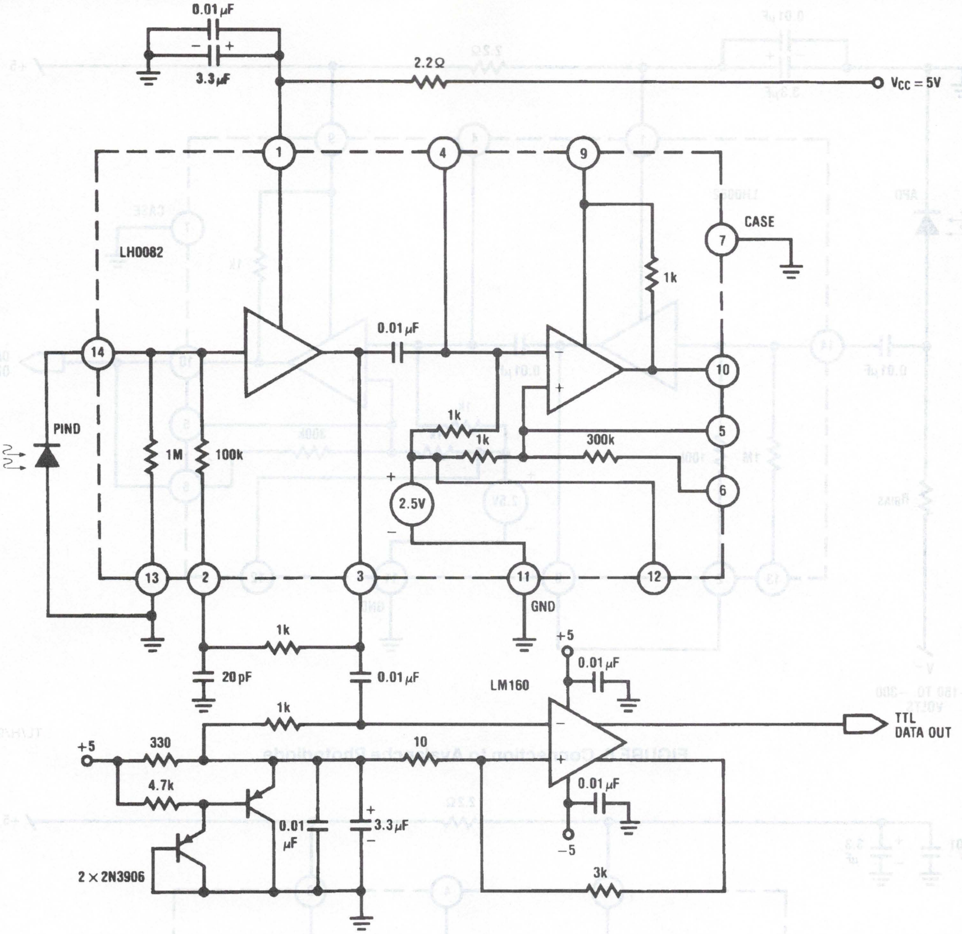
## Applications Information (Continued)


0.01 μF
−
+
3.3 μF
2.2Ω
V_CC = 5V
0.01 μF
1
4
9
LH0082
CASE
7
1k
14
PIND
1M
100k
0.01 μF
1k
1k
300k
−
+
10
DATA OUT
5
6
+
2.5V
−
13
2
3
11
GND
12

TL/H/9325-13

FIGURE 4. Fiber-Optic Receiver, Basic Low Sensitivity: 2 μW, 5 Mbit, NRZ

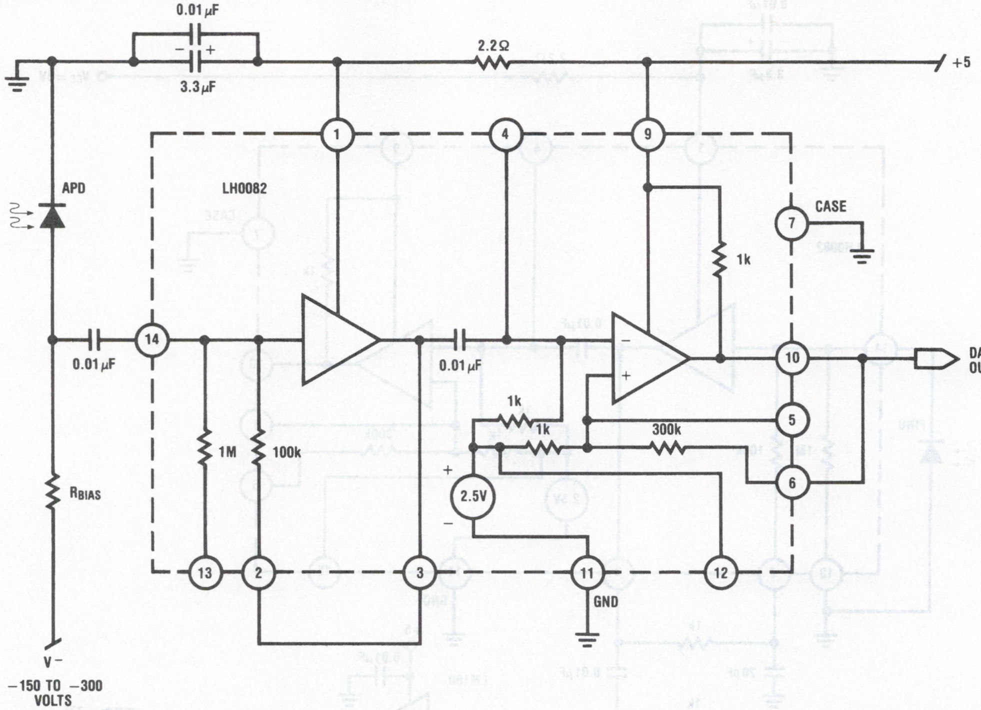
## Applications Information (Continued)


0.01 µF
3.3 µF
2.2Ω
V_CC = 5V
1
4
9
CASE
7
LH0082
1k
0.01 µF
14
10
PIND
1M
100k
1k
1k
300k
5
6
2.5V
13
2
3
11
12
GND
1k
20 pF
0.01 µF
+5
0.01 µF
LM160
1k
TTL DATA OUT
+5
330
10
4.7k
0.01 µF
3.3 µF
2 × 2N3906
0.01 µF
−5
3k

TL/H/9325-14

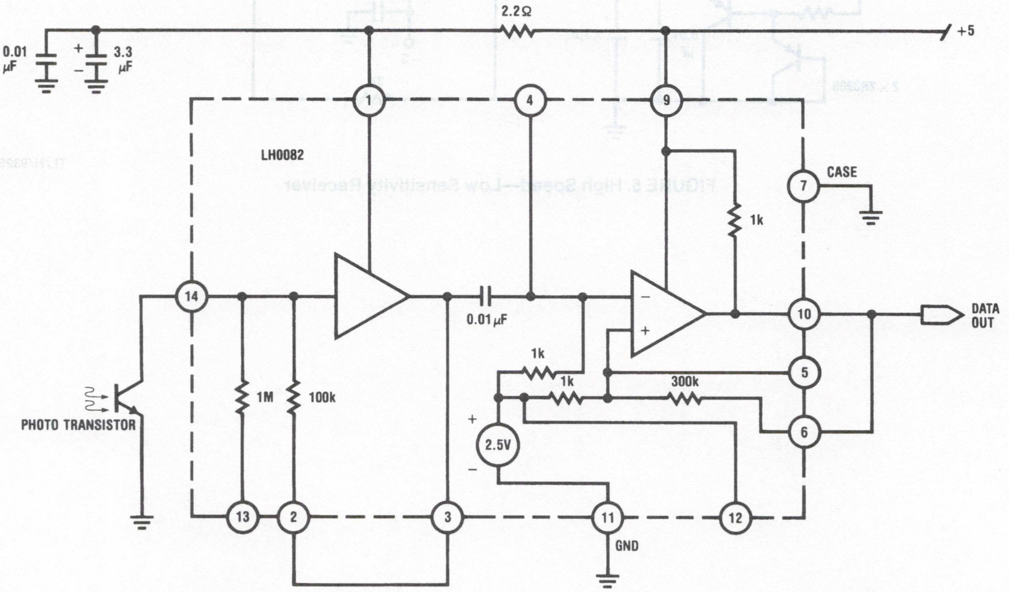
FIGURE 5. High Speed—Low Sensitivity Receiver

## Applications Information (Continued)


0.01 μF
3.3 μF
2.2Ω
+5
APD
LH0082
1
4
9
CASE
7
1k
14
0.01 μF
0.01 μF
10
DATA OUT
1k
1k
300k
5
1M
100k
RBIAS
2.5V
6
13
2
3
11
12
GND
V−
−150 TO −300 VOLTS

TL/H/9325-15

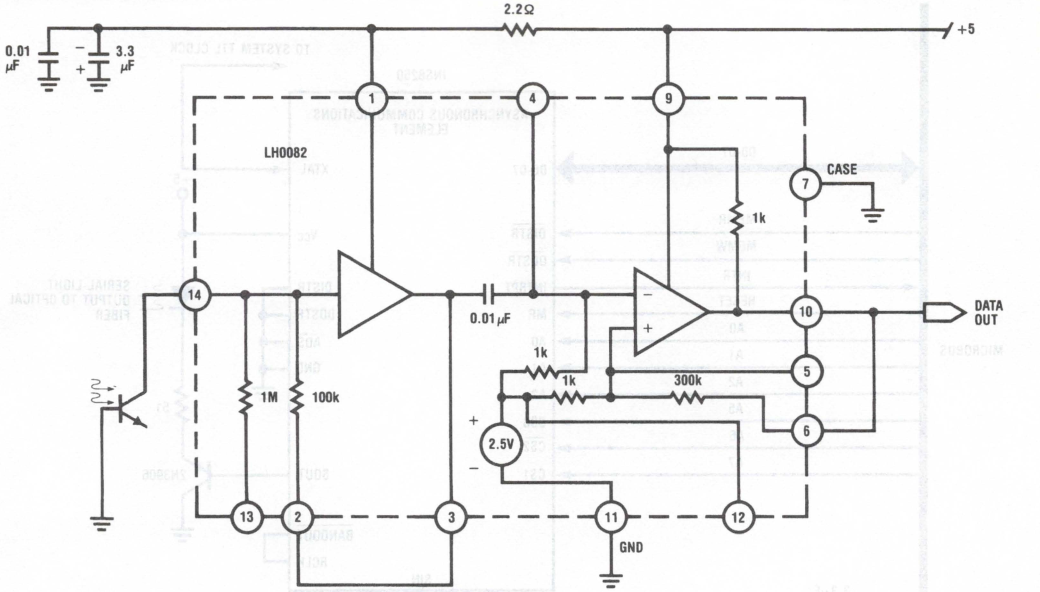
**FIGURE 6. Connection to Avalanche Photodiode**


2.2Ω
+5
0.01 μF
3.3 μF
1
4
9
LH0082
CASE
7
1k
14
0.01 μF
10
DATA OUT
1k
1k
300k
5
1M
100k
PHOTO TRANSISTOR
2.5V
6
13
2
3
11
12
GND

TL/H/9325-16

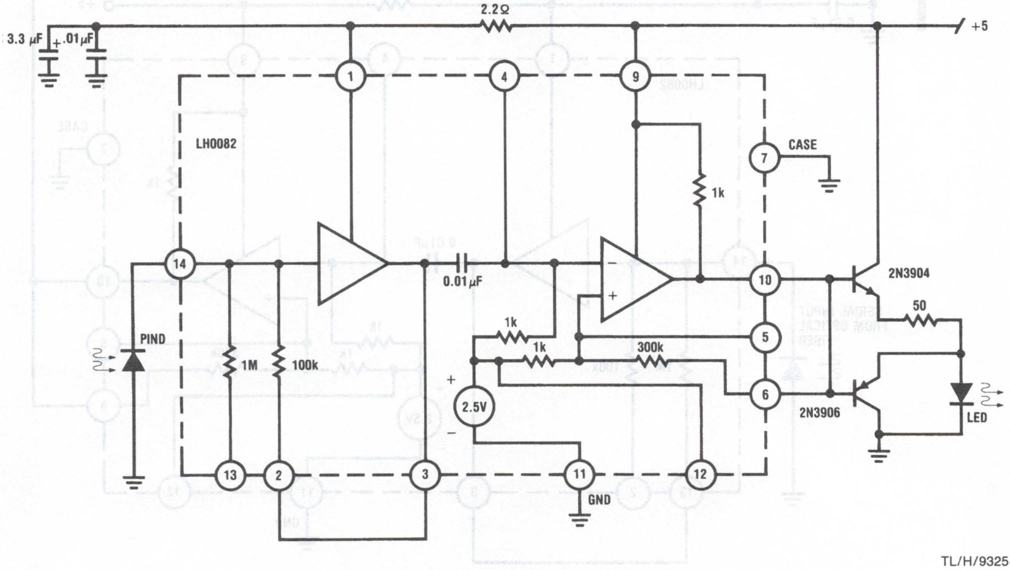
**FIGURE 7. Connection to Phototransistor—High Sensitivity, Low Speed**

## Applications Information (Continued)


2.2Ω
+5
0.01 µF
3.3 µF
LH0082
1
4
9
7
CASE
1k
14
0.01 µF
1k
1k
300k
10
DATA OUT
5
6
1M
100k
2.5V
13
2
3
11
12
GND

TL/H/9325–17

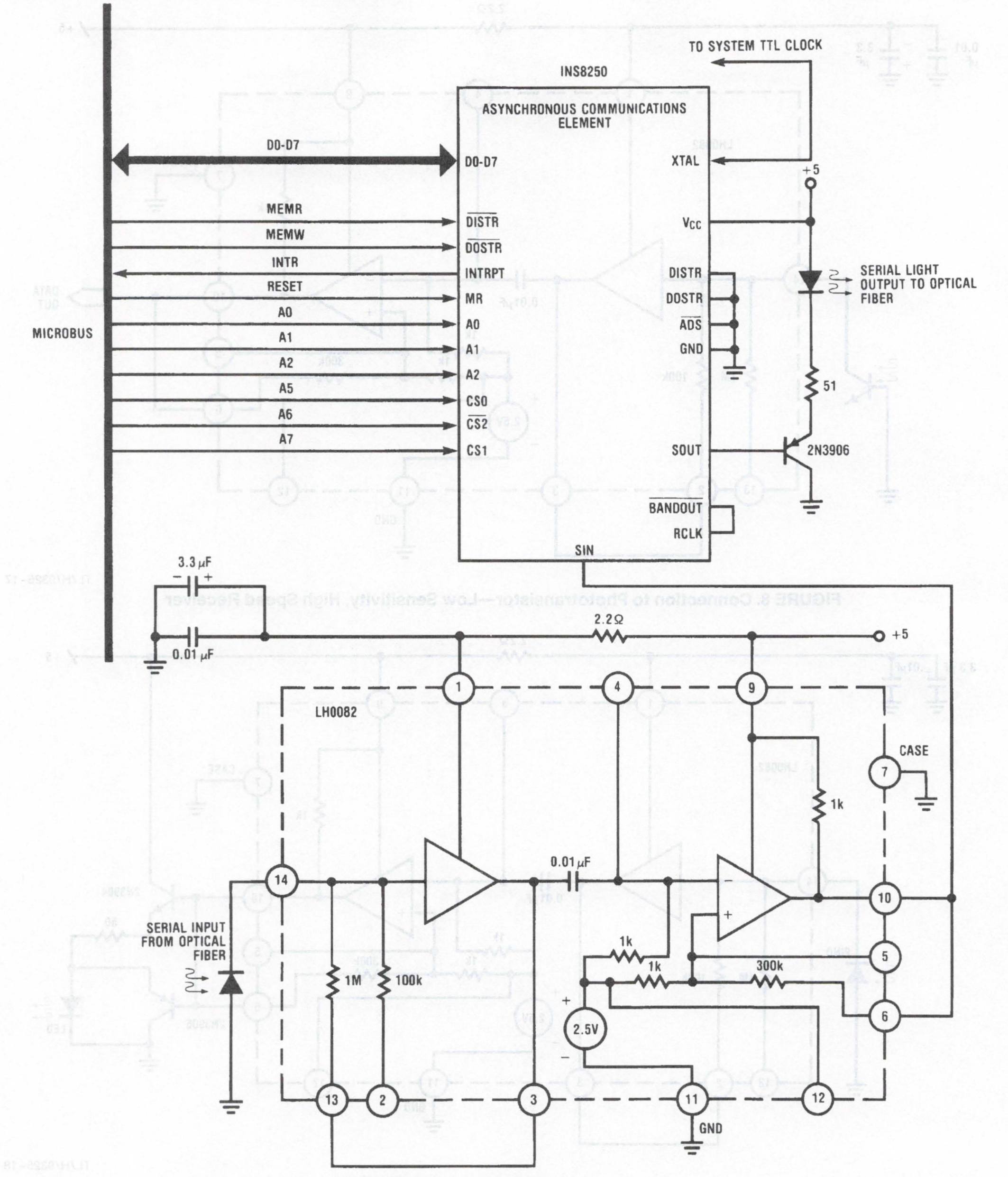
FIGURE 8. Connection to Phototransistor—Low Sensitivity, High Speed Receiver


3.3 µF
.01µF
2.2Ω
+5
LH0082
1
4
9
7
CASE
1k
14
0.01 µF
10
2N3904
50
PIND
1M
100k
1k
1k
300k
5
6
2N3906
LED
2.5V
13
2
3
11
12
GND

TL/H/9325–18

FIGURE 9. Fiber-Optic Link Repeater

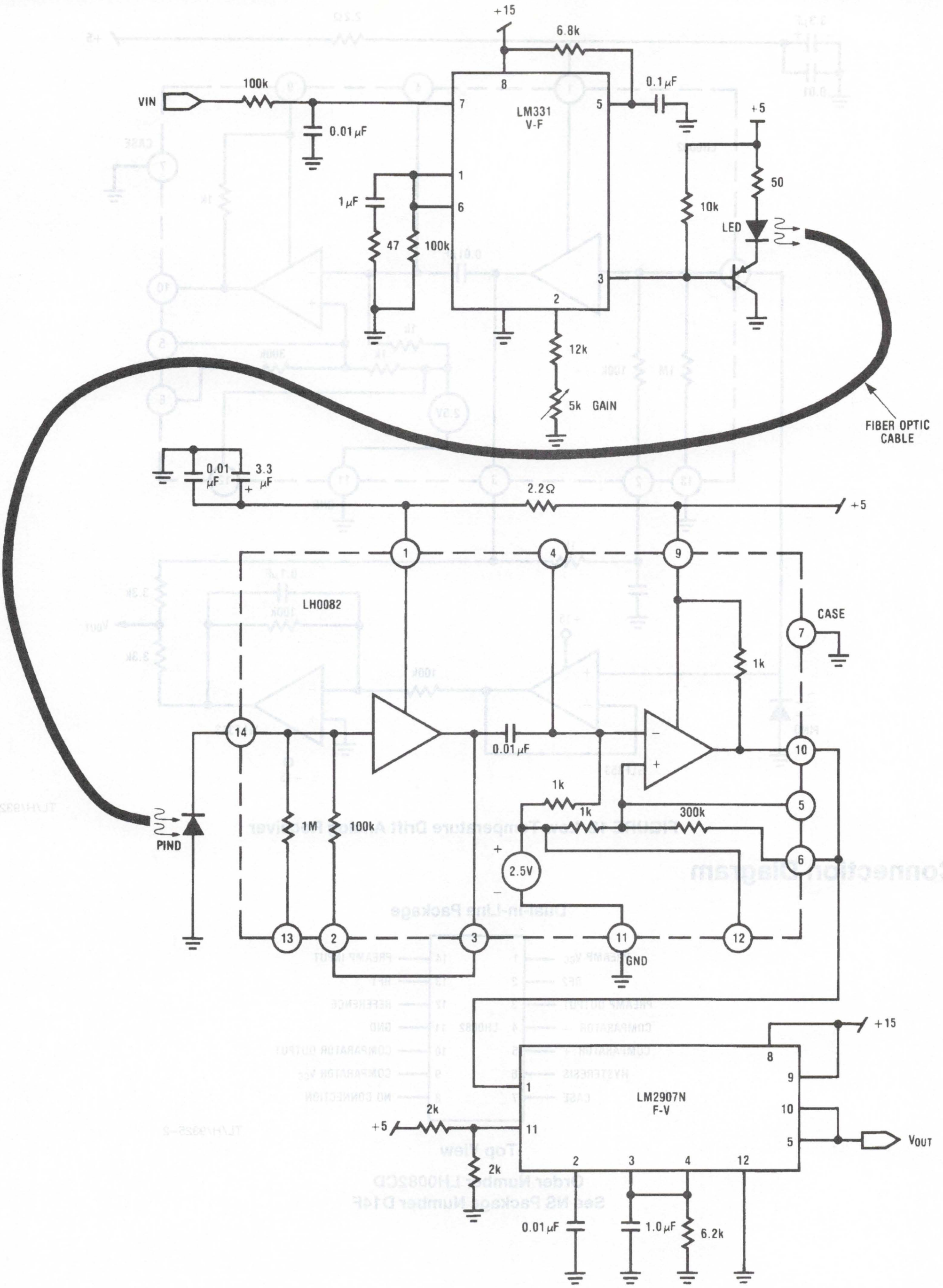
## Applications Information (Continued)


TO SYSTEM TTL CLOCK
INS8250
ASYNCHRONOUS COMMUNICATIONS ELEMENT
D0-D7
D0-D7
XTAL
+5
MEMR
DISTR
MEMW
DOSTR
VCC
INTR
INTRPT
DISTR
RESET
MR
DOSTR
A0
A0
ADS
MICROBUS
A1
A1
GND
A2
A2
A5
CS0
A6
CS2
A7
CS1
SOUT
2N3906
51
SERIAL LIGHT OUTPUT TO OPTICAL FIBER
BANDOUT
RCLK
SIN
3.3 μF
0.01 μF
2.2Ω
+5
1
4
9
LH0082
CASE
7
1k
14
0.01 μF
10
SERIAL INPUT FROM OPTICAL FIBER
1k
1k
300k
5
1M
100k
2.5V
6
13
2
3
11
12
GND

TL/H/9325-19

FIGURE 10. Optical Link to Microbus

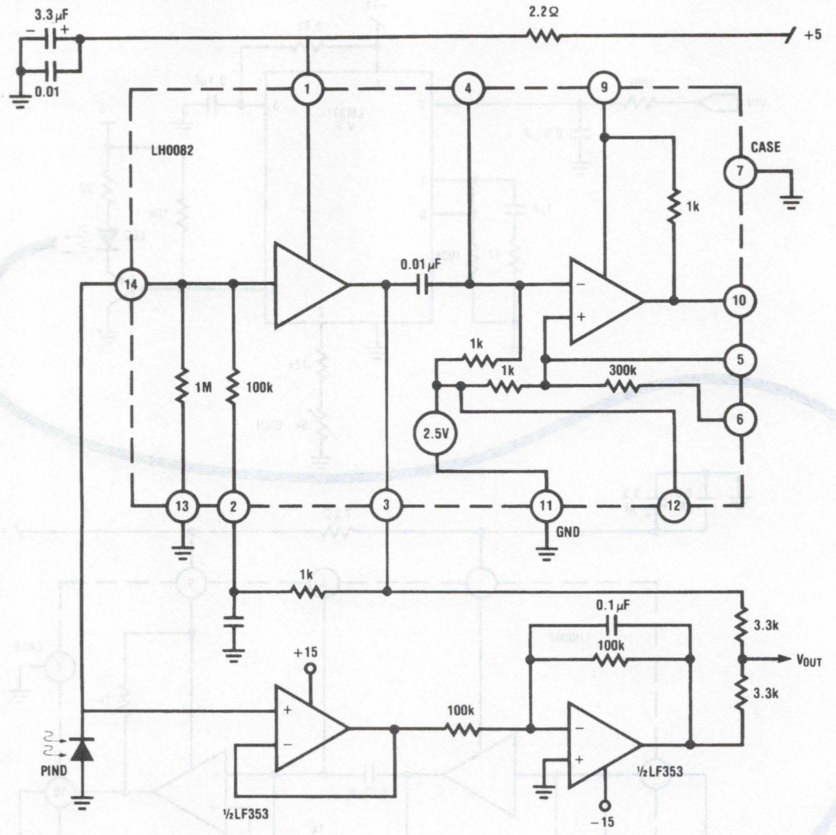
## Applications Information (Continued)


+15
6.8k
100k
VIN
8
7
5
LM331
V-F
0.1 μF
0.01 μF
+5
1
6
1 μF
47
100k
50
10k
LED
3
2
12k
5k GAIN
FIBER OPTIC
CABLE
0.01 μF
3.3 μF
+
2.2Ω
+5
1
4
9
LH0082
CASE
7
1k
14
0.01 μF
10
1k
1k
5
300k
+
2.5V
−
6
1M
100k
PIND
13
2
3
11
GND
12
+15
8
9
1
LM2907N
F-V
10
+5
2k
11
5
VOUT
2k
2
3
4
12
0.01 μF
1.0 μF
6.2k

TL/H/9325-20

FIGURE 11. Analog Data Link Using V/F and F/V

## Applications Information (Continued)

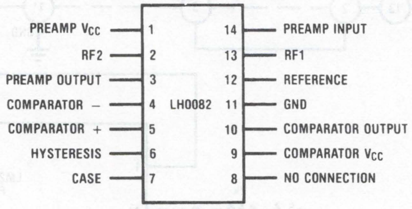

3.3 μF
0.01
2.2Ω
+5
LH0082
1
4
9
CASE
7
1k
14
0.01 μF
10
5
1k
1k
300k
6
1M
100k
2.5V
13
2
3
11
GND
12
1k
0.1 μF
100k
3.3k
V_OUT
3.3k
+15
100k
PIND
½LF353
½LF353
−15

TL/H/9325-21

FIGURE 12. Low Temperature Drift Analog Receiver

## Connection Diagram

### Dual-In-Line Package


PREAMP V_CC 1
RF2 2
PREAMP OUTPUT 3
COMPARATOR − 4
COMPARATOR + 5
HYSTERESIS 6
CASE 7
LH0082
14 PREAMP INPUT
13 RF1
12 REFERENCE
11 GND
10 COMPARATOR OUTPUT
9 COMPARATOR V_CC
8 NO CONNECTION

TL/H/9325-2

**Top View**

**Order Number LH0082CD**
**See NS Package Number D14F**

**National Semiconductor Corporation**

# LH0086/LH0086C
# Digitally-Programmable-Gain Amplifier

## General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

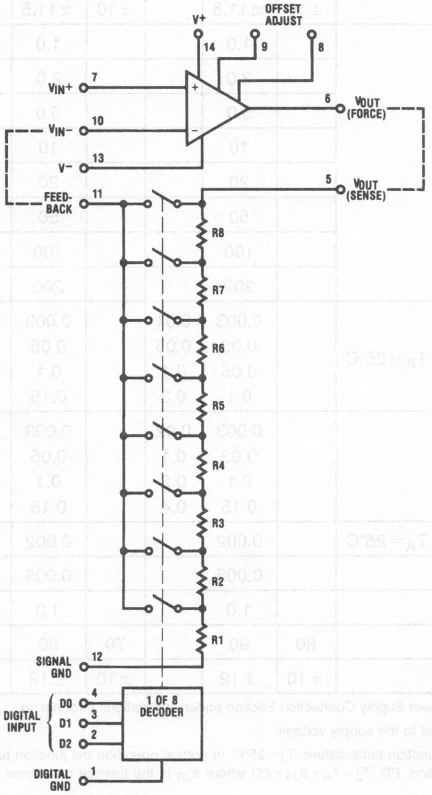
## Features

- 0.01% maximum gain accuracy at gain = 1
- 0.005% typical gain non-linearity
- 1 ppm/°C typical gain drift
- $10^{10}\Omega$ input impedance
- 80 dB minimum PSRR.
- TTL-compatible digital inputs
- 2 μs settling to 0.01%

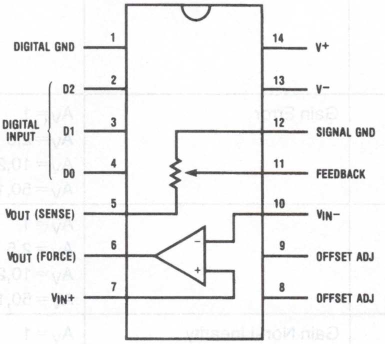
## Applications

- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

## Simplified Schematic and Connection Diagrams


V+
14
OFFSET ADJUST
9
8
7
VIN+
6
VOUT (FORCE)
10
VIN−
13
V−
5
VOUT (SENSE)
11
FEED-BACK
R8
R7
R6
R5
R4
R3
R2
R1
12
SIGNAL GND
4
D0
3
D1
2
D2
DIGITAL INPUT
1 OF 8 DECODER
1
DIGITAL GND

**Dual-In-Line Package**


DIGITAL GND
1
D2
2
DIGITAL INPUT
D1
3
D0
4
VOUT (SENSE)
5
VOUT (FORCE)
6
VIN+
7
14
V+
13
V−
12
SIGNAL GND
11
FEEDBACK
10
VIN−
9
OFFSET ADJ
8
OFFSET ADJ

**Top View**

**CASE IS ELECTRICALLY ISOLATED**

**Order Number LH0086D or LH0086CD**
**See NS Package Number D14F**

TL/K/5657–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | | |
|---|---|---|
| $V_S$ | Supply Voltage (Note 1) | ±18V |
| $V_{IN}$ | Analog Input Voltage (Note 2) | ±15V |
| $V_{IL(H)}$ | Digital Input Voltage | $-4V, +V_S$ |
| $P_D$ | Power Dissipation | 500 mW |
| | Output Short Circuit Duration | Continuous |
| $T_A$ | Operating Temperature Range: | |
| | LH0086 | −55°C to +125°C |
| | LH0086C | −25°C to +85°C |
| $T_{STG}$ | Storage Temperature | −65°C to +150°C |
| | Lead Temperature (Soldering, 10 seconds) | +300°C |

ESD rating to be determined.

## DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

| Symbol | Parameter | Conditions | | LH0086 | | | LH0086C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | | $T_J = 25°C$ | | 0.3 | 5.0 | | 0.3 | 10 | mV |
| | | | | | | 7.0 | | | 13 | |
| $V_{OS}/\Delta T$ | Input Offset Voltage Change with Temperature | $V_{IN} = 0V$ | | | 10 | | | 10 | | µV/°C |
| $I_B$ | Input Bias Current | (Notes 3, 4) | $T_J = 25°C$ | | 100 | 500 | | 100 | 500 | pA |
| | | | | | | 500 | | | 100 | nA |
| $R_{IN}$ | Input Resistance | | | | 10 | | | 10 | | GΩ |
| $V_{IN}$ | Input Voltage Range | | | ±10 | ±11.5 | | ±10 | ±11.5 | | V |
| $A_V$ | Voltage Gain | See Table 1 for Digital Gain-Control Codes | | | 1.0 | | | 1.0 | | V/V |
| | | | | | 2.0 | | | 2.0 | | |
| | | | | | 5.0 | | | 5.0 | | |
| | | | | | 10 | | | 10 | | |
| | | | | | 20 | | | 20 | | |
| | | | | | 50 | | | 50 | | |
| | | | | | 100 | | | 100 | | |
| | | | | | 200 | | | 200 | | |
| | Gain Error | $A_V = 1$ | $T_A = 25°C$ | | 0.003 | 0.01 | | 0.003 | 0.03 | % |
| | | $A_V = 2,5$ | | | 0.03 | 0.05 | | 0.05 | 0.1 | |
| | | $A_V = 10,20$ | | | 0.05 | 0.1 | | 0.1 | 0.2 | |
| | | $A_V = 50,100,200$ | | | 0.1 | 0.3 | | 0.15 | 0.4 | |
| | | $A_V = 1$ | | | 0.003 | 0.02 | | 0.003 | 0.06 | |
| | | $A_V = 2,5$ | | | 0.03 | 0.1 | | 0.05 | 0.2 | |
| | | $A_V = 10,20$ | | | 0.1 | 0.2 | | 0.1 | 0.3 | |
| | | $A_V = 50,100,200$ | | | 0.15 | 0.4 | | 0.15 | 0.5 | |
| | Gain Non-Linearity | $A_V = 1$ | $T_A = 25°C$ | | 0.002 | | | 0.002 | | % |
| | | | | | 0.005 | | | 0.005 | | |
| $\Delta A_V/\Delta T$ | Gain Temperature Coefficient | $A_V = 1$ | | | 1.0 | | | 1.0 | | ppm/°C |
| PSRR | Power Supply Rejection Ratio | $\pm 8V \le V_S \le \pm 18V$ | | 80 | 90 | | 70 | 90 | | dB |
| $V_O$ | Output Voltage Swing | $R_L \ge 10\ k\Omega$ | | ±10 | ±12 | | ±10 | ±12 | | V |

**Note 1:** Improper supply power-on sequence may damage the device. See Power Supply Connection Section under Applications Information.

**Note 2:** for supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

**Note 3:** Due to short production test time, these parameters are specified at junction temperature, $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature, $T_A$, as a result of the internal power dissipation, PD. $T_J = T_A + \theta_{JA} \times PD$ where $\theta_{JA}$ is the thermal resistance from junction to ambient (typically 65°C/W).

**Note 4:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

**Note 5:** Refer to RETS0086D for LH0086D military specifications.

## DC Electrical Characteristics (Continued)

$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting).

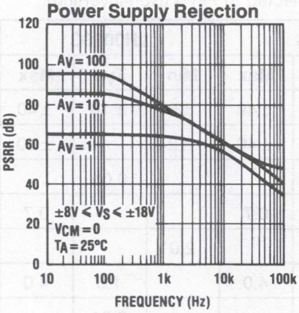
| Symbol | Parameter | Conditions | LH0086 | | | LH0086C | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{SC}$ | Output Short-Circuit Current | $T_A = 25°C$ | ±5 | ±18 | ±40 | ±5 | ±18 | ±40 | mA |
| | | | ±2 | | ±40 | ±2 | | ±40 | |
| $R_O$ | Output Resistance | $A_{VCL} = 1$ | | 0.05 | | | 0.05 | | Ω |
| $V_{IL}$ | Digital "0" Input Voltage | | | | 0.7 | | | 0.7 | V |
| $V_{IH}$ | Digital "1" Input Voltage | | 2.0 | | | 2.0 | | | |
| $I_{IL}$ | Digital "0" Input Current | $V_{IN} = 0.4V$ | | 1.5 | 4.0 | | 1.5 | 4.0 | μA |
| $I_{IH}$ | Digital "1" Input Current | $V_{IN} = 2.4V$ | | 0.01 | | | 0.01 | | |
| $V_S$ | Supply Voltage Range | | ±8.0 | | ±18 | ±8.0 | | ±18 | V |
| $I_S(+)$ | Positive Supply Current | $V_S = \pm 18V$ | | 8.5 | 15.5 | | 8.5 | 15.5 | mA |
| $I_S(-)$ | Negative Supply Current | | | −4.5 | −8.5 | | −4.5 | −8.5 | |

## AC Electrical Characteristics

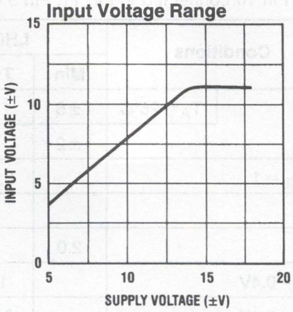
$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-Inverting)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| BW | Small Signal Bandwidth | −3 dB | $A_V = 1$ | | 3000 | | kHz |
| | | | $A_V = 50$ | | 60 | | |
| | | | $A_V = 200$ | | 15 | | |
| | | −1% | $A_V = 1$ | | 425 | | |
| | | | $A_V = 50$ | | 8.5 | | |
| | | | $A_V = 200$ | | 2 | | |
| PBW | Power Bandwidth | $V_O = \pm 10V$ | | | 159 | | kHz |
| SR | Slew Rate | | | | 10 | | V/μs |
| $t_S$ | Settling Time (*Figure 7*) 0.01% | $\Delta V_O = 20V$ | $A_V = 1$ | | 2.5 | | μs |
| | | | $A_V = 50$ | | 20 | | μs |
| | | | $A_V = 200$ | | 75 | | μs |
| $t_S$ | Settling Time After Gain Change | | | | 10 | | |
| $\bar{e}_N$ | Equivalent Input Noise Voltage (*Figure 6*) | $R_S = 100\Omega$<br>$A_V = 100$ | BW = 0.1-10 Hz | | 3 | | μVp-p |
| | | | f = 1 kHz | | 25 | | nV/$\sqrt{Hz}$ |
| $\bar{I}_N$ | Equivalent Input Noise Current | | | | 0.01 | | pA/$\sqrt{Hz}$ |

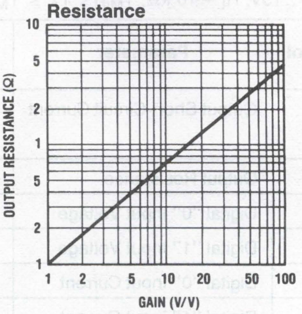
**Power Supply Rejection**



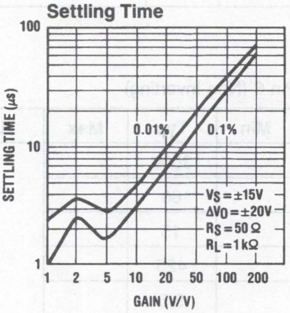
**Input Voltage Range**



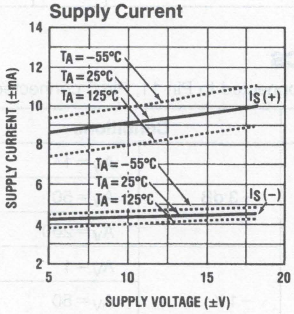
**Closed Loop Output Resistance**



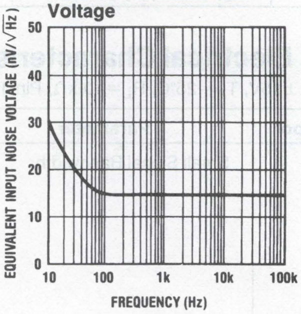
**Settling Time**



**Supply Current**

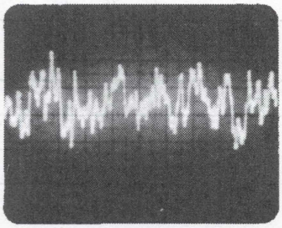


**Equivalent Input Noise Voltage**



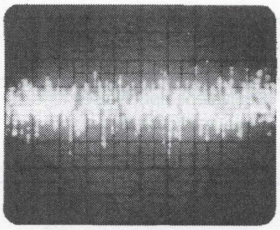
TL/K/5657-2

**Wideband Noise**



TL/K/5657-3

$R_S$ = 50Ω. Bandwidth = 0.1 Hz to 10 Hz
1 μV/division Vertical, 5 seconds/division Horizontal



TL/K/5657-4

$R_S$ = 50Ω. Bandwidth = 10 Hz to 10 kHz
5 μV/division Vertical, 1 ms/division Horizontal

## Applications Information

### Theory of Operation

The LH0086 is a digitally programmable gain amplifier with 3-bit digital gain control. It contains a FET-input operational amplifier, a precision resistor ladder, and a digitally programmable switch network.

The LH0086 was designed for use in a non-inverting configuration, thus the following discussion covers the LH0086 as used as a non-inverting amplifier. The gain of the LH0086 is given by the familiar gain equation of a non-inverting amplifier.

$$A_V = 1 + \frac{R_F}{R_S}$$

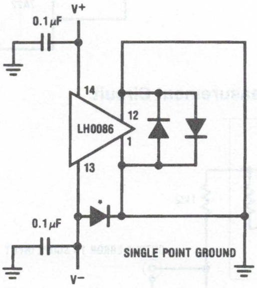
Each gain step is set by the ratio of the ladder resistors. The resistor ladder is constructed with high stability, low temperature-coefficient resistors precision laser-trimmed to the required values. FET switches are used to select the desired ratio. Since the FET switches are in series with the operational amplifier input, their "on resistance" and temperature drift do not degrade amplifier accuracy. The FET switches are selected by a 1 of 8 decoder, by applying the proper logic levels at digital inputs D0, D1, and D2. The gains are set as given in Table I.

**TABLE I. Gain-Control Codes**

| Gain | D2 | D1 | D0 |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 |
| 10 | 0 | 1 | 1 |
| 20 | 1 | 0 | 0 |
| 50 | 1 | 0 | 1 |
| 100 | 1 | 1 | 0 |
| 200 | 1 | 1 | 1 |

### Power Supply Connection

Proper power supply connections are shown in *Figure 1*. The power supplies should be bypassed to ground as close as possible to device supply pins. For most applications, the bypass capacitor should be 0.1 $\mu$F.



*GERMANIUM OR SCHOTTKY

**FIGURE 1. Power Supply and Ground Connections**

Care must be taken in the power-on sequence. The LH0086 may suffer irreversible damage if the V+ supply is applied prior to the powering on of the V− supply. In most applications using dual-tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V− pin as shown in *Figure 1*.

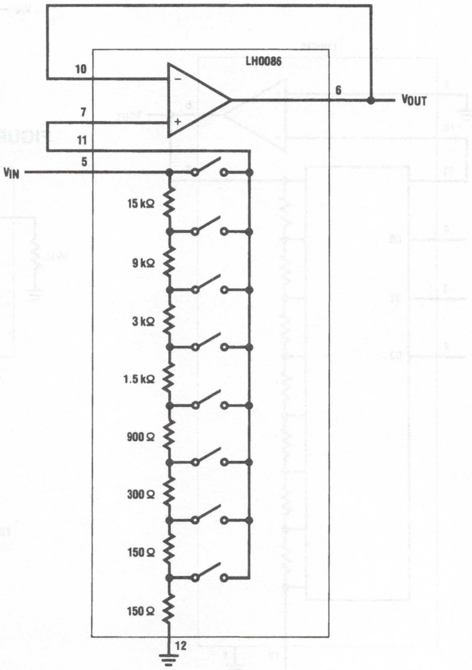
### Grounding Considerations

Care should be taken in the connection of digital and analog grounds. Digital switching currents can introduce noise on the analog ground pin. If possible, both grounds should go to a ground plane beneath the device, otherwise each ground should be run separately to a single point ground. The idea is to keep digital current from passing through the analog ground line. If long ground leads are used, diode clamps should be placed as close to the device as possible (*Figure 1*).

### Programmable Attenuator

The LH0086 may be used as a programmable attenuator when connected as in *Figure 2*. The accuracy of this attenuator will be typically 0.1%.

**Note:** Max. $V_{IN} = \pm 11$ Volts.



TL/K/5657–5

**FIGURE 2. Programmable Attenuator**

## Applications Information (Continued)

**TABLE II. Attenuator Codes**

| D2 | D1 | D0 | Attenuation |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 5 |
| 0 | 1 | 1 | 10 |
| 1 | 0 | 0 | 20 |
| 1 | 0 | 1 | 50 |
| 1 | 1 | 0 | 100 |
| 1 | 1 | 1 | 200 |

### Inverting Mode

The LH0086 may be used in the inverting mode, however, there are several design considerations.

1. Input resistance is low at high gains (see gain chart for input resistance at each gain).
2. Each gain step gets a one subtracted from the non-inverting gain. (See inverting gain chart for available gains.)
3. The first gain step (digital code of 000) cannot be used because the output will remain at virtual ground regardless of the input.

**TABLE III. Inverting Gain Chart**

| D2 | D1 | D0 | Gain | $R_{IN}$ (Ω) |
|---|---|---|---|---|
| 0 | 0 | 0 | $A_V = 0$ | 30k |
| 0 | 0 | 1 | $A_V = 1$ | 15k |
| 0 | 1 | 0 | $A_V = 4$ | 6k |
| 0 | 1 | 1 | $A_V = 9$ | 3k |
| 1 | 0 | 0 | $A_V = 19$ | 1.5k |
| 1 | 0 | 1 | $A_V = 49$ | 600 |
| 1 | 1 | 0 | $A_V = 99$ | 300 |
| 1 | 1 | 1 | $A_V = 199$ | 150 |

### Remote Output Sense

The $V_{OUT}$ sense pin of the LH0086 should be connected at the load in order to eliminate errors due to lead resistance. In any case the output sense and output force must be tied together at some point. See *Figure 4*.

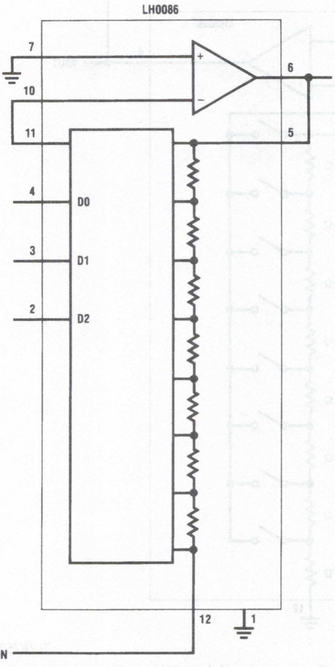

LH0086
7
10
11
6
VOUT
5
4
D0
3
D1
2
D2
12
1
VIN

FIGURE 3. LH0086 Inverting Gain Configuration

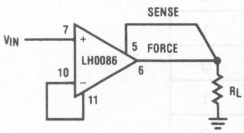

SENSE
VIN
7
5
FORCE
10
LH0086
6
11
RL

FIGURE 4. Remote Output Sense

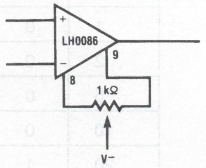

LH0086
9
8
1 kΩ
V−

FIGURE 5. Offset Adjustment

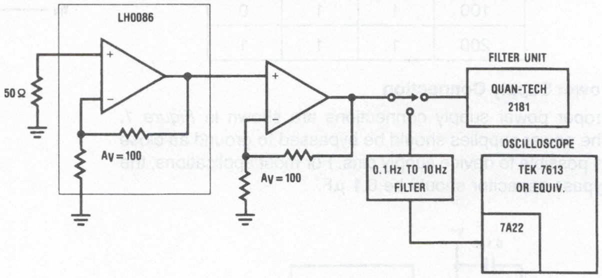
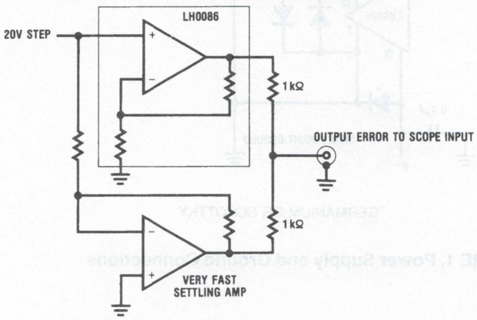

LH0086
50 Ω
Av = 100
Av = 100
FILTER UNIT
QUAN-TECH
2181
OSCILLOSCOPE
0.1 Hz TO 10 Hz
FILTER
TEK 7613
OR EQUIV.
7A22

FIGURE 6. Noise Measurement Circuit


20V STEP
LH0086
1 kΩ
OUTPUT ERROR TO SCOPE INPUT
1 kΩ
VERY FAST
SETTLING AMP

TL/K/5657-6

FIGURE 7. Settling Time Test Circuit

# Definition of Terms

| | |
|---|---|
| $V_{OS}$ | **Offset Voltage:** The voltage that must be applied to force the output to 0 volts. |
| $I_B$ | **Input Bias Current:** The current into Pin 7 with the device connected in the non-inverting configuration. |
| $R_{IN}$ | **Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded. |
| $V_{IN}$ | **Input Voltage Range:** The voltage range for which the device is operational. |
| PSRR | **Power Supply Rejection Ratio:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range. |
| $A_V$ | **Voltage Gain:** The ratio of output voltage change to the input voltage change producing it. |
| | **Gain Error:** The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain. |
| | **Gain Non-Linearity:** The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full scale (10V for operation with ±15V supplies). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain. |
| $V_O$ | **Output Voltage Swing:** The peak output voltage swing referenced to ground into specified load. |
| $I_{O(SC)}$ | **Output Short-Circuit Current:** The current supplied by the device with the output connected directly to ground. |
| $R_O$ | **Closed Loop Output Resistance:** The ratio of change in output voltage to change to output current at a specific gain. |
| $V_S$ | **Supply Voltage Range:** The supply voltage range for which the device is operational. |
| $I_S$ | **Supply Current:** The current required from the supply to operate the device with no load and with the analog as well as the digital inputs at 0V. |
| $P_D$ | **Power Dissipation:** The power dissipated in the device with no load and with the analog as well as the digital inputs at 0V. |
| $V_{IH}$ | **Digital "1" Input Voltage:** Minimum voltage required at the digital input to guarantee a high logic state. |
| $V_{IL}$ | **Digital "0" Input Voltage:** The current into a digital input at specified logic level. |
| $\Delta V_{OS}/\Delta T$ | **Average Input Offset Voltage Drift:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range. |
| $\Delta A_V/\Delta T$ | **Average Gain Temperature Coefficient:** The ratio in gain from 25°C to either temperature extreme divided by the temperature range. |
| BW | **Bandwidth:** The frequency at which the voltage gain is reduced to 3 dB below the low frequency value. |
| PBW | **Power Bandwidth:** Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion. |
| SR | **Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input. |
| $t_S$ | **Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage. |
| | **Gain Switching Time:** The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value. |
| $e_N$ | **Equivalent Input Noise Voltage:** The rms or peak noise voltage referred to the input (RTI) over a specified frequency band. |
| $i_N$ | **Equivalent Input Noise Current:** The rms or peak noise current referred to the input (RTI) over a specified frequency band. |

**National Semiconductor Corporation**

# LH0101/LH0101C, LH0101A/LH0101AC Power Operational Amplifier

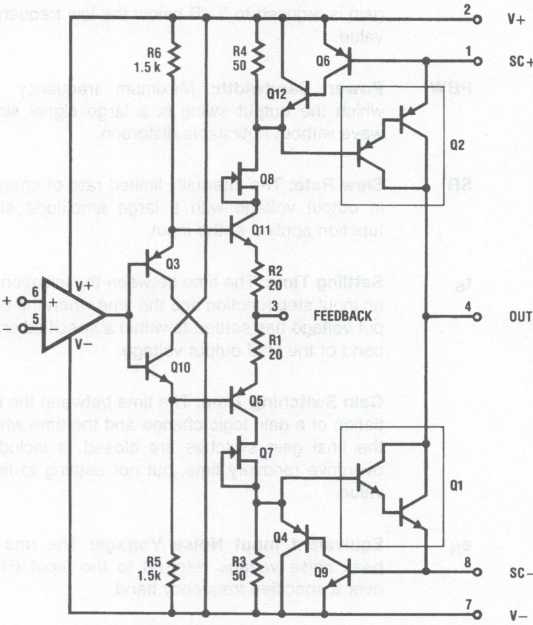
## General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 60 watts with a suitable heat sink.

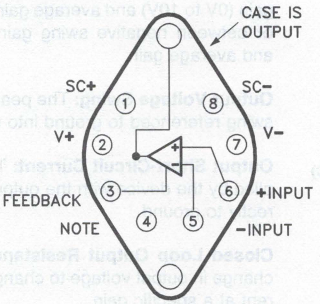
## Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μs slew rate
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth

## Schematic and Connection Diagrams


2
V+
1
SC+
R6
1.5k
R4
50
Q6
Q12
Q2
Q8
Q11
Q3
R2
20
6
+
+
V+
5
−
3
FEEDBACK
4
OUTPUT (CASE)
V−
R1
20
Q10
Q5
Q7
Q1
Q4
R5
1.5k
R3
50
Q9
8
SC−
7
V−

TL/K/5558-1


CASE IS OUTPUT
SC+
SC−
1
8
V+
V−
2
7
+
−
FEEDBACK
3
6
+INPUT
NOTE
4
5
−INPUT

TL/K/5558-2

**Top View**

**Order Numbers LH0101K, LH0101CK, LH0101AK or LH0101ACK**
**See NS Package Number K08A**

**Note:** Electrically connected internally, no connection should be made to pin.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±22V |
| Power Dissipation at $T_A = 25°C$, $P_D$ | 5W |
| Derate linearly at 25°C/W to zero at 150°C, | |
| Power Dissipation at $T_C = 25°C$ | 62W |
| Derate linearly at 2°C/W to zero at 150°C | |
| Differential Input Voltage, $V_{IN}$ | $\pm 40V$ but $< \pm V_S$ |
| Input Voltage Range, $V_{CM}$ | $\pm 20V$ but $< \pm V_S$ |
| Thermal Resistance— See Typical Performance Characteristics | |
| Peak Output Current (50 ms pulse), $I_{O(PK)}$ | 5A |
| Output Short Circuit Duration (within rated power dissipation, $R_{SC} = 0.35\Omega$, $T_A = 25°C$) | Continuous |
| Operating Temperature Range, $T_A$ | |
| LH0101AC, LH0101C | −25°C to +85°C |
| LH0101A, LH0101 | −55°C to +125°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temperature (Soldering <10 sec.) | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | | LH0101AC<br>LH0101A | | | LH0101C<br>LH0101 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | | | | 1 | 3 | | 5 | 10 | mV |
| | | $T_{MIN} \le T_A \le T_{MAX}$ | | | | 7 | | | 15 | |
| $\Delta V_{OS}/\Delta P_D$ | Change in Input Offset Voltage with Dissipated Power | (Note 2) | | | 150 | | | 300 | | μV/W |
| $\Delta V_{OS}/\Delta T$ | Change in Input Offset Voltage with Temperature | $V_{CM} = 0$ | | | 10 | | | 10 | | μV/°C |
| $I_B$ | Input Bias Current | | | | | 300 | | | 1000 | pA |
| | | $T_A \le T_{MAX}$ | LH0101C/AC | | | 60 | | | 60 | nA |
| | | | LH0101/A | | | 300 | | | 1000 | |
| $I_{OS}$ | Input Offset Current | | | | | 75 | | | 250 | pA |
| | | $T_A \le T_{MAX}$ | LH0101C/AC | | | 15 | | | 15 | nA |
| | | | LH0101/A | | | 75 | | | 250 | |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_O = \pm 10V$ $R_L = 10\Omega$ | | 50 | 200 | | 50 | 200 | | V/mV |
| $V_O$ | Output Voltage Swing | $R_{SC} = 0$ | $R_L = 100\Omega$ | ±12 | ±12.5 | | ±12 | ±12.5 | | V |
| | | $A_V = +1$ | $R_L = 10\Omega$ | ±11.25 | ±11.6 | | ±11.25 | ±11.6 | | |
| | | Note 3 | $R_L = 5\Omega$ | ±10.5 | ±11 | | ±10.5 | ±11 | | |
| CMRR | Common Mode Rejection Ratio | $\Delta V_{IN} = \pm 10V$ | | 85 | 100 | | 85 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $\Delta V_S = \pm 5V$ to $\pm 15V$ | | 85 | 100 | | 85 | 100 | | |
| $I_S$ | Quiescent Supply Current | | | | 28 | 35 | | 28 | 35 | mA |

## AC Electrical Characteristics (Note 1), $V_S = \pm 15V$, $T_A = 25°C$

| Symbol | Parameter | Conditions | | LH0101<br>LH0101A Min | Typ | Max | LH0101C<br>LH0101AC Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $e_n$ | Equivalent Input Noise Voltage | f = 1 kHz | | | 25 | | | 25 | | $nV/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | f = 1 MHz | | | 3.0 | | | 3.0 | | pF |
| | Power Bandwidth, −3 dB | | | | 300 | | | 300 | | kHz |
| SR | Slew Rate | $R_L = 10\Omega$ | $A_V = +1$ | 7.5<br>(Note 4) | 10 | | | 10 | | V/μs |
| $t_r$, $t_f$ | Small Signal Rise or Fall Time | | | | 200 | | | 200 | | ns |
| | Small Signal Overshoot | | | | 10 | | | 10 | | % |
| GBW | Gain-Bandwidth Product | $R_L = \infty$ | | 4.0<br>(Note 4) | 5.0 | | | 5.0 | | MHz |
| $t_s$ | Large Signal Settling Time to 0.01% | | | | 2.0 | | | 2.0 | | μs |
| THD | Total Harmonic Distortion | $P_O = 10W$, f = 1 kHz<br>$R_L = 10\Omega$ | | | 0.008 | | | 0.008 | | % |

**Note 1:** Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, $V_{OS}$ may change 0.5 mV and $I_B$ and $I_{OS}$ will change significantly during warm-ups. Refer to the $I_B$ vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

**Note 2:** Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

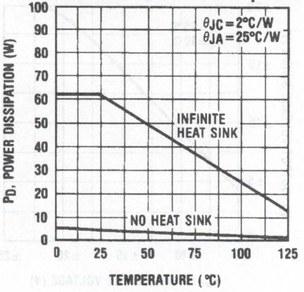
**Note 3:** At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

**Note 4:** These parameters are sample tested to 10% LTPD.

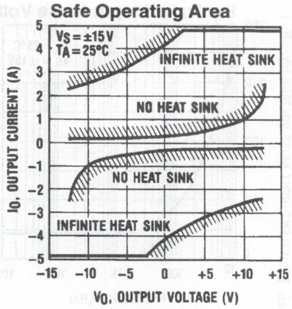
**Note 5:** Refer to RETS0101AK for the LH0101AK military specifications and RETS0101K for the LH0101K military specifications.

## Typical Performance Characteristics

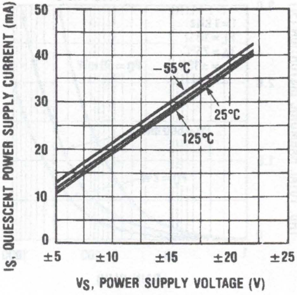
### Maximum Power Dissipation



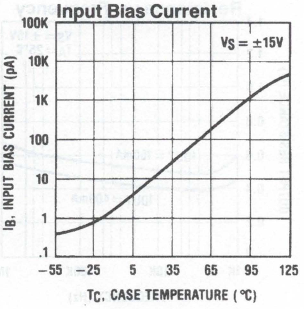
### Safe Operating Area



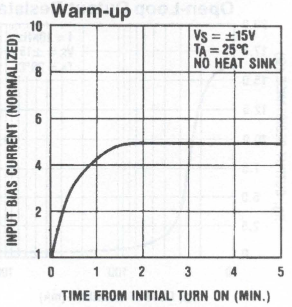
### Quiescent Power Supply Current



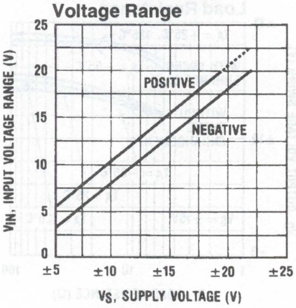
### Input Bias Current



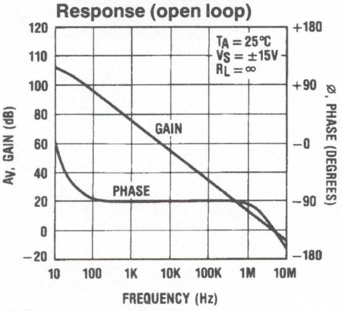
### Input Bias Current after Warm-up



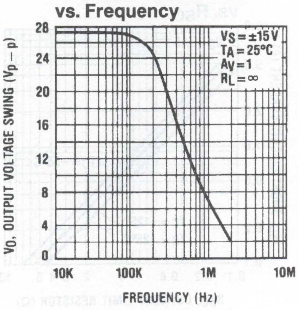
### Input Common-Mode Voltage Range



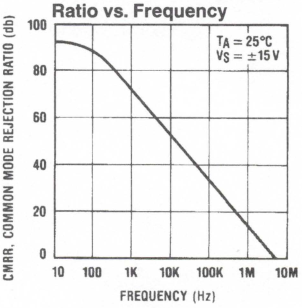
### Small Signal Frequency Response (open loop)



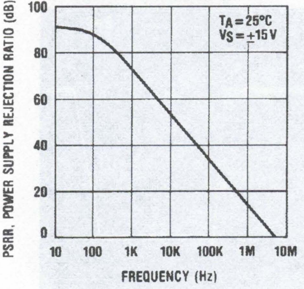
### Output Voltage Swing vs. Frequency



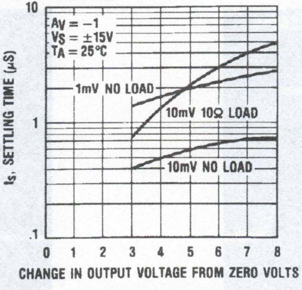
### Common-Mode Rejection Ratio vs. Frequency



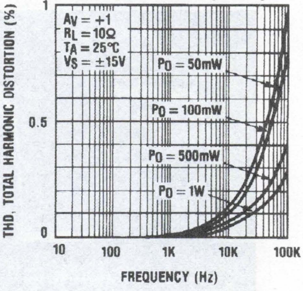
### Power Supply Rejection Ratio vs. Frequency



### Settling Time



### Total Harmonic Distortion vs. Frequency



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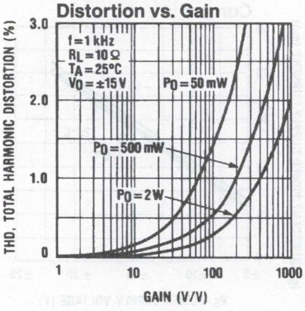
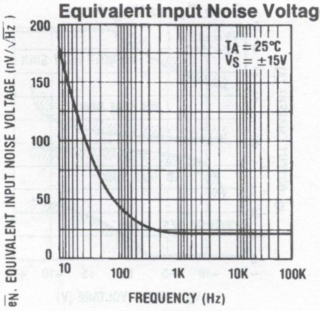
## Typical Performance Characteristics (Continued)

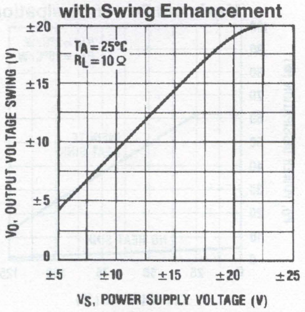
**Total Harmonic Distortion vs. Gain**



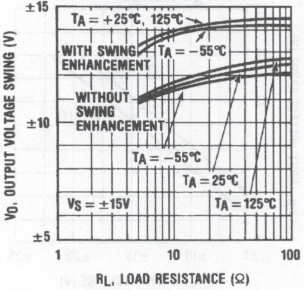
**Equivalent Input Noise Voltage**



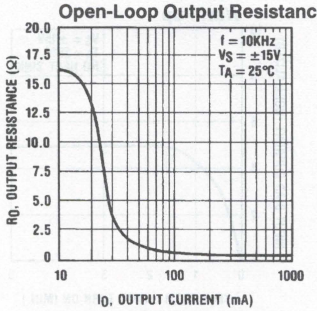
**Output Voltage Swing with Swing Enhancement**



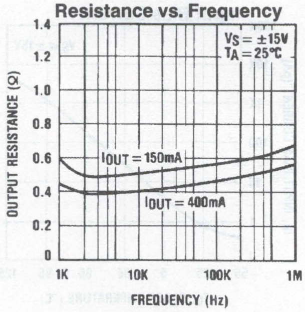
**Output Voltage Swing vs. Load Resistance**



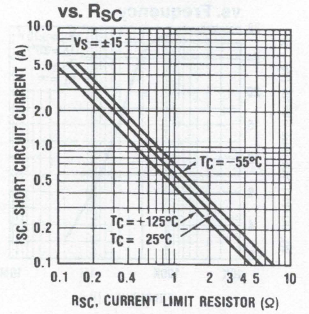
**Open-Loop Output Resistance**



**Open-Loop Output Resistance vs. Frequency**



**Short Circuit Current vs. $R_{SC}$**



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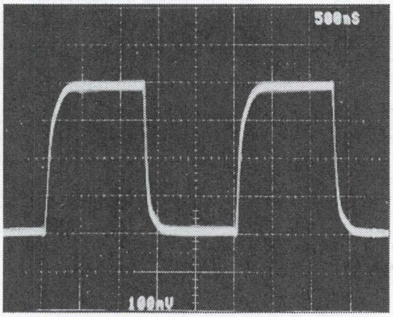
**Small Signal Pulse Response (No Load)**



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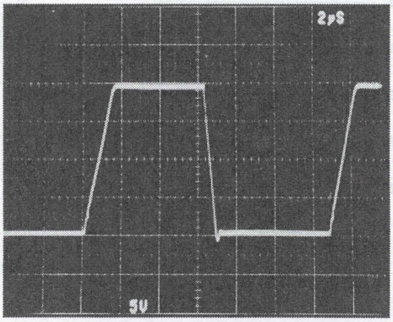
**Large Signal Pulse Response ($R_L$ = 10Ω)**



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## Application Hints

### Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

### Layout Considerations

When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.

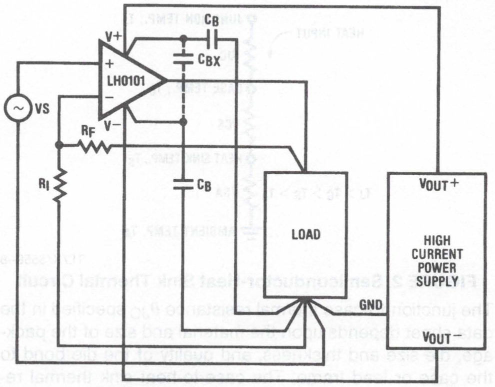

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**FIGURE 1. Single-Point Grounding**

Bypass capacitor $C_{BX}$ should be used if the lead lengths of bypass capacitors $C_B$ are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

### Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately .3%.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

## Application Hints (Continued)

### Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} \,°C/W$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures $T_J$, $T_C$ and $T_S$ (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.

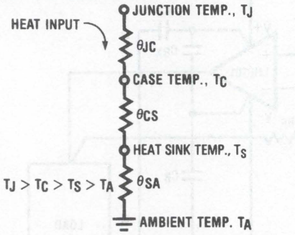

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**FIGURE 2. Semiconductor-Heat Sink Thermal Circuit**

The junction-to-case thermal resistance $\theta_{JC}$ specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance $\theta_{CS}$ depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical $\theta_{CS}$ for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance $\theta_{SA}$ depends on the quality of the heat sink and the ambient conditions.

Cooling is normally required to maintain the worst case operating junction temperature $T_J$ of the device below the specified maximum value $T_{J(MAX)}$. $T_J$ can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \,°C/W$$

$$T_J = T_A + P_D \theta_{JA} \,°C$$

Where: $P_D$ $(V_S - V_{OUT})I_{OUT} + |V+ - (V-)|I_Q$ for a DC Signal

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and $V_S$ = Supply Voltage

$\theta_{JC}$ for the LH0101 is about 2°C/W.

### Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Some inductive loads may cause output stage oscillation. A .01 µF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.

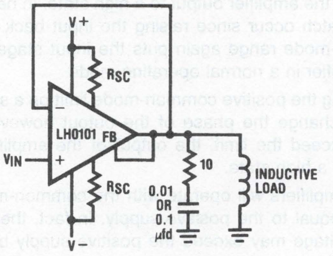

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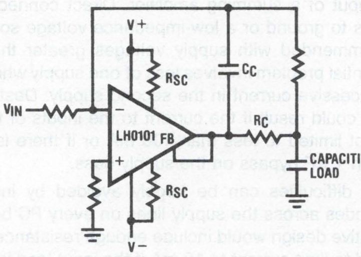
**FIGURE 3. Driving Inductive Loads**

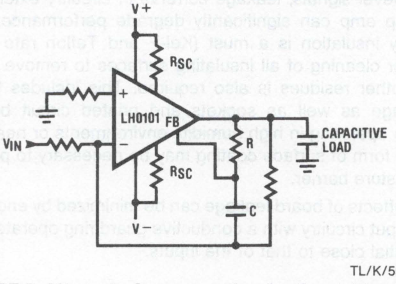
Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):



TL/K/5558–10

**FIGURE 4. $R_C$ and $C_C$ Selected to Compensate for Capacitive Load**

A similar but alternative technique may be used for the LH0101:



TL/K/5558–11

**FIGURE 5. Alternate Compensation for Capacitive Load**

## Application Hints (Continued)

### Output Swing Enhancement

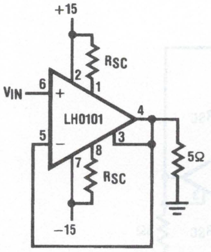
When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

### Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under on Ω for load currents exceeding 100 mA.

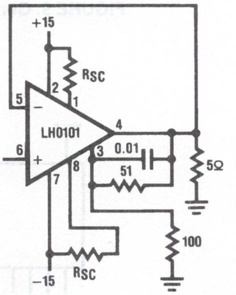
## Typical Applications

See AN261 for more information.



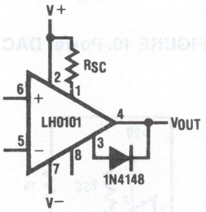
TL/K/5558-12

**FIGURE 6. High Power Voltage Follower**



TL/K/5558-13

**FIGURE 7. High Power Voltage Follower with Swing Enhancement**



TL/K/5558-14

**FIGURE 8. Restricting Outputs to Positive Voltages Only**

Following is a partial list of sockets and heat dissipators for use with the LH0101. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

**SOCKETS**

- Keystone 4626 or 4627
- Robinson Nugent 0002011
- Azimuth 6028 (test socket)

**HEAT SINKS**

Thermalloy 2266B (35°C/W)
- IERC LAIC3B4CB
- IERC HP1-TO3-33CB (7°C/W)
- AAVID 5791B

**MICA WASHERS**

- Keystone 4658

AAVID Engineering
30 Cook Court
Laconla, New Hampshire 03246

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92572

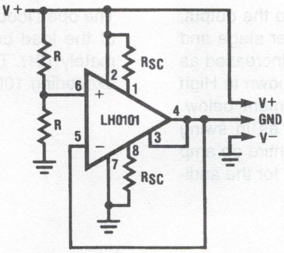
IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150

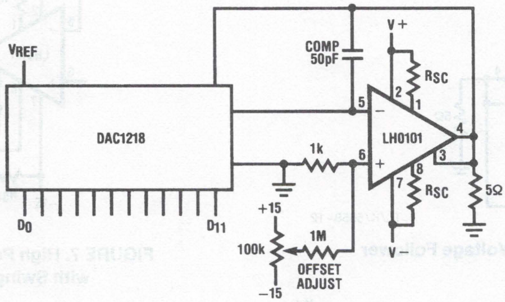
Thermalloy
P.O. Box 34829
Dallas, TX 75234

## Typical Applications (Continued)


V+
R
RSC
6
+
2
1
R
LH0101
4
V+
GND
V−
5
−
3
8
7
RSC

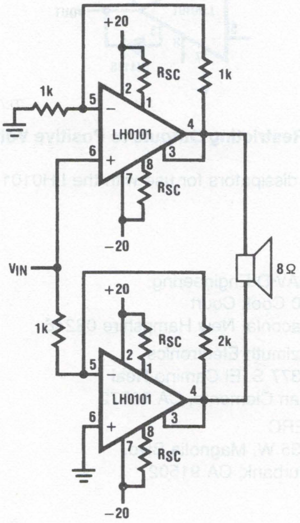
TL/K/5558-15

FIGURE 9. Generating a Split Supply from a Single Voltage Supply


VREF
DAC1218
D0
D11
COMP
50pF
V+
RSC
5
−
2
1
LH0101
4
1k
6
+
3
8
7
RSC
5Ω
+15
1M
100k
OFFSET
ADJUST
−15

TL/K/5558-16

FIGURE 10. Power DAC


+20
RSC
1k
1k
5
−
2
1
LH0101
4
6
+
3
8
7
RSC
−20
VIN
8Ω
+20
1k
RSC
2k
5
−
2
1
LH0101
4
6
+
3
8
7
RSC
−20

TL/K/5558-17

FIGURE 11. Bridge Audio Amplifier

## Typical Applications (Continued)

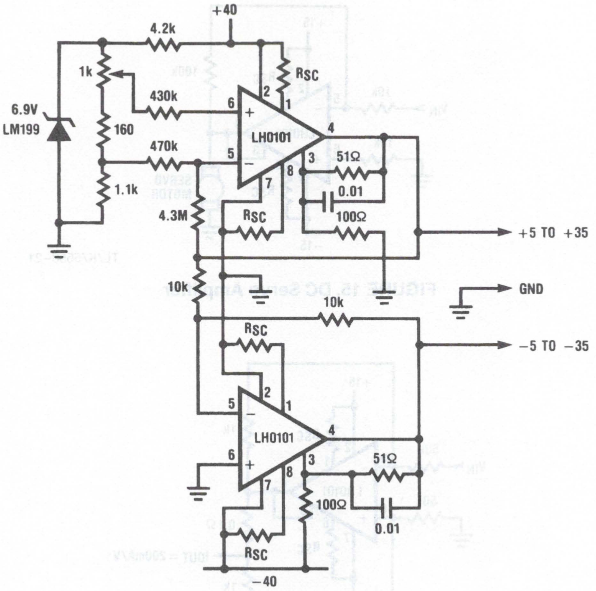

+40
4.2k
1k
6.9V
LM199
160
1.1k
430k
470k
RSC
LH0101
6
+
5
−
2
1
4
3
8
7
51Ω
0.01
100Ω
4.3M
RSC
10k
10k
RSC
+5 TO +35
GND
−5 TO −35
LH0101
51Ω
100Ω
0.01
RSC
−40
TL/K/5558–18

FIGURE 12. ±5 to ±35 Power Source or Sink

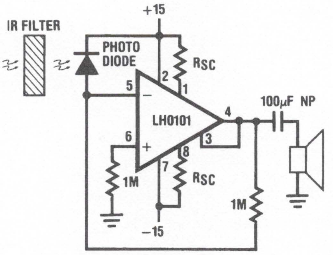

+15
IR FILTER
PHOTO DIODE
RSC
LH0101
100μF NP
1M
RSC
1M
−15
TL/K/5558–19

FIGURE 13. Remote Loudspeaker via Infrared Link

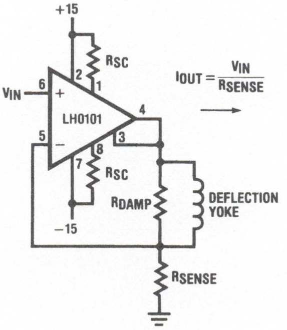
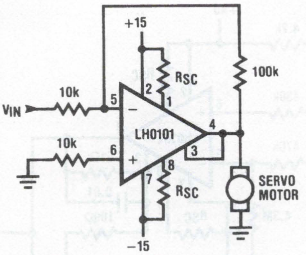

+15
RSC
VIN
LH0101
$I_{OUT} = \frac{V_{IN}}{R_{SENSE}}$
RSC
RDAMP
DEFLECTION YOKE
−15
RSENSE
TL/K/5558–20

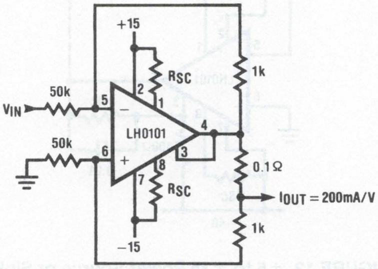
FIGURE 14. CRT Deflection Yoke Driver

## Typical Applications (Continued)


+15
RSC
100k
2
1
10k
VIN
5
−
LH0101
4
10k
6
+
3
8
7
RSC
SERVO MOTOR
−15

TL/K/5558-21

FIGURE 15. DC Servo Amplifier


+15
RSC
1k
50k
VIN
5
2
1
−
LH0101
4
50k
6
+
3
8
0.1Ω
7
RSC
IOUT = 200mA/V
1k
−15

TL/K/5558-22

FIGURE 16. High Current Source/Sink

**National Semiconductor Corporation**

# LH4101/LH4101C Wideband High Current Operational Amplifier

## General Description

The LH4101 is a high slew rate, FET input, wideband operational amplifier designed for applications that require an op amp to provide up to 200 mA peak and 100 mA continuous output current. This feature eliminates the need for a buffer to provide the additional current drive not available with most wideband op amps.

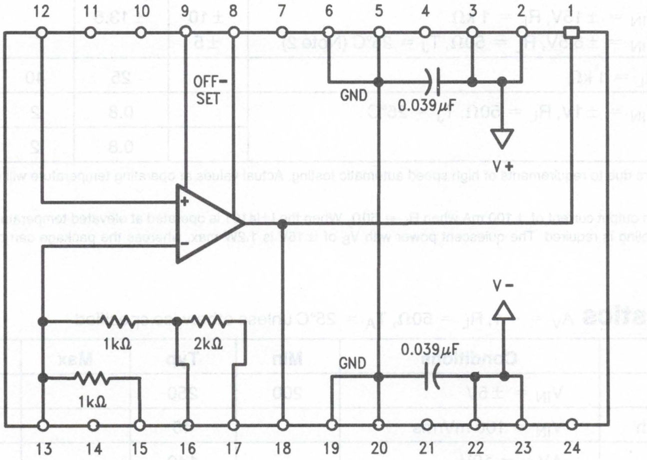
Designed for use with minimum external circuitry, the LH4101 provides internal compensation for unity gain stability and all the gain set resistors for most popular gain settings, as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions. These features are provided in a 24 pin hermetic dual in-line package.

## Features

- 45 MHz bandwidth
- $10^{12}\Omega$ input impedance
- Pin strappable gain settings of 1, 2, 3, 4, −1, −2, −3
- Unity gain stable
- Internal supply bypassing
- 100 mA continuous output current
- 24 pin hermetic DIP
- Directly drives 50Ω loads

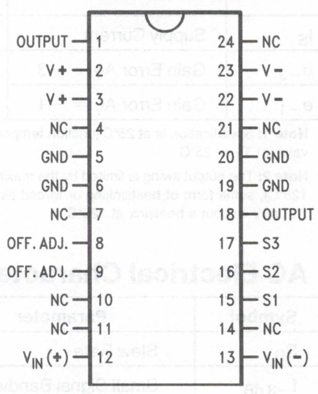
The LH4101's wide bandwidth, programmable gain settings, and high output current make it an ideal choice for fast buffering applications such as video distribution. It is also appropriate for use in summing amplifiers, sample and hold circuits, and high speed integrators.

## Block and Connection Diagrams


12
11
10
9
8
7
6
5
4
3
2
1
OFF-SET
GND
0.039µF
V+
+
V−
1kΩ
2kΩ
1kΩ
0.039µF
GND
13
14
15
16
17
18
19
20
21
22
23
24

TL/K/8543-1

**Dual In-Line Package**


OUTPUT 1
V+ 2
V+ 3
NC 4
GND 5
GND 6
NC 7
OFF. ADJ. 8
OFF. ADJ. 9
NC 10
NC 11
V_IN (+) 12
24 NC
23 V−
22 V−
21 NC
20 GND
19 GND
18 OUTPUT
17 S3
16 S2
15 S1
14 NC
13 V_IN (−)

TL/K/8543-2

**Order Number LH4101D or LH4101CD**
**See NS Package Number D24D**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±17V |
| Power Dissipation, at $T_A = 25°C$, $P_D$ | 2W |
| Input Voltage Range, $V_{CM}$ | $\pm V_S$ |
| Steady State Output Current, $I_O$ | ±100 mA |
| Operating Temperature Range, $T_A$ | |
| LH4101CD | −25°C to +85°C |
| LH4101D | −55°C to +125°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_J$ | 175°C |
| Lead Temperature (Soldering <10 sec.) | 300°C |
| ESD rating to be determined | |

## DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{IN} = 0V$ | $T_A = T_J = 25°C$ (Note 1) | | | 15<br>25 | mV<br>mV |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Average Offset Voltage Drift | | | | 25 | | μV/°C |
| $I_B$ | Input Bias Current | | $T_A = T_J = 25°C$ (Note 1)<br>$T_A = T_J = T_{max}$ | | | 500<br>500 | pA<br>nA |
| $I_{OS}$ | Input Offset Current | | $T_A = T_J = 25°C$ (Note 1)<br>$T_A = T_J = T_{max}$ | | | 200<br>200 | pA<br>nA |
| CMRR | Common Mode Rejection Ratio | $\Delta V_{IN} = \pm 10V$ | | 50 | 60 | | dB |
| PSRR | Power Supply Rejection Ratio | $\Delta V_S = \pm 10V$ | | 50 | 60 | | dB |
| $A_{VOL}$ | Open-Loop Voltage Gain | $V_O = \pm 10V$, $R_L = 1\ k\Omega$, $f = 1\ kHz$<br>$V_O = \pm 5V$, $R_L = 50\Omega$, $f = 1\ kHz$, $T_A = 25°C$ | | 60<br>57 | 65<br>62 | | dB<br>dB |
| $V_O$ | Output Voltage Swing | $V_{IN} = \pm 15V$, $R_L = 1\ k\Omega$<br>$V_{IN} = \pm 5.5V$, $R_L = 50\Omega$, $T_J = 25°C$ (Note 2) | | ±10<br>±5 | ±13.5 | | V<br>V |
| $I_S$ | Supply Current | $R_L = 1\ k\Omega$ | | | 25 | 40 | mA |
| $e_{-3}$ | Gain Error $A_V = -3$ | $V_{IN} = \pm 1V$, $R_L = 50\Omega$, $T_J = 25°C$ | | | 0.8 | 2 | % |
| $e_{-1}$ | Gain Error $A_V = -1$ | | | | 0.8 | 2 | % |

**Note 1:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$.

**Note 2:** The output swing is limited by the maximum output current of ±100 mA when $R_L = 50\Omega$. When the LH4101 is operated at elevated temperature (such as 125°C), some form of heatsinking or forced air cooling is required. The quiescent power with $V_S$ of ±15V is 1.2W max, whereas the package can only handle 750 mW without a heatsink at 125°C.

## AC Electrical Characteristics $A_V = +1$, $R_L = 50\Omega$, $T_A = 25°C$ unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $S_R$ | Slew Rate | $V_{IN} = \pm 5V$ | 200 | 250 | | V/μs |
| $f_{-3\ dB}$ | Small Signal Bandwidth | $V_{IN} = 100\ mVrms$ | | 45 | | MHz |
| $t_S$ | Settling Time to 1%<br>Settling Time to 0.1% | $\Delta V_{IN} = 10V$ | | 140<br>300 | | ns<br>ns |
| $t_r$ | Small Signal Rise Time | $V_{IN} = 0V$ to $+100\ mV$ | | 10 | | ns |

## Applications Information

### Power Supply Bypassing

The LH4101 will perform well in most circuit boards even without external supply bypassing; however, it is recommended that some bulk bypassing be provided. One 10 μF electrolytic on each supply is recommended. Proximity to the device pins is not critical, but the bypass will be most effective if located within an inch of the part.

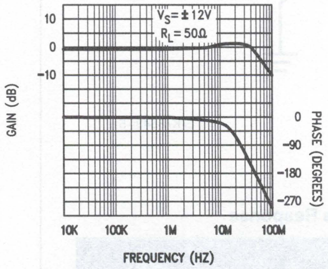
### Input Capacitance

The input capacitance to the LH4101 is typically 5 pF and for source impedances greater than 100Ω, the input time constant should be considered.

### Gain Settings

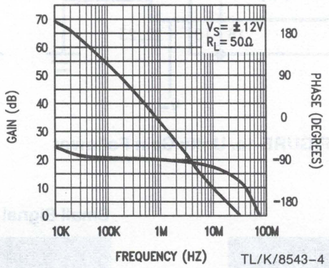
The LH4101 provides internal gain set resistors for most popular gain settings. A chart is provided to assist in determining the proper pins to connect to achieve these gains. The internal gain resistors are trimmed and matched to insure the gain accuracy to 0.8% typically. The LH4101 can operate at other gain settings, but the user must supply additional gain set resistors external to the part.

**Frequency Response ($A_V = +1$ Closed Loop)**



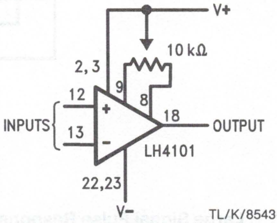
TL/K/8543-3

**Frequency Response (Open Loop)**



TL/K/8543-4

**Offset Null**



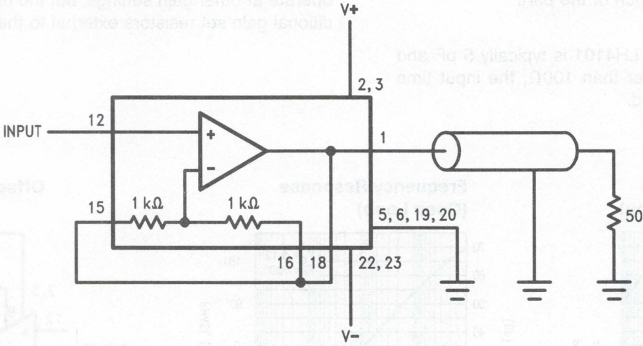
TL/K/8543-7

| Gain | Connect | Pin Number | Comment |
|---|---|---|---|
| +1 | $V_{out}$ to S1<br>$V_{out}$ to S2 | 18 to 15<br>18 to 16 | For all positive gains, the input is $V_{in(+)}$, pin 12. |
| +2 | $V_{out}$ to S2<br>and<br>S1 to GND | 18 to 16<br><br>15 to 19 | |
| +3 | $V_{out}$ to S3<br>and<br>S2 to $V_{in(-)}$<br>and<br>S1 to GND | 18 to 17<br><br>16 to 13<br><br>15 to 19 | |
| +4 | $V_{out}$ to S3<br>and<br>S1 to GND | 18 to 17<br><br>15 to 19 | |
| −1 | S2 to $V_{out}$ | 16 to 18 | For all negative gains, input is S1, pin 15. Also, $V_{in(+)}$, pin 12, MUST BE CONNECTED TO GROUND. |
| −2 | $V_{in(-)}$ to S2<br>and<br>S3 to $V_{out}$ | 13 to 16<br><br>17 to 18 | |
| −3 | S3 to $V_{out}$ | 17 to 18 | |

# Typical Applications

## Unity Gain Follower

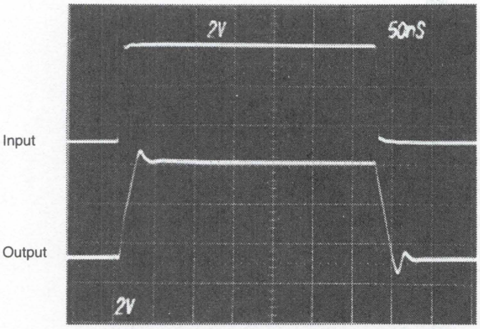
The LH4101 can be used as a unity gain follower to provide output current to drive 50Ω or 75Ω coax cable directly. By shorting pins 15, 16 and 18, a follower circuit is configured as seen in *Figure 1a*. This configuration features a bandwidth greater than 40 MHz with an input signal of 1.0 $V_{p-p}$ and greater than 16 MHz with a 5 $V_{p-p}$ input signal. This is all achieved without any external components. *Figures 1b* and *1c* show the small and large signal pulse responses, respectively.



TL/K/8543-5

FIGURE 1a. Unity Gain Follower

Large Signal Pulse Response

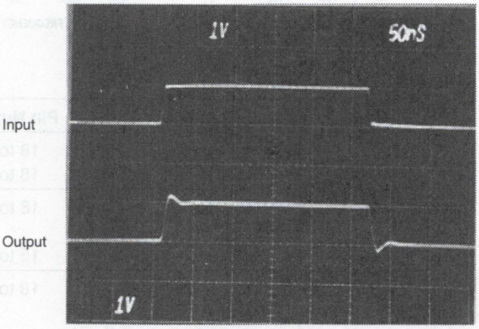


$V_S$ = ±15V
$A_V$ = 1
$R_L$ = 50Ω

TL/K/8543-9

FIGURE 1b

Small Signal Pulse Response

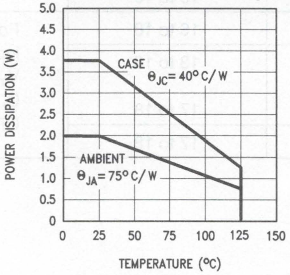


$V_S$ = ±15V
$A_V$ = 1
$R_L$ = 50Ω

TL/K/8543-10

FIGURE 1c

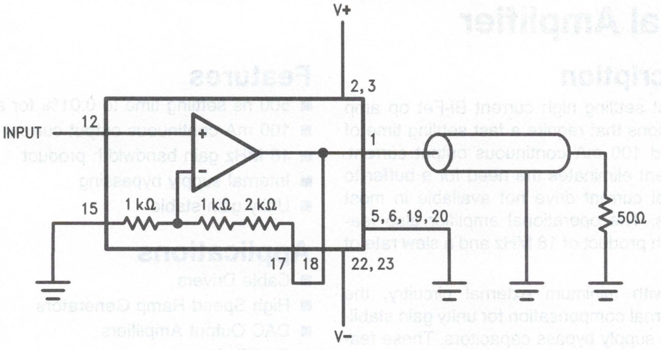
Maximum Power Dissipation



TL/K/8543-13

### Non-Inverting Amplifier

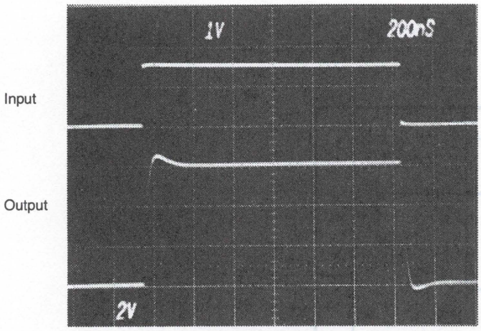
To configure the LH4101 as a non-inverting amplifier with a gain of 4, short pins 17 to 18 and 15 to 19, as shown in *Figure 2a*. Again, no external components are necessary. This configuration provides a bandwidth of 25 MHz with an input sine wave of 1.0 $V_{p\text{-}p}$ and a bandwidth of 10 MHz with an input of 5 $V_{p\text{-}p}$ while providing 100 mA of output current. This eliminates the need of an additional buffer in the circuit to provide the output current to drive large loads. *Figures 2b* and *2c* show the small and large signal pulse responses, respectively.



TL/K/8543-8

**FIGURE 2a. Non-Inverter with Gain of +4**

**Large Signal Pulse Response**

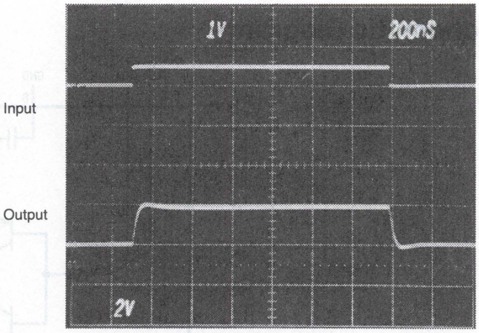


$V_S = \pm 15V$
$A_V = 4$
$R_L = 50\Omega$

TL/K/8543-11

**FIGURE 2b**

**Small Signal Pulse Response**



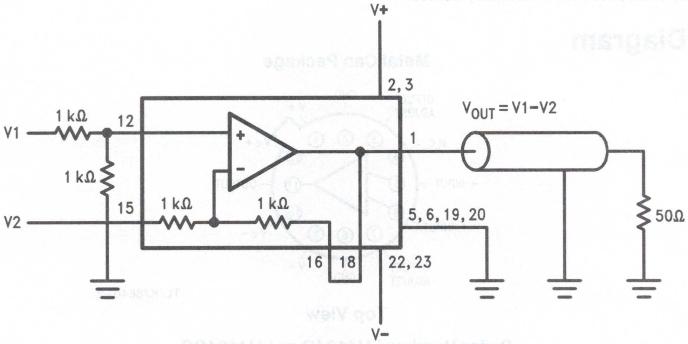
$V_S = \pm 15V$
$A_V = 4$
$R_L = 50\Omega$

TL/K/8543-12

**FIGURE 2c**

### Differential Amplifier

To configure the LH4101 as a differential amplifier, two additional 1 kΩ resistors are required. *Figure 3* shows this configuration, where $V_0 = V_1 - V_2$. The gain accuracy of this circuit is dependent upon the gain accuracy of the additional 1 kΩ resistors.



TL/K/8543-6

**FIGURE 3. Wideband Differential Amplifier**

**National Semiconductor Corporation**

**PRELIMINARY**

# LH4104/LH4104C Fast Settling High Current Operational Amplifier

## General Description

The LH4104 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4104 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

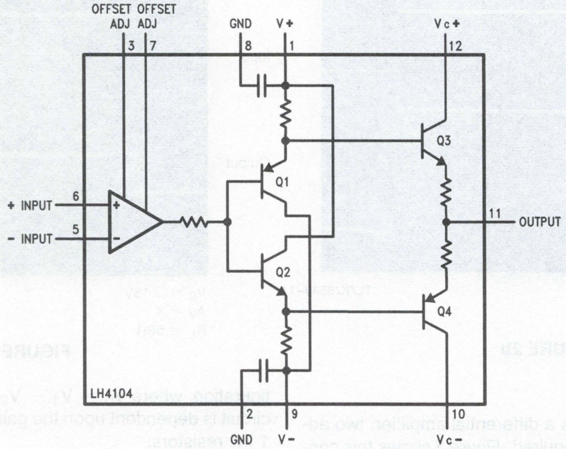
## Features

- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- 18 MHz gain bandwidth product
- Internal supply bypassing
- Unity gain stable

## Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

## Schematic Diagram

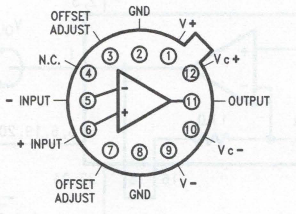

OFFSET ADJ
OFFSET ADJ
3
7
GND
8
V+
1
Vc+
12
Q3
Q1
+ INPUT
6
− INPUT
5
11
OUTPUT
Q2
Q4
LH4104
2
GND
9
V−
10
Vc−

TL/K/8840–1

Pins #2 & #8 are internally connected. Case is electrically isolated.

## Connection Diagram

**Metal Can Package**


OFFSET ADJUST
GND
V+
N.C.
Vc+
− INPUT
OUTPUT
+ INPUT
Vc−
OFFSET ADJUST
GND
V−
1
2
3
4
5
6
7
8
9
10
11
12

TL/K/8840–2

**Top View**

**Order Number LH4104G or LH4104CG**
**See NS Package Number H12B**

**Note:** 2 and 8 are internally connected. Case is electrically isolated.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±18V |
| Steady State Output Current, $I_o$ | 100 mA |
| Power Dissipation at, $P_D$ | |
| $T_A = 25°C$, derate linearly at 100°C/W | 2.5W |
| $T_C = 25°C$, derate linearly at 50°C/W | 1.5W |
| Differential Input Voltage, $V_{IN}$ | $\pm 30V$ but $\leq \pm 2V_s$ |
| Input Voltage Range, $V_{CM}$ | $\pm 18V$ but $\leq \pm V_s$ |
| Operating Temperature Range, $T_A$ | |
| LH4104 | −55°C to +125°C |
| LH4104C | −25°C to +85°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_j$ | 150°C |
| Lead Temperature (Soldering < 10 sec.) | 300°C |

ESD rating is to be determined.

## DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Note 1)

| Symbol | Parameter | Conditions | LH4104C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$ | 2 | 5 | **10** | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | $R_S = 50\Omega$ | 20 | | | μV/°C |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Note 4) $V_{CM} = 0V$ | 200 | 600 | | pA |
| | | | | | **250** | nA |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, $V_{CM} = 0V$ | 20 | 400 | | pA |
| | | | | | **200** | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | $10^{11}$ | | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L = 100\Omega$ | 106 | 87 | | dB (Min) |
| | | $R_L = 1\ k\Omega$ | 106 | 87 | **80** | |
| $V_O$ | Output Voltage Swing | $R_L = 100\Omega$ (Note 5) | | ±10 | | V (Min) |
| | | $R_L = 1\ k\Omega$ | ±13 | ±10 | **±10** | |
| $V_{CM}$ | Input Common Mode Range | | ±12 | ±11 | **±10** | V (Min) |
| CMRR | Common Mode Rejection Ratio | $V_{IN} = -11V$ to $+11V$ | 100 | 80 | **70** | dB (Min) |
| PSRR | Power Supply Rejection Ratio | $V_{CC} = \pm 10V$ to $\pm 15V$ | 100 | 80 | **70** | dB (Min) |
| $I_S$ | Supply Current | | 20 | 25 | | mA |

## AC Electrical Characteristics $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | LH4104C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $t_S$ | Settling Time to 0.01% | $A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$ | 500 | 800 | | ns |
| $S_R$ | Slew Rate | $V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$ | 40 | | 32 | V/μs(min) |
| GBW | Gain Bandwidth Product | | 18 | | | MHz |
| $t_r$ | Small Signal Rise Time | $A_V = 1$, $R_L = 100\Omega$ | 10 | | 20 | ns |

## DC Electrical Characteristics $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Notes 1 and 6)

| Symbol | Parameter | Conditions | LH4104<br>Typ | LH4104<br>Tested Limit (Note 2) | LH4104<br>Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$ | 2 | **10** | | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | $R_S = 50\Omega$ | 20 | | | $\mu V/°C$ |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Note 4) $V_{CM} = 0V$ | 200 | 600 | | pA |
| | | | | **350** | | nA |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, $V_{CM} = 0V$ | 20 | 400 | | pA |
| | | | | **250** | | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | $10^{11}$ | | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L = 100\Omega$ | 106 | 87 | | dB (Min) |
| | | $R_L = 1\ k\Omega$ | 106 | 87 | | |
| | | | | **80** | | |
| $V_O$ | Output Voltage Swing | $R_L = 100\Omega$ (Note 5) | | ±10 | | V (Min) |
| | | $R_L = 1\ k\Omega$ | ±13 | **±10** | | |
| $V_{CM}$ | Input Common Mode Range | | ±12 | **±10** | | V (Min) |
| CMRR | Common Mode Rejection Ratio | $V_{IN}$ −11V to +11V | 100 | 80 | | dB (Min) |
| | | | | **70** | | |
| PSRR | Power Supply Rejection Ratio | $V_{CC} = \pm 10V$ to $\pm 15V$ | 100 | 80 | | dB (Min) |
| | | | | **70** | | |
| $I_S$ | Supply Current | | 20 | 25 | | mA |

## AC Electrical Characteristics $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | LH4104<br>Typ | LH4104<br>Tested Limit (Note 2) | LH4104<br>Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| $t_S$ | Settling Time to 0.01% | $A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$ | 500 | 800 | | ns |
| $S_R$ | Slew Rate | $V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$ | 40 | | 32 | $V/\mu s$(min) |
| GBW | Gain Bandwidth Product | | 18 | | | MHz |
| $t_r$ | Small Signal Rise Time | $A_V = 1$, $R_L = 100\Omega$ | 10 | | 20 | ns |

**Note 1: Boldface limits are guaranteed over full temperature range.** Operating ambient temperature range of LH4104C is −25°C to +85°C, and LH4104 is −55°C to +125°C.

**Note 2:** Tested limits are guaranteed and 100% production tested.

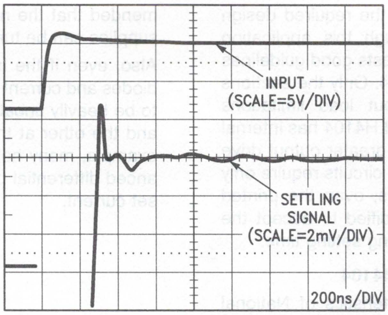
**Note 3:** Design limits are guaranteed (but not production tested).

**Note 4:** Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

**Note 5:** The output swing is limited by the maximum output current of ±100 mA when $R_L = 100\Omega$.

**Note 6:** When the LH4104 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with $V_{CC}$ of ±15V is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

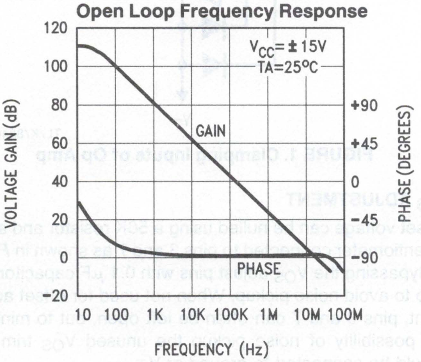
**Settling Signal**



TL/K/8840-3

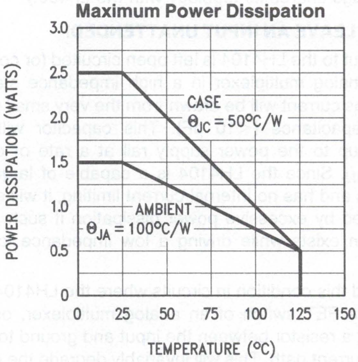
## Typical Performance Characteristics

**Open Loop Frequency Response**



TL/K/8840-4

**Maximum Power Dissipation**



TL/K/8840-5

## Applications Information

### POWER SUPPLY BYPASSING

The LH4104 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 μF disc ceramic capacitor and 1 μF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

### COMPENSATION

To minimize the effects of input capacitance at the LH4104's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

### INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias ($I_B$) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. $I_B$ will normally double with each 11°C rise in junction temperature.

### LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4104. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

### PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4104, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the

## Applications Information (Continued)

LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4104. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4104 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4104 without impacting setting time.

### PROTECTION SCHEMES FOR THE LH4104

The LH4104 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4104's input stage shares its topology with the LF400.)

### NEVER LEAVE AN INPUT UNATTENDED!

If an input to the LH4104 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance ($<10$ pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4104 is a capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

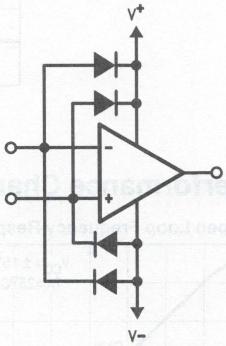
To avoid this condition in circuits where the LH4104 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected" state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

### POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor apears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can cause this problem. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.



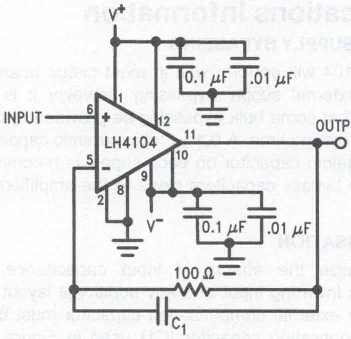
TL/K/8840–13

**FIGURE 1. Clamping Inputs of Op Amp**

### $V_{OS}$ ADJUSTMENT

Offset voltage can be nulled using a 56K resistor and a 25K potentiometer connected to pins 3 and 7 as shown in *Figure 3.* Bypassing the $V_{OS}$ adjust pins with 0.1 µF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 3 and 7 can often be left open, but to minimize the possibility of noise pickup the unused $V_{OS}$ trim pins should be connected to ground or V−.

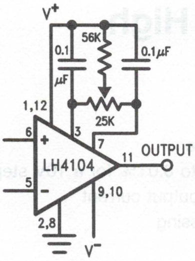
## Test Circuit for Pulse Response



TL/K/8840–6

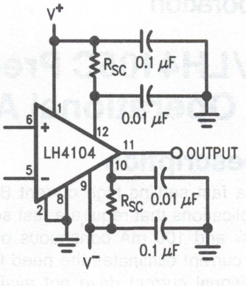
**FIGURE 2**

# Typical Applications


V+
56K
0.1 µF
0.1µF
1,12
25K
6
3
7
LH4104
11
OUTPUT
5
9,10
2,8
V−

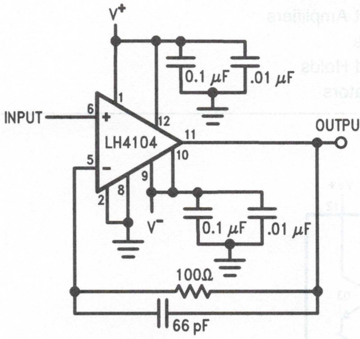
TL/K/8840–8

FIGURE 3. Offset Null


V+
RSC
0.1 µF
0.01 µF
6
1
12
11
LH4104
OUTPUT
10
5
9
8
2
RSC
0.01 µF
0.1 µF
V−

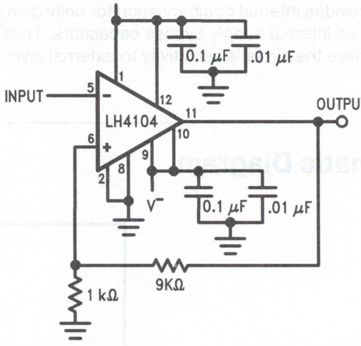
TL/K/8840–9

FIGURE 4. Using Resistor Current Limiting


V+
0.1 µF
.01 µF
INPUT
6
1
12
LH4104
11
OUTPUT
5
10
9
2
8
V−
0.1 µF
.01 µF
100Ω
66 pF

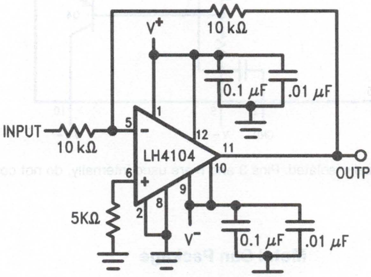
TL/K/8840–10

FIGURE 5. Unity Gain Follower


V+
0.1 µF
.01 µF
INPUT
5
1
12
LH4104
11
OUTPUT
6
10
9
2
8
V−
0.1 µF
.01 µF
9KΩ
1 kΩ

TL/K/8840–11

FIGURE 6. 10X Buffer Amplifier


10 kΩ
V+
0.1 µF
.01 µF
INPUT
10 kΩ
5
1
12
11
LH4104
6
10
OUTPUT
9
5KΩ
2
8
V−
0.1 µF
.01 µF

TL/K/8840–12

FIGURE 7. Unity Gain Inverter

**National Semiconductor Corporation**

**PRELIMINARY**

# LH4105/LH4105C Precision Fast Settling High Current Operational Amplifier

## General Description

The LH4105 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4105 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

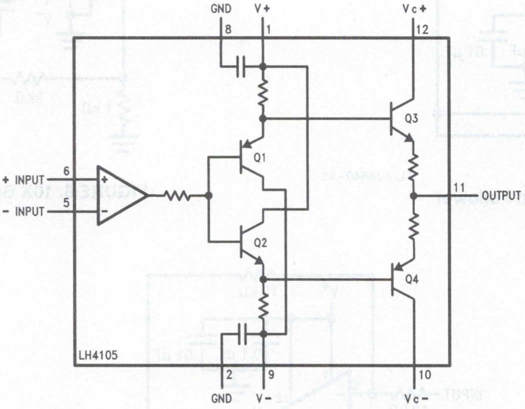
## Features

- 500 μV offset voltage
- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- Internal supply bypassing
- Unity gain stable

## Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

## Schematic Diagram

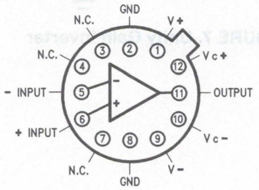


TL/K/9159-1

Pins #2 & #8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally, do not connect to these pins

## Connection Diagram

**Metal Can Package**



TL/K/9159-2

**Top View**

**Note:** 2 and 8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally. Do not connect to these pins.

**Order Number LH4105G or LH4105CG**
**See NS Package Number G12B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±18V |
| Steady State Output Current, $I_O$ | 100 mA |
| Power Dissipation at, $P_D$ | |
| $T_A = 25°C$, derate linearly at 100°C/W | 2.5W |
| $T_C = 25°C$, derate linearly at 50°C/W | 1.5W |
| Differential Input Voltage, $V_{IN}$ | ±30V but ≤ ±2$V_s$ |
| Input Voltage Range, $V_{CM}$ | ±18V but ≤ ±$V_s$ |
| Operating Temperature Range, $T_A$ | |
| LH4105 | −55°C to +125°C |
| LH4105C | −25°C to +85°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_j$ | 150°C |
| Lead Temperature (Soldering < 10 sec.) | 300°C |

ESD rating is to be determined.

## DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Note 1)

| Symbol | Parameter | Conditions | LH4105C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$ | 0.2 | 0.5 | **2** | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | $R_S = 50\Omega$ | 20 | | | µV/°C |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Note 4) $V_{CM} = 0V$ | 200 | 600 | | pA |
| | | | | | **250** | nA |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, $V_{CM} = 0V$ | 20 | 400 | | pA |
| | | | | | **200** | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | $10^{11}$ | | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L = 100\Omega$ | 106 | 87 | | dB (Min) |
| | | $R_L = 1\ k\Omega$ | 106 | 87 | **80** | |
| $V_O$ | Output Voltage Swing | $R_L = 100\Omega$ (Note 5) | | ±10 | | V (Min) |
| | | $R_L = 1\ k\Omega$ | ±13 | ±10 | **±10** | |
| $V_{CM}$ | Input Common Mode Range | | ±12 | ±11 | **±10** | V (Min) |
| CMRR | Common Mode Rejection Ratio | $V_{IN} = -11V$ to $+11V$ | 100 | 80 | **70** | dB (Min) |
| PSRR | Power Supply Rejection Ratio | $V_{CC} = \pm 10V$ to $\pm 15V$ | 100 | 80 | **70** | dB (Min) |
| $I_S$ | Supply Current | | 20 | 25 | | mA |

## AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | LH4105C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $t_S$ | Settling Time to 0.01% | $A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$ | 500 | 800 | | ns |
| $S_R$ | Slew Rate | $V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$ | 40 | | 32 | V/µs(min) |
| GBW | Gain Bandwidth Product | | 18 | | | MHz |
| $t_r$ | Small Signal Rise Time | $A_V = 1$, $R_L = 100\Omega$ | 10 | | 20 | ns |

## DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Notes 1 and 6)

| Symbol | Parameter | Conditions | LH4105 | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$ | 0.2 | **2** | | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | $R_S = 50\Omega$ | 20 | | | $\mu V/°C$ |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Note 4) $V_{CM} = 0V$ | 200 | 600 | | pA |
| | | | | **350** | | nA |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, $V_{CM} = 0V$ | 20 | 400 | | pA |
| | | | | **250** | | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | $10^{11}$ | | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L = 100\Omega$ | 106 | 87 | | dB (Min) |
| | | $R_L = 1\ k\Omega$ | 106 | 87 | | |
| | | | | **80** | | |
| $V_O$ | Output Voltage Swing | $R_L = 100\Omega$ (Note 5) | | ±10 | | V (Min) |
| | | $R_L = 1\ k\Omega$ | ±13 | **±10** | | |
| $V_{CM}$ | Input Common Mode Range | | ±12 | **±10** | | V (Min) |
| CMRR | Common Mode Rejection Ratio | $V_{IN}$ −11V to +11V | 100 | 80 | | dB (Min) |
| | | | | **70** | | |
| PSRR | Power Supply Rejection Ratio | $V_{CC} = \pm 10V$ to $\pm 15V$ | 100 | 80 | | dB (Min) |
| | | | | **70** | | |
| $I_S$ | Supply Current | | 20 | 25 | | mA |

## AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | LH4105 | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $t_S$ | Settling Time to 0.01% | $A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$ | 500 | 800 | | ns |
| $S_R$ | Slew Rate | $V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$ | 40 | | 32 | V/μs(min) |
| GBW | Gain Bandwidth Product | | 18 | | | MHz |
| $t_r$ | Small Signal Rise Time | $A_V = 1$, $R_L = 100\Omega$ | 10 | | 20 | ns |

**Note 1: Boldface limits are guaranteed over full temperature range.** Operating ambient temperature range of LH4105C is −25°C to +85°C, and LH4105 is −55°C to +125°C.

**Note 2:** Tested limits are guaranteed and 100% production tested.

**Note 3:** Design limits are guaranteed (but not production tested). These limits are not used to calculate outgoing quality levels.

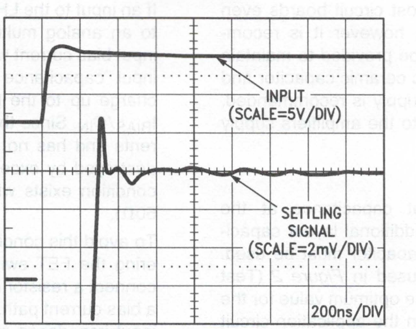
**Note 4:** Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

**Note 5:** The output swing is limited by the maximum output current of ±100 mA when $R_L = 100\Omega$.

**Note 6:** When the LH4105 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with $V_{CC}$ of ±15V is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

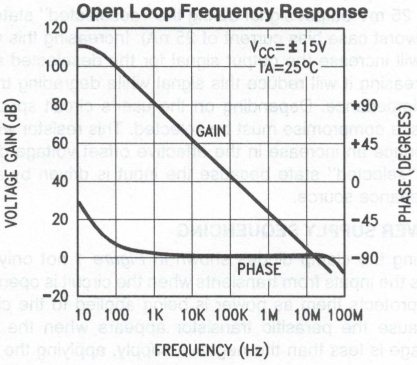
## Typical Performance Characteristics

**Settling Signal**



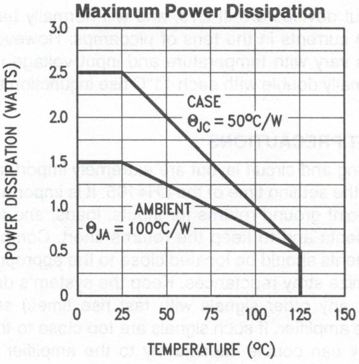
TL/K/9159-3

**Open Loop Frequency Response**



TL/K/9159-4

**Maximum Power Dissipation**



TL/K/9159-5

# Applications Information

### POWER SUPPLY BYPASSING

The LH4105 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 µF disc ceramic capacitor and 1 µF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

### COMPENSATION

To minimize the effects of input capacitance at the LH4105's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

### INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias ($I_B$) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. $I_B$ will normally double with each 11°C rise in junction temperature.

### LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4105. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

### PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4105, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4105. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4105 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4105 without impacting settling time. In addition, bypassing offset adjust pins 3 and 7 with 0.1 µF capacitors will minimize noise pickup and preserve the settling time.

### PROTECTION SCHEMES FOR THE LH4104

The LH4105 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4105's input stage shares its topology with the LF400.)

### NEVER LEAVE AN INPUT UNATTENDED

If an input to the LH4105 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance (<10 pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4105 is capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

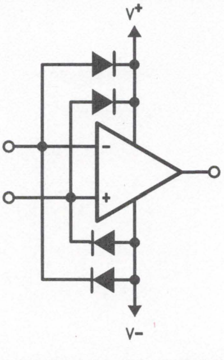
To avoid this condition in circuits where the LH4105 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

### POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor appears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can damage the device. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

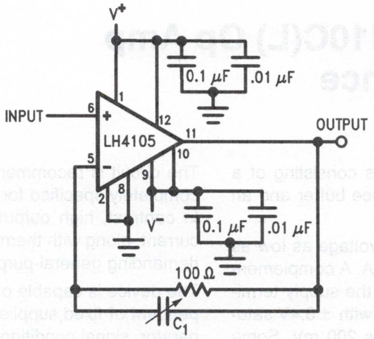
Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.



TL/K/9159-6

**FIGURE 1. Clamping Inputs of Op Amp**

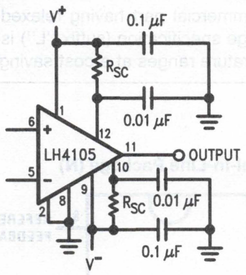
## Test Circuit for Pulse Response


V+
0.1 µF
.01 µF
INPUT
6
+
1
12
LH4105
11
10
OUTPUT
5
−
9
8
2
V−
0.1 µF
.01 µF
100 Ω
C1

TL/K/9159-7

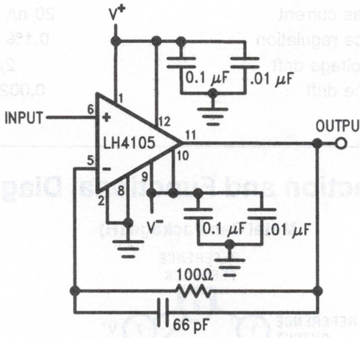
FIGURE 2

## Typical Applications


V+
0.1 µF
RSC
0.01 µF
6
+
1
12
LH4105
11
OUTPUT
5
−
10
9
8
2
RSC
0.01 µF
0.1 µF
V−

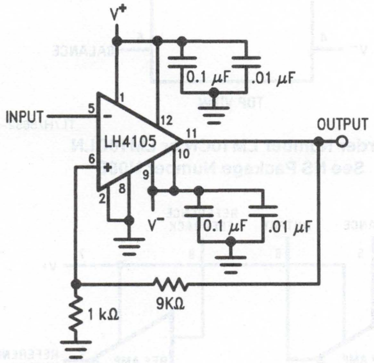
TL/K/9159-8

FIGURE 3. Using Resistor Current Limiting


V+
0.1 µF
.01 µF
INPUT
6
+
1
12
11
OUTPUT
LH4105
10
5
−
9
8
2
V−
0.1 µF
.01 µF
100Ω
66 pF

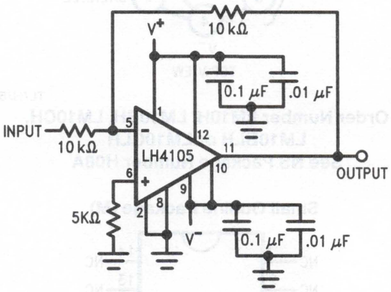
TL/K/9159-9

FIGURE 4. Unity Gain Follower


V+
0.1 µF
.01 µF
INPUT
5
−
1
12
LH4105
11
OUTPUT
6
+
10
9
8
2
V−
0.1 µF
.01 µF
9KΩ
1 kΩ

TL/K/9159-10

FIGURE 5. 10X Buffer Amplifier


10 kΩ
V+
0.1 µF
.01 µF
INPUT
10 kΩ
5
−
12
LH4105
11
OUTPUT
6
+
10
9
8
2
5KΩ
V−
0.1 µF
.01 µF

TL/K/9159-11

FIGURE 6. Unity Gain Inverter

National Semiconductor Corporation

# LM10/LM10B(L)/LM10C(L) Op Amp and Voltage Reference

## General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

| | |
|---|---|
| ■ input-offset voltage | 2.0 mV (max) |
| ■ input-offset current | 0.7 nA (max) |
| ■ input-bias current | 20 nA (max) |
| ■ reference regulation | 0.1% (max) |
| ■ offset-voltage drift | 2μV/°C |
| ■ reference drift | 0.002%/°C |

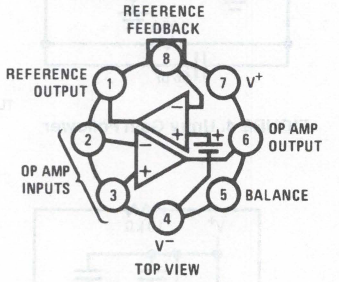
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

## Connection and Functional Diagrams

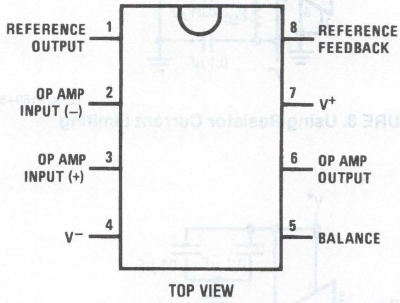
### Metal Can Package (H)


REFERENCE FEEDBACK
8
REFERENCE OUTPUT
1
7
V+
2
6
OP AMP OUTPUT
OP AMP INPUTS
3
5
BALANCE
4
V−
TOP VIEW

TL/H/5652-1

**Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH**
**See NS Package Number H08A**

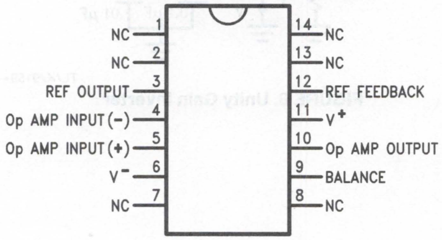
### Dual-In-Line Package (N)


REFERENCE OUTPUT
1
OP AMP INPUT (−)
2
OP AMP INPUT (+)
3
V−
4
8
REFERENCE FEEDBACK
7
V+
6
OP AMP OUTPUT
5
BALANCE
TOP VIEW

TL/H/5652-15

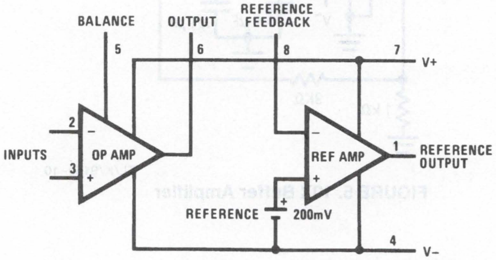
**Order Number LM10CN or LM10CLN**
**See NS Package Number N08E**

### Small Outline Package (M)


NC 1
NC 2
REF OUTPUT 3
Op AMP INPUT (−) 4
Op AMP INPUT (+) 5
V− 6
NC 7
14 NC
13 NC
12 REF FEEDBACK
11 V+
10 Op AMP OUTPUT
9 BALANCE
8 NC

TL/H/5652-17

**Order Number LM10CWM or LM10CLWM**
**See NS Package Number M14B**


BALANCE
5
OUTPUT
6
REFERENCE FEEDBACK
8
7
V+
2
−
INPUTS
3
+
OP AMP
−
REF AMP
+
1
REFERENCE OUTPUT
REFERENCE
+
200mV
4
V−

TL/H/5652-16

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 7)**

| | **LM10/LM10B/LM10C** | **LM10BL/LM10CL** |
|---|---|---|
| Total Supply Voltage | 45V | 7V |
| Differential Input Voltage (note 1) | ±40V | ±7V |
| Power Dissipation (note 2) | internally limited | |
| Output Short-circuit Duration (note 3) | indefinite | |
| Storage-Temp. Range | −55°C to +150°C | |
| Lead Temp. (Soldering, 10 seconds) | | |
| Metal Can | 300°C | |
| Lead Temp. (Soldering, 10 seconds) DIP | 260°C | |
| Vapor Phase (60 seconds) | 215°C | |
| Infrared (15 seconds) | 220°C | |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

ESD rating is to be determined.

## Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (note 4) **(Boldface type refers to limits over temperature range)**

| Parameter | Conditions | LM10/LM10B | | | LM10C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input offset voltage | | | 0.3 | 2.0 | | 0.5 | 4.0 | mV |
| | | | | **3.0** | | | **5.0** | mV |
| Input offset current (note 5) | | | 0.25 | 0.7 | | 0.4 | 2.0 | nA |
| | | | | **1.5** | | | **3.0** | nA |
| Input bias current | | | 10 | 20 | | 12 | 30 | nA |
| | | | | **30** | | | **40** | nA |
| Input resistance | | 250 | 500 | | 150 | 400 | | kΩ |
| | | **150** | | | **115** | | | kΩ |
| Large signal voltage gain | $V_S = \pm 20V$, $I_{OUT} = 0$ | 120 | 400 | | 80 | 400 | | V/mV |
| | $V_{OUT} = \pm 19.95V$ | **80** | | | **50** | | | V/mV |
| | $V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$ | 50 | 130 | | 25 | 130 | | V/mV |
| | $I_{OUT} = \pm 20$ mA **(±15 mA)** | **20** | | | **15** | | | V/mV |
| | $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA | 1.5 | 3.0 | | 1.0 | 3.0 | | V/mV |
| | $V_{OUT} = \pm 0.4V$ **(±0.3V), $V_{CM} = -0.4V$** | **0.5** | | | **0.75** | | | V/mV |
| Shunt gain (note 6) | 1.2V **(1.3V)** $\le V_{OUT} \le 40V$, | 14 | 33 | | 10 | 33 | | V/mV |
| | $R_L = 1.1$ kΩ | | | | | | | |
| | 0.1 mA $\le I_{OUT} \le 5$ mA | **6** | | | **6** | | | V/mV |
| | $1.5V \le V^+ \le 40V$, $R_L = 250\Omega$ | 8 | 25 | | 6 | 25 | | V/mV |
| | 0.1 mA $\le I_{OUT} \le 20$ mA | **4** | | | **4** | | | V/mV |
| Common-mode rejection | $-20V \le V_{CM} \le 19.15V$ **(19V)** | 93 | 102 | | 90 | 102 | | dB |
| | $V_S = \pm 20V$ | **87** | | | **87** | | | dB |
| Supply-voltage rejection | $-0.2V \ge V^- \ge -39V$ | 90 | 96 | | 87 | 96 | | dB |
| | $V^+ = 1.0V$ **(1.1V)** | **84** | | | **84** | | | dB |
| | 1.0V **(1.1V)** $\le V^+ \le 39.8V$ | 96 | 106 | | 93 | 106 | | dB |
| | $V^- = -0.2V$ | **90** | | | **90** | | | dB |
| Offset voltage drift | | | 2.0 | | | 5.0 | | μV/°C |
| Offset current drift | | | 2.0 | | | 5.0 | | pA/°C |
| Bias current drift | $T_C < 100°C$ | | 60 | | | 90 | | pA/°C |

## Electrical Characteristics

$T_J=25°C$, **$T_{MIN} \le T_J \le T_{MAX}$**, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

| Parameter | Conditions | LM10/LM10B |  |  | LM10C |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Line regulation | 1.2V (**1.3V**) $\le V_S \le$ 40V<br>$0 \le I_{REF} \le$ 1.0 mA, $V_{REF}$ = 200 mV |  | 0.001 | 0.003<br>**0.006** |  | 0.001 | 0.008<br>**0.01** | %/V<br>%/V |
| Load regulation | $0 \le I_{REF} \le$ 1.0 mA<br>$V^+ - V_{REF} \ge$ 1.0V (**1.1V**) |  | 0.01 | 0.1<br>**0.15** |  | 0.01 | 0.15<br>**0.2** | %<br>% |
| Amplifier gain | 0.2V $\le V_{REF} \le$ 35V | 50<br>**23** | 75 |  | 25<br>**15** | 70 |  | V/mV<br>V/mV |
| Feedback sense voltage |  | 195<br>**194** | 200 | 205<br>**206** | 190<br>**189** | 200 | 210<br>**211** | mV<br>mV |
| Feedback current |  |  | 20 | 50<br>**65** |  | 22 | 75<br>**90** | nA<br>nA |
| Reference drift |  |  | 0.002 |  |  | 0.003 |  | %/°C |
| Supply current |  |  | 270 | 400<br>**500** |  | 300 | 500<br>**570** | μA<br>μA |
| Supply current change | 1.2V (**1.3V**) $\le V_S \le$ 40V |  | 15 | **75** |  | 15 | **75** | μA |

| Parameter | Conditions | LM10BL |  |  | LM10CL |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input offset voltage |  |  | 0.3 | 2.0<br>**3.0** |  | 0.5 | 4.0<br>**5.0** | mV<br>mV |
| Input offset current (note 5) |  |  | 0.1 | 0.7<br>**1.5** |  | 0.2 | 2.0<br>**3.0** | nA<br>nA |
| Input bias current |  |  | 10 | 20<br>**30** |  | 12 | 30<br>**40** | nA<br>nA |
| Input resistance |  | 250<br>**150** | 500 |  | 150<br>**115** | 400 |  | kΩ<br>kΩ |
| Large signal voltage gain | $V_S = \pm$3.25V, $I_{OUT}$ = 0<br>$V_{OUT} = \pm$3.2V<br>$V_S = \pm$3.25V, $I_{OUT}$ = 10 mA<br>$V_{OUT} = \pm$2.75 V<br>$V_S = \pm$0.6V (**0.65V**), $I_{OUT} = \pm$2 mA<br>$V_{OUT} = \pm$0.4V (±**0.3V**), $V_{CM}$ = −0.4V | 60<br>**40**<br>10<br>**4**<br>1.5<br>**0.5** | 300<br><br>25<br><br>3.0<br> | <br><br><br><br><br> | 40<br>**25**<br>5<br>**3**<br>1.0<br>**0.75** | 300<br><br>25<br><br>3.0<br> | <br><br><br><br><br> | V/mV<br>V/mV<br>V/mV<br>V/mV<br>V/mV<br>V/mV |
| Shunt gain (note 6) | 1.5V $\le V^+ \le$ 6.5V, $R_L$ = 500Ω<br>0.1 mA $\le I_{OUT} \le$ 10 mA | 8<br>**4** | 30 |  | 6<br>**4** | 30 |  | V/mV<br>V/mV |
| Common-mode rejection | −3.25V $\le V_{CM} \le$ 2.4V (**2.25V**)<br>$V_S = \pm$3.25V | 89<br>**83** | 102 |  | 80<br>**74** | 102 |  | dB<br>dB |
| Supply-voltage rejection | −0.2V $\ge V^- \ge$ −5.4V<br>$V^+$ = 1.0V (**1.2V**)<br>1.0V (**1.1V**) $\le V^+ \le$ 6.3V<br>$V^-$ = 0.2V | 86<br>**80**<br>94<br>**88** | 96<br><br>106<br> |  | 80<br>**74**<br>80<br>**74** | 96<br><br>106<br> |  | dB<br>dB<br>dB<br>dB |
| Offset voltage drift |  |  | 2.0 |  |  | 5.0 |  | μV/°C |
| Offset current drift |  |  | 2.0 |  |  | 5.0 |  | pA/°C |
| Bias current drift |  |  | 60 |  |  | 90 |  | pA/°C |

## Electrical Characteristics

$T_J = 25°C$, $\mathbf{T_{MIN} \leq T_J \leq T_{MAX}}$, (note 4) **(Boldface type refers to limits over temperature range)**

| Parameter | Conditions | LM10BL |  |  | LM10CL |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Line regulation | $1.2V$ **(1.3V)** $\leq V_S \leq 6.5V$<br>$0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV |  | 0.001 | 0.01<br>**0.02** |  | 0.001 | 0.02<br>**0.03** | %/V<br>%/V |
| Load regulation | $0 \leq I_{REF} \leq 0.5$ mA<br>$V^+ - V_{REF} \geq 1.0V$ **(1.1V)** |  | 0.01 | 0.1<br>**0.15** |  | 0.01 | 0.15<br>**0.2** | %<br>% |
| Amplifier gain | $0.2V \leq V_{REF} \leq 5.5V$ | 30<br>**20** | 70 |  | 20<br>**15** | 70 |  | V/mV<br>V/mV |
| Feedback sense voltage |  | 195<br>**194** | 200 | 205<br>**206** | 190<br>**189** | 200 | 210<br>**211** | mV<br>mV |
| Feedback current |  |  | 20 | 50<br>**65** |  | 22 | 75<br>**90** | nA<br>nA |
| Reference drift |  |  | 0.002 |  |  | 0.003 |  | %/°C |
| Supply current |  |  | 260 | 400<br>**500** |  | 280 | 500<br>**570** | µA<br>µA |

**Note 1:** The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

**Note 2:** The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

**Note 3:** Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

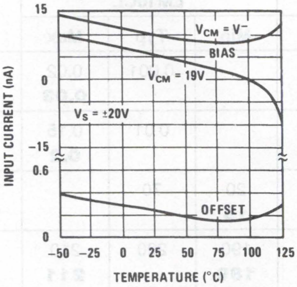
**Note 4:** These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

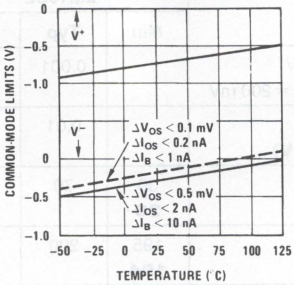
**Note 5:** For $T_J > 90°C$, $I_{OS}$ may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

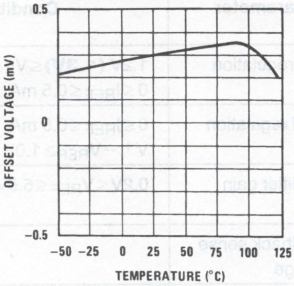
**Note 6:** This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the $V^+$ terminal of the IC and input common mode is referred to $V^-$ (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

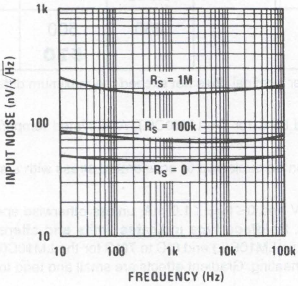
**Note 7:** Refer to RETS10X for LM10H military specifications.

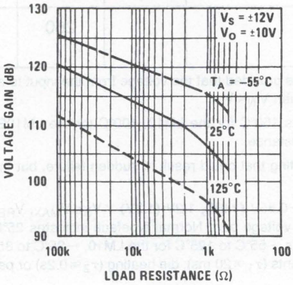
# Typical Performance Characteristics (Op Amp)

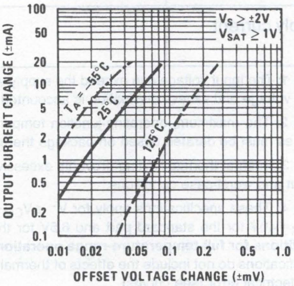

Input Current

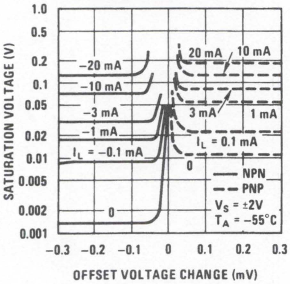

Common Mode Limits

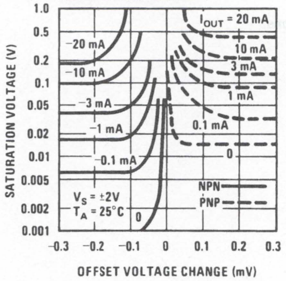

Offset Voltage Drift

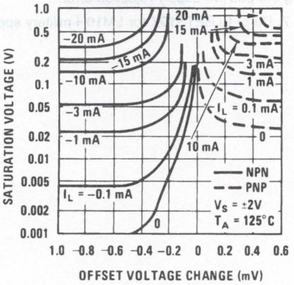

Input Noise Voltage

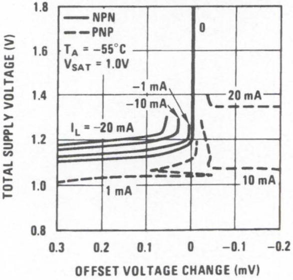

DC Voltage Gain

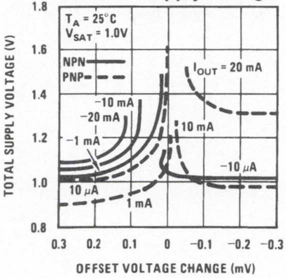

Transconductance

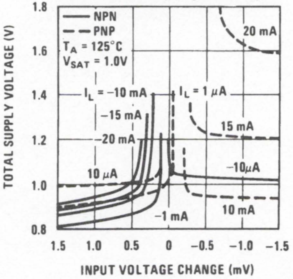

Output Saturation Characteristics


Output Saturation Characteristics


Output Saturation Characteristics


Minimum Supply Voltage


Minimum Supply Voltage


Minimum Supply Voltage

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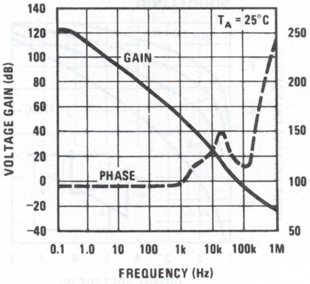
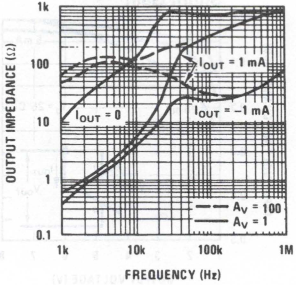
## Typical Performance Characteristics (Op Amp) (Continued)

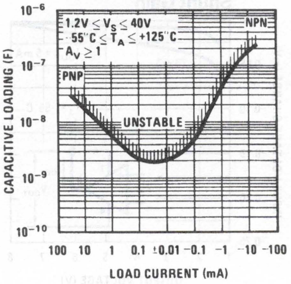
### Frequency Response



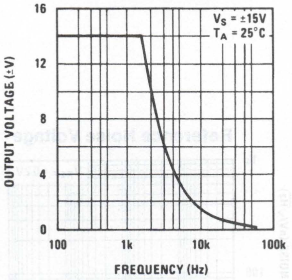
### Output Impedance



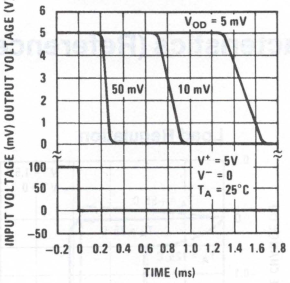
### Typical Stability Range



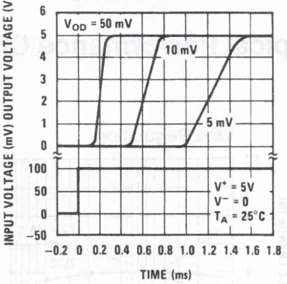
### Large Signal Response



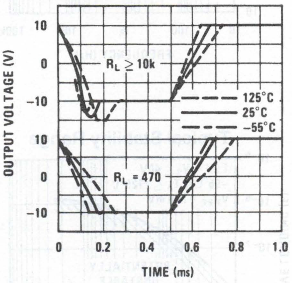
### Comparator Response Time For Various Input Overdrives



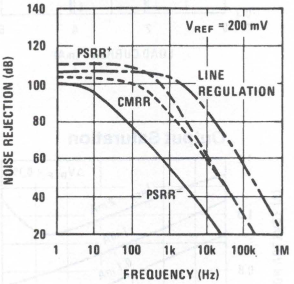
### Comparator Response Time For Various Input Overdrives



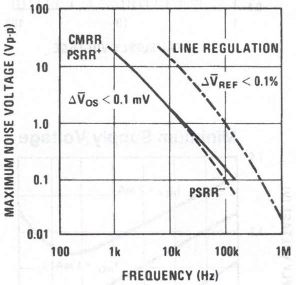
### Follower Pulse Response



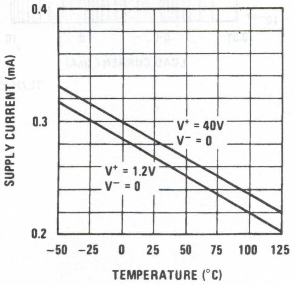
### Noise Rejection



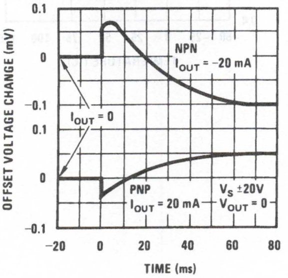
### Rejection Slew Limiting



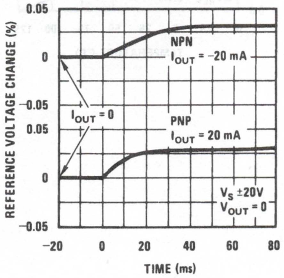
### Supply Current



### Thermal Gradient Feedback

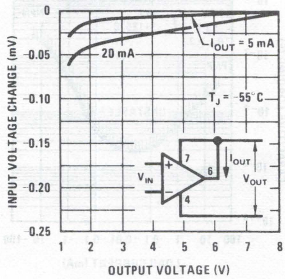


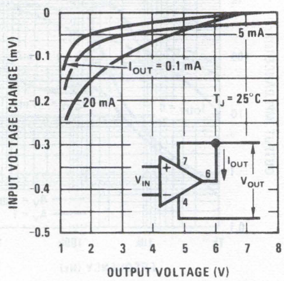
### Thermal Gradient Cross-coupling

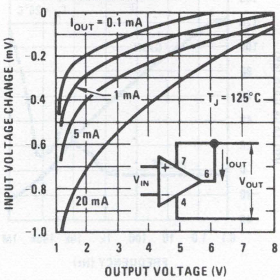


TL/H/5652–3

## Typical Performance Characteristics (Op Amp) (Continued)

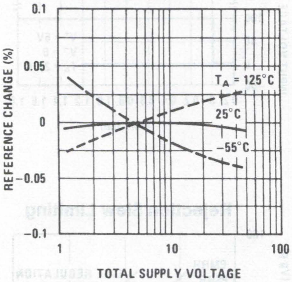

Shunt Gain

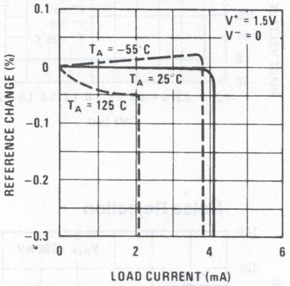

Shunt Gain

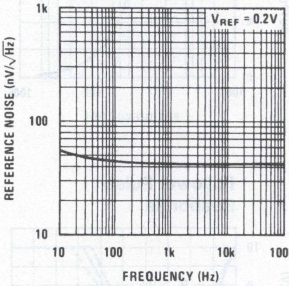

Shunt Gain

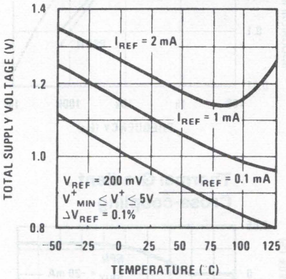
TL/H/5652–4

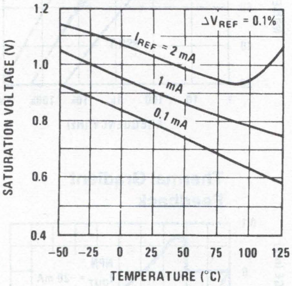
## Typical Performance Characteristics (Reference)

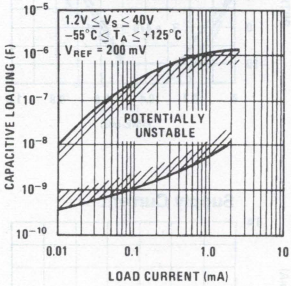

Line Regulation


Load Regulation


Reference Noise Voltage


Minimum Supply Voltage


Output Saturation


Typical Stability Range

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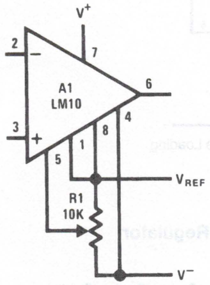
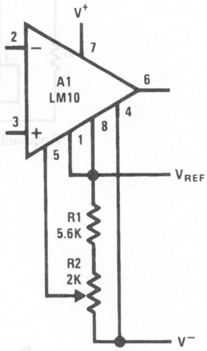
## Typical Applications†† (Pin numbers are for devices in 8-pin packages)

### Op Amp Offset Adjustment

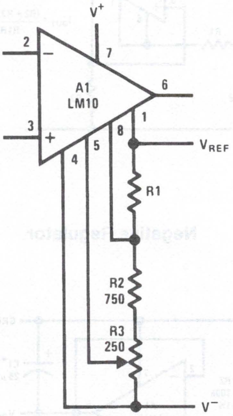
**Standard**


$V^+$
2
−
7
A1
LM10
6
3
+
4
8
1
5
$V_{REF}$
R1
10K
$V^-$

**Limited Range**

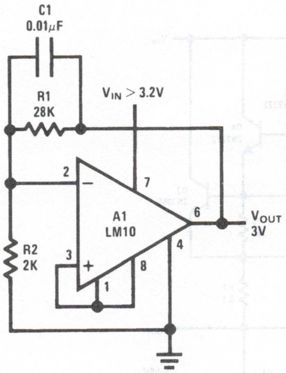

$V^+$
2
−
7
A1
LM10
6
3
+
4
8
1
5
$V_{REF}$
R1
5.6K
R2
2K
$V^-$

**Limited Range With Boosted Reference**

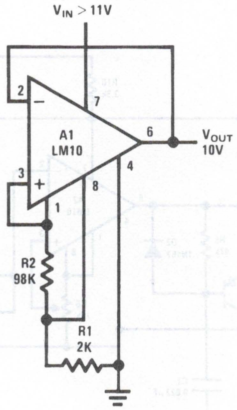

$V^+$
2
−
7
A1
LM10
6
3
+
1
8
5
4
$V_{REF}$
R1
R2
750
R3
250
$V^-$

### Positive Regulators†

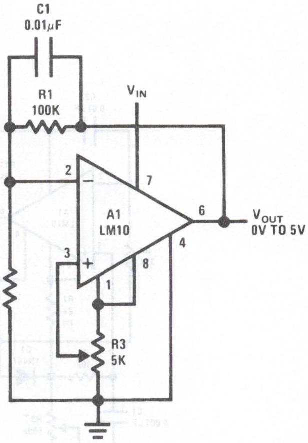
**Low Voltage**


C1
0.01μF
R1
28K
$V_{IN} > 3.2V$
2
−
7
A1
LM10
6
$V_{OUT}$
3V
4
R2
2K
3
+
8
1

**Best Regulation**


$V_{IN} > 11V$
2
−
7
A1
LM10
6
$V_{OUT}$
10V
4
3
+
8
1
R2
98K
R1
2K

**Zero Output**


C1
0.01μF
R1
100K
$V_{IN}$
2
−
7
A1
LM10
6
$V_{OUT}$
0V TO 5V
4
3
+
8
1
R2
3.9K
R3
5K

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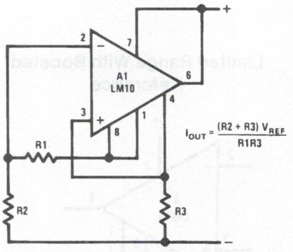
†Use only electrolytic output capacitors.

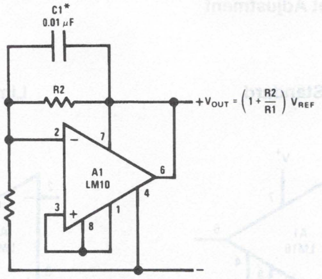
††Circuit descriptions available in application note AN-211.

## Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

### Current Regulator

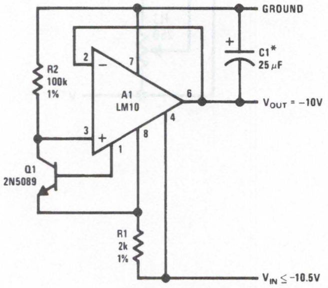

+
2
7
A1
LM10
6
4
3
1
8
R1
R2
R3
−
$I_{OUT} = \frac{(R2 + R3)\ V_{REF}}{R1R3}$

### Shunt Regulator


C1*
0.01 µF
R2
$+V_{OUT} = \left(1 + \frac{R2}{R1}\right) V_{REF}$
2
7
A1
LM10
6
4
R1
3
1
8
−

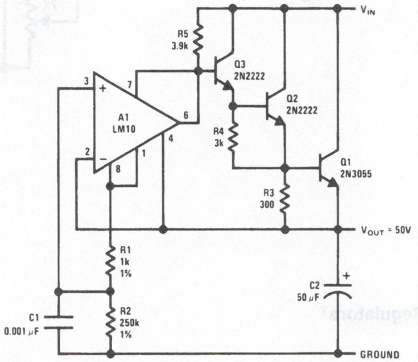
*Required For Capacitive Loading

### Negative Regulator

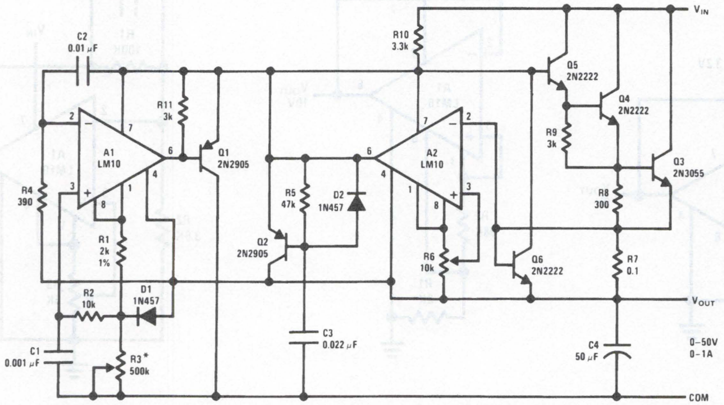

GROUND
C1*
25 µF
R2
100k
1%
2
7
A1
LM10
6
4
3
1
8
$V_{OUT} = -10V$
Q1
2N5089
R1
2k
1%
$V_{IN} \le -10.5V$

*Electrolytic

### Precision Regulator


$V_{IN}$
R5
3.9k
Q3
2N2222
Q2
2N2222
3
7
A1
LM10
6
4
2
1
8
R4
3k
Q1
2N3055
R3
300
$V_{OUT} = 50V$
R1
1k
1%
C2
50 µF
C1
0.001 µF
R2
250k
1%
GROUND

### Laboratory Power Supply


$V_{IN}$
R10
3.3k
C2
0.01 µF
Q5
2N2222
R11
3k
Q4
2N2222
2
7
A1
LM10
6
4
3
1
8
Q1
2N2905
R5
47k
D2
1N457
A2
LM10
R9
3k
Q3
2N3055
R4
390
R8
300
R1
2k
1%
Q2
2N2905
R6
10k
Q6
2N2222
R7
0.1
R2
10k
D1
1N457
$V_{OUT}$
C3
0.022 µF
C4
50 µF
0–50V
0–1A
C1
0.001 µF
R3*
500k
COM

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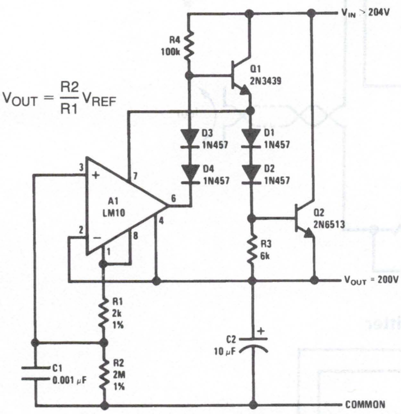
$*V_{OUT} = 10^{-4}\ R3$

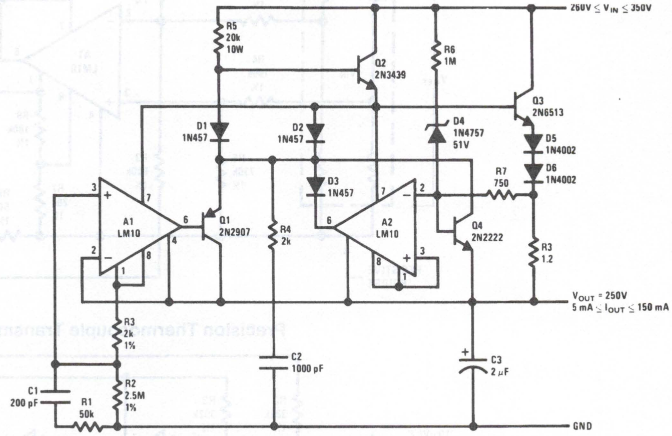
††Circuit descriptions available in application note AN-211.

## Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

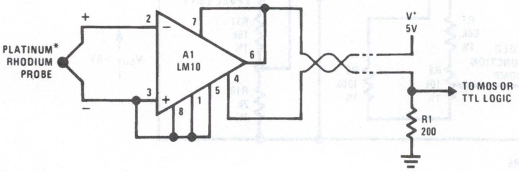
### HV Regulator


VOUT = R2/R1 VREF
VIN > 204V
R4 100k
Q1 2N3439
D3 1N457
D4 1N457
D1 1N457
D2 1N457
Q2 2N6513
R3 6k
A1 LM10
VOUT = 200V
R1 2k 1%
R2 2M 1%
C1 0.001 μF
C2 10 μF
COMMON

### Protected HV Regulator

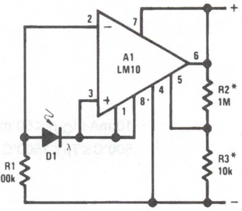

260V ≤ VIN ≤ 350V
R5 20k 10W
Q2 2N3439
R6 1M
Q3 2N6513
D1 1N457
D2 1N457
D3 1N457
D4 1N4757 51V
D5 1N4002
D6 1N4002
R7 750
A1 LM10
Q1 2N2907
R4 2k
A2 LM10
Q4 2N2222
R3 1.2
VOUT = 250V
5 mA ≤ IOUT ≤ 150 mA
R3 2k 1%
R2 2.5M 1%
C1 200 pF
R1 50k
C2 1000 pF
C3 2 μF
GND

### Flame Detector


PLATINUM* RHODIUM PROBE
A1 LM10
V+ 5V
TO MOS OR TTL LOGIC
R1 200

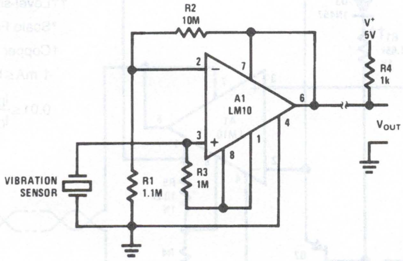
*800°C Threshold Is Established By Connecting Balance To $V_{REF}$.

### Light Level Sensor

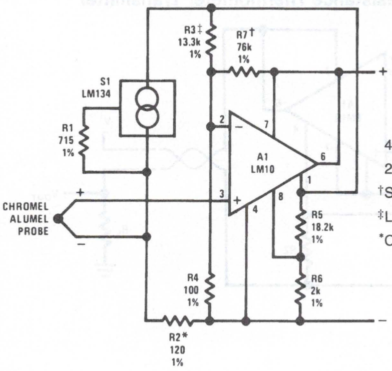

A1 LM10
D1
R1 200k
R2* 1M
R3* 10k

*Provides Hysteresis

### Remote Amplifier


R2 10M
A1 LM10
V+ 5V
R4 1k
VOUT
VIBRATION SENSOR
R1 1.1M
R3 1M

### Remote Thermocouple Amplifier


R3‡ 13.3k 1%
R7† 76k 1%
S1 LM134
R1 715 1%
A1 LM10
CHROMEL ALUMEL PROBE
R5 18.2k 1%
R6 2k 1%
R4 100 1%
R2* 120 1%

$4V \le V_{OUT} \le 20V$

$200°C \le T_P \le 700°C$

†Span Trim

‡Level-shift Trim

*Cold-junction Trim

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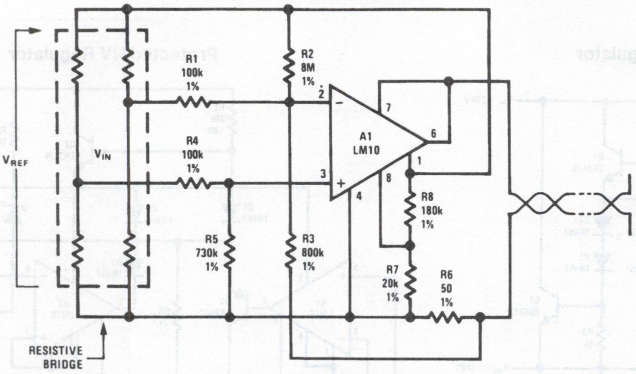
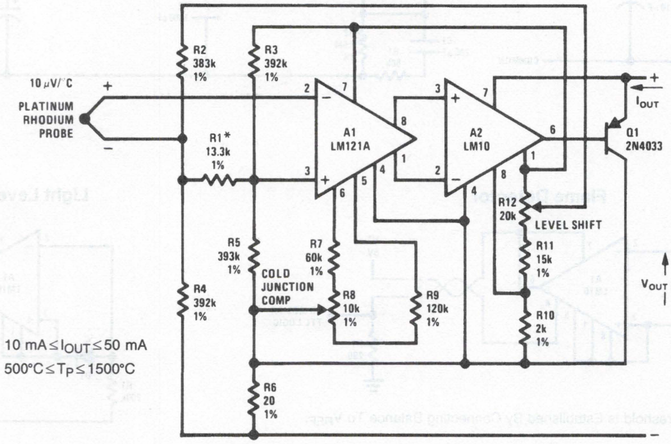
††Circuit descriptions available in application note AN-211.

## Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

### Transmitter for Bridge Sensor


R1
100k
1%
R2
8M
1%
R4
100k
1%
V<sub>REF</sub>
V<sub>IN</sub>
A1
LM10
2
3
7
6
1
8
4
R5
730k
1%
R3
800k
1%
R8
180k
1%
R7
20k
1%
R6
50
1%
I<sub>OUT</sub>
RESISTIVE
BRIDGE

### Precision Thermocouple Transmitter

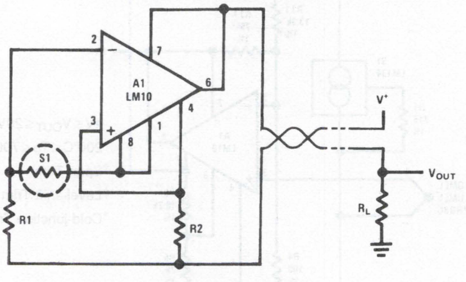

R2
383k
1%
R3
392k
1%
10 µV/°C
PLATINUM
RHODIUM
PROBE
+
−
R1*
13.3k
1%
A1
LM121A
A2
LM10
2
3
7
8
1
4
5
6
Q1
2N4033
I<sub>OUT</sub>
R12
20k
LEVEL SHIFT
R11
15k
1%
R10
2k
1%
V<sub>OUT</sub> > 6V
R5
393k
1%
R7
60k
1%
COLD
JUNCTION
COMP
R8
10k
1%
R9
120k
1%
R4
392k
1%
R6
20
1%

$10\text{ mA} \le I_{OUT} \le 50\text{ mA}$

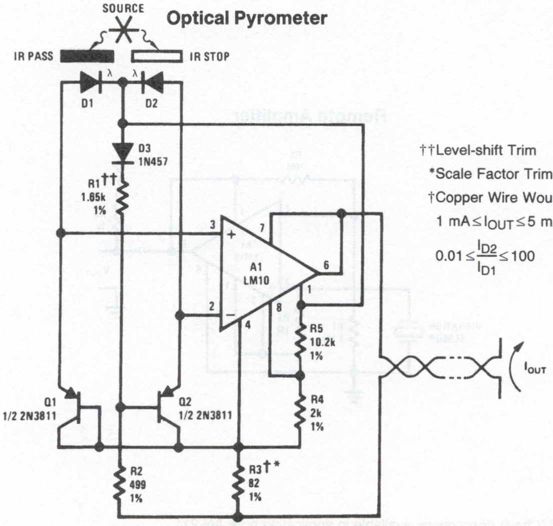
$500°C \le T_P \le 1500°C$

*Gain Trim

### Resistance Thermometer Transmitter


A1
LM10
2
3
7
6
1
8
4
S1
R1
R2
V⁺
V<sub>OUT</sub>
R<sub>L</sub>

### Optical Pyrometer


SOURCE
IR PASS
IR STOP
λ
λ
D1
D2
D3
1N457
R1††
1.65k
1%
A1
LM10
3
2
7
6
1
8
4
R5
10.2k
1%
R4
2k
1%
I<sub>OUT</sub>
Q1
1/2 2N3811
Q2
1/2 2N3811
R2
499
1%
R3†*
82
1%

††Level-shift Trim

*Scale Factor Trim

†Copper Wire Wound

$1\text{ mA} \le I_{OUT} \le 5\text{ mA}$

$0.01 \le \frac{I_{D2}}{I_{D1}} \le 100$

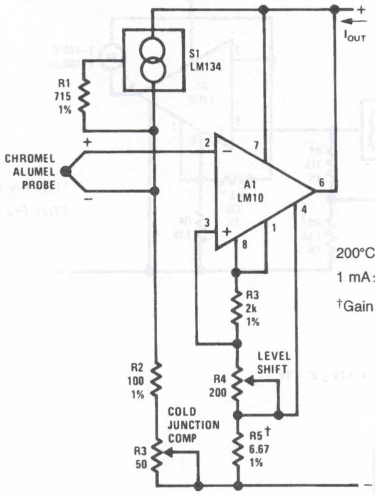
---

††Circuit descriptions available in application note AN-211.

TL/H/5652–9

## Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

### Thermocouple Transmitter



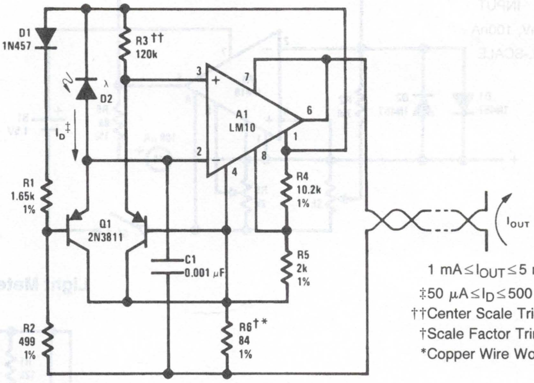
+
I_OUT
S1
LM134
R1
715
1%
CHROMEL
ALUMEL
PROBE
+
−
2
7
A1
LM10
6
3
4
1
8
R3
2k
1%
LEVEL
SHIFT
R2
100
1%
R4
200
COLD
JUNCTION
COMP
R5†
6.67
1%
R3
50
−

200°C ≤ $T_p$ ≤ 700°C

1 mA ≤ $I_{OUT}$ ≤ 5 mA

†Gain Trim

### Logarithmic Light Sensor



D1
1N457
R3 ††
120k
D2
λ
$I_D$‡
3
7
A1
LM10
6
1
2
8
4
R1
1.65k
1%
Q1
2N3811
C1
0.001 μF
R4
10.2k
1%
R5
2k
1%
R2
499
1%
R6†*
84
1%
I_OUT

1 mA ≤ $I_{OUT}$ ≤ 5 mA

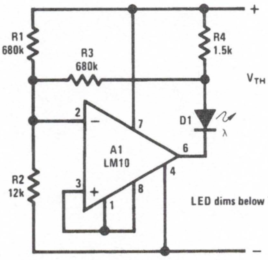
‡50 μA ≤ $I_D$ ≤ 500 μA

††Center Scale Trim

†Scale Factor Trim

*Copper Wire Wound

### Battery-level Indicator

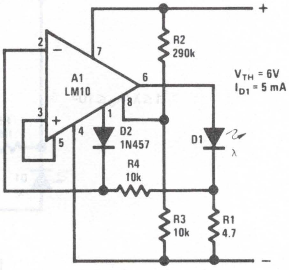


+
R1
680k
R3
680k
R4
1.5k
2
7
D1
λ
A1
LM10
6
4
R2
12k
3
8
1
−

$V_{TH}$ = 6V

LED dims below 7V

### Battery-threshold Indicator

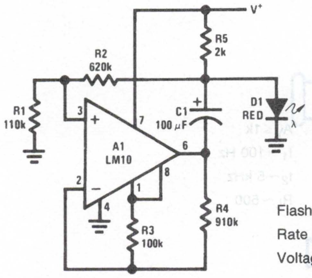


+
R2
290k
2
7
A1
LM10
6
8
3
1
4
5
D2
1N457
D1
λ
R4
10k
R3
10k
R1
4.7
−

$V_{TH}$ = 6V

$I_{D1}$ = 5 mA

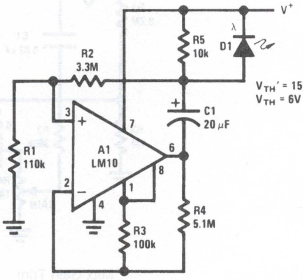
### Single-cell Voltage Monitor



V⁺
R5
2k
R2
620k
R1
110k
3
7
C1
100 μF
D1
RED
λ
A1
LM10
6
8
2
1
4
R3
100k
R4
910k

Flashes Above 1.2V Rate Increases With Voltage

### Double-ended Voltage Monitor



V⁺
R5
10k
D1
λ
R2
3.3M
3
7
C1
20 μF
R1
110k
A1
LM10
6
8
2
1
4
R3
100k
R4
5.1M

$V_{TH}'$ = 15V

$V_{TH}$ = 6V

Flash Rate Increases Above 6V and Below 15V

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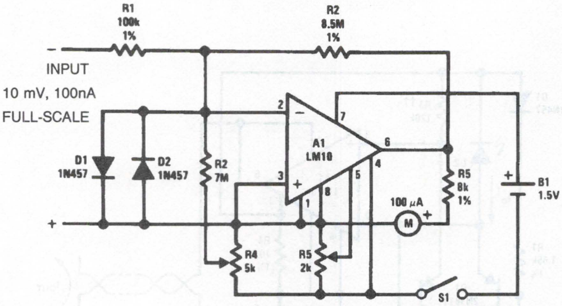
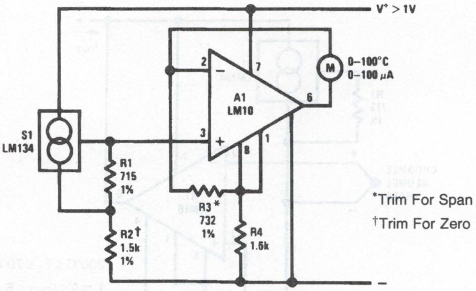
††Circuit descriptions available in application note AN-211.

## Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

### Meter Amplifier


R1
100k
1%
R2
8.5M
1%
–
INPUT
10 mV, 100nA
FULL-SCALE
+
D1
1N457
D2
1N457
R2
7M
A1
LM10
2
3
7
6
4
5
8
1
R5
8k
1%
B1
1.5V
100 µA
M
R4
5k
R5
2k
S1

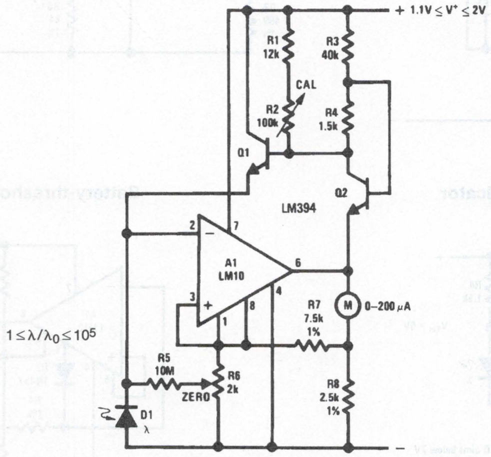
### Thermometer


V+ > 1V
0–100°C
0–100 µA
M
A1
LM10
2
3
7
6
1
8
S1
LM134
R1
715
1%
R3*
732
1%
R4
1.6k
R2†
1.5k
1%
–

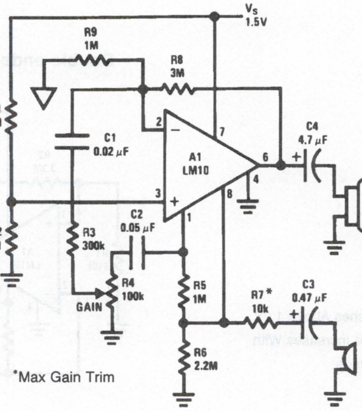
*Trim For Span

†Trim For Zero

### Light Meter


+ 1.1V ≤ V+ ≤ 2V
R1
12k
R3
40k
CAL
R2
100k
R4
1.5k
Q1
Q2
LM394
A1
LM10
2
3
7
6
4
8
1
M
0–200 µA
R7
7.5k
1%
R8
2.5k
1%
R5
10M
R6
2k
ZERO
D1
λ
$1 \le \lambda/\lambda_0 \le 10^5$
–

### Microphone Amplifier


$V_S$
1.5V
R9
1M
R8
3M
R1
6.2M
C1
0.02 µF
A1
LM10
2
3
7
6
4
8
1
C4
4.7 µF
R2
1M
R3
300k
C2
0.05 µF
R4
100k
GAIN
R5
1M
R7*
10k
C3
0.47 µF
R6
2.2M

$Z_{OUT} \sim 680\Omega$
@ 5 kHz

$A_V \le 1k$
$f_1 \sim 100$ Hz
$f_2 \sim 5$ kHz
$R_L \sim 500$

*Max Gain Trim

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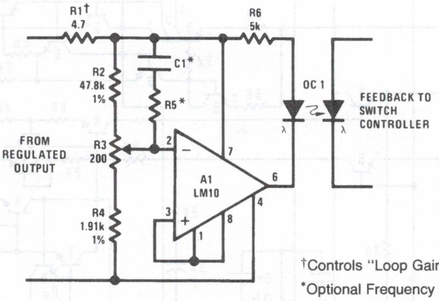
---

††Circuit descriptions available in application note AN-211.

## Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

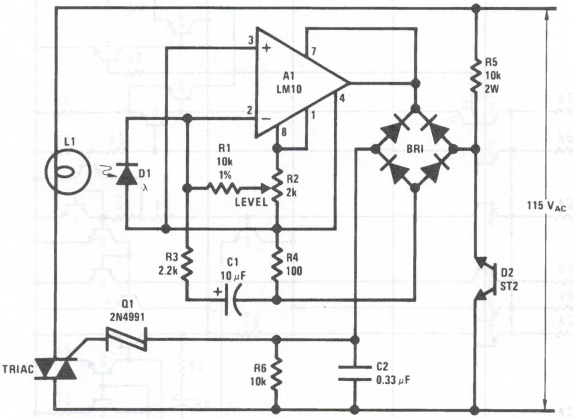
### Isolated Voltage Sensor


R1†
4.7
R6
5k
C1*
R2
47.8k
1%
R5*
OC 1
FEEDBACK TO
SWITCH
CONTROLLER
FROM
REGULATED
OUTPUT
R3
200
A1
LM10
R4
1.91k
1%

†Controls "Loop Gain"

*Optional Frequency Shaping

### Light-level Controller


A1
LM10
R5
10k
2W
BRI
L1
D1
R1
10k
1%
LEVEL
R2
2k
115 V_AC
R3
2.2k
C1
10 µF
R4
100
D2
ST2
Q1
2N4991
TRIAC
R6
10k
C2
0.33 µF

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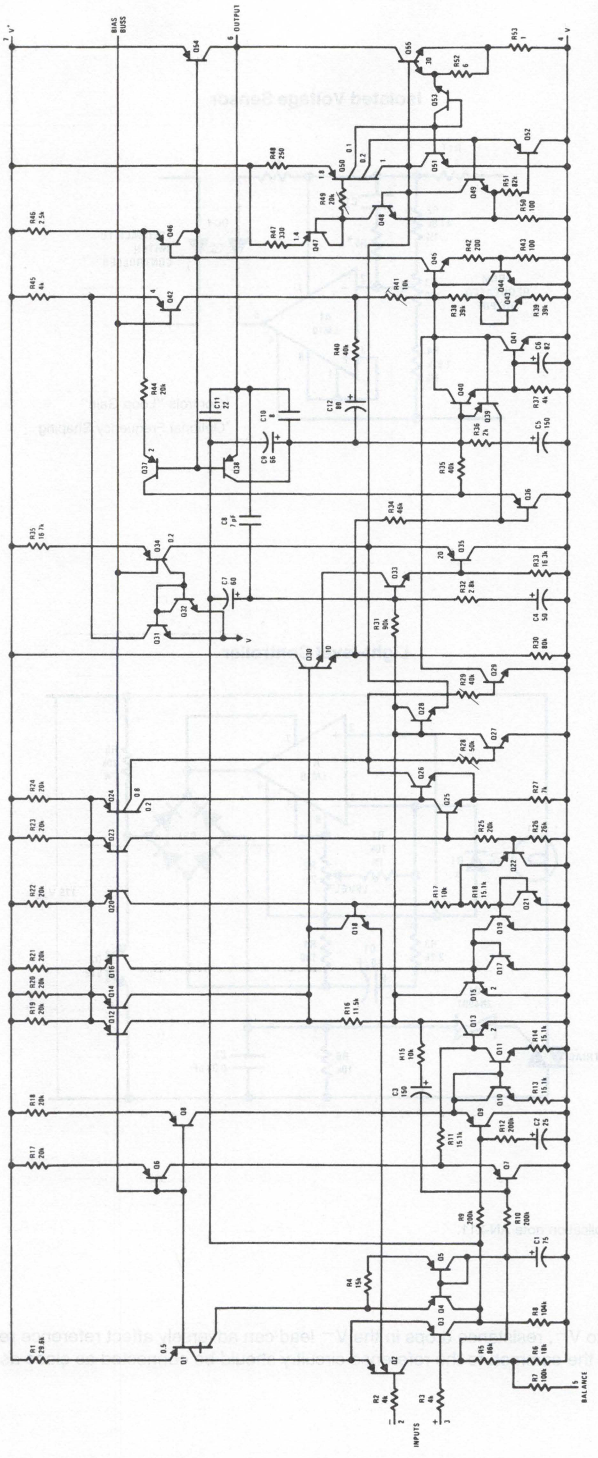
††Circuit descriptions available in application note AN-211.

## Application Hints

With heavy amplifier loading to $V^-$, resistance drops in the $V^-$ lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

## Operational Amplifier Schematic (Pin numbers are for 8-pin packages)


7 V+
BIAS BUSS
6 OUTPUT
4 V−
R53 1
Q55
30
R52 6
Q53
Q52
Q54
R48 250
Q50
Q51
R51 82k
Q49
R50 100
R49 20k
R47 330
Q47
Q48
R46 2.5k
Q46
R42 200
R43 100
Q45
R45 4k
Q42
R41 10k
R38 39k
R39 39k
Q43
Q44
Q41
C6 82
R44 20k
C11 22
C10 8
R40 40k
C12 80
Q40
R37 4k
R36 2k
Q39
C5 150
C9 66
Q37
Q38
R35 40k
Q36
R34 46k
C8 7 pF
R35 16.7k
Q34
Q35
R33 16.3k
C7 60
Q32
Q33
R32 2.8k
C4 50
Q31
R31 90k
R30 80k
Q30
Q29
R29 40k
Q28
Q27
R28 50k
Q26
R24 20k
Q24
R27 7k
R23 20k
Q23
Q25
R25 20k
R26 26k
Q22
R22 20k
Q20
R17 10k
R18 15.1k
Q21
Q18
Q19
R21 20k
Q16
Q17
R20 20k
Q14
Q15
R19 20k
Q12
R16 11.5k
Q13
Q11
R14 15.1k
R15 10k
C3 150
R13 15.1k
R18 20k
Q8
Q9
Q10
R11 15.1k
R12 200k
C2 25
R17 20k
Q6
Q7
R9 200k
R10 200k
C1 75
Q5
R4 15k
Q3
Q4
R8 104k
R1 29.8k
Q1
Q2
R5 86k
R6 18k
R7 100k
R2 4k
R3 4k
− 2
+ 3
INPUTS
5 BALANCE

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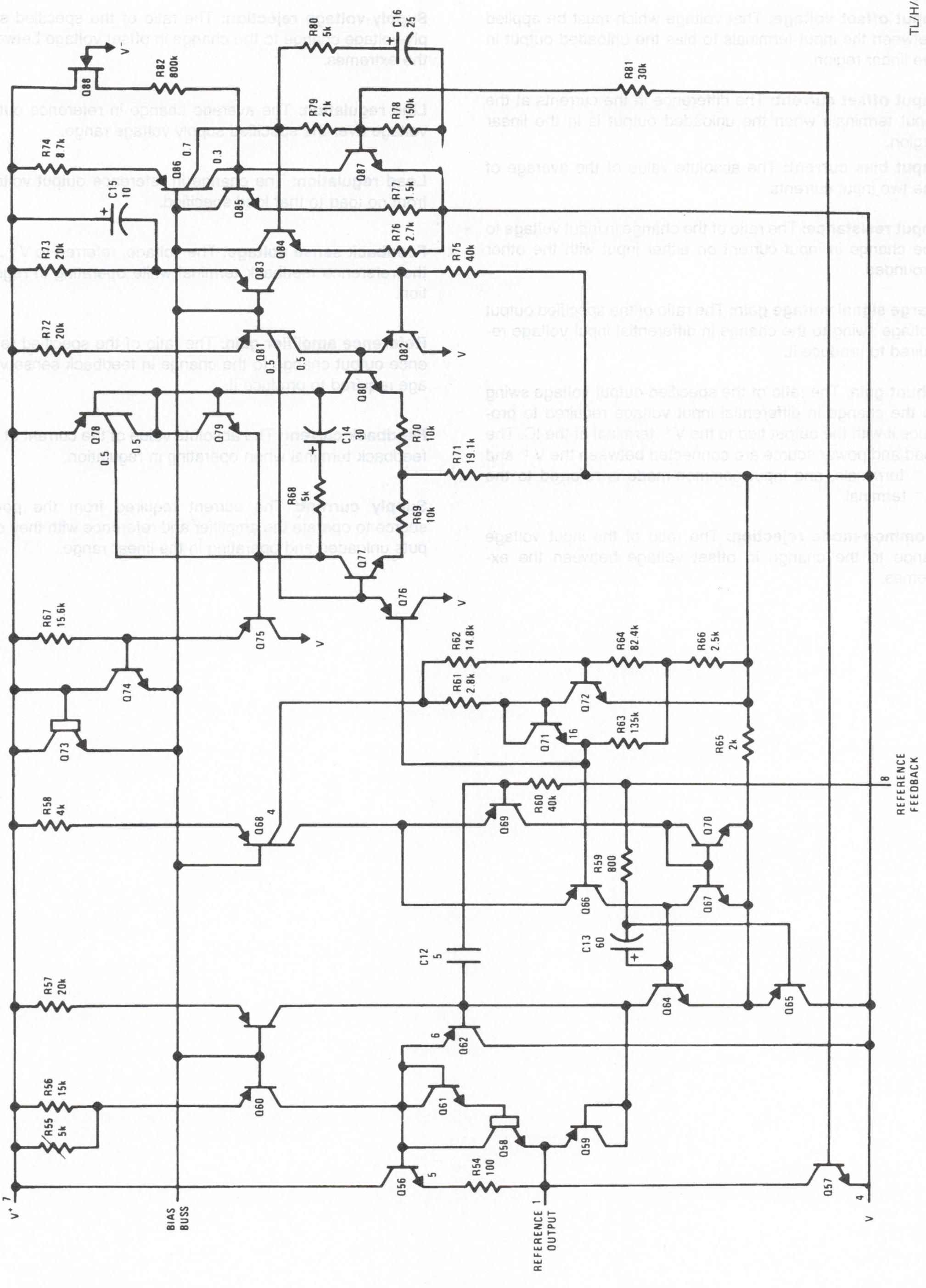
## Reference and Internal Regulator (Pin numbers are for 8-pin packages)


V+ 7
BIAS BUSS
REFERENCE OUTPUT 1
4 V−
8 REFERENCE FEEDBACK
Q88
R82 800k
V−
R80 5k
C16 25
R81 30k
R74 8.7k
Q86 0.7
0.3
R79 21k
R78 150k
Q87
C15 10
Q85
R77 1.5k
R76 2.7k
Q84
R73 20k
Q83
R75 40k
R72 20k
Q81 0.5
Q82
V−
Q80
Q78 0.1
0.5
Q79
C14 30
R70 10k
R71 19.1k
R68 5k
R69 10k
Q77
Q76
V−
R67 15.6k
Q75
V−
Q74
R62 14.8k
R61 2.8k
R64 82.4k
R66 2.5k
Q72
Q71
16
R63 135k
R65 2k
Q73
R58 4k
Q68
4
R60 40k
Q69
Q70
R59 800
Q66
Q67
C12 5
C13 60
R57 20k
Q64
Q65
6
Q62
R56 15k
Q60
Q61
R55 5k
Q58
Q59
Q56
5
R54 100
Q57

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# Definition of Terms

**Input offset voltage:** That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

**Input offset current:** The difference in the currents at the input terminals when the unloaded output is in the linear region.

**Input bias current:** The absolute value of the average of the two input currents.

**Input resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Large signal voltage gain:** The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

**Shunt gain:** The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V$^+$ terminal of the IC. The load and power source are connected between the V$^+$ and V$^-$ terminals, and input common-mode is referred to the V$^-$ terminal.

**Common-mode rejection:** The ratio of the input voltage range to the change in offset voltage between the extremes.

**Supply-voltage rejection:** The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

**Line regulation:** The average change in reference output voltage over the specified supply voltage range.

**Load regulation:** The change in reference output voltage from no load to that load specified.

**Feedback sense voltage:** The voltage, referred to V$^-$, on the reference feedback terminal while operating in regulation.

**Reference amplifier gain:** The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

**Feedback current:** The absolute value of the current at the feedback terminal when operating in regulation.

**Supply current:** The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

**National Semiconductor Corporation**

# LM11/LM11C/LM11CL Operational Amplifiers

## General Description

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been approved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**−55°C to 125°C**) are:

- offset voltage: 100 μV (**200 μV**)
- bias current: 25 pA (**65 pA**)
- offset current: 0.5 pA (**3 pA**)
- temperature drift: **1 μV/°C**
- long-term stability: 10 μV/year

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

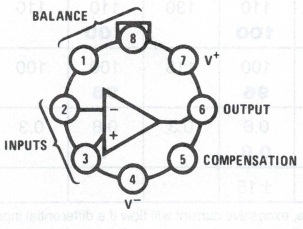
Otherwise, the device is the electrical equivalent of the LM108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obviously applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

## Connection Diagrams

**Metal Can***



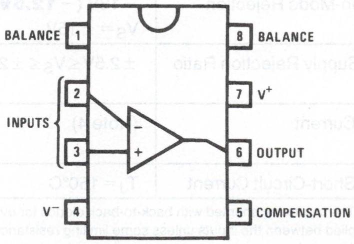
TL/H/5653–1

**Top View**

**Order Number LM11H, LM11CH or LM11CLH**
**See NS Package H08C**

*Case connected to V−

**Mini-DIP**



TL/H/5653–31

**Top View**

**Order Number LM11CN or LM11CLN**
**See NS Package N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

Total Supply Voltage 40V
Input Current (Note 1) ±10 mA
Power Dissipation (Note 2) 500 mW
Output Short-Circuit Duration (Note 3) Indefinite
Storage Temperature Range −65°C to +150°C
Lead Temp. (Soldering, 10 seconds)
(DIP) 260°C
(Metal Can) 300°C
ESD Tolerance
($R_{ZAP}$ = 1.5k, $C_{ZAP}$ = 100 pF) 1500V

## Electrical Characteristics $T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (Note 4)

**(Boldface type refers to limits over temperature range.)**

| Parameter | Conditions | LM11 Typ | LM11 Lim | LM11C Typ | LM11C Lim | LM11CL Typ | LM11CL Lim | Units |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | (Note 4) | 0.1 | 0.3 | 0.2 | 0.6 | 0.5 | 5 | mV |
| | | | **0.6** | | **0.8** | | **6** | mV |
| Input Offset Current | (Note 4) | 0.5 | 10 | 1 | 10 | 4 | 25 | pA |
| | | | **30** | | **20** | | **50** | pA |
| Input Bias Current | (Note 4) | 25 | 50 | 40 | 100 | 70 | 200 | pA |
| | | | **150** | | **150** | | **300** | pA |
| Input Resistance | (Note 4) | $10^{11}$ | | $10^{11}$ | | $10^{11}$ | | Ω |
| Offset Voltage Drift | (Note 4) | 1 | **3** | 2 | **5** | 3 | | μV/°C |
| Offset Current Drift | (Note 4) | 20 | | 10 | | 50 | | fA/°C |
| Bias Current Drift | (Note 4) | 0.5 | **1.5** | 0.8 | **3** | 1.4 | | pA/°C |
| Large Signal Voltage Gain | $V_S$ ±15V, $I_{OUT}$ = ±2 mA | 300 | 100 | 300 | 100 | 300 | 25 | V/mV |
| | $V_{OUT}$ = ±12V(±**11.5V**) | | **50** | | **50** | | **15** | V/mV |
| | $V_S$ = ±15V, $I_{OUT}$ = ±0.5 mA | 1200 | 250 | 1200 | 250 | 800 | 50 | V/mV |
| | $V_{OUT}$ ±12V | | **100** | | **100** | | **30** | V/mV |
| Common-Mode Rejection | −13V (−**12.5V**) ≤ $V_{CM}$ ≤ 14V | 130 | 110 | 130 | 110 | 110 | 96 | dB |
| | $V_S$ = ±15V | | **100** | | **100** | | **90** | dB |
| Power Supply Rejection Ratio | ±2.5V ≤ $V_S$ ≤ ±20V | 118 | 100 | 118 | 100 | 100 | 84 | dB |
| | | | **96** | | **96** | | **80** | dB |
| Supply Current | (Note 4) | 0.3 | 0.6 | 0.3 | 0.8 | 0.3 | 0.8 | mA |
| | | | **0.8** | | **1** | | **1** | mA |
| Output Short-Circuit Current | $T_J$ = 150°C | | ±15 | | | | | mA |

**Note 1:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

**Note 2:** The maximum operating-junction temperature is 150°C for the LM11 and 85°C for the LM11C(L). Devices must be derated at 150°C/W for the metal can and 155°C/W for the plastic DIP. The metal can has a thermal resistance of 45°C/W for the junction to case if a heat sink is used.

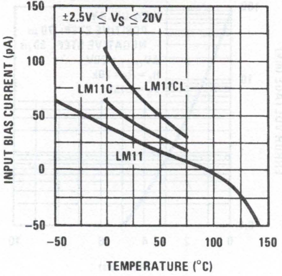
**Note 3:** Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

**Note 4:** These specifications apply for $V^- + 2V$ (**2.5V**) $\le V_{CM} \le V^+ - 1V$ and $\pm 2.5V \le V_S \le \pm 20V$, unless otherwise specified. Normal typeface indicates 25°C limits. **Boldface type indicates limits for full-temperature range operation.** This is $-55°C \le T_J \le 125°C$ for the LM11 and $0°C \le T_J \le 70°C$ for the LM11C(L).

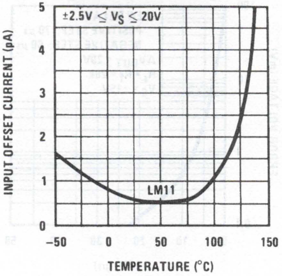
**Note 5:** Refer to RETS11X for LM11 military specifications.

## Typical Characteristics

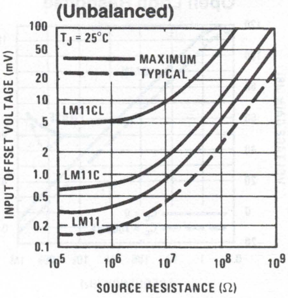
**Input Bias Current**



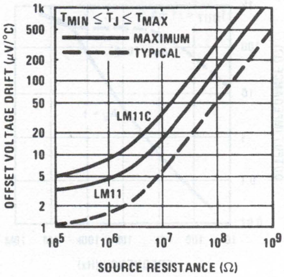
**Input Offset Current**



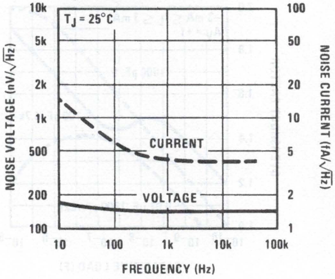
**Offset: Single Source Resistor (Unbalanced)**



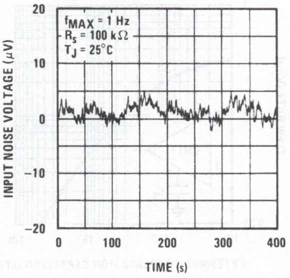
**Drift: Single Source Resistor (Unbalanced)**



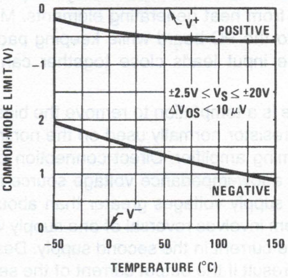
**Input Noise**



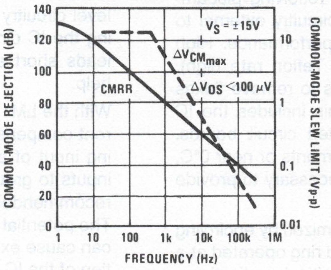
**Input Noise**



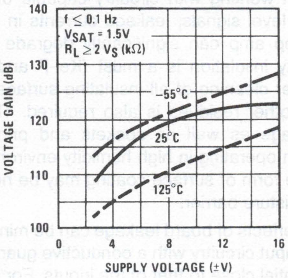
**Common-Mode Limits**



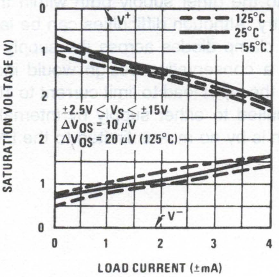
**Common-Mode Rejection**



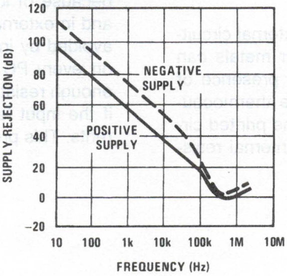
**Large Signal Voltage Gain**



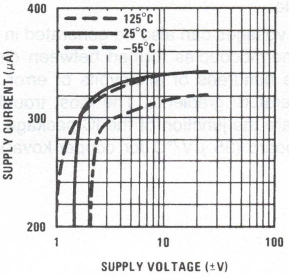
**Output Saturation Threshold**



**Supply Rejection**



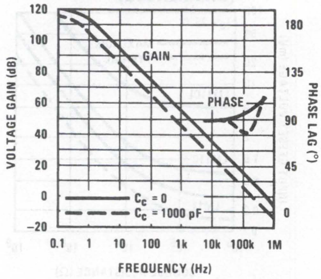
**Supply Current**



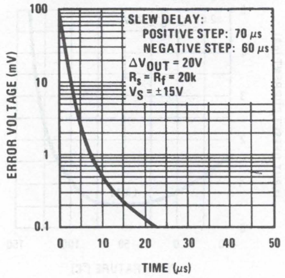
TL/H/5653–2

## Typical Characteristics (Continued)

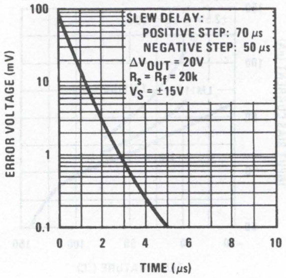
### Open Loop Response



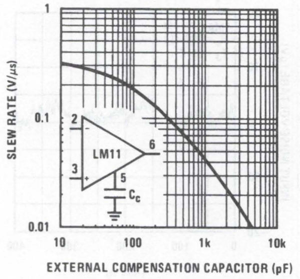
### Follower Final Settling Time



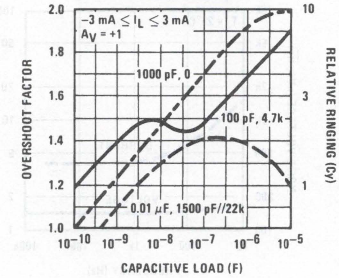
### Inverter Final Settling Time



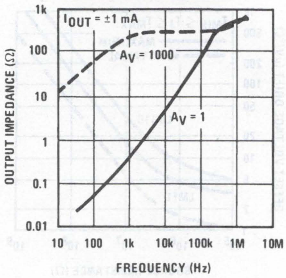
### Slew Rate



### Stability With Over-Compensation



### Closed Loop Output Impedance



TL/H/5653-3

## Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 μV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

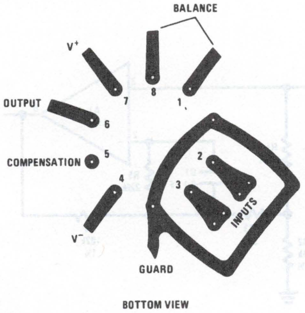
With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the noninverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 μF bypass on the supply buss.

Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

## Application Hints (Continued)

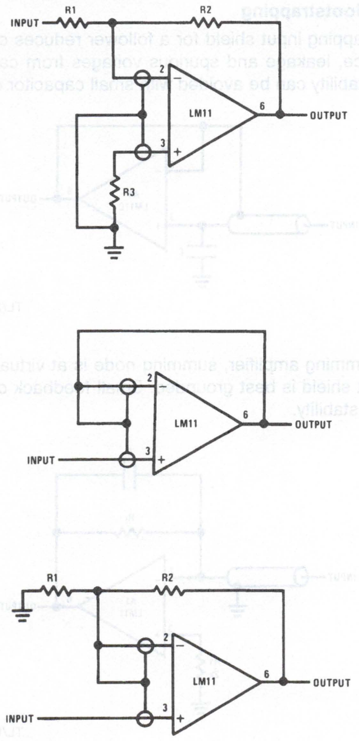
### Input Guarding

Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.


BALANCE
V+
OUTPUT
7
8
1
6
COMPENSATION
5
4
2
3
INPUTS
V−
GUARD
BOTTOM VIEW

TL/H/5653-4

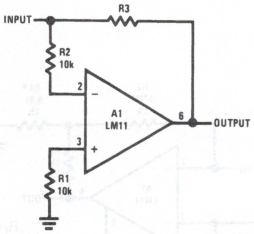
Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are here.


INPUT
R1
R2
2
LM11
6
OUTPUT
3
R3
2
LM11
6
OUTPUT
INPUT
3
R1
R2
2
LM11
6
OUTPUT
INPUT
3

TL/H/5653-7

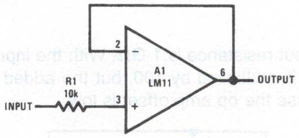
### Input Protection

Current is limited by R2 even when input is connected to voltage source outside common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.


INPUT
R3
R2
10k
2
A1
LM11
6
OUTPUT
3
R1
10k

TL/H/5653-5

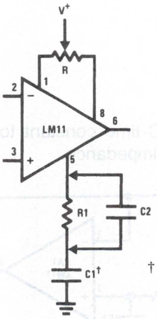
Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.


2
A1
LM11
6
OUTPUT
R1
10k
INPUT
3

TL/H/5653-6

### Balancing And Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.


V+
R
2
1
8
6
LM11
3
5
R1
C2
C1†

† See stability with over-compensation curve

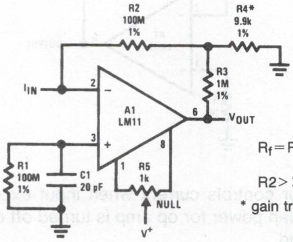
TL/H/5653-8

| min. adj range | R |
|---|---|
| ±4 mV | 100 kΩ |
| ±2 | 10k |
| ±0.8 | 3k |
| ±0.4 | 1k |

## Application Hints (Continued)

### Resistance Multiplication

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.


R2
100M
1%
R4*
9.9k
1%
R3
1M
1%
$I_{IN}$
2
A1
LM11
6
$V_{OUT}$
3
8
R1
100M
1%
C1
20 pF
1
R5
1k
NULL
$V^+$

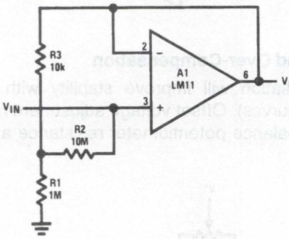
$$R_f = R2\left(1+\frac{R3}{R4}\right)$$

$$R2 >> R3 \| R4$$

* gain trim

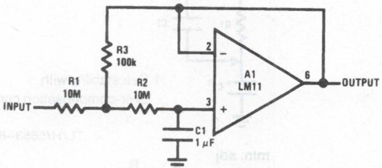
TL/H/5653-9

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.


R3
10k
2
A1
LM11
6
$V_{OUT}$
$V_{IN}$
3
R2
10M
R1
1M

TL/H/5653-11

This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.

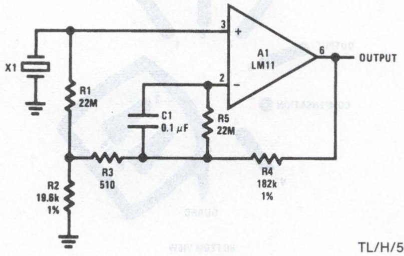

R3
100k
2
A1
LM11
6
OUTPUT
R1
10M
R2
10M
INPUT
3
C1
1 µF

TL/H/5653-13

$$\tau = \frac{R1C}{R3}(R2+R3)$$

$$\Delta V_{OUT} = \frac{R1+R3}{R3}(I_B R2 + V_{OS})$$

A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.

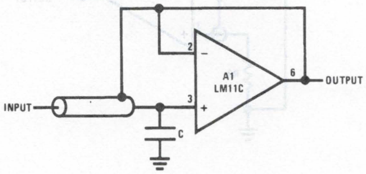

X1
3
+
A1
LM11
6
OUTPUT
2
−
R1
22M
C1
0.1 µF
R5
22M
R3
510
R4
182k
1%
R2
19.6k
1%

TL/H/5653-10

$$R_{IN} = R1\left(1+\frac{R2}{R3}\right) \quad A_V = \frac{R2+R3+R4}{R2+R3}$$

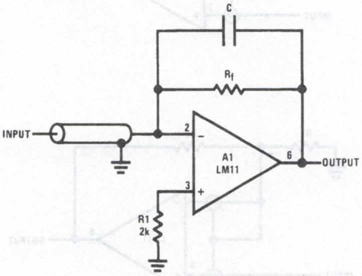
### Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.


2
−
A1
LM11C
6
OUTPUT
INPUT
3
+
C

TL/H/5653-12

With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

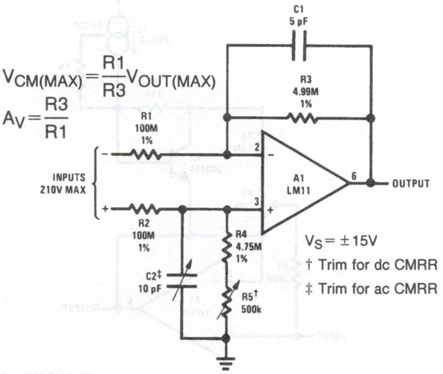

C
$R_f$
INPUT
2
−
A1
LM11
6
OUTPUT
3
+
R1
2k

TL/H/5653-14

## Application Hints (Continued)

### Differential Amplifiers

This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.


C1
5 pF
R3
4.99M
1%
R1
100M
1%
INPUTS
210V MAX
R2
100M
1%
C2‡
10 pF
R4
4.75M
1%
R5†
500k
A1
LM11
OUTPUT
2
3
6
−
+

$$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$$

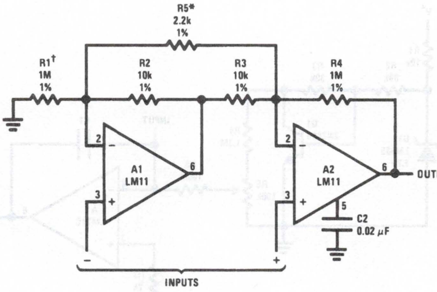
$$A_V = \frac{R3}{R1}$$

$V_S = \pm 15V$

† Trim for dc CMRR

‡ Trim for ac CMRR

Two op-amp instrumentation amplifier has poor ac common mode rejection. This can be improved at the expense of differential bandwidth with C2.


R5*
2.2k
1%
R1†
1M
1%
R2
10k
1%
R3
10k
1%
R4
1M
1%
A1
LM11
A2
LM11
C2
0.02 μF
OUTPUT
INPUTS
2
3
6
5
−
+

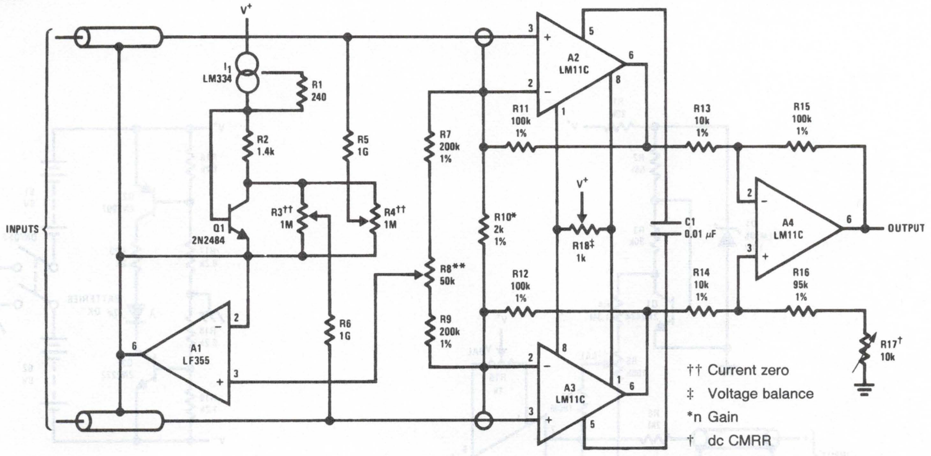
* Gain set

† Trim for dc CMRR

$f_o = 10$ Hz

TL/H/5653–15

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.


V+
I1
LM334
R1
240
R2
1.4k
R5
1G
Q1
2N2484
R3††
1M
R4††
1M
R6
1G
A1
LF355
INPUTS
R7
200k
1%
R8**
50k
R9
200k
1%
R10*
2k
1%
R11
100k
1%
R12
100k
1%
R18‡
1k
V+
A2
LM11C
A3
LM11C
C1
0.01 μF
R13
10k
1%
R15
100k
1%
R14
10k
1%
R16
95k
1%
R17†
10k
A4
LM11C
OUTPUT
1
2
3
5
6
8

†† Current zero

‡ Voltage balance

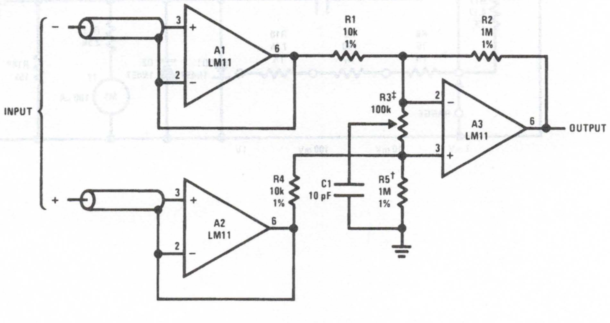
*n Gain

† dc CMRR

** ac CMRR

TL/H/5653–16

For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.


INPUT
−
+
A1
LM11
A2
LM11
R1
10k
1%
R2
1M
1%
R3‡
100k
R4
10k
1%
C1
10 pF
R5†
1M
1%
A3
LM11
OUTPUT
2
3
6

R1 = R3; R2 = R4

$$A_V = \frac{R2}{R1}$$

†Trim for dc CMRR

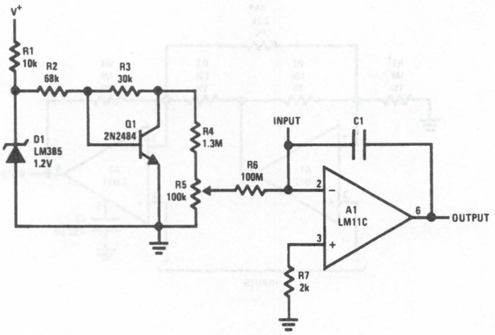
‡Set for ac CMRR

TL/H/5653–17

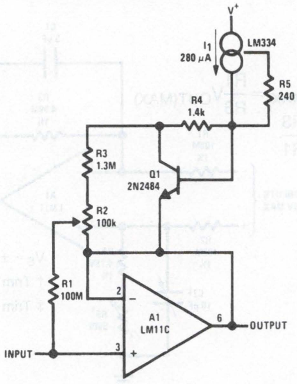
## Application Hints (Continued)

### Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.


V+
R1
10k
R2
68k
R3
30k
Q1
2N2484
D1
LM385
1.2V
R4
1.3M
R5
100k
R6
100M
INPUT
C1
2
3
6
A1
LM11C
OUTPUT
R7
2k

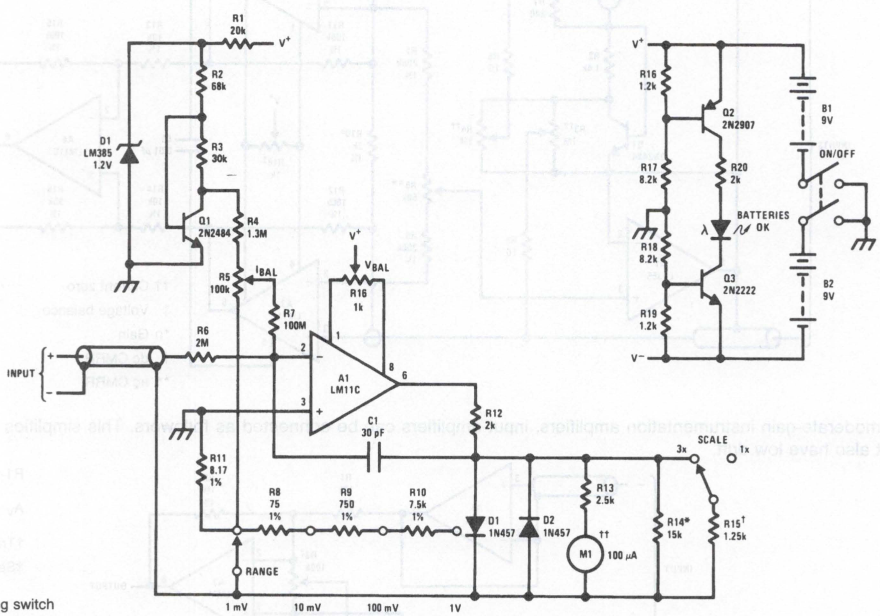
This circuit shows how bias current compensation can be used on a voltage follower.


V+
I1
280 μA
LM334
R5
240
R4
1.4k
R3
1.3M
Q1
2N2484
R2
100k
R1
100M
2
3
6
A1
LM11C
INPUT
OUTPUT

TL/H/5653-18

### Voltmeter

High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.


R1
20k
V+
R2
68k
D1
LM385
1.2V
R3
30k
Q1
2N2484
R4
1.3M
R5
100k
IBAL
V+
VBAL
R16
1k
R7
100M
R6
2M
INPUT
+
−
1
2
3
8
6
A1
LM11C
C1
30 pF
R12
2k
R11
8.17
1%
R8
75
1%
R9
750
1%
R10
7.5k
1%
D1
1N457
D2
1N457
R13
2.5k
††
M1
100 μA
R14*
15k
R15†
1.25k
SCALE
3x
1x
RANGE
1 mV
10 mV
100 mV
1V
V+
R16
1.2k
Q2
2N2907
R17
8.2k
R20
2k
BATTERIES
OK
R18
8.2k
Q3
2N2222
R19
1.2k
V−
B1
9V
ON/OFF
B2
9V

* 1×scale calibrate

† 3×scale calibrate

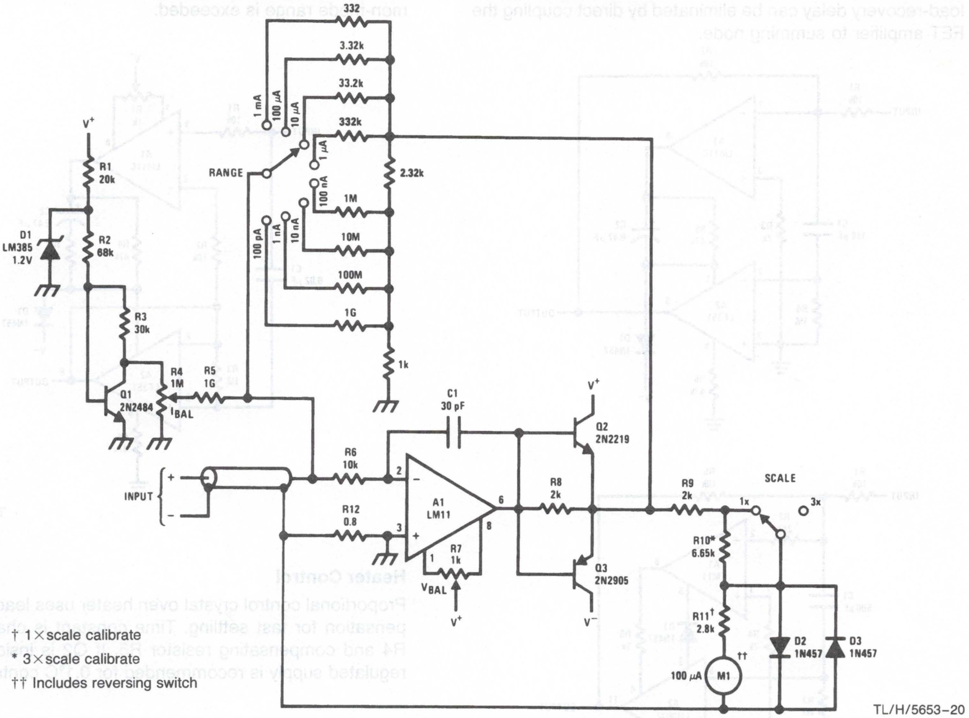
†† Includes reversing switch

TL/H/5653-19

## Application Hints (Continued)

### Ammeter

Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



332
3.32k
33.2k
332k
2.32k
1M
10M
100M
1G
1k
1 mA
100 μA
10 μA
1 μA
100 nA
10 nA
1 nA
100 pA
RANGE
V+
R1
20k
D1
LM385
1.2V
R2
68k
R3
30k
Q1
2N2484
R4
1M
R5
1G
I_BAL
INPUT
+
−
R6
10k
R12
0.8
C1
30 pF
A1
LM11
2
3
6
8
1
R7
1k
V_BAL
V+
Q2
2N2219
Q3
2N2905
V+
V−
R8
2k
R9
2k
SCALE
1x
3x
R10*
6.65k
R11†
2.8k
D2
1N457
D3
1N457
††
100 μA
M1

† 1 × scale calibrate

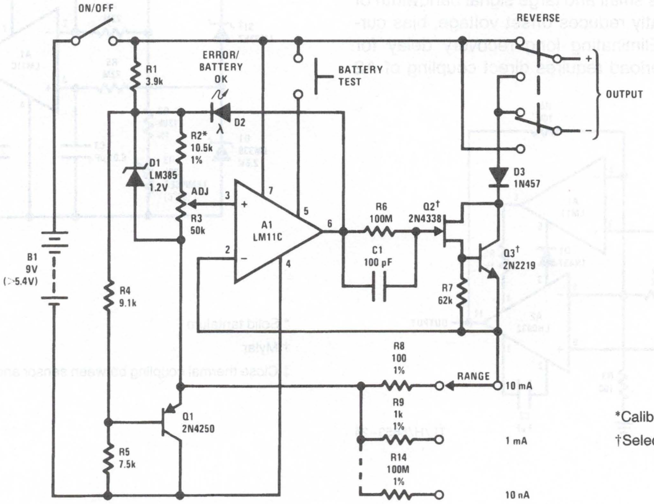
* 3 × scale calibrate

†† Includes reversing switch

TL/H/5653–20

### Current Source

Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



ON/OFF
R1
3.9k
ERROR/
BATTERY
OK
D2
BATTERY
TEST
REVERSE
+
−
OUTPUT
R2*
10.5k
1%
D1
LM385
1.2V
ADJ
R3
50k
B1
9V
(>5.4V)
3
7
5
6
2
4
A1
LM11C
R6
100M
Q2†
2N4338
C1
100 pF
Q3†
2N2219
D3
1N457
R7
62k
R4
9.1k
R8
100
1%
RANGE
10 mA
R9
1k
1%
1 mA
R14
100M
1%
10 nA
Q1
2N4250
R5
7.5k

*Calibrate range

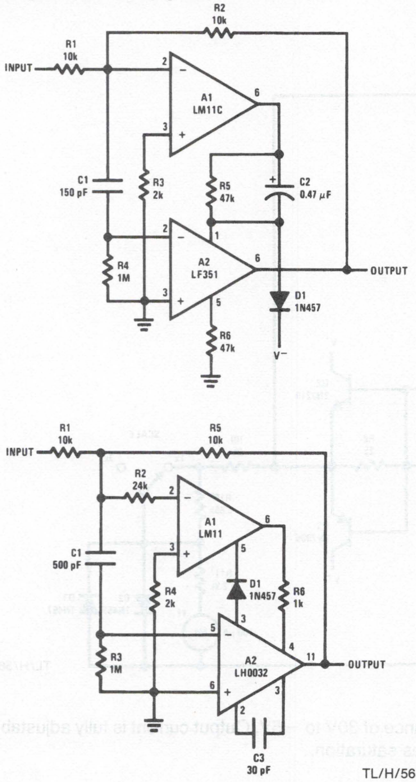
†Select for $I_{CBO} \leq 100$ pA

TL/H/5653–21

## Application Hints (Continued)

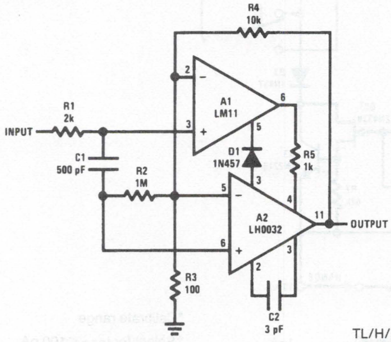
### Fast Amplifiers

These inverters have bias current and offset voltage of LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 $\mu$S. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.


R2
10k
R1
10k
INPUT
A1
LM11C
C1
150 pF
R3
2k
R5
47k
C2
0.47 µF
R4
1M
A2
LF351
OUTPUT
D1
1N457
R6
47k
V−
R1
10k
R5
10k
INPUT
R2
24k
A1
LM11
C1
500 pF
D1
1N457
R6
1k
R4
2k
R3
1M
A2
LH0032
OUTPUT
C3
30 pF

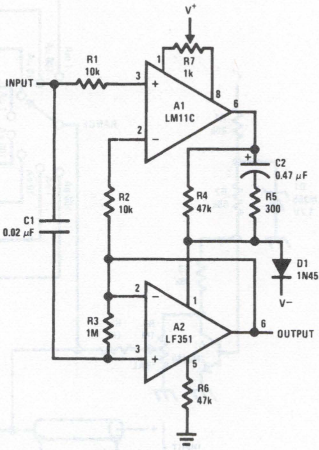
TL/H/5653-22

This 100× amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.


R4
10k
A1
LM11
R1
2k
INPUT
C1
500 pF
R2
1M
D1
1N457
R5
1k
A2
LH0032
OUTPUT
R3
100
C2
3 pF

TL/H/5653-24

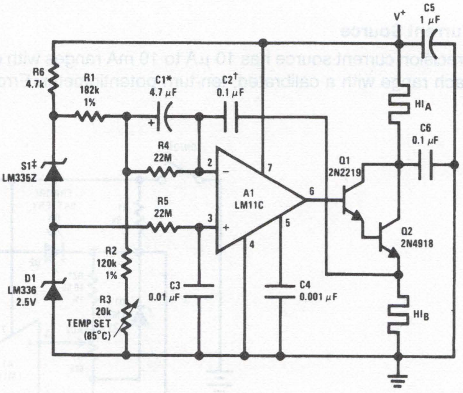
Follower has 10 $\mu$S setting to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.


V+
R7
1k
R1
10k
INPUT
A1
LM11C
C2
0.47 µF
R2
10k
R4
47k
R5
300
C1
0.02 µF
D1
1N457
V−
R3
1M
A2
LF351
OUTPUT
R6
47k

TL/H/5653-23

### Heater Control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.


V+
C5
1 µF
R6
4.7k
R1
182k
1%
C1*
4.7 µF
C2†
0.1 µF
HIA
C6
0.1 µF
S1‡
LM335Z
R4
22M
Q1
2N2219
R5
22M
A1
LM11C
Q2
2N4918
R2
120k
1%
D1
LM336
2.5V
R3
20k
TEMP SET
(85°C)
C3
0.01 µF
C4
0.001 µF
HIB

TL/H/5653-25

* Solid tantalum

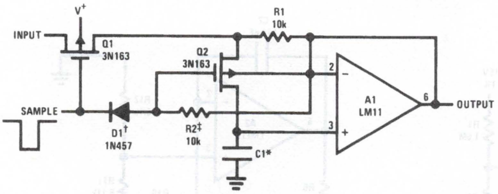
† Mylar

‡ Close thermal coupling between sensor and oven shell is recommended.

## Application Hints (Continued)

### Leakage Isolation

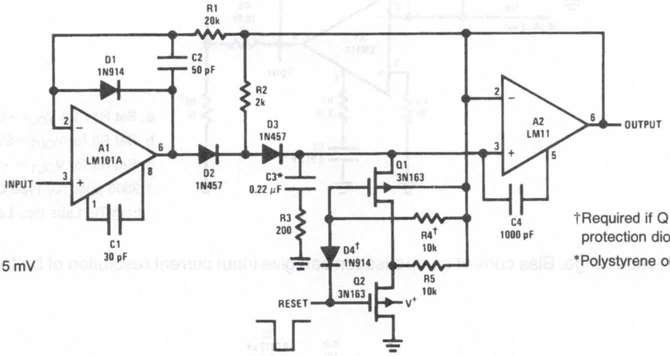
Switch leakage in this sample and hold does not reach storage capacitor.


V+
INPUT
Q1
3N163
SAMPLE
D1†
1N457
Q2
3N163
R2‡
10k
R1
10k
C1*
2
3
A1
LM11
6
OUTPUT

*Polystyrene or Teflon
†Required if protected-gate switch is used

TL/H/5653–26

A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

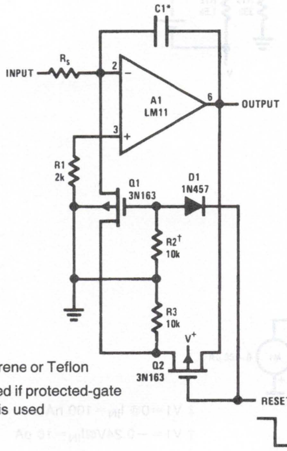

R1
20k
D1
1N914
C2
50 pF
R2
2k
2
A1
LM101A
6
3
8
1
INPUT
C1
30 pF
D2
1N457
D3
1N457
C3*
0.22 μF
R3
200
D4†
1N914
Q1
3N163
R4†
10k
R5
10k
Q2
3N163
V+
RESET
2
3
A2
LM11
6
5
OUTPUT
C4
1000 pF

300 μS min single pulse
200 μS min repetitive pulse
300 Hz max sine wave error < 5 mV

†Required if Q1 has gate-protection diode
*Polystyrene or Teflon

TL/H/5653–27

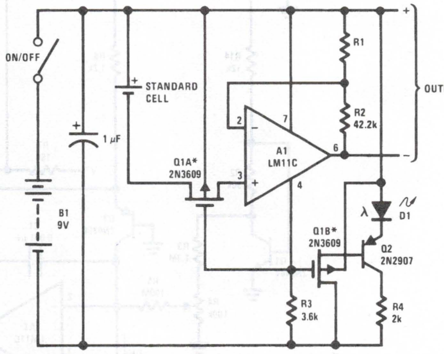
Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.


C1*
INPUT
$R_S$
2
3
A1
LM11
6
OUTPUT
R1
2k
Q1
3N163
D1
1N457
R2†
10k
R3
10k
V+
Q2
3N163
RESET

*Polystyrene or Teflon
†Required if protected-gate switch is used

### Standard-Cell Buffer

Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.


ON/OFF
+
STANDARD
CELL
+
1 μF
B1
9V
Q1A*
2N3609
2
3
7
4
6
A1
LM11C
R1
R2
42.2k
+
−
OUTPUT
λ
D1
Q1B*
2N3609
Q2
2N2907
R3
3.6k
R4
2k

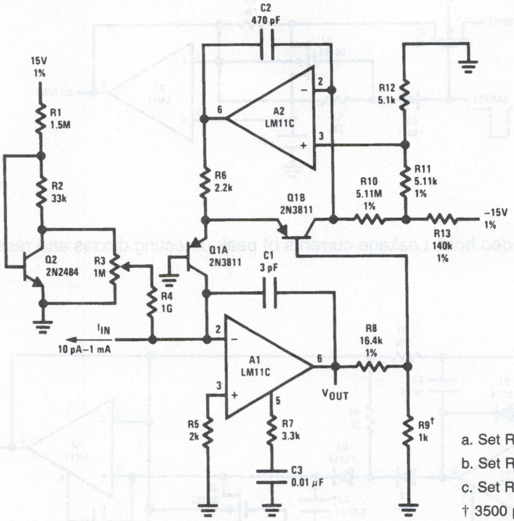
TL/H/5653–28

*Cannot have gate protection diode; $V_{TH} > V_{OUT}$

## Application Hints (Continued)

### Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs, time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.


C2
470 pF
15V
1%
R1
1.5M
R2
33k
Q2
2N2484
R3
1M
R4
1G
A2
LM11C
R6
2.2k
Q1A
2N3811
Q1B
2N3811
C1
3 pF
R12
5.1k
R11
5.11k
1%
R10
5.11M
1%
R13
140k
1%
−15V
1%
I_IN
10 pA–1 mA
A1
LM11C
R8
16.4k
1%
V_OUT
R9†
1k
R5
2k
R7
3.3k
C3
0.01 μF

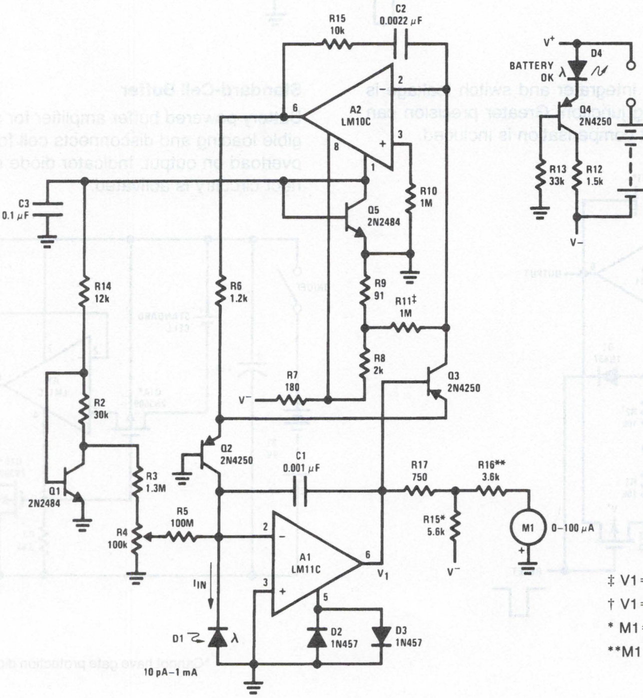
a. Set R11 for $V_{OUT}=0$ at $I_{IN}=100$ nA

b. Set R8 for $V_{OUT}=3V$ at $I_{IN}=100$ μA

c. Set R3 for $V_{OUT}=-4V$ at $I_{IN}=10$ pA

† 3500 ppM/°C. Type Q81 available from Tel Labs Inc., Londonderry, N.H.

Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.


R15
10k
C2
0.0022 μF
A2
LM10C
V+
BATTERY OK
D4
Q4
2N4250
B1
9V
R13
33k
R12
1.5k
V−
C3
0.1 μF
R10
1M
Q5
2N2484
R14
12k
R6
1.2k
R9
91
R11‡
1M
R8
2k
Q3
2N4250
R7
180
V−
R2
30k
Q2
2N4250
C1
0.001 μF
R17
750
R16**
3.6k
Q1
2N2484
R3
1.3M
R5
100M
R15*
5.6k
V−
M1
0–100 μA
R4
100k
A1
LM11C
V1
I_IN
D1
D2
1N457
D3
1N457
10 pA–1 mA

‡ V1 = 0@ $I_{IN}=100$ nA

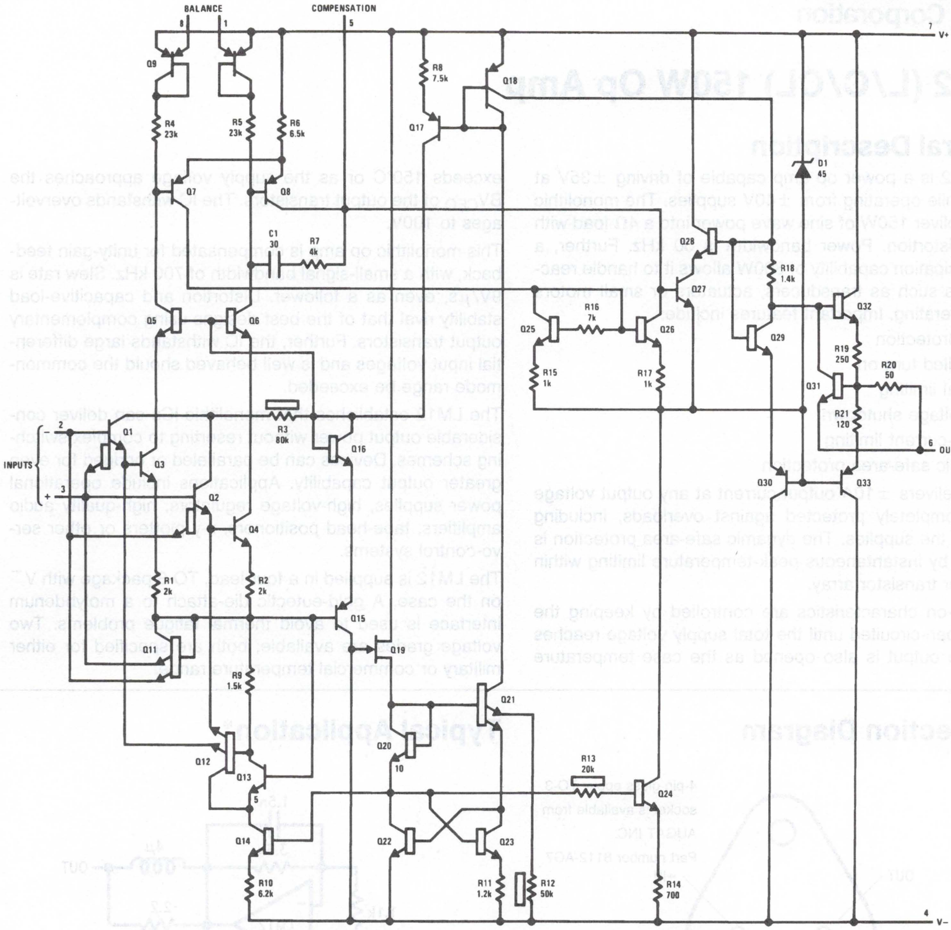
† V1 = −0.24V@$I_{IN}=10$ pA

* M1 = 0@$I_{IN}=10$ pA

**M1 = $f_S$@$I_{IN}=1$ mA

TL/H/5653–29

## Schematic Diagram


BALANCE
8
1
COMPENSATION
5
7
V+
Q9
R8
7.5k
Q18
R4
23k
R5
23k
R6
6.5k
Q17
D1
45
Q7
Q8
C1
30
R7
4k
Q28
R18
1.4k
Q27
Q5
Q6
R16
7k
Q32
Q25
Q26
Q29
R15
1k
R17
1k
R19
250
R20
50
Q31
R21
120
R3
80k
2
−
Q1
INPUTS
+
3
Q3
Q16
6
OUTPUT
Q30
Q33
Q2
Q4
R1
2k
R2
2k
Q15
Q11
Q19
R9
1.5k
Q21
Q20
10
R13
20k
Q12
Q13
Q24
5
Q14
Q22
Q23
R10
6.2k
R11
1.2k
R12
50k
R14
700
4
V−

TL/H/5653-30

## Definition of Terms

**Input offset voltage:** That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

**Input offset current:** The difference in the currents at the input terminals when the output is unloaded in the linear region.

**Input bias current:** The absolute value of the average of the two input currents.

**Input resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Large signal voltage gain:** The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

**Common-mode rejection:** The ratio of the input voltage range to the change in offset voltage between the extremes.

**Temperature drift:** The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

**Power Supply Rejection Ratio:** The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

**Supply current:** The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor Corporation

**PRELIMINARY**

# LM12 (L/C/CL) 150W Op Amp

## General Description

The LM12 is a power op amp capable of driving ±35V at ±10A while operating from ±40V supplies. The monolithic IC can deliver 150W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

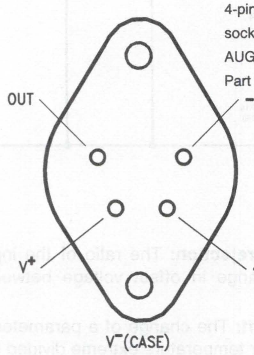
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150°C or as the supply voltage approaches the $BV_{CEO}$ of the output transistors. The IC withstands overvoltages to 100V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/μs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with $V^-$ on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. Two voltage grades are available; both are specified for either military or commercial temperature range.

## Connection Diagram

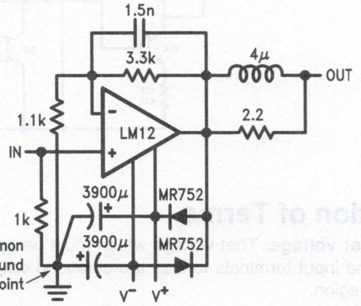


4-pin glass epoxy TO-3 socket is available from AUGAT INC. Part number 8112-AG7

TL/H/8704–1

**Bottom View**

## Typical Application*



TL/H/8704–2

*Low distortion (0.01%) audio amplifier

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | | |
|---|---|---|
| total supply voltage | LM12/LM12C | 100V |
| | LM12L/LM12CL | 80V |
| input voltage | | Note 1 |
| output current | | internally limited |
| junction temperature | | Note 2 |
| storage temperature range | | −65°C to 150°C |
| lead temperature (soldering, 10 seconds) | | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ 25°C | LM12 LM12L | LM12C LM12CL | Units |
|---|---|---|---|---|---|
| | | | Limits | Limits | |
| input offset voltage | $\pm 10V \le V_S \le \pm 0.5 V_{MAX}$, $V_{CM} = 0$ | 2 | 7/**15** | 15/**20** | mV (max) |
| input bias current | $V^- + 4V \le V_{CM} \le V^+ - 2V$ | 0.15 | 0.3/**1.0** | 0.7/**1.0** | μA (max) |
| input offset current | $V^- + 4V \le V_{CM} \le V^+ - 2V$ | 0.03 | 0.1/**0.3** | 0.2/**0.3** | μA (max) |
| common mode rejection | $V^- + 4V \le V_{CM} \le V^+ - 2V$ | 86 | 75/**70** | 70/**65** | dB (min) |
| power supply rejection | $V^+ = 0.5 V_{MAX}$, $-6V \ge V^- \ge -0.5 V_{MAX}$<br>$V^- = -0.5 V_{MAX}$, $6V \le V^+ \le 0.5 V_{MAX}$ | 90<br>110 | 75/**70**<br>80/**75** | 70/**65**<br>75/**70** | dB (min)<br>dB (min) |
| output saturation threshold | $t_{ON} = 1$ ms, $\Delta V_{IN} = 5$ (**10**) mV, $I_{OUT} = 1A$<br>8A<br>10A | 1.8<br>4<br>5 | 2.2/**2.5**<br>5/**7**<br>8 | 2.2/**2.5**<br>5/**7** | V (max)<br>V (max)<br>V (max) |
| large signal voltage gain | $t_{ON} = 2$ ms, $V_{SAT} = 2V$, $I_{OUT} = 0$<br>$V_{SAT} = 8V$, $R_L = 4\Omega$ | 100<br>50 | 50/**30**<br>20/**15** | 30/**20**<br>15/**10** | V/mV (min)<br>V/mV (min) |
| thermal gradient feedback | $P_{DISS} = 50W$, $t_{ON} = 65$ ms | 30 | 50 | 100 | μV/W (max) |
| output-current limit | $t_{ON} = 10$ ms, $V_{DISS} = 10V$<br>$t_{ON} = 100$ ms, $V_{DISS} = 58V$<br><br>LM12/LM12C $t_{ON} = 100$ ms, $V_{DISS} = 78V$ | 13<br>1.5<br>1.5<br>0.7 | 16<br>1.0/**0.6**<br>1.7<br>0.6/**0.4** | 16<br>0.9/**0.6**<br>1.7<br>0.5/**0.35** | A (max)<br>A (min)<br>A (max)<br>A (min) |
| power dissipation rating | $t_{ON} = 100$ mS, $V_{DISS} = 20V$<br>$V_{DISS} = 58V$ | 100<br>80 | 90/**40**<br>58/**35** | 80/**55**<br>52/**35** | W (min)<br>W (min) |
| dc thermal resistance | (Note 4) $V_{DISS} = 20V$<br>$V_{DISS} = 58V$ | 2.3<br>2.7 | 2.6<br>4.0 | 2.9<br>4.5 | °C/W (max)<br>°C/W (max) |
| ac thermal resistance | (Note 4) | 1.6 | 1.9 | 2.1 | °C/W (max) |
| supply current | $V_{OUT} = 0$, $I_{OUT} = 0$ | 60 | 80/**90** | 120/**140** | mA (max) |

**Note 1.** Neither input should exceed the supply voltage by more than 50 volts nor should the voltage between one input and any other terminal exceed 80 volts for the LM12/LM12C or 60 volts for the LM12L/LM12CL.

**Note 2.** Operating junction temperature is internally limited near 225°C within the power transistor and 160°C for the control circuitry.

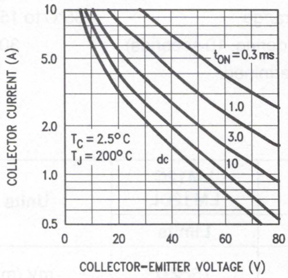
**Note 3.** The supply voltage is ±40V ($V_{MAX} = 80V$) for the LM12/LM12C and ±30V ($V_{MAX} = 60V$) for the LM12L/LM12CL, unless otherwise specified. The voltage across the conducting output transistor (supply to output) is $V_{DISS}$ and internal power dissipation is $P_{DISS}$. Temperature range is $-55°C \le T_C \le 125°C$ for the LM12/LM12L and $0°C \le T_C \le 70°C$ for LM12C/LM12CL, where $T_C$ is the case temperature. Standard typeface indicates limits at 25°C **while boldface type refers to limits or special conditions over full temperature range.** With no heat sink, the package will heat at a rate of 35°C/sec per 100W of internal dissipation.

**Note 4.** This thermal resistance is based upon a peak temperature of 200°C in the center of the power transistor and a case temperature of 25°C measured at the center of the package bottom. The maximum junction temperature of the control circuitry can be estimated based upon a dc thermal resistance of 0.9°C/W or an ac thermal resistance of 0.6°C/W for any operating voltage.

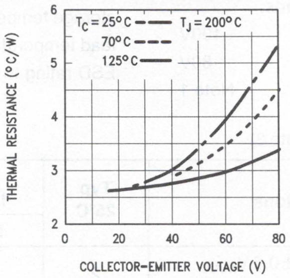
**Although the output and supply leads are resistant to electrostatic discharges from handling, the input leads are not. The part should be treated accordingly.**

## Output-Transistor Ratings (guaranteed)†

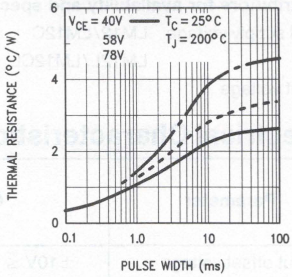
safe area



dc thermal resistance



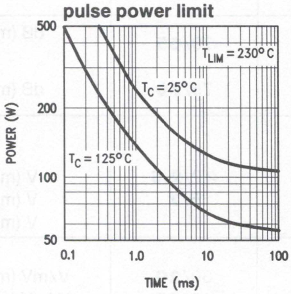
pulse thermal resistance



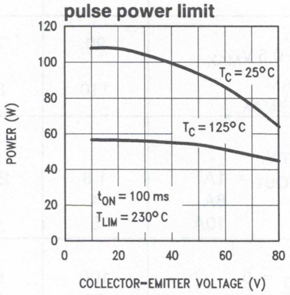
TL/H/8704-3

## Typical Performance Characteristics

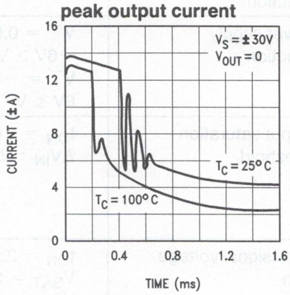
pulse power limit



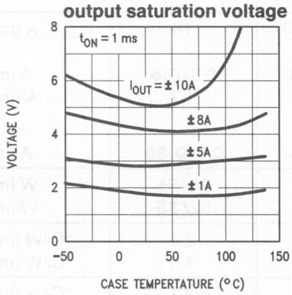
pulse power limit



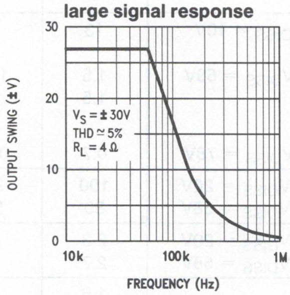
peak output current



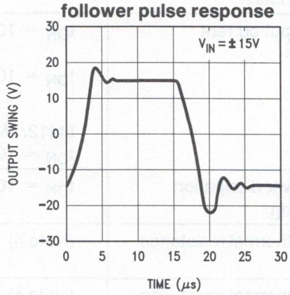
output saturation voltage



large signal response



follower pulse response

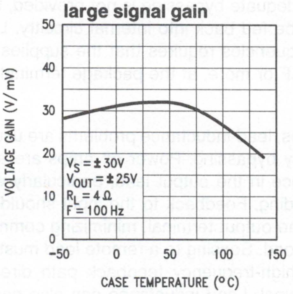


TL/H/8704-4

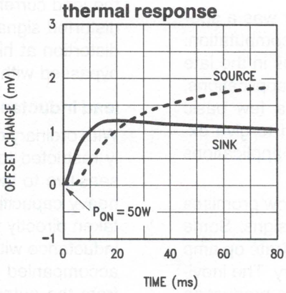
†LM12/LM12L. The power ratings of the LM12C/LM12CL are 10-percent less at 20V and 15-percent less at 60V, with a corresponding increase in thermal resistance and decrease in safe area current.

## Typical Performance Characteristics (Continued)

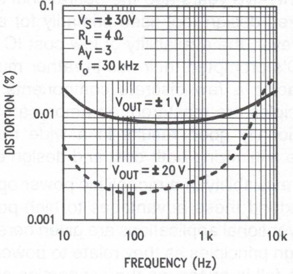
**large signal gain**



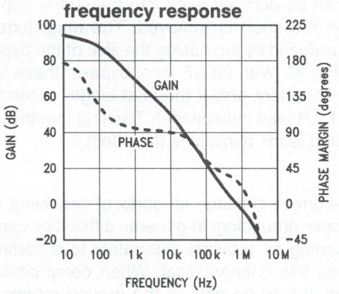
**thermal response**



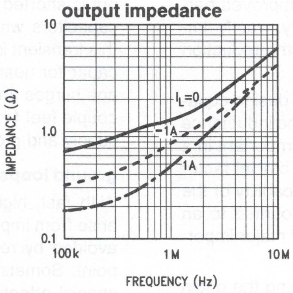
**total harmonic distortion**



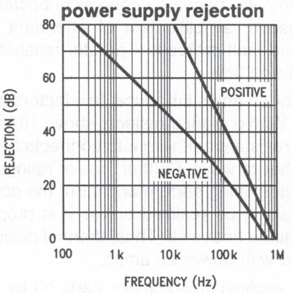
**frequency response**



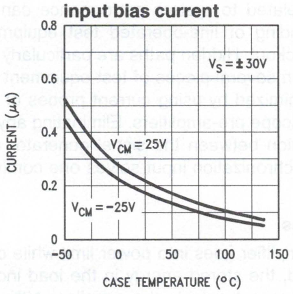
**output impedance**



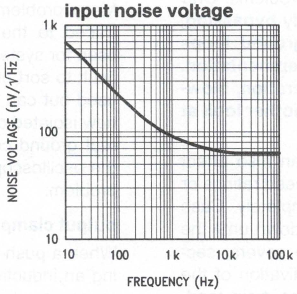
**power supply rejection**



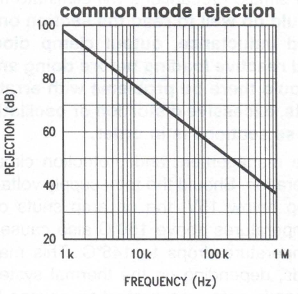
**input bias current**



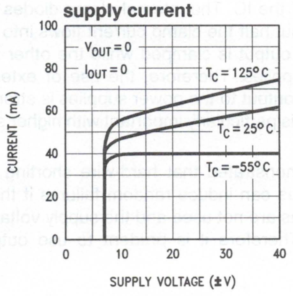
**input noise voltage**



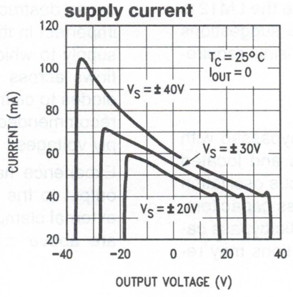
**common mode rejection**



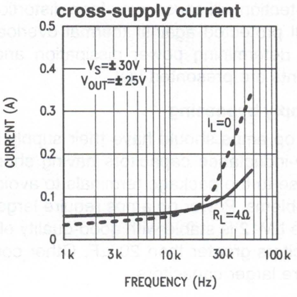
**supply current**



**supply current**



**cross-supply current**



TL/H/8704–5

## Application Information

### general

Twenty five years ago the operational amplifier was a specialized design tool used primarily for analog computation. However, the availability of low cost IC op amps in the late 1960's prompted their use in rather mundane applications, replacing a few discrete components. Once a few basic principles are mastered, op amps can be used to give exceptionally good results in a wide range of applications while minimizing both cost and design effort.

The availability of a monolithic power op amp now promises to extend these advantages to high-power designs. Some conventional applications are given here to illustrate op amp design principles as they relate to power circuitry. The inevitable fall in prices, as the economies of volume production are realized, will prompt their use in applications that might now seem trivial. Replacing single power transistors with an op amp will become economical because of improved performance, simplification of attendant circuitry, vastly improved fault protection, greater reliability and the reduction of design time.

Power op amps introduce new factors into the design equation. With current transients above 10A, both the inductance and resistance of wire interconnects become important in a number of ways. Further, power ratings are a crucial factor in determining performance. But the power capability of the IC cannot be realized unless it is properly mounted to an adequate heat sink. Thus, thermal design is of major importance with power op amps.

This application summary starts off by identifying the origin of strange problems observed while using the LM12 in a wide variety of designs with all sorts of fault conditions. A few simple precautions will eliminate these problems. **One would do well to read the section on supply bypassing, lead inductance, output clamp diodes, ground loops and reactive loading before doing any experimentation. Should there be problems with erratic operation, blowouts, excessive distortion or oscillation, another look at these sections is in order.**

The management and protection circuitry can also affect operation. Should the total supply voltage exceed ratings or drop below 15V, the op amp shuts off completely. Case temperatures above 150°C also cause shut down until the temperature drops to 145°C. This may take several seconds, depending on the thermal system. Activation of the dynamic safe-area protection causes both the main feedback loop to lose control and a reduction in output power, with possible oscillations. In ac applications, the dynamic protection will cause waveform distortion. Since the LM12 is well protected against thermal overloads, the suggestions for determining power dissipation and heat sink requirements are presented last.

### supply bypassing

All op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals to avoid spurious oscillation problems. Power op amps require larger bypass capacitors. The LM12 is stable with good-quality electrolytic bypass capacitors greater than 20 $\mu$F. Other considerations may require larger capacitors.

The current in the supply leads is a rectified component of the load current. If adequate bypassing is not provided, this distorted signal can be fed back into internal circuitry. Low distortion at high frequencies requires that the supplies be bypassed with 470 $\mu$F or more, at the package terminals.

### lead inductance

With ordinary op amps, lead-inductance problems are usually restricted to supply bypassing. Power op amps are also sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load. Sensing to a remote load must be accompanied by a high-frequency feedback path directly from the output terminal. Lead inductance can also cause voltage surges on the supplies. With long leads to the power source, energy stored in the lead inductance when the output is shorted can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With 20 $\mu$F local bypass, these voltage surges are important only if the lead length exceeds a couple feet ($>$ 1 $\mu$H lead inductance). Twisting together the supply and ground leads minimizes the effect.

### ground loops

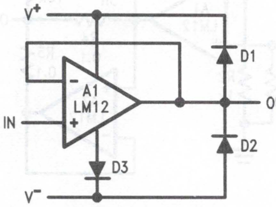
With fast, high-current circuitry, all sorts of problems can arise from improper grounding. In general, difficulties can be avoided by returning all grounds separately to a common point. Sometimes this is impractical. When compromising, special attention should be paid to the ground returns for the supply bypasses, load and input signal. Ground planes also help to provide proper grounding.

Many problems unrelated to system performance can be traced to the grounding of line-operated test equipment used for system checkout. Hidden paths are particularly difficult to sort out when several pieces of test equipment are used but can be minimized by using current probes or the new isolated oscilloscope pre-amplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope synchronization input solves one common problem.

### output clamp diodes

When a push-pull amplifier goes into power limit while driving an inductive load, the stored energy in the load inductance can drive the output outside the supplies. Although the LM12 has internal clamp diodes that can handle several amperes for a few milliseconds, extreme conditions can cause destruction of the IC. The internal clamp diodes are imperfect in that about half the clamp current flows into the supply to which the output is clamped while the other half flows across the supplies. Therefore, the use of external diodes to clamp the output to the power supplies is strongly recommended. This is particularly important with higher supply voltages.

Experience has demonstrated that hard-wire shorting the output to the supplies can induce random failures if these external clamp diodes are not used and the supply voltages are above ±20V. Therefore it is prudent to use output-clamp diodes even when the load is not particularly inductive. This also applies to experimental setups in that blowouts have been observed when diodes were not used. In packaged equipment, it may be possible to eliminate these diodes, providing that fault conditions can be controlled.



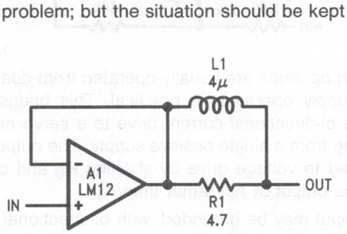
TL/H/8704–6

Heat sinking of the clamp diodes is usually unimportant in that they only clamp current transients. Forward drop with 15A fault transients is of greater concern. Usually, these transients die out rapidly. The clamp to the negative supply can have somewhat reduced effectiveness under worst case conditions should the forward drop exceed 1.0V. Mounting this diode to the power op amp heat sink improves the situation. Although the need has only been demonstrated with some motor loads, including a third diode (D3 above) will eliminate any concern about the clamp diodes. This diode, however, must be capable of dissipating continuous power as determined by the negative supply current of the op amp.

**reactive loading**

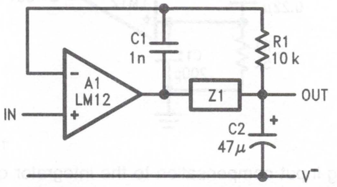
The LM12 is normally stable with resistive, inductive or smaller capacitive loads. Larger capacitive loads interact with the open-loop output resistance (about $1\Omega$) to reduce the phase margin of the feedback loop, ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier; a unity-gain follower can handle about 0.01 $\mu$F, while more than 1 $\mu$F does not cause problems if the loop gain is ten. With loop gains greater than unity, a speedup capacitor across the feedback resistor will aid stability. In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled and high-frequency feedback is derived directly from the output terminal, as recommended earlier.

So-called capacitive loads are not always capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this is not usually a problem; but the situation should be kept in mind.



TL/H/8704–7

Large capacitive loads (including series-resonant) can be accommodated by isolating the feedback amplifier from the load as shown above. The inductor gives low output impedance at lower frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series resonant circuits formed by capacitive loads. A low inductance, carbon-composition resistor is recommended. Optimum values of L and R depend upon the feedback gain and expected nature of the load, but are not critical. A 4 $\mu$H inductor is obtained with 14 turns of number 18 wire, close spaced, around a one-inch-diameter form.



TL/H/8704–8

The LM12 can be made stable for all loads with a large capacitor on the output, as shown above. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. It is appropriate for such applications as voltage regulators.

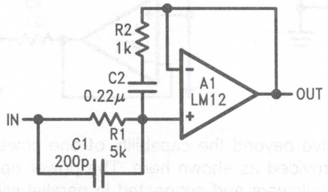
A feedback capacitor, $C_1$, is connected directly to the output pin of the IC. The output capacitor, $C_2$, is connected at the output terminal with short leads. Single-point grounding to avoid dc and ac ground loops is advised.

The impedance, $Z_1$, is the wire connecting the op amp output to the load capacitor. About 3-inches of number-18 wire (70 nH) gives good stability and 18-inches (400 nH) begins to degrade load-transient response. The minimum load capacitance is 47 $\mu$F, if a solid-tantalum capacitor with an equivalent series resistance (ESR) of $0.1\Omega$ is used. Electrolytic capacitors work as well, although capacitance may have to be increased to 200 $\mu$F to bring ESR below $0.1\Omega$.

Loop stability is not the only concern when op amps are operated with reactive loads. With time-varying signals, power dissipation can also increase markedly. This is particularly true with the combination of capacitive loads and high-frequency excitation.

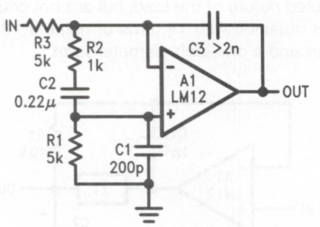
**input compensation**

The LM12 is prone to low-amplitude oscillation bursts coming out of saturation if the high-frequency loop gain is near unity. The voltage follower connection is most susceptible. This glitching can be eliminated at the expense of small-signal bandwidth using input compensation. Input compensation can also be used in combination with LR load isolation to improve capacitive load stability.



TL/H/8704–9

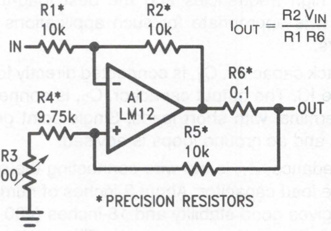
An example of a voltage follower with input compensation is shown here. The $R_2C_2$ combination across the input works with $R_1$ to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, $C_1$, improves phase margin at the unity-gain crossover frequency. Proper operation requires that the output impedance of the circuitry driving the follower be well under 1 k$\Omega$ at frequencies up to a few hundred kilohertz.


IN
R3
5k
R2
1k
C3 >2n
C2
0.22µ
−
A1
LM12
+
OUT
R1
5k
C1
200p

TL/H/8704-10

Extending input compensation to the integrator connection is shown here. Both the follower and this integrator will handle 1 µF capacitive loading without LR output isolation.

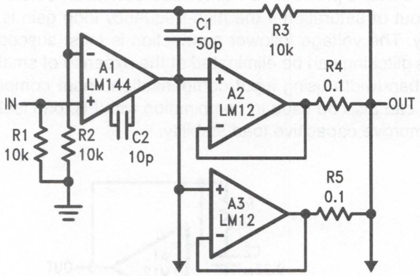
**current drive**


R1*
10k
R2*
10k
$I_{OUT} = \frac{R2\,V_{IN}}{R1\,R6}$
IN
R6*
0.1
R4*
9.75k
A1
LM12
OUT
R5*
10k
R3
500
* PRECISION RESISTORS

TL/H/8704-11

This circuit provides an output current proportional to the input voltage. Current drive is sometimes preferred for servo motors because it aids in stabilizing the servo loop by reducing phase lag caused by motor inductance. In applications requiring high output resistance, such as operational power supplies running in the current mode, matching of the feedback resistors to 0.01% is required. Alternately, an adjustable resistor can be used for trimming.

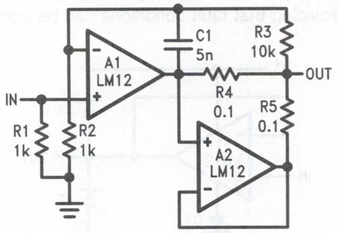
**parallel operation**


C1
50p
R3
10k
A1
LM144
A2
LM12
R4
0.1
OUT
IN
R1
10k
R2
10k
C2
10p
A3
LM12
R5
0.1

TL/H/8704-12

Output drive beyond the capability of one power amplifier can be provided as shown here. The power op amps are wired as followers and connected in parallel with the outputs coupled through equalization resistors. A standard, high-voltage op amp is used to provide voltage gain. Overall feedback compensates for the voltage dropped across the equalization resistors.

With parallel operation, there may be an increase in unloaded supply current related to the offset voltage across the equalization resistors. More output buffers, with individual equalization resistors, may be added to meet even higher drive requirements.

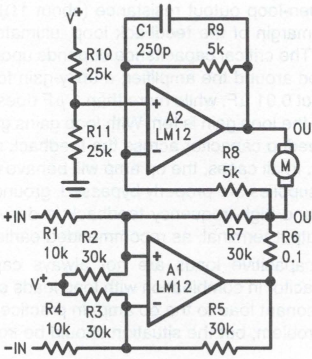

C1
5n
R3
10k
A1
LM12
OUT
IN
R4
0.1
R5
0.1
R1
1k
R2
1k
A2
LM12

TL/H/8704-13

This connection allows increased output capability without requiring a separate control amplifier. The output buffer, $A_2$, provides load current through $R_5$ equal to that supplied by the main amplifier, $A_1$, through $R_4$. Again, more output buffers can be added.

Current sharing among paralleled amplifiers can be affected by gain error as the power-bandwidth limit is approached. In the first circuit, the operating current increase will depend upon the matching of high-frequency characteristics. In the second circuit, however, the entire input error of $A_2$ appears across $R_4$ and $R_5$. The supply current increase can cause power limiting to be activated as the slew limit is approached. This will not damage the LM12. It can be avoided in both cases by connecting $A_1$ as an inverting amplifier and restricting bandwidth with $C_1$.

**single-supply operation**

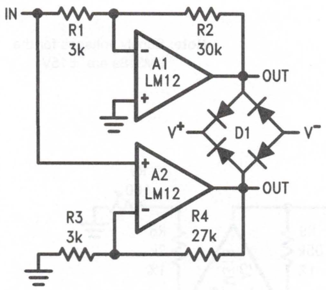

V+
C1
250p
R9
5k
R10
25k
A2
LM12
OUT
R11
25k
R8
5k
M
+IN
OUT
R1
10k
R2
30k
R7
30k
R6
0.1
A1
LM12
V+
R4
10k
R3
30k
R5
30k
−IN

TL/H/8704-14

Although op amps are usually operated from dual supplies, single-supply operation is practical. This bridge amplifier supplies bi-directional current drive to a servo motor while operating from a single positive supply. The output is easily converted to voltage drive by shorting $R_6$ and connecting $R_7$ to the output of $A_2$, rather than $A_1$.

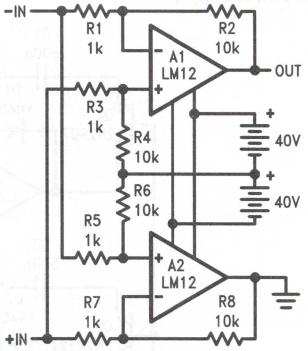
Either input may be grounded, with bi-directional drive provided to the other. It is also possible to connect one input to a positive reference, with the input signal varying about this voltage. If the reference voltage is above 5V, $R_2$ and $R_3$ are not required.

## high voltage amplifiers


IN
R1
3k
R2
30k
A1
LM12
OUT
D1
V+
V−
A2
LM12
OUT
R3
3k
R4
27k

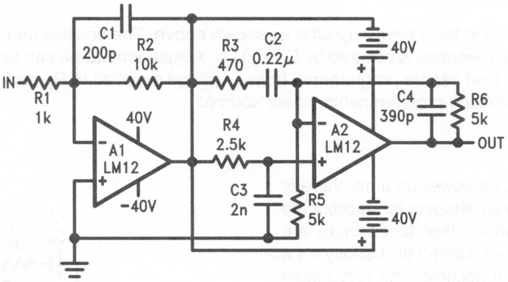
TL/H/8704–15

The voltage swing delivered to the load can be doubled by using the bridge connection shown here. Output clamping to the supplies can be provided by using a bridge-rectifier assembly.


−IN
R1
1k
R2
10k
A1
LM12
OUT
R3
1k
R4
10k
40V
R6
10k
40V
R5
1k
A2
LM12
R7
1k
R8
10k
+IN

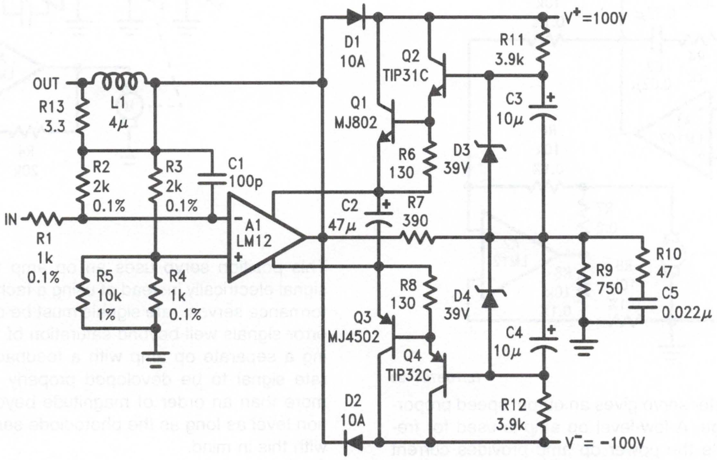
TL/H/8704–16

One limitation of the standard bridge connection is that the load cannot be returned to ground. This can be circumvented by operating the bridge with floating supplies, as shown above. For single-ended drive, either input can be grounded.


C1
200p
R2
10k
R3
470
C2
0.22μ
40V
IN
R1
1k
40V
A1
LM12
−40V
R4
2.5k
C4
390p
R6
5k
A2
LM12
OUT
C3
2n
R5
5k
40V

TL/H/8704–17

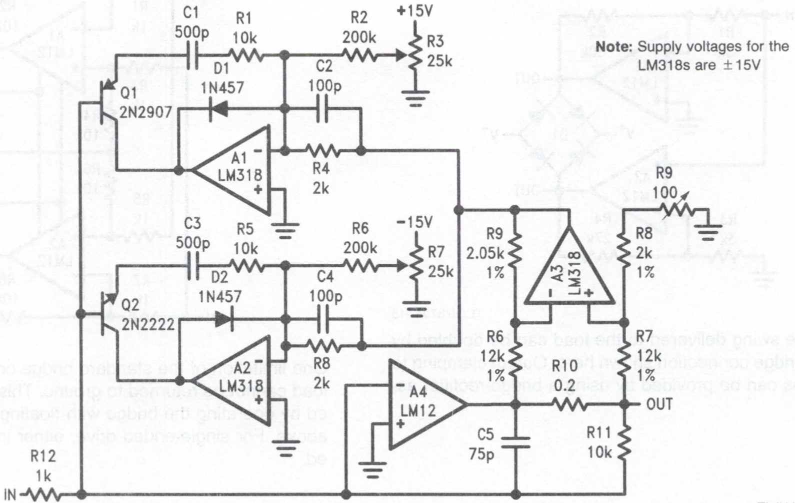
This circuit shows how two amplifiers can be cascaded to double output swing. The advantage over the bridge is that the output can be increased with any number of stages, although separate supplies are required for each.


D1
10A
Q2
TIP31C
V+=100V
R11
3.9k
OUT
R13
3.3
L1
4μ
Q1
MJ802
C3
10μ
R6
130
D3
39V
R2
2k
0.1%
R3
2k
0.1%
C1
100p
C2
47μ
R7
390
IN
R1
1k
0.1%
A1
LM12
R5
10k
1%
R4
1k
0.1%
R8
130
D4
39V
R9
750
R10
47
C5
0.022μ
Q3
MJ4502
C4
10μ
Q4
TIP32C
D2
10A
R12
3.9k
V−= −100V

TL/H/8704–18

Discrete transistors can be used to increase output drive to ±90V at ±10A as shown above. With proper thermal design, the IC will provide safe-area protection for the external transistors. Voltage gain is about thirty.

### operational power supply


C1
500p
R1
10k
R2
200k
+15V
R3
25k
D1
1N457
C2
100p
Q1
2N2907
A1
LM318
R4
2k
C3
500p
R5
10k
R6
200k
−15V
R7
25k
D2
1N457
C4
100p
Q2
2N2222
A2
LM318
R8
2k
R9
2.05k
1%
A3
LM318
R9
100
R8
2k
1%
R6
12k
1%
R7
12k
1%
A4
LM12
R10
0.2
OUT
C5
75p
R11
10k
R12
1k
IN

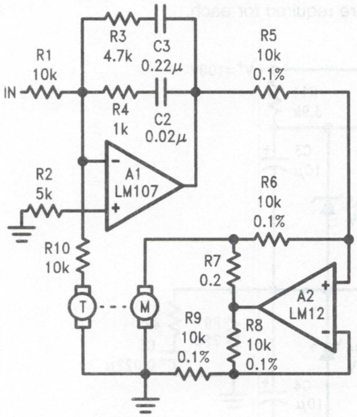
**Note:** Supply voltages for the LM318s are ±15V

TL/H/8704–19

External current limit can be provided for a power op amp as shown above. The positive and negative current limits can be set precisely and independently. Fast response is assured by $D_1$ and $D_2$. Adjustment range can be set down to zero with potentiometers $R_3$ and $R_7$. Alternately, the limit can be programmed from a voltage supplied to $R_2$ and $R_6$. This is the set up required for an operational power supply or voltage-programmable power source.

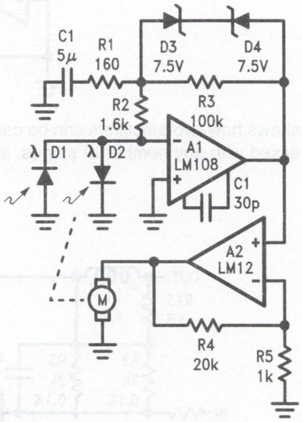
### servo amplifiers

When making servo systems with a power op amp, there is a temptation to use it for frequency shaping to stabilize the servo loop. Sometimes this works; other times there are better ways; and occasionally it just doesn't fly. Usually it's a matter of how quickly and to what accuracy the servo must stabilize.


R3
4.7k
C3
0.22µ
R5
10k
0.1%
R1
10k
IN
R4
1k
C2
0.02µ
R2
5k
A1
LM107
R6
10k
0.1%
R10
10k
R7
0.2
A2
LM12
T
M
R9
10k
0.1%
R8
10k
0.1%

TL/H/8704–20

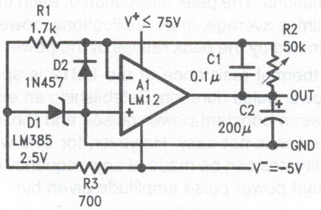
This motor/tachometer servo gives an output speed proportional to input voltage. A low-level op amp is used for frequency shaping while the power op amp provides current drive to the motor. Current drive eliminates loop phase shift due to motor inductance and makes high-performance servos easier to stabilize.


C1
5µ
R1
160
D3
7.5V
D4
7.5V
R2
1.6k
R3
100k
λ D1
λ D2
A1
LM108
C1
30p
A2
LM12
M
R4
20k
R5
1k

TL/H/8704–21

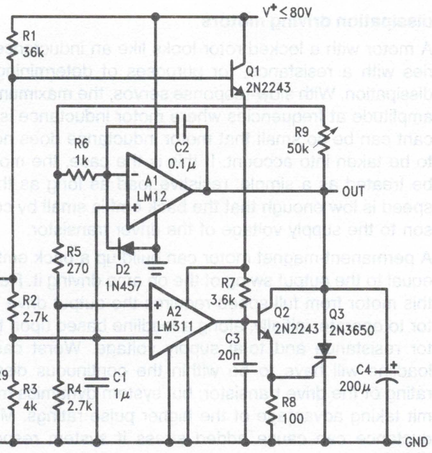
This position servo uses an op amp to develop the rate signal electrically instead of using a tachometer. In high-performance servos, rate signals must be developed with large error signals well beyond saturation of the motor drive. Using a separate op amp with a feedback clamp allows the rate signal to be developed properly with position errors more than an order of magnitude beyond the loop-saturation level as long as the photodiode sensors are positioned with this in mind.

### voltage regulators


R1
1.7k
V+ ≤ 75V
R2
50k
D2
1N457
C1
0.1µ
A1
LM12
OUT
C2
200µ
D1
LM385
2.5V
GND
V− = −5V
R3
700

TL/H/8704–22

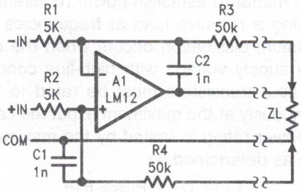
An op amp can be used as a positive or negative regulator. Unlike most regulators, it can sink current to absorb energy dumped back into the output. This positive regulator has a 0–70V output range.


V+ ≤ 80V
R1
36k
Q1
2N2243
R6
1k
C2
0.1µ
R9
50k
A1
LM12
OUT
R5
270
D2
1N457
R2
2.7k
A2
LM311
R7
3.6k
Q2
2N2243
Q3
2N3650
C3
20n
C4
200µ
D1
LM329
7V
R3
4k
R4
2.7k
C1
1µ
R8
100
GND

TL/H/8704–23

Dual supplies are not required to use an op amp as a voltage regulator if zero output is not required. This 4V to 70V regulator operates from a single supply. Should the op amp not be able to absorb enough energy to control an overvoltage condition, a SCR will crowbar the output.

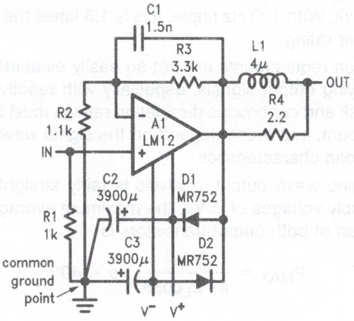
### remote sensing


R1
5K
R3
50k
−IN
C2
1n
A1
LM12
R2
5K
+IN
ZL
COM
C1
1n
R4
50k

TL/H/8704–24

Remote sensing as shown above allows the op amp to correct for dc drops in cables connecting the load. Even so, cable drop will affect transient response. Degradation can be minimized by using twisted, heavy-gauge wires on the output line. Normally, common and one input are connected together at the sending end.

### audio amplifiers


C1
1.5n
R3
3.3k
L1
4µ
OUT
R4
2.2
R2
1.1k
A1
LM12
IN
C2
3900µ
D1
MR752
R1
1k
C3
3900µ
D2
MR752
common
ground
point
V−
V+

TL/H/8704–25

A power amplifier suitable for use in high-quality audio equipment is shown above. Harmonic distortion is about 0.01-percent. Intermodulation distortion (60 Hz/7 kHz, 4:1) measured 0.015-percent. Transient response and saturation recovery are clean, and the 9 V/µs slew rate of the LM12 virtually eliminates transient intermodulation distortion. Using separate amplifiers to drive low- and high-frequency speakers gets rid of high-level crossover networks and attenuators. Further, it prevents clipping on the low-frequency channel from distorting the high frequencies.

### determining maximum dissipation

It is a simple matter to establish power requirements for an op amp driving a resistive load at frequencies well below 10 Hz. Maximum dissipation occurs when the output is at one-half the supply voltage with high-line conditions. The individual output transistors must be rated to handle this power continuously at the maximum expected case temperature. The power rating is limited by the maximum junction temperature as determined by

$$T_J = T_C + P_{DISS}\,\theta_{JC},$$

where $T_C$ is the case temperature as measured at the center of the package bottom, $P_{DISS}$ is the maximum power dissipation and $\theta_{JC}$ is the thermal resistance at the operating voltage of the output transistor. Recommended maximum junction temperatures are 200°C within the power transistor and 150°C for the control circuitry.

If there is ripple on the supply bus, it is valid to use the average value in worst-case calculations as long as the peak rating of the power transistor is not exceeded at the ripple peak. With 120 Hz ripple, this is 1.5 times the continuous power rating.

Dissipation requirements are not so easily established with time varying output signals, especially with reactive loads. Both peak and continuous dissipation ratings must be taken into account, and these depend on the signal waveform as well as load characteristics.

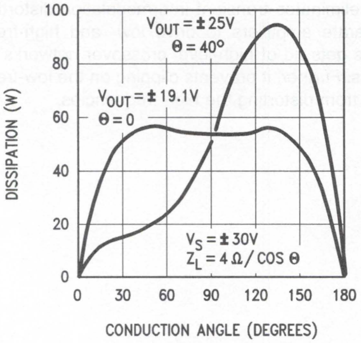
With a sine wave output, analysis is fairly straightforward. With supply voltages of $\pm V_S$, the maximum average power dissipation of both output transistors is

$$P_{MAX} = \frac{2V_S{}^2}{\pi^2 Z_L \cos\theta}, \quad \theta < 40°;$$

and

$$P_{MAX} = \frac{V_S{}^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right], \quad \theta \geq 40°,$$

where $Z_L$ is the magnitude of the load impedance and $\theta$ its phase angle. Maximum average dissipation occurs below maximum output swing for $\theta < 40°$.



TL/H/8704–26

The instantaneous power dissipation over the conducting half cycle of one output transistor is shown here. Power dissipation is near zero on the other half cycle. The output level is that resulting in maximum peak and average dissipation. Plots are given for a resistive and a series RL load. The latter is representative of a 4Ω loudspeaker operating below resonance and would be the worst case condition in most audio applications. The peak dissipation of each transistor is about four times average. In ac applications, power capability is often limited by the peak ratings of the power transistor.

The pulse thermal resistance of the LM12 is specified for constant power pulse duration. Establishing an exact equivalency between constant-power pulses and those encountered in practice is not easy. However, for sine waves, reasonable estimates can be made at any frequency by assuming a constant power pulse amplitude given by:

$$P_{PK} \cong \frac{V_S{}^2}{2Z_L}\Big[\,1\text{-}\cos\,(\phi - \theta)\Big],$$

where $\phi = 60°$ and $\theta$ is the absolute value of the phase angle of $Z_L$. Equivalent pulse width is $t_{ON} \cong 0.4\tau$ for $\theta = 0$ and $t_{ON} \cong 0.2\tau$ for $\theta \geq 20°$, where $\tau$ is the period of the output waveform.

### dissipation driving motors

A motor with a locked rotor looks like an inductance in series with a resistance, for purposes of determining driver dissipation. With slow-response servos, the maximum signal amplitude at frequencies where motor inductance is significant can be so small that motor inductance does not have to be taken into account. If this is the case, the motor can be treated as a simple, resistive load as long as the rotor speed is low enough that the back emf is small by comparison to the supply voltage of the driver transistor.

A permanent-magnet motor can build up a back emf that is equal to the output swing of the op amp driving it. Reversing this motor from full speed requires the output drive transistor to operate, initially, along a loadline based upon the motor resistance and total supply voltage. Worst case, this loadline will have to be within the continuous dissipation rating of the drive transistor; but system dynamics may permit taking advantage of the higher pulse ratings. Motor inductance can cause added stress if system response is fast.

Shunt- and series-wound motors can generate back emf's that are considerably more than the total supply voltage, resulting in even higher peak dissipation than a permanent-magnet motor having the same locked-rotor resistance.

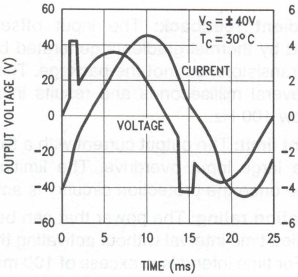
### voltage regulator dissipation

The pass transistor dissipation of a voltage regulator is easily determined in the operating mode. Maximum continuous dissipation occurs with high line voltage and maximum load current. As discussed earlier, ripple voltage can be averaged if peak ratings are not exceeded; however, a higher average voltage will be required to insure that the pass transistor does not saturate at the ripple minimum.

Conditions during start-up can be more complex. If the input voltage increases slowly such that the regulator does not go into current limit charging output capacitance, there are no problems. If not, load capacitance and load characteristics must be taken into account. This is also the case if automatic restart is required in recovering from overloads.

Automatic restart or start-up with fast-rising input voltages cannot be guaranteed unless the continuous dissipation rating of the pass transistor is adequate to supply the load current continuously at all voltages below the regulated output voltage. In this regard, the LM12 performs much better than IC regulators using foldback current limit, especially with high-line input voltage above 20V.

### power limiting



TL/H/8704-27

Should the power ratings of the LM12 be exceeded, dynamic safe-area protection is activated. Waveforms with this power limiting are shown for the LM12 driving ±36V at 40 Hz into 4Ω in series with 24 mH ($\theta = 45°$). With an inductive load, the output clamps to the supplies in power limit, as above. With resistive loads, the output voltage drops in limit. Behavior with more complex RCL loads is between these extremes.

Secondary thermal limit is activated should the case temperature exceed 150°C. This thermal limit shuts down the IC completely (open output) until the case temperature drops to about 145°C. Recovery may take several seconds.

### power supplies

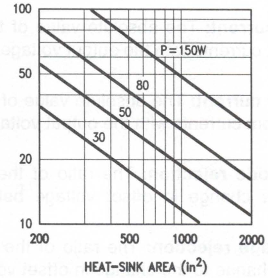
Power op amps do not require regulated supplies. However, the worst-case output power is determined by the low-line supply voltage in the ripple trough. The worst-case power dissipation is established by the average supply voltage with high-line conditions. The loss in power output that can be guaranteed is the square of the ratio of these two voltages.

Relatively simple off-line switching power supplies can provide voltage conversion, line isolation and 5-percent regulation while reducing size and weight.

The regulation against ripple and line variations can provide a substantial increase in the power output that can be guaranteed under worst-case conditions. In addition, switching power supplies can convert low-voltage power sources such as automotive batteries up to regulated, dual, high-voltage supplies optimized for powering power op amps.

### heat sinking

A semiconductor manufacturer has no control over heat sink design. Temperature rating can only be based upon case temperature as measured at the center of the package bottom. With power pulses of longer duration than 100 ms, case temperature is almost entirely dependent on heat sink design and the mounting of the IC to the heat sink.



TL/H/8704-28

The design of heat sink is beyond the scope of this work. Convection-cooled heat sinks are available commercially, and their manufacturers should be consulted for ratings. The preceding figure is a rough guide for temperature rise as a function of fin area (both sides) available for convection cooling.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important. Four to six inch-pounds is recommended.

Should it be necessary to isolate $V^-$ from the heat sink, an insulating washer is required. Hard washers like berylium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound. Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

## Definition of Terms

**Input offset voltage:** The absolute value of the voltage between the input terminals with the output voltage and current at zero.

**Input bias current:** The absolute value of the average of the two input currents with the output voltage and current at zero.

**Input offset current:** The absolute value of the difference in the two input currents with the output voltage and current at zero.

**Common-mode rejection:** The ratio of the input voltage range to the change in offset voltage between the extremes.

**Supply-voltage rejection:** The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

**Output saturation threshold:** The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

**Large signal voltage gain:** The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

**Thermal gradient feedback:** The input offset voltage change caused by thermal gradients generated by heating of the output transistors, but not the package. This effect is delayed by several milliseconds and results in increased gain error below 100 Hz.

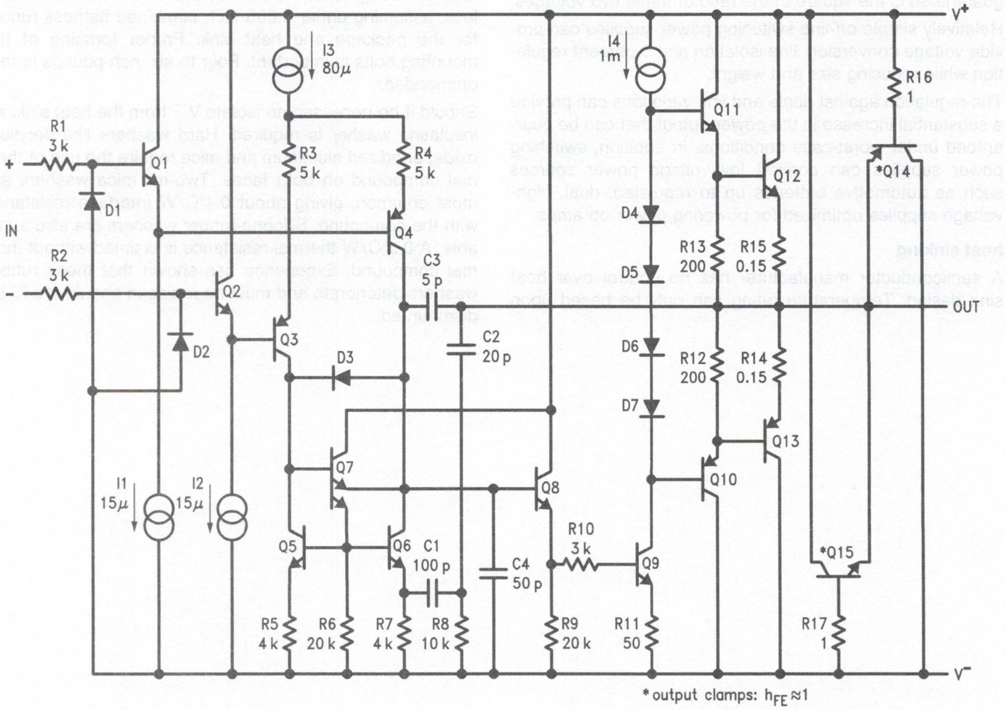
**Output-current limit:** The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once the protection circuitry is activated.

**Power dissipation rating:** The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

**Thermal resistance:** The peak, junction-temperature rise, per unit of internal power dissipation, above the case temperature as measured at the center of the package bottom. The dc thermal resistance applies when one output transistor is operating continuously. The ac thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

**Supply current:** The current required from the power source to operate the amplifier with the output voltage and current at zero.

## Equivalent Schematic (excluding active protection circuitry)



*output clamps: $h_{FE} \approx 1$

TL/H/8704-29

**National Semiconductor Corporation**

# LM101A/LM201A/LM301A Operational Amplifiers

## General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

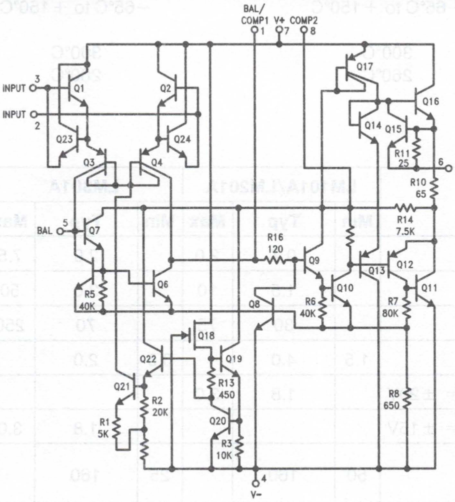
- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

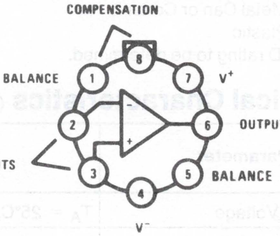
The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.

## Schematic** and Connection Diagrams (Top View)


BAL/ COMP1
V+
COMP2
1
7
8
INPUT 3
INPUT 2
Q1
Q2
Q23
Q24
Q3
Q4
Q17
Q16
Q14
Q15
R11 25
6 OUT
R10 65
R14 7.5K
5 BAL
Q7
R16 120
Q9
Q12
Q13
Q10
Q11
R5 40K
Q6
Q8
R6 40K
R7 80K
Q18
Q22
Q19
Q21
R2 20K
R13 450
R8 650
R1 5K
Q20
R3 10K
4
V−

TL/H/7752–1

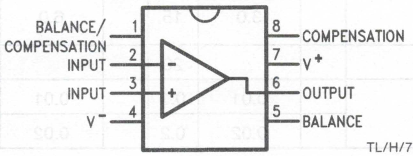
### Metal Can Package


COMPENSATION
8
BALANCE
1
7
V+
2
6
OUTPUT
INPUTS
3
5
BALANCE
4
V−

TL/H/7752–2

**Order Number LM101AH, LM201AH or LM301AH**
**See NS Package Number H08C**

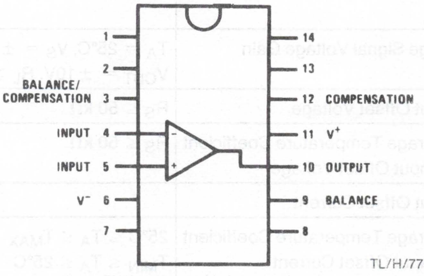
### Dual-In-Line Package


BALANCE/ COMPENSATION
1
INPUT
2
INPUT
3
V−
4
8
COMPENSATION
7
V+
6
OUTPUT
5
BALANCE

TL/H/7752–4

**Order Number LM101AJ, LM201AJ, LM301AJ, LM201AN or LM301AN**
**See NS Package Number J08A or N08A**

### Dual-In-Line Package


1
2
BALANCE/ COMPENSATION 3
INPUT 4
INPUT 5
V− 6
7
14
13
12 COMPENSATION
11 V+
10 OUTPUT
9 BALANCE
8

TL/H/7752–3

**Note:** Pin 6 connected to bottom of package.

**Order Number LM101AJ-14A, LM201AJ-14 or LM301AJ-14**
**See NS Package Number J14A**

**Pin connections shown are for 8-pin packages.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | LM101A/LM201A | LM301A |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±30V | ±30V |
| Input Voltage (Note 1) | ±15V | ±15V |
| Output Short Circuit Duration (Note 2) | Indefinite | Indefinite |
| Operating Junction Temp. Range | −55°C to +125°C (LM101A)<br>−25°C to +85°C (LM201A) | |
| $T_J$ Max | | |
| H-Package | 150°C | 100°C |
| N-Package | 150°C | 100°C |
| J-Package | 150°C | 100°C |
| M-Package | | |
| Power Dissipation at $T_A$ = 25°C | | |
| H-Package (Still Air) | 500 mW | 300 mW |
| (400 LF/Min Air Flow) | 1200 mW | 700 mW |
| N-Package | 900 mW | 500 mW |
| J-Package | 1000 mW | 650 mW |
| M-Package | | |
| Thermal Resistance (Typical) $\theta_{jA}$ | | |
| H-Package (Still Air) | 230°C/W | 230°C/W |
| (400 LF/Min Air Flow) | 95°C/W | 95°C/W |
| N Package | 135°C/W | 135°C/W |
| J-Package | 110°C/W | 110°CmW |
| M-Package | | |
| (Typical) $\theta_{jC}$ | | |
| H-Package (Still Air) | 25°C/W | 25°C/W |
| (400 LF/Min Air Flow) | 10°C/W | 10°C/W |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | | |
| Metal Can or Ceramic | 300°C | 300°C |
| Plastic | 260°C | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Note 3) $T_A = T_J$

| Parameter | Conditions | | LM101A/LM201A | | | LM301A | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A$ = 25°C, $R_S \leq 50\ k\Omega$ | | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A$ = 25°C | | | 1.5 | 10 | | 3.0 | 50 | nA |
| Input Bias Current | $T_A$ = 25°C | | | 30 | 75 | | 70 | 250 | nA |
| Input Resistance | $T_A$ = 25°C | | 1.5 | 4.0 | | 0.5 | 2.0 | | MΩ |
| Supply Current | $T_A$ = 25°C | $V_S = \pm 20V$ | | 1.8 | 3.0 | | | | mA |
| | | $V_S = \pm 15V$ | | | | | 1.8 | 3.0 | mA |
| Large Signal Voltage Gain | $T_A$ = 25°C, $V_S = \pm 15V$<br>$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$ | | 50 | 160 | | 25 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 50\ k\Omega$ | | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $R_S \leq 50\ k\Omega$ | | | 3.0 | 15 | | 6.0 | 30 | μV/°C |
| Input Offset Current | | | | | 20 | | | 70 | nA |
| Average Temperature Coefficient of Input Offset Current | 25°C $\leq T_A \leq T_{MAX}$ | | | 0.01 | 0.1 | | 0.01 | 0.3 | nA/°C |
| | $T_{MIN} \leq T_A \leq$ 25°C | | | 0.02 | 0.2 | | 0.02 | 0.6 | nA/°C |

## Electrical Characteristics (Note 3) $T_A = T_J$ (Continued)

| Parameter | Conditions | | LM101A/LM201A | | | LM301A | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | | | | | 0.1 | | | 0.3 | μA |
| Supply Current | $T_A = T_{MAX}$, $V_S = \pm 20V$ | | | 1.2 | 2.5 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$<br>$R_L \geq 2k$ | | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$ | $R_L = 10\ k\Omega$ | ±12 | ±14 | | ±12 | ±14 | | V |
| | | $R_L = 2\ k\Omega$ | ±10 | ±13 | | ±10 | ±13 | | V |
| Input Voltage Range | $V_S = \pm 20V$ | | ±15 | | | | | | V |
| | $V_S = \pm 15V$ | | | ±15, −13 | | ±12 | +15, −13 | | V |
| Common-Mode Rejection Ratio | $R_S \leq 50\ k\Omega$ | | 80 | 96 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 50\ k\Omega$ | | 80 | 96 | | 70 | 96 | | dB |

**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

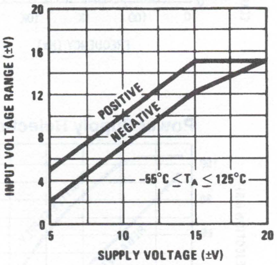
**Note 2:** Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

**Note 3:** Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

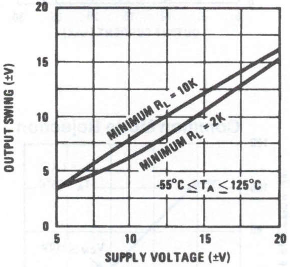
**Note 4:** Refer to RETS101AX for LM101A military specifications.

## Guaranteed Performance Characteristics LM101A/LM201A

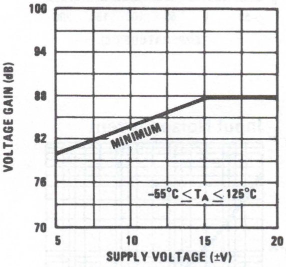
### Input Voltage Range



### Output Swing



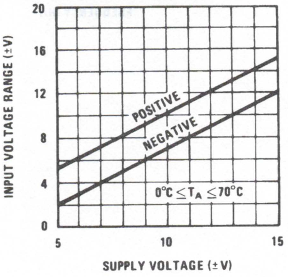
### Voltage Gain



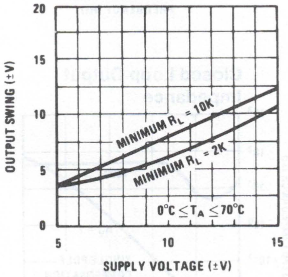
TL/H/7752–5

## Guaranteed Performance Characteristics LM301A

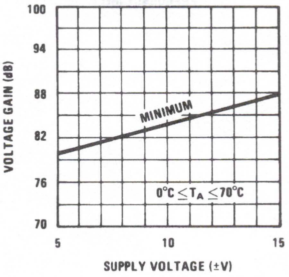
### Input Voltage Range



### Output Swing



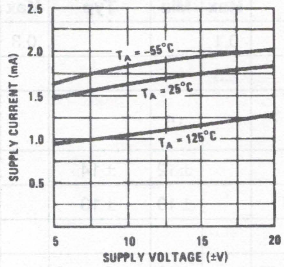
### Voltage Gain



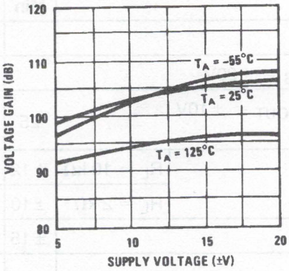
TL/H/7752–6

## Typical Performance Characteristics

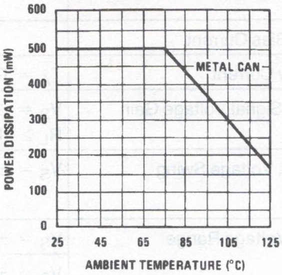
Supply Current



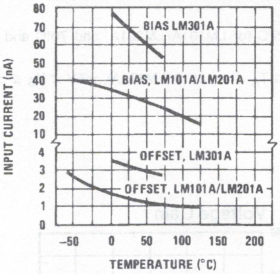
Voltage Gain



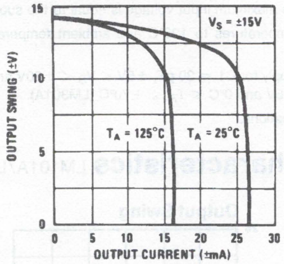
Maximum Power Dissipation



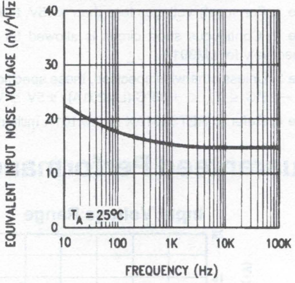
Input Current, LM101A/LM201A/LM301A



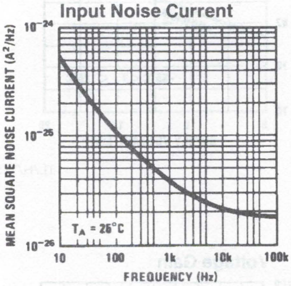
Current Limiting



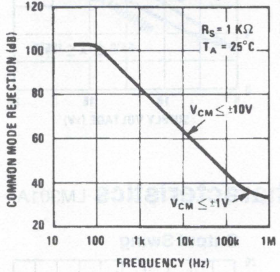
Input Noise Voltage



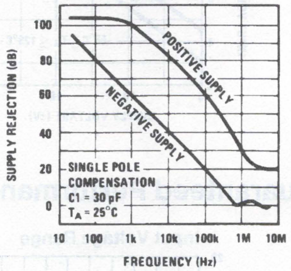
Input Noise Current



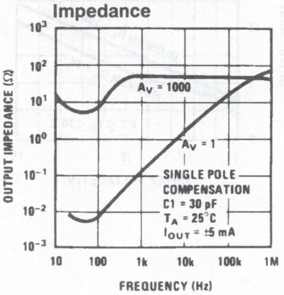
Common Mode Rejection



Power Supply Rejection



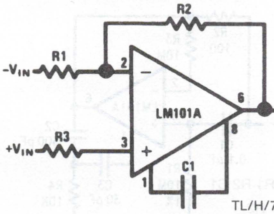
Closed Loop Output Impedance



TL/H/7752–7

# Typical Performance Characteristics for Various Compensation Circuits**

### Single Pole Compensation

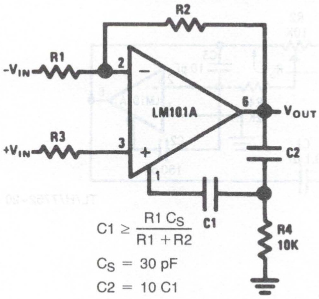

R2
R1
-VIN
2
−
LM101A
6
VOUT
8
R3
+VIN
3
+
C1
1

TL/H/7752-8

$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

$C_S = 30$ pF

### Two Pole Compensation


R2
R1
-VIN
2
−
LM101A
6
VOUT
R3
+VIN
3
+
1
C2
C1
R4
10K

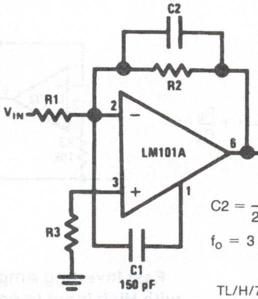
$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

$C_S = 30$ pF

$C2 = 10\,C1$

TL/H/7752-12

### Feedforward Compensation

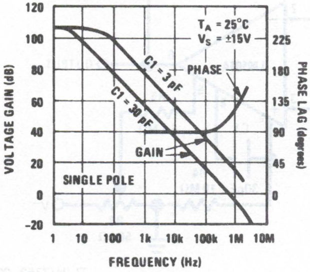

C2
R2
R1
VIN
2
−
LM101A
6
VOUT
3
+
1
R3
C1
150 pF

$$C2 = \frac{1}{2\pi f_o R2}$$

$f_o = 3$ MHz

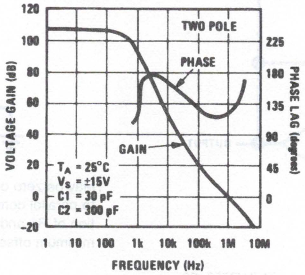
TL/H/7752-16

### Open Loop Frequency Response



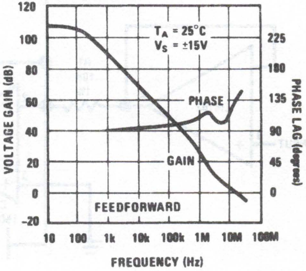
TL/H/7752-9

### Open Loop Frequency Response



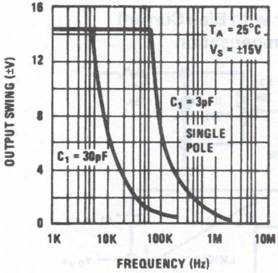
TL/H/7752-13

### Open Loop Frequency Response



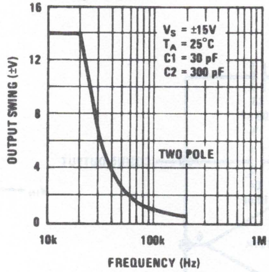
TL/H/7752-17

### Large Signal Frequency Response



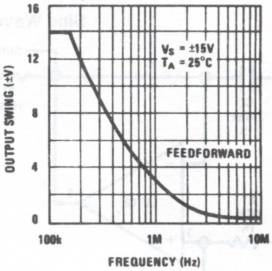
TL/H/7752-10

### Large Signal Frequency Response



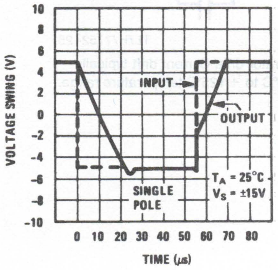
TL/H/7752-14

### Large Signal Frequency Response



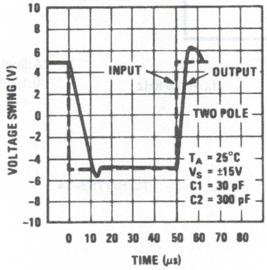
TL/H/7752-18

### Voltage Follower Pulse Response



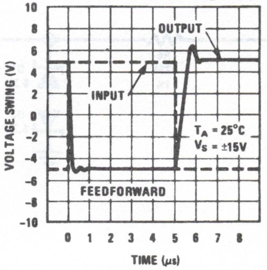
TL/H/7752-11

### Voltage Follower Pulse Response



TL/H/7752-15

### Inverter Pulse Response

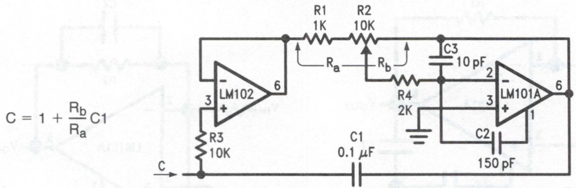


TL/H/7752-19

**Pin connections shown are for 8-pin packages.

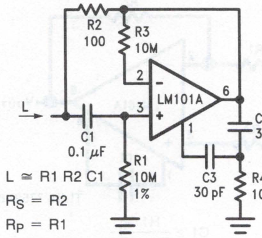
# Typical Applications**

## Variable Capacitance Multiplier


$C = 1 + \frac{R_b}{R_a} C1$
R1
1K
R2
10K
$R_a$
$R_b$
C3
10 pF
LM102
6
3
R3
10K
R4
2K
2
3
LM101A
6
1
C2
150 pF
C1
0.1 µF
C

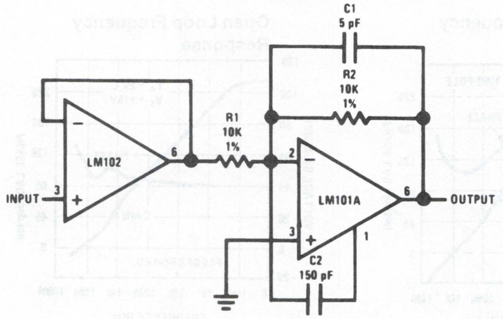
TL/H/7752-20

## Simulated Inductor


R2
100
R3
10M
2
3
LM101A
6
1
L
C1
0.1 µF
R1
10M
1%
C2
300 pF
C3
30 pF
R4
10K
$L \cong R1\ R2\ C1$
$R_S = R2$
$R_P = R1$

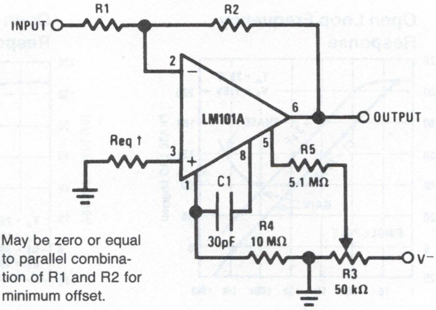
TL/H/7752-21

## Fast Inverting Amplifier with High Input Impedance


C1
5 pF
R2
10K
1%
LM102
6
3
INPUT
R1
10K
1%
2
LM101A
6
3
1
C2
150 pF
OUTPUT

TL/H/7752-22

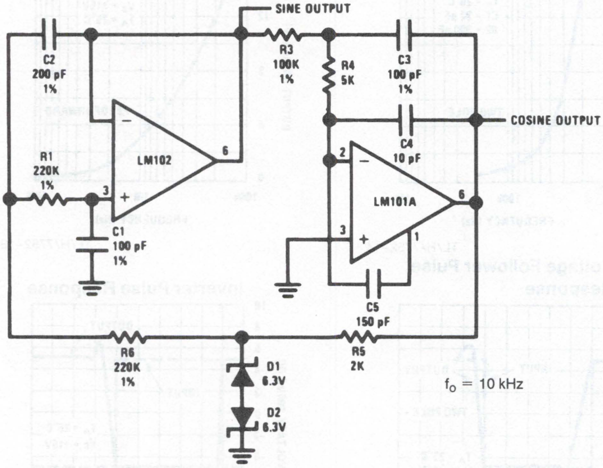
## Inverting Amplifier with Balancing Circuit


INPUT
R1
R2
2
LM101A
6
OUTPUT
Req †
3
8
5
1
C1
30pF
R5
5.1 MΩ
R4
10 MΩ
R3
50 kΩ
V⁻

†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

TL/H/7752-23

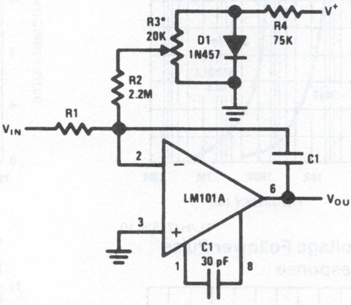
## Sine Wave Oscillator


SINE OUTPUT
C2
200 pF
1%
R3
100K
1%
R4
5K
C3
100 pF
1%
COSINE OUTPUT
C4
10 pF
LM102
6
R1
220K
1%
3
C1
100 pF
1%
2
3
LM101A
6
1
C5
150 pF
R6
220K
1%
R5
2K
D1
6.3V
D2
6.3V

$f_o = 10\ \text{kHz}$

TL/H/7752-24

## Integrator with Bias Current Compensation


R3*
20K
D1
1N457
R4
75K
V⁺
R2
2.2M
$V_{IN}$
R1
2
C1
LM101A
6
$V_{OUT}$
3
C1
30 pF
1
8

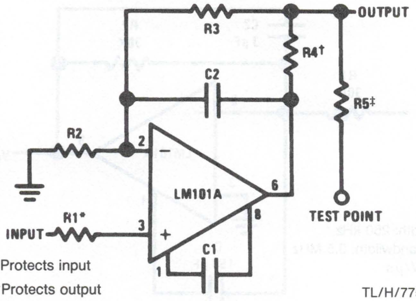
TL/H/7752-25

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

**Pin connections shown are for 8-pin packages.

## Application Hints**

### Protecting Against Gross Fault Conditions



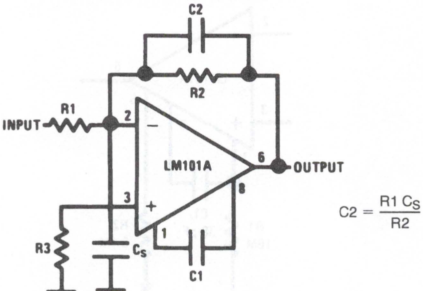
*Protects input

†Protects output

‡Protects output—not needed when R4 is used.

TL/H/7752–26

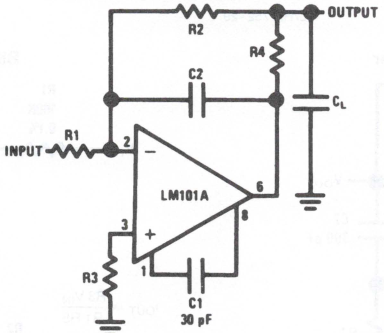
### Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\,C_S}{R2}$$

TL/H/7752–27

### Isolating Large Capacitive Loads



TL/H/7752–28

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V+ and V− will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

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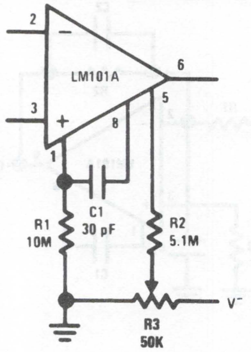
**Pin connections shown are for 8-pin packages.

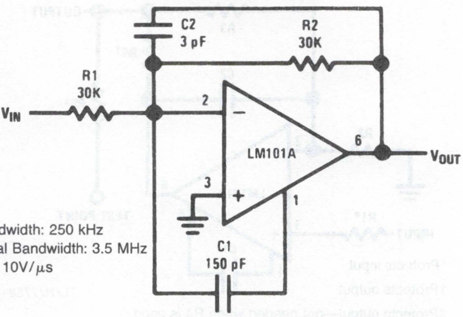
## Typical Applications** (Continued)

### Standard Compensation and Offset Balancing Circuit


2
3
6
5
8
1
LM101A
R1
10M
C1
30 pF
R2
5.1M
R3
50K
V⁻

TL/H/7752-29

### Fast Summing Amplifier


C2
3 pF
R2
30K
R1
30K
V_IN
2
3
6
1
LM101A
V_OUT
C1
150 pF

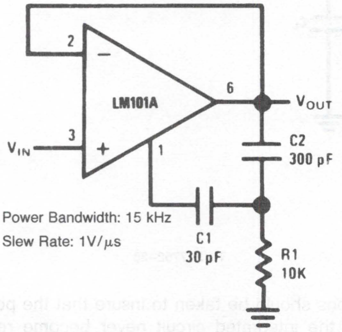
Power Bandwidth: 250 kHz

Small Signal Bandwidth: 3.5 MHz

Slew Rate: 10V/$\mu$s

TL/H/7752-30

### Fast Voltage Follower

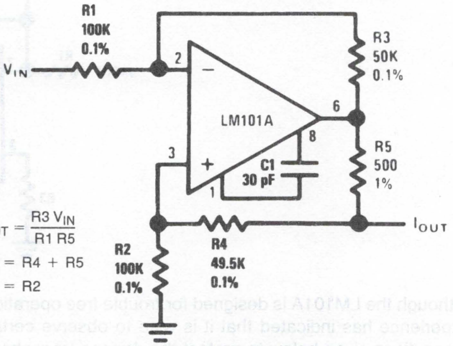

2
3
6
1
LM101A
V_IN
V_OUT
C2
300 pF
C1
30 pF
R1
10K

Power Bandwidth: 15 kHz

Slew Rate: 1V/$\mu$s

TL/H/7752-31

### Bilateral Current Source


R1
100K
0.1%
V_IN
2
3
6
8
1
LM101A
C1
30 pF
R3
50K
0.1%
R5
500
1%
R2
100K
0.1%
R4
49.5K
0.1%
I_OUT

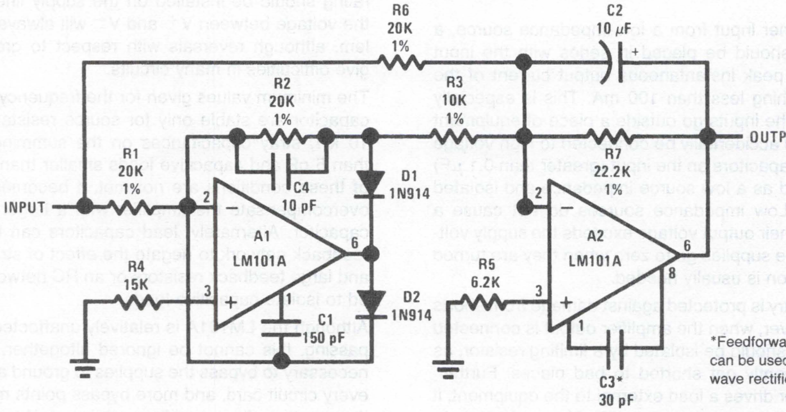
$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$

R3 = R4 + R5

R1 = R2

TL/H/7752-32

### Fast AC/DC Converter*


R6
20K
1%
C2
10 µF
R2
20K
1%
R3
10K
1%
R1
20K
1%
INPUT
C4
10 pF
D1
1N914
A1
LM101A
2
3
6
1
R4
15K
C1
150 pF
D2
1N914
R7
22.2K
1%
OUTPUT
A2
LM101A
2
3
6
8
R5
6.2K
C3*
30 pF

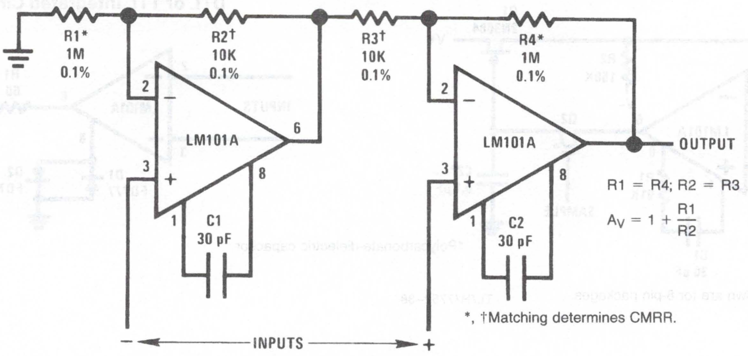
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

TL/H/7752-33

**Pin connections shown are for 8-pin packages.

## Typical Applications** (Continued)

### Instrumentation Amplifier


R1*
1M
0.1%
R2†
10K
0.1%
R3†
10K
0.1%
R4*
1M
0.1%
2
3
6
8
1
LM101A
C1
30 pF
C2
30 pF
OUTPUT
− INPUTS +

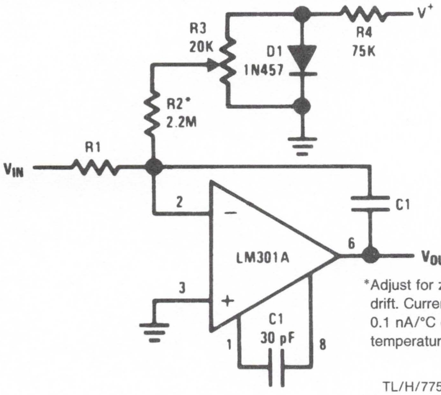
R1 = R4; R2 = R3

$A_V = 1 + \frac{R1}{R2}$

*, †Matching determines CMRR.

TL/H/7752–34

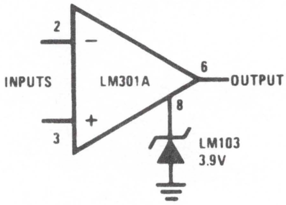
### Integrator with Bias Current Compensation


V+
R4
75K
R3
20K
D1
1N457
R2*
2.2M
R1
$V_{IN}$
C1
2
3
6
1
8
LM301A
C1
30 pF
$V_{OUT}$

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to +70°C temperature range.

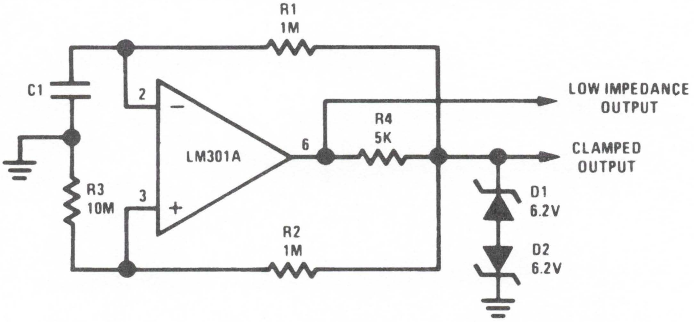
TL/H/7752–35

### Voltage Comparator for Driving RTL Logic or High Current Driver


2
3
6
8
INPUTS
LM301A
OUTPUT
LM103
3.9V

TL/H/7752–37

### Low Frequency Square Wave Generator

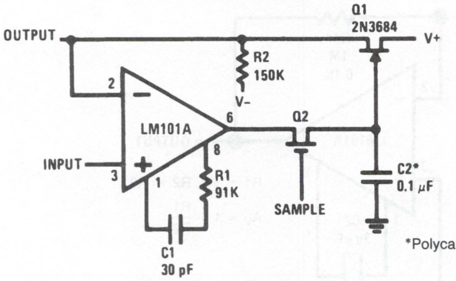

R1
1M
C1
2
3
6
LM301A
R4
5K
R3
10M
R2
1M
LOW IMPEDANCE OUTPUT
CLAMPED OUTPUT
D1
6.2V
D2
6.2V

TL/H/7752–36

**Pin connections shown are for 8-pin packages.

## Typical Applications** (Continued)

### Low Drift Sample and Hold

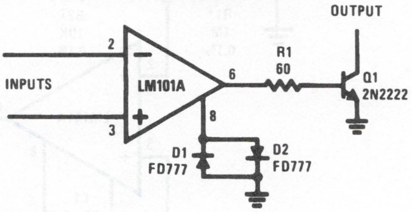

OUTPUT
Q1
2N3684
V+
R2
150K
V-
2
LM101A
6
Q2
8
INPUT
3
1
R1
91K
C2*
0.1 μF
SAMPLE
C1
30 pF

*Polycarbonate-dielectric capacitor

**Pin connections shown are for 8-pin packages.

TL/H/7752-38

### Voltage Comparator for Driving DTL or TTL Integrated Circuits


OUTPUT
2
INPUTS
LM101A
6
R1
60
Q1
2N2222
8
3
D1
FD777
D2
FD777

TL/H/7752-39

**National Semiconductor Corporation**

# LM107/LM207/LM307 Operational Amplifiers

## General Description

The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741.

The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

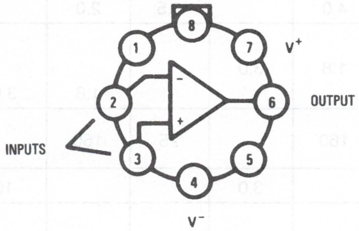
The LM107 is guaranteed over a −55°C to +125°C temperature range, the LM207 from −25°C to +85°C and the LM307 from 0°C to +70°C.

## Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

## Connection Diagrams

**Metal Can Package**

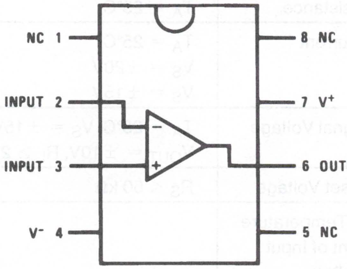


TL/H/7757-2

**Top View**

**Order Number LM107H, LM207H or LM307H**
**See NS Package Number H08C**

**Dual-in-Line Package**



TL/H/7757-3

Note: Pin 4 connected to bottom of package.

**Top View**

**Order Number LM107J, LM207J or LM307J**
**See NS Package Number J08A**
**Order Number LM307M**
**See NS Package Number M08A**
**Order Number LM307N**
**See NS Package Number N08A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 4)**

| | LM107/LM207 | LM307 |
|---|---|---|
| Supply Voltage | ±22V | ±18V |
| Power Dissipation (Note 1) | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V |
| Input Voltage (Note 2) | ±15V | ±15V |
| Output Short Circuit Duration | Indefinite | Indefinite |
| Operating Temperature Range ($T_A$) | | |
| (LM107) | −55°C to +125°C | 0°C to +70°C |
| (LM207) | −25°C to +85°C | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C | 260°C |

| | $T_{MIN}$ | $T_{MAX}$ |
|---|---|---|
| LM107 | −55°C | +125°C |
| LM207 | −25°C | +85°C |
| LM307 | 0°C | +70°C |

ESD rating to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM107/LM207 | | | LM307 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C, R_S \leq 50\ k\Omega$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 1.5 | 10 | | 3.0 | 50 | nA |
| Input Bias Current | $T_A = 25°C$ | | 30 | 75 | | 70 | 250 | nA |
| Input Resistance | $T_A = 25°C$ | 1.5 | 4.0 | | 0.5 | 2.0 | | MΩ |
| Supply Current | $T_A = 25°C$<br>$V_S = \pm 20V$<br>$V_S = \pm 15V$ | | <br>1.8<br> | <br>3.0<br> | | <br><br>1.8 | <br><br>3.0 | <br>mA<br>mA |
| Large Signal Voltage Gain | $T_A = 25°C, V_S = \pm 15V$<br>$V_{OUT} = \pm 10V, R_L \geq 2\ k\Omega$ | 50 | 160 | | 25 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 50\ k\Omega$ | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 15 | | 6.0 | 30 | μV/°C |
| Input Offset Current | | | | 20 | | | 70 | nA |
| Average Temperature Coefficient of Input Offset Current | $25°C \leq T_A \leq T_{MAX}$<br>$T_{MIN} \leq T_A \leq 25°C$ | | 0.01<br>0.02 | 0.1<br>0.2 | | 0.01<br>0.02 | 0.3<br>0.6 | nA/°C<br>nA/°C |
| Input Bias Current | | | | 100 | | | 300 | nA |
| Supply Current | $T_A = +125°C, V_S = \pm 20V$ | | 1.2 | 2.5 | | | | mA |

## Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM107/LM207 | | | LM307 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $V_S = \pm15V$, $V_{OUT} = \pm10V$<br>$R_L \geq 2\ k\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm15V$<br>$R_L = 10\ k\Omega$<br>$R_L = 2\ k\Omega$ | ±12<br>±10 | ±14<br>±13 | | ±12<br>±10 | ±14<br>±13 | | V<br>V |
| Input Voltage Range | $V_S = \pm20V$<br>$V_S = \pm15V$ | ±15 | +15<br>−13 | | ±12 | +15<br>−13 | | V<br>V |
| Common Mode Rejection Ratio | $R_S \leq 50\ k\Omega$ | 80 | 96 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 50\ k\Omega$ | 80 | 96 | | 70 | 96 | | dB |

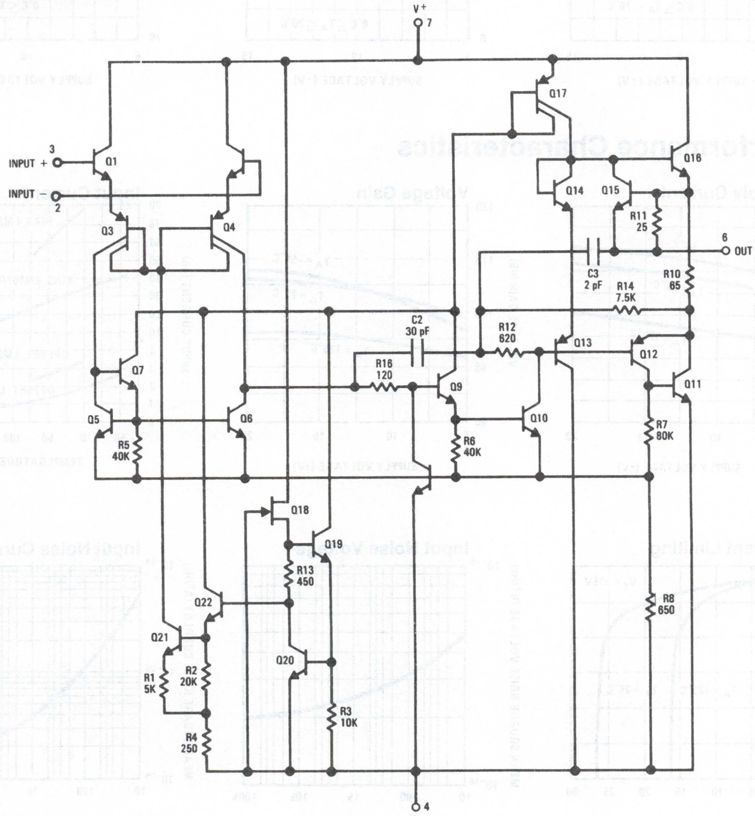
**Note 1:** The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 225°C/W, junction to ambient, or 30°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 2:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** These specifications apply for $\pm5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq +125°C$ for the LM107 or $-25°C \leq T_A$ $+85°C$ for the LM207, and $0°C \leq T_A \leq +70°C$ and $\pm5V \leq V_S \leq \pm15V$ for the LM307 unless otherwise specified.

**Note 4:** Refer to RETS107X for LM107H and LM107J military specifications.

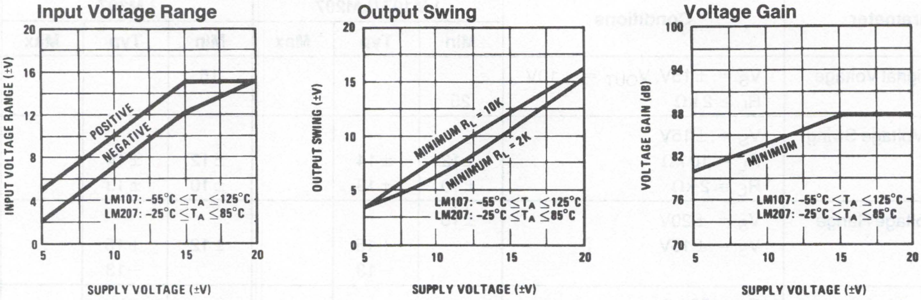
## Schematic Diagram*


V+
7
INPUT +
3
INPUT −
2
Q1
Q3
Q4
Q5
Q6
Q7
R5
40K
Q9
R16
120
C2
30 pF
R6
40K
Q10
Q17
Q16
Q14
Q15
R11
25
6
OUT
C3
2 pF
R14
7.5K
R10
65
R12
620
Q13
Q12
Q11
R7
80K
R8
650
Q18
Q19
R13
450
Q22
Q21
R1
5K
R2
20K
Q20
R3
10K
R4
250
4
V−

*Pin connections shown are for metal can.

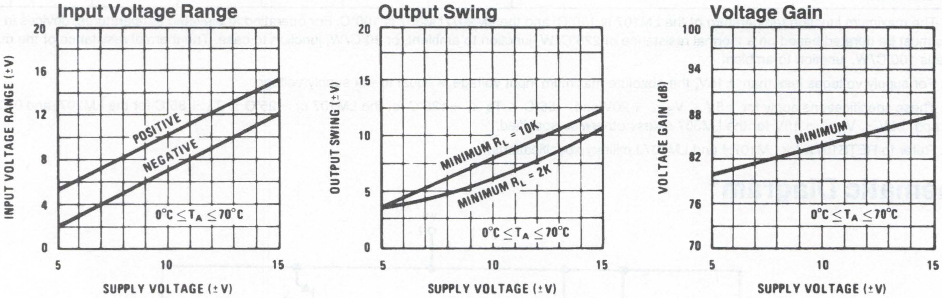
TL/H/7757-1

## Guaranteed Performance Characteristics LM107/LM207



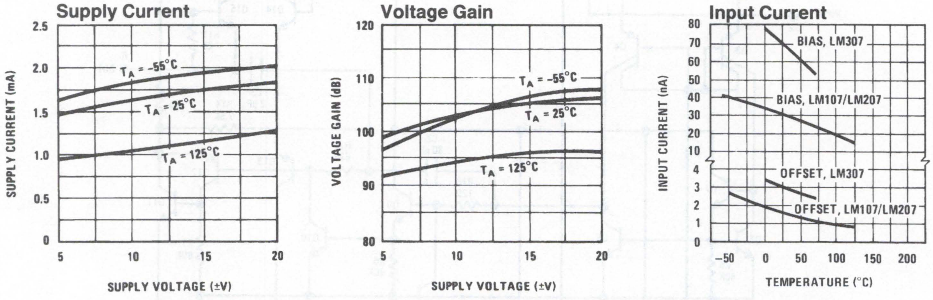
TL/H/7757-4

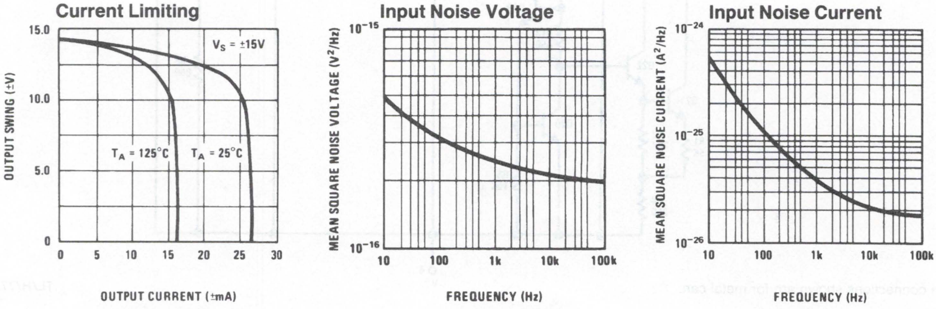
## Guaranteed Performance Characteristics LM307



TL/H/7757-5

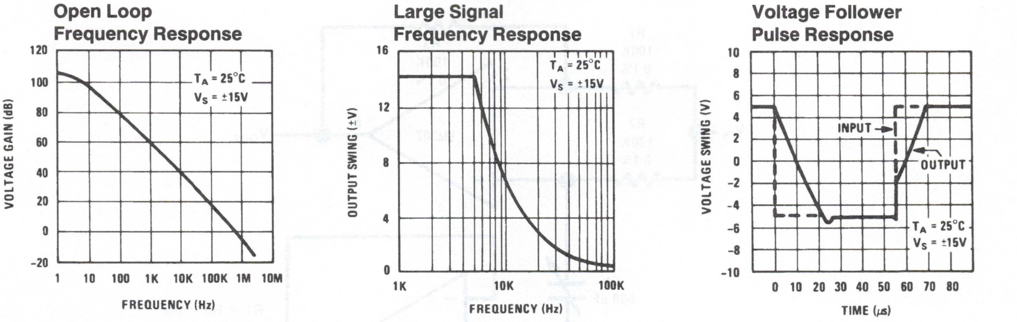
## Typical Performance Characteristics





TL/H/7757-6

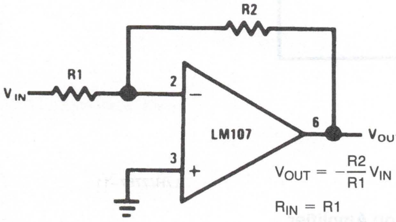
## Typical Performance Characteristics (Continued)



TL/H/7757-7

## Typical Applications**

### Inverting Amplifier

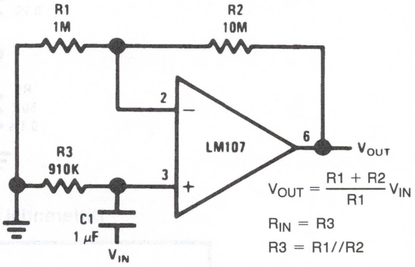

R2
R1
$V_{IN}$
2
3
6
LM107
$V_{OUT}$

$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

$R_{IN} = R1$

TL/H/7757-8

### Non-Inverting AC Amplifier


R1
1M
R2
10M
2
3
6
LM107
$V_{OUT}$
R3
910K
C1
1 μF
$V_{IN}$

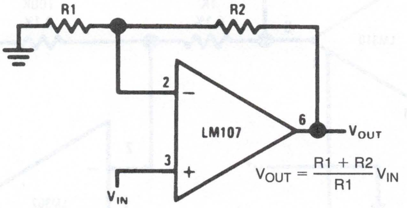
$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

$R_{IN} = R3$

$R3 = R1//R2$

TL/H/7757-9

### Non-Inverting Amplifier


R1
R2
2
3
6
LM107
$V_{OUT}$
$V_{IN}$

$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

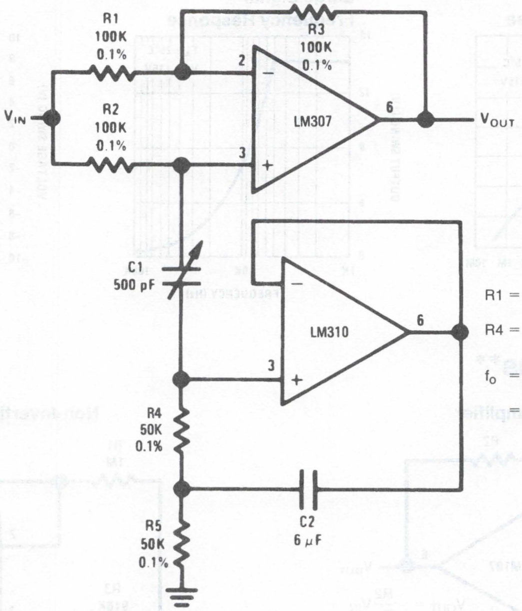
TL/H/7757-10

---

**Pin connections shown are for metal can.

## Typical Applications** (Continued)

### Turntable Notch Filter


R1
100K
0.1%
R2
100K
0.1%
R3
100K
0.1%
V_IN
2
3
6
LM307
V_OUT
C1
500 pF
LM310
6
3
R4
50K
0.1%
R5
50K
0.1%
C2
6 μF

$R1 = R2 = R3$

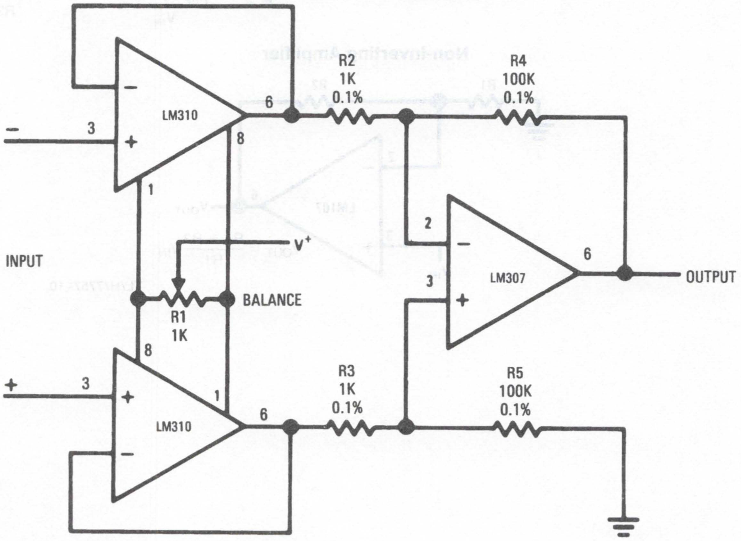
$R4 = R5 = \frac{R1}{2}$

$f_o = \frac{1}{2\pi\sqrt{C_1 C_2 R_4 R_5}}$

$= 60\text{ Hz}$

TL/H/7757–11

### Differential Input Instrumentation Amplifier


−
3
LM310
6
8
1
R2
1K
0.1%
R4
100K
0.1%
INPUT
V⁺
BALANCE
R1
1K
2
3
LM307
6
OUTPUT
+
3
8
1
LM310
6
R3
1K
0.1%
R5
100K
0.1%

TL/H/7757–12

**Pin connections shown are for metal can.

National Semiconductor Corporation

# LM108/LM208/LM308 Operational Amplifiers

## General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

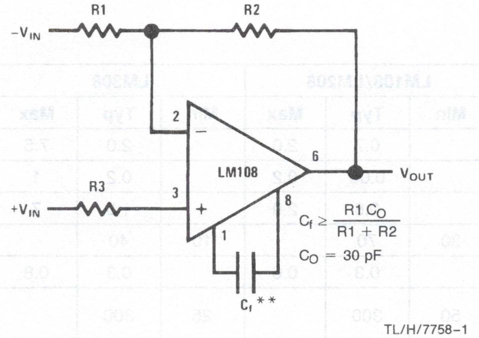
The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

## Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

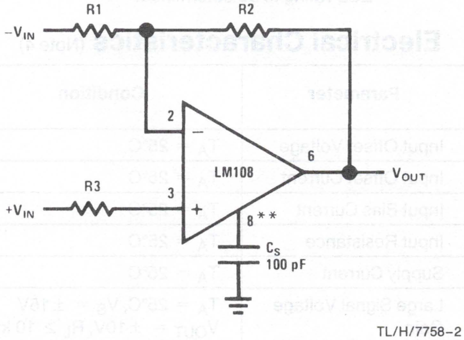
## Compensation Circuits

### Standard Compensation Circuit


R1
R2
$-V_{IN}$
2
−
LM108
6
$V_{OUT}$
R3
3
$+V_{IN}$
+
8
1
$C_f \geq \frac{R1\,C_O}{R1 + R2}$
$C_O = 30$ pF
$C_f$ **
TL/H/7758-1

**Bandwidth and slew rate are proportional to $1/C_f$

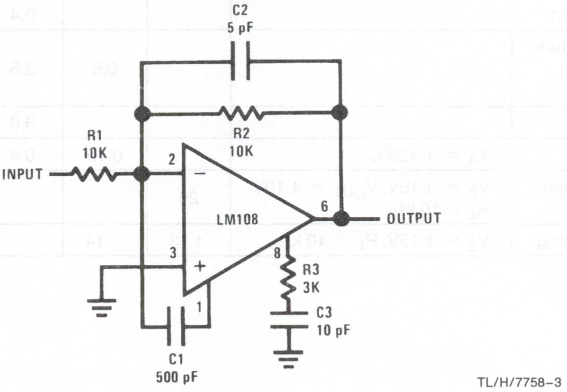
### Alternate* Frequency Compensation


R1
R2
$-V_{IN}$
2
−
LM108
6
$V_{OUT}$
R3
3
$+V_{IN}$
+
8 **
$C_S$
100 pF
TL/H/7758-2

*Improves rejection of power supply noise by a factor of ten.

**Bandwidth and slew rate are proportional to $1/C_S$

### Feedforward Compensation


C2
5 pF
R1
10K
R2
10K
INPUT
2
−
LM108
6
OUTPUT
3
+
8
R3
3K
C3
10 pF
1
C1
500 pF
TL/H/7758-3

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 5)**

| | LM108/LM208 | LM308 |
|---|---|---|
| Supply Voltage | ±20V | ±18V |
| Power Dissipation (Note 1) | 500 mW | 500 mW |
| Differential Input Current (Note 2) | ±10 mA | ±10 mA |
| Input Voltage (Note 3) | ±15V | ±15V |
| Output Short-Circuit Duration | Indefinite | Indefinite |
| Operating Temperature Range (LM108) | −55°C to +125°C | 0°C to +70°C |
| (LM208) | −25°C to +85°C | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C | 260°C |
| DIP | 300°C | 300°C |
| H Package Lead Temp (Soldering 10 seconds) | | |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | |
| Infrared (15 seconds) | 220°C | |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Condition | LM108/LM208 | | | LM308 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 0.05 | 0.2 | | 0.2 | 1 | nA |
| Input Bias Current | $T_A = 25°C$ | | 0.8 | 2.0 | | 1.5 | 7 | nA |
| Input Resistance | $T_A = 25°C$ | 30 | 70 | | 10 | 40 | | MΩ |
| Supply Current | $T_A = 25°C$ | | 0.3 | 0.6 | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = \pm 15V$<br>$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$ | 50 | 300 | | 25 | 300 | | V/mV |
| Input Offset Voltage | | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 15 | | 6.0 | 30 | μV/°C |
| Input Offset Current | | | | 0.4 | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 0.5 | 2.5 | | 2.0 | 10 | pA/°C |
| Input Bias Current | | | | 3.0 | | | 10 | nA |
| Supply Current | $T_A = +125°C$ | | 0.15 | 0.4 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$<br>$R_L \geq 10\ k\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | ±13 | ±14 | | ±13 | ±14 | | V |

## Electrical Characteristics (Note 4) (Continued)

| Parameter | Condition | LM108/LM208 | | | LM308 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | $V_S = \pm 15V$ | ±13.5 | | | ±14 | | | V |
| Common Mode Rejection Ratio | | 85 | 100 | | 80 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 80 | 96 | | 80 | 96 | | dB |

**Note 1:** The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

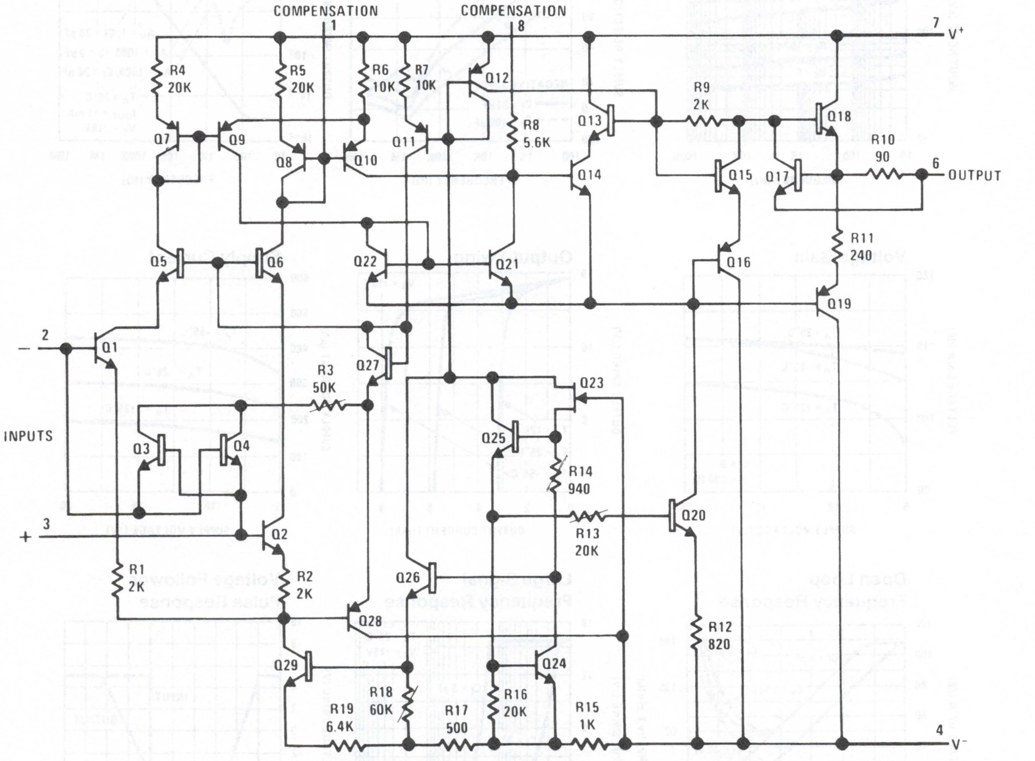
**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm 5V \le V_S \le +20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \le T_A \le 85°C$, and for the LM308 they are limited to $0°C \le T_A \le 70°C$.

**Note 5:** Refer to RETS108X for LM108 military specifications.

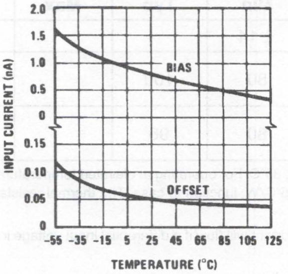
## Schematic Diagram


COMPENSATION
1
COMPENSATION
8
7
V+
R4
20K
R5
20K
R6
10K
R7
10K
Q12
R8
5.6K
R9
2K
Q13
Q18
Q7
Q9
Q8
Q10
Q11
R10
90
6
OUTPUT
Q14
Q15
Q17
R11
240
Q5
Q6
Q22
Q21
Q16
Q19
2
−
Q1
R3
50K
Q27
Q23
INPUTS
Q3
Q4
Q25
R14
940
Q20
3
+
Q2
R13
20K
R1
2K
R2
2K
Q26
Q28
R12
820
Q29
Q24
R19
6.4K
R18
60K
R17
500
R16
20K
R15
1K
4
V−

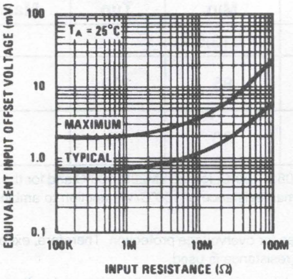
TL/H/7758-8

## Typical Performance Characteristics LM108/LM208

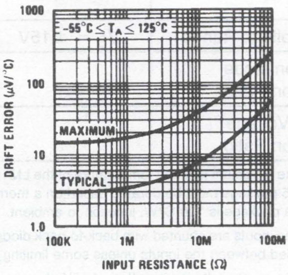
### Input Currents



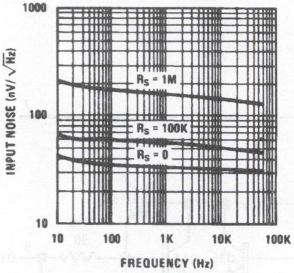
### Offset Error



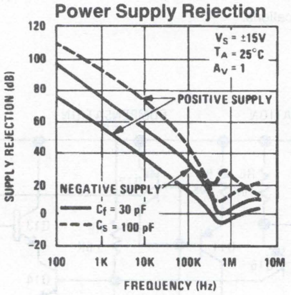
### Drift Error



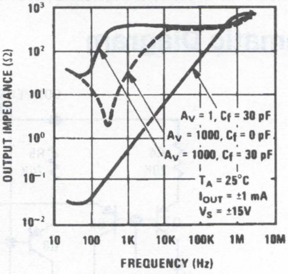
### Input Noise Voltage



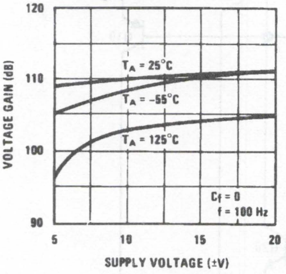
### Power Supply Rejection



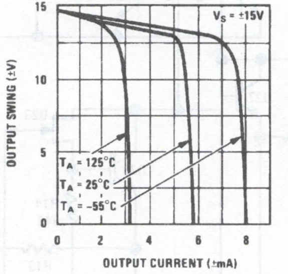
### Closed Loop Output Impedance



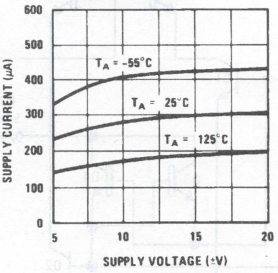
### Voltage Gain



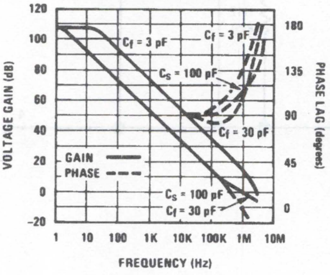
### Output Swing



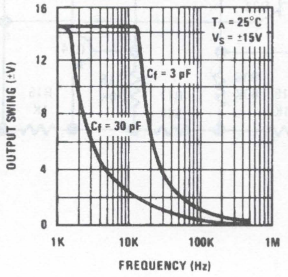
### Supply Current



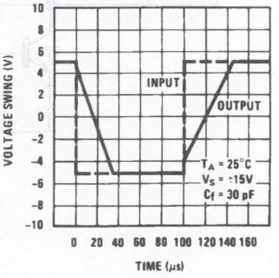
### Open Loop Frequency Response



### Large Signal Frequency Response



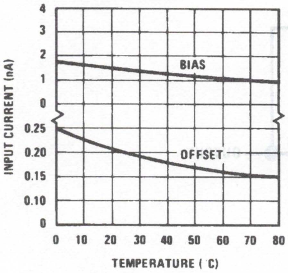
### Voltage Follower Pulse Response



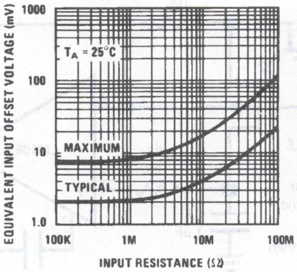
TL/H/7758–6

## Typical Performance Characteristics LM308

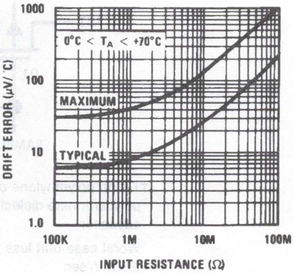
**Input Currents**



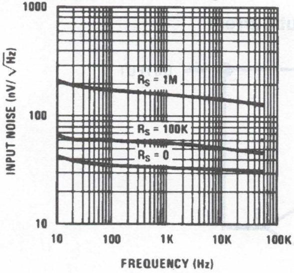
**Offset Error**



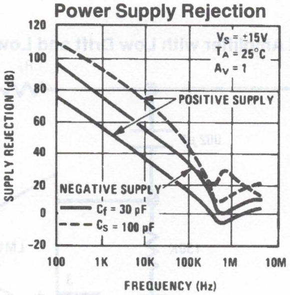
**Drift Error**



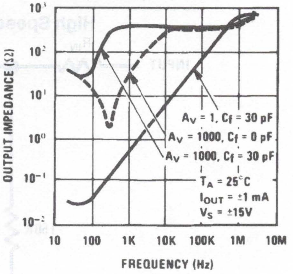
**Input Noise Voltage**



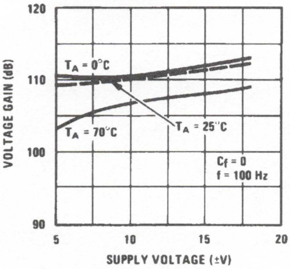
**Power Supply Rejection**



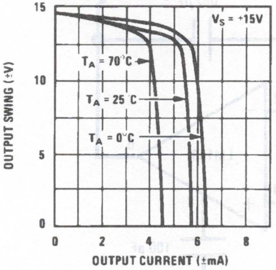
**Closed Loop Output Impedance**



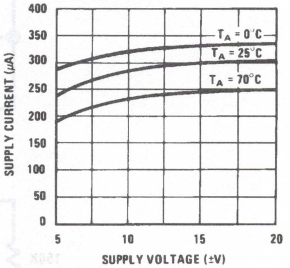
**Voltage Gain**



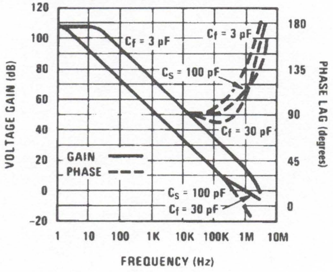
**Output Swing**



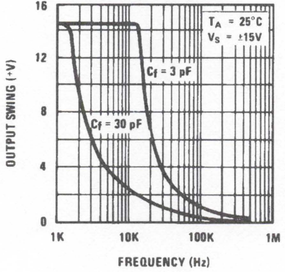
**Supply Current**



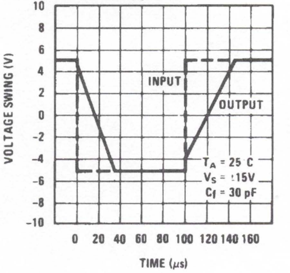
**Open Loop Frequency Response**



**Large Signal Frequency Response**



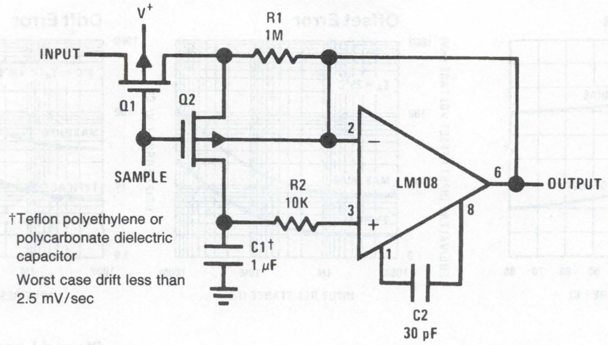
**Voltage Follower Pulse Response**



TL/H/7758-7

## Typical Applications

### Sample and Hold

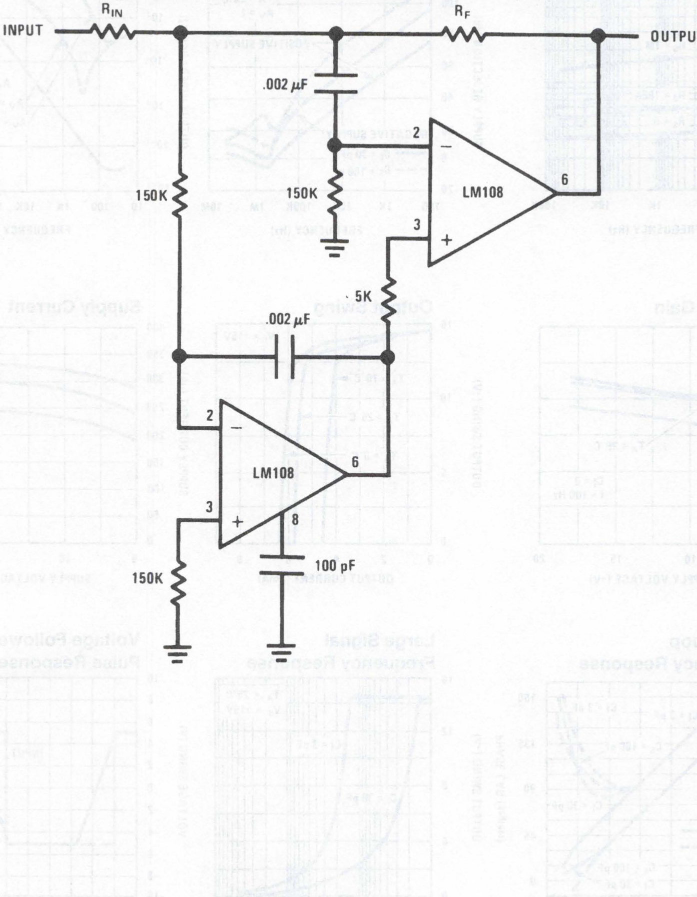

V+
INPUT
R1
1M
Q1
Q2
SAMPLE
2
−
+
3
LM108
6
OUTPUT
R2
10K
8
1
C1†
1 μF
C2
30 pF

†Teflon polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

TL/H/7758-4

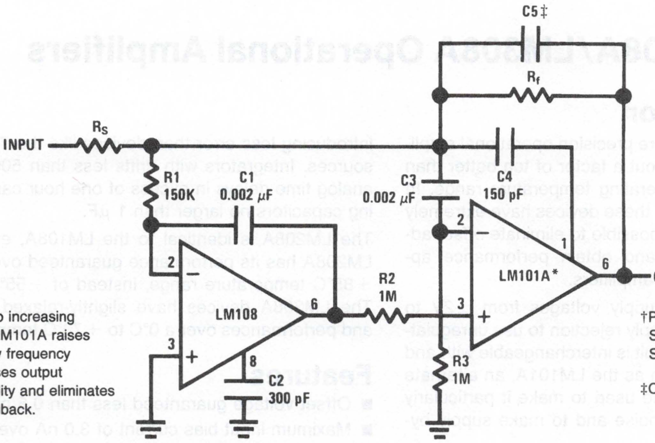
### High Speed Amplifier with Low Drift and Low Input Current


RIN
INPUT
RF
OUTPUT
.002 μF
2
−
LM108
6
3
+
150K
150K
5K
.002 μF
2
−
LM108
6
3
+
8
100 pF
150K

TL/H/7758-5

## Typical Applications (Continued)

### Fast† Summing Amplifier


C5‡
Rf
RS
INPUT
R1
150K
C1
0.002 μF
C3
0.002 μF
C4
150 pF
2
3
6
1
8
LM108
LM101A*
R2
1M
R3
1M
C2
300 pF
OUTPUT

*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

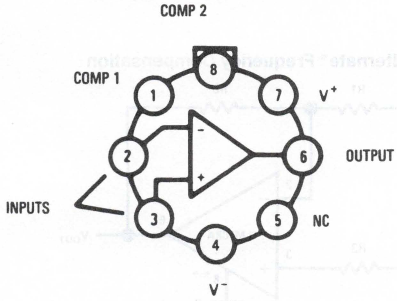
†Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

$$‡C5 = \frac{6 \times 10^{-8}}{R_f}$$

TL/H/7758-12

## Connection Diagrams

### Metal Can Package


COMP 2
COMP 1
8
1
7
V+
2
6
OUTPUT
INPUTS
3
5
NC
4
V−

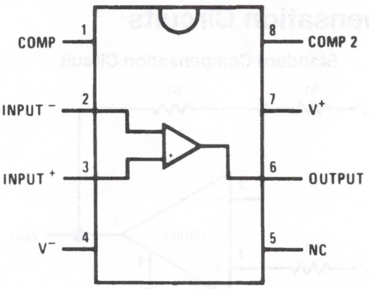
TL/H/7758-13

**Order Number LM108H, LM208H or LM308H**
**See NS Package Number H08C**

*Package is connected to Pin 4 (V−)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

### Dual-In-Line Package


COMP
1
8
COMP 2
INPUT −
2
7
V+
INPUT +
3
6
OUTPUT
V−
4
5
NC

TL/H/7758-15

**Top View**

**Order Number LM108J-8, LM208J-8, LM308J-8, LM308M or LM308N**
**See NS Package Number J08A, M08A or N08E**

**National Semiconductor Corporation**

# LM108A/LM208A/LM308A Operational Amplifiers

## General Description

The LM108/LM108A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±18V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

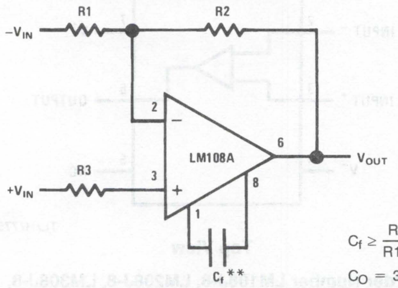
The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a −25°C to +85°C temperature range, instead of −55°C to +125°C. The LM308A devices have slightly-relaxed specifications and performances over a 0°C to +70°C temperature range.

## Features

- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 μV/°C drift

## Compensation Circuits

### Standard Compensation Circuit



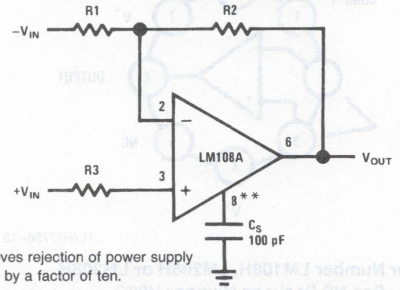
$C_f \geq \frac{R1\,C_O}{R1+R2}$

$C_O = 30$ pF

TL/H/7759–1

**Bandwidth and slew rate are proportional to $1/C_f$.

### Alternate* Frequency Compensation

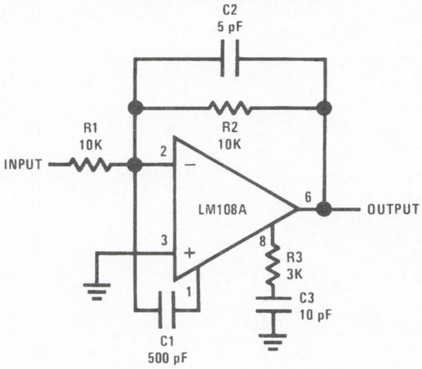


*Improves rejection of power supply noise by a factor of ten.

TL/H/7759–2

**Bandwidth and slew rate are proportional to $1/C_s$.

### Feedforward Compensation



TL/H/7759–3

## LM108A/LM208A Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Free Air Temperature Range | |
| LM108A | −55°C to +125°C |
| LM208A | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) (DIP) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ | | 0.3 | 0.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 0.05 | 0.2 | nA |
| Input Bias Current | $T_A = 25°C$ | | 0.8 | 2.0 | nA |
| Input Resistance | $T_A = 25°C$ | 30 | 70 | | MΩ |
| Supply Current | $T_A = 25°C$ | | 0.3 | 0.6 | mA |
| Large Signal Voltage Gain | $T_A = 25°C, V_S = \pm 15V,$ $V_{OUT} = \pm 10V, R_L \geq 10\ k\Omega$ | 80 | 300 | | V/mV |
| Input Offset Voltage | | | | 1.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 1.0 | 5.0 | µV/°C |
| Input Offset Current | | | | 0.4 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 0.5 | 2.5 | pA/°C |
| Input Bias Current | | | | 3.0 | nA |
| Supply Current | $T_A = 125°C$ | | 0.15 | 0.4 | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V, V_{OUT} = \pm 10V,$ $R_L \geq 10\ k\Omega$ | 40 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V, R_L = 10\ k\Omega$ | ±13 | ±14 | | V |
| Input Voltage Range | $V_S = \pm 15V$ | ±13.5 | | | V |
| Common Mode Rejection Ratio | | 96 | 110 | | dB |
| Supply Voltage Rejection Ratio | | 96 | 110 | | dB |

**Note 1:** The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

**Note 5:** Refer to RETS108AX for LM108AH and LM108AJ-8 military specifications.

## LM308A Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| H-Package Lead Temperature (Soldering, 10 sec.) | 300°C |
| Lead Temperature (Soldering, 10 sec.) (DIP) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ | | 0.3 | 0.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 0.2 | 1 | nA |
| Input Bias Current | $T_A = 25°C$ | | 1.5 | 7 | nA |
| Input Resistance | $T_A = 25°C$ | 10 | 40 | | MΩ |
| Supply Current | $T_A = 25°C$, $V_S = \pm15V$ | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$ | 80 | 300 | | V/mV |
| Input Offset Voltage | $V_S = \pm15V$, $R_S = 100\Omega$ | | | 0.73 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $V_S = \pm15V$, $R_S = 100\Omega$ | | 2.0 | 5.0 | μV/°C |
| Input Offset Current | | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 2.0 | 10 | pA/°C |
| Input Bias Current | | | | 10 | nA |
| Large Signal Voltage Gain | $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$ | 60 | | | V/mV |
| Output Voltage Swing | $V_S = \pm15V$, $R_L = 10\ k\Omega$ | ±13 | ±14 | | V |
| Input Voltage Range | $V_S = \pm15V$ | ±14 | | | V |
| Common Mode Rejection Ratio | | 96 | 110 | | dB |
| Supply Voltage Rejection Ratio | | 96 | 110 | | dB |

**Note 1:** The maximum junction temperature of the LM308A is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

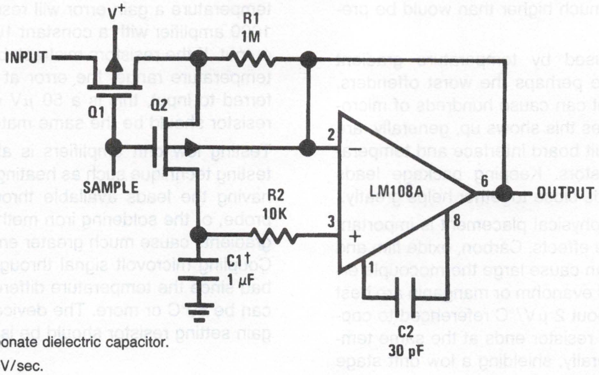
**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm5V \leq V_S \leq \pm15V$ and $0°C \leq T_A \leq +70°C$, unless otherwise specified.

## Typical Applications

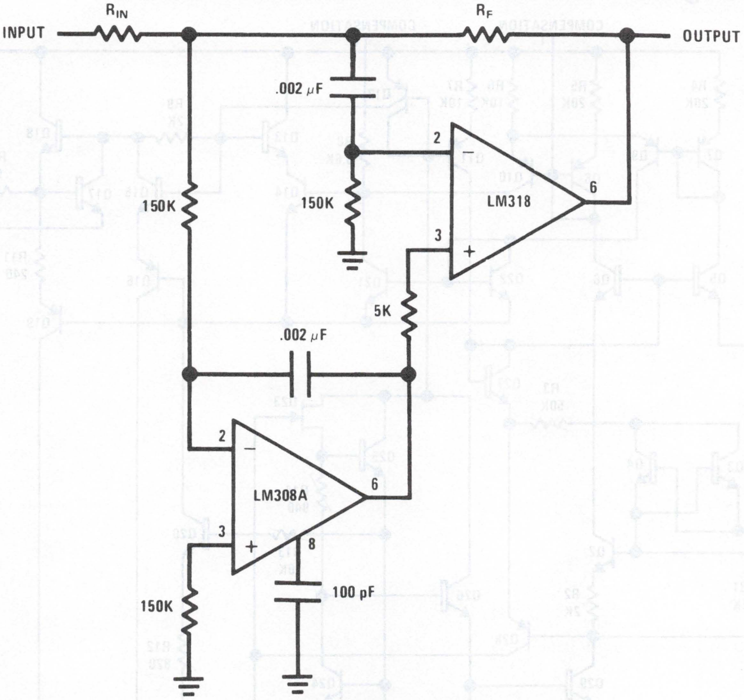
### Sample and Hold


V+
R1
1M
INPUT
Q1
Q2
SAMPLE
R2
10K
C1†
1 μF
2
3
6
8
1
LM108A
OUTPUT
C2
30 pF

†Teflon, polyethylene or polycarbonate dielectric capacitor.
Worst case drift less than 2.5 mV/sec.

TL/H/7759-4

### High Speed Amplifier with Low Drift and Low Input Current


INPUT
R_IN
R_F
OUTPUT
.002 μF
2
6
3
LM318
150K
150K
5K
.002 μF
2
6
3
8
LM308A
100 pF
150K

TL/H/7759-5

## Application Hints

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted.

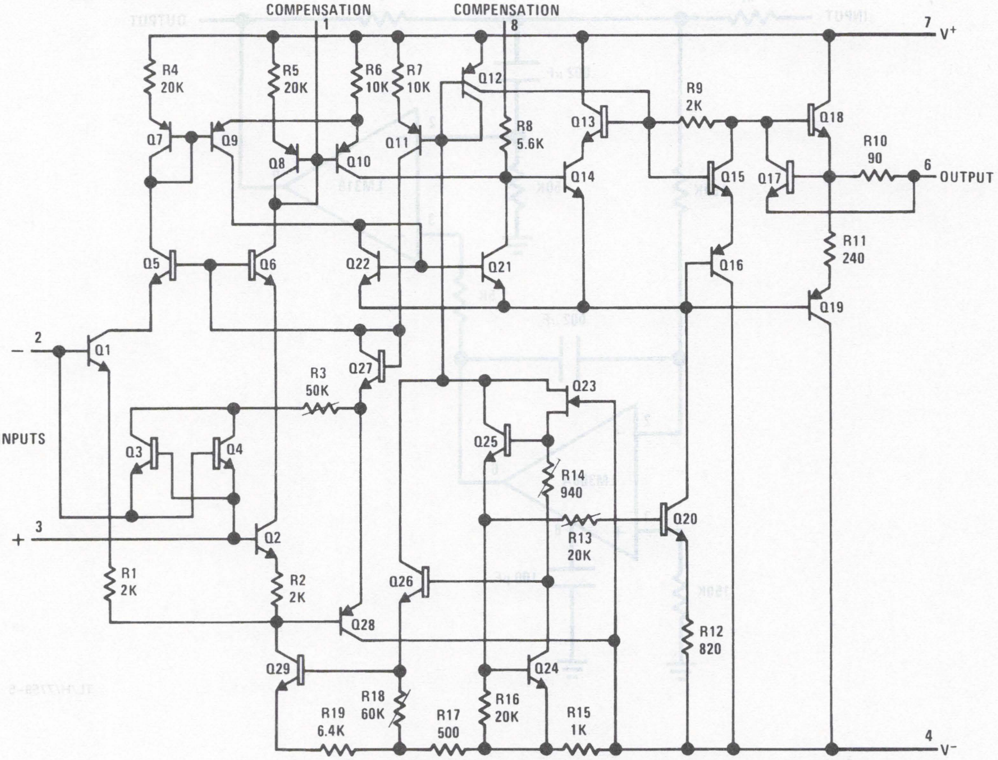
Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally, are the package-to-printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together helps greatly.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evanohm or manganin are best since they only generate about 2 $\mu$V/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example, a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 $\mu$V error. All of the gain fixing resistor should be the same material.

Testing low drift amplifiers is also difficult. Standard drift testing technique such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method—do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal.

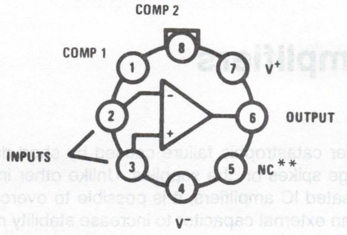
## Schematic Diagram


COMPENSATION
1
COMPENSATION
8
7
V+
R4
20K
R5
20K
R6
10K
R7
10K
Q12
R9
2K
Q7
Q9
Q8
Q10
Q11
R8
5.6K
Q13
Q18
R10
90
6
OUTPUT
Q14
Q15
Q17
Q5
Q6
Q22
Q21
R11
240
Q16
Q19
2
−
Q1
R3
50K
Q27
Q23
INPUTS
Q3
Q4
Q25
R14
940
3
+
Q2
R13
20K
Q20
R1
2K
R2
2K
Q26
Q28
R12
820
Q29
Q24
R19
6.4K
R18
60K
R17
500
R16
20K
R15
1K
4
V−

TL/H/7759–6

## Connection Diagrams

### Metal Can Package


COMP 2
COMP 1
8
1
7
V+
2
6
OUTPUT
INPUTS
3
5
NC**
4
V−

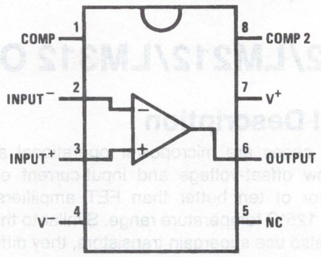
TL/H/7759–7

Pin 4 is connected to the case.

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

**Order Number LM108AH, LM208AH or LM208AH**
**See NS Package Number H08C**

### Dual-In-Line Package


COMP
1
8
COMP 2
INPUT−
2
7
V+
INPUT+
3
6
OUTPUT
V−
4
5
NC

TL/H/7759–8

**Top View**

**Order Number LM108AJ-8, LM208AJ-8, LM308AJ-8, LM308AM or LM308AN**
**See NS Package Number J08A, M08A or N08E**

**National Semiconductor Corporation**

# LM112/LM212/LM312 Operational Amplifiers

## General Description

The LM112 series are micropower operational amplifiers with very low offset-voltage and input-current errors—at least a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range. Similar to the LM108 series, that also use supergain transistors, they differ in that they include internal frequency compensation and have provisions for offset adjustment with a single potentiometer.

These amplifiers will operate on supply voltages of ±2V to ±20V, drawing a quiescent current of only 300 μA. Performance is not appreciably affected over this range of voltages, so operation from unregulated power sources is easily accomplished. They can also be run from a single supply like the 5V used for digital circuits.

The LM112 series are the first IC amplifiers to improve reliability by including overvoltage protection for the MOS compensation capacitor. Without this feature, IC's have been known to suffer catastrophic failure caused by short-duration overvoltage spikes on the supplies. Unlike other internally-compensated IC amplifiers, it is possible to overcompensate with an external capacitor to increase stability margin.

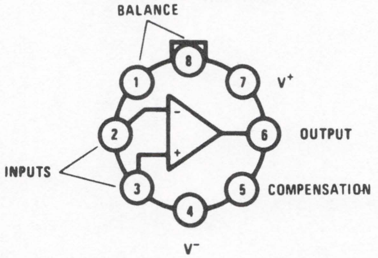
The LM212 is identical to the LM112, except that the LM212 has its performance guaranteed over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM312 is guaranteed over a 0°C to +70°C temperature range.

## Features

- Maximum input bias current of 3 nA over temperature
- Offset current less than 400 pA over temperature
- Low noise
- Guaranteed drift specifications

## Connection Diagram

**Metal Can Package**



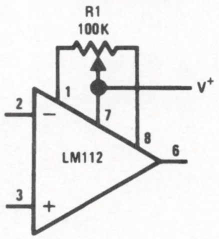
TL/H/7751-4

**Top View**

**Order Number LM112H, LM212H, or LM312H**
**See NS Package Number H08C**

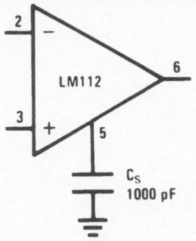
## Auxiliary Circuits

**Offset Balancing**



TL/H/7751-2

**Overcompensation for Greater Stability Margin**



TL/H/7751-3

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)**

| | LM112/LM212 | LM312 |
|---|---|---|
| Supply Voltage | ±20V | ±18V |
| Power Dissipation (Note 1) | 500 mW | 500 mW |
| Differential Input Current (Note 2) | ±10 mA | ±10 mA |
| Input Voltage (Note 3) | ±15V | ±15V |
| Output Short-Circuit Duration | Indefinite | Indefinite |
| Operating Temperature Range | | |
| LM112 | −55°C to +125°C | 0°C to +70°C |
| LM212 | −25°C to +85°C | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM112/LM212 | | | LM312 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 0.05 | 0.2 | | 0.2 | 1 | nA |
| Input Bias Current | $T_A = 25°C$ | | 0.8 | 2.0 | | 1.5 | 7 | nA |
| Input Resistance | $T_A = 25°C$ | 30 | 70 | | 10 | 40 | | MΩ |
| Supply Current | $T_A = 25°C$ | | 0.3 | 0.6 | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = \pm15V$<br>$V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$ | 50 | 300 | | 25 | 300 | | V/mV |
| Input Offset Voltage | | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 15 | | 6.0 | 30 | µV/°C |
| Input Offset Current | | | | 0.4 | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 0.5 | 2.5 | | 2.0 | 10 | pA/°C |
| Input Bias Current | | | | 3.0 | | | 10 | nA |
| Supply Current | $T_A = 125°C$ | | 0.15 | 0.4 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm15V$, $V_{OUT} = \pm10V$<br>$R_L \geq 10\ k\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm15V$, $R_L = 10\ k\Omega$ | ±13 | ±14 | | ±13 | ±14 | | V |
| Input Voltage Range | $V_S = \pm15V$ | ±13.5 | | | ±14 | | | V |
| Common-Mode Rejection Ratio | | 85 | 100 | | 80 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 80 | 96 | | 80 | 96 | | dB |

**Note 1:** The maximum junction temperature of the LM112 is 150°C, LM212 is 100°C and LM312 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

**Note 2:** The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

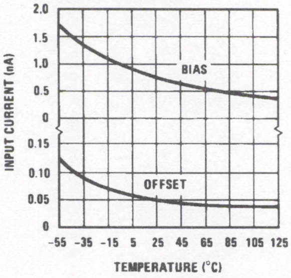
**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq +125°C$ (LM112), $-25°C \leq T_A \leq +85°C$ (LM212), $\pm5V \leq V_S \leq \pm15V$ and $0°C \leq T_A \leq +70°C$ (LM312) unless otherwise noted.

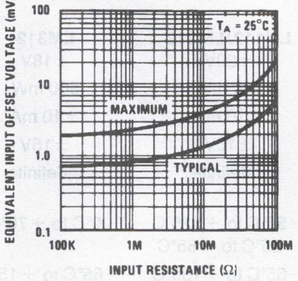
**Note 5:** Refer to RETS112X for LM112H military specifications.

## Typical Performance Characteristics LM112/LM212

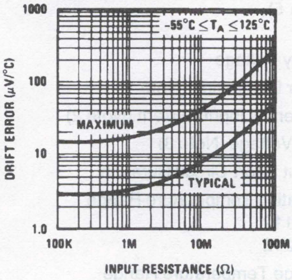
### Input Currents



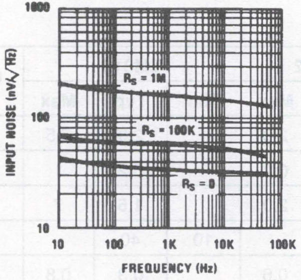
### Offset Error



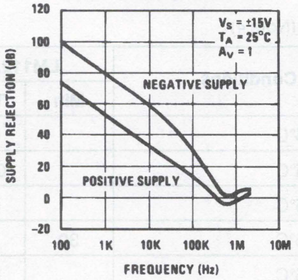
### Drift Error



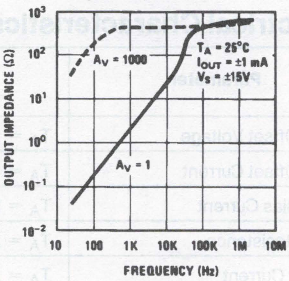
### Input Noise Voltage



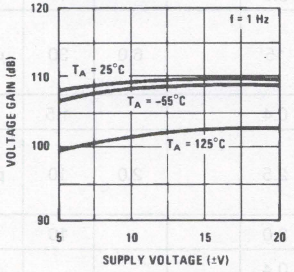
### Power Supply Rejection



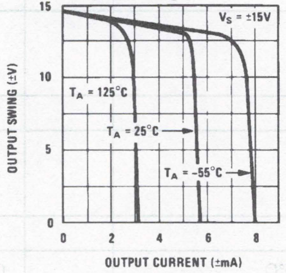
### Closed Loop Output Impedance



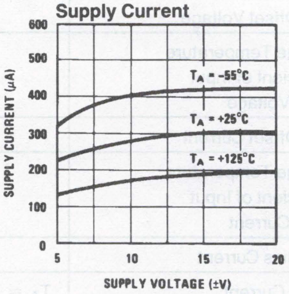
### Voltage Gain



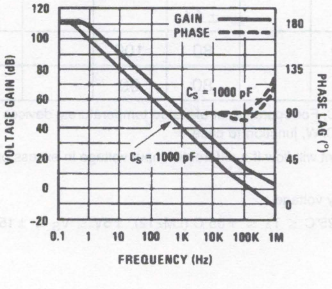
### Output Swing



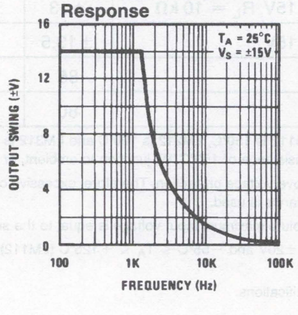
### Supply Current



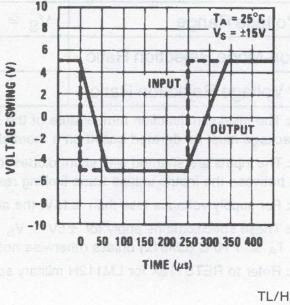
### Open Loop Frequency Response



### Large Signal Frequency Response



### Voltage Follower Pulse Response



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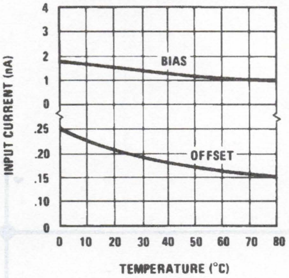
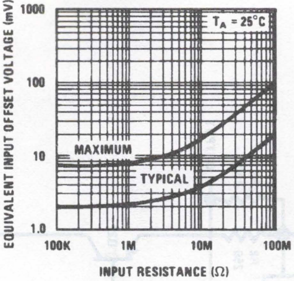
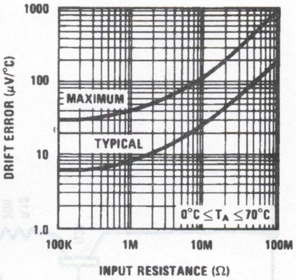
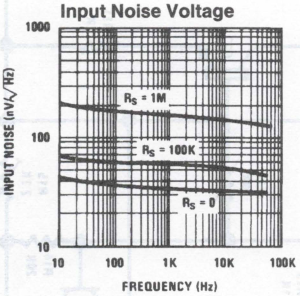
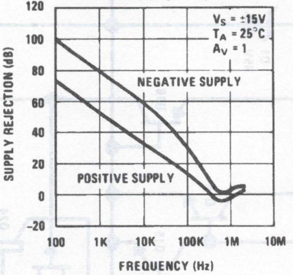
## Typical Performance Characteristics LM312

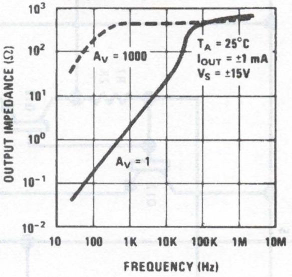

Input Currents

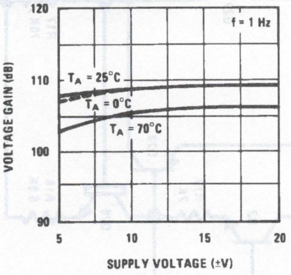

Offset Error

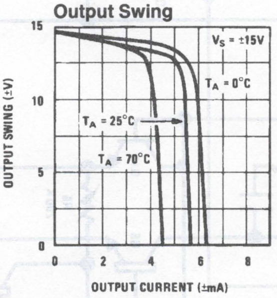

Drift Error

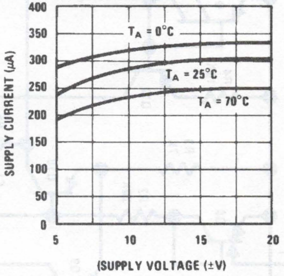

Input Noise Voltage

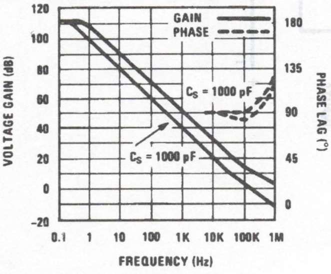

Power Supply Rejection

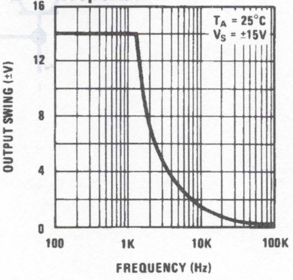

Closed Loop Output Impedance

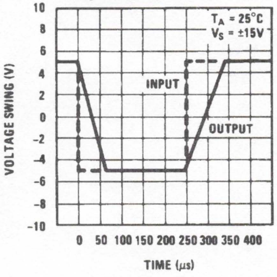

Voltage Gain


Output Swing


Supply Current

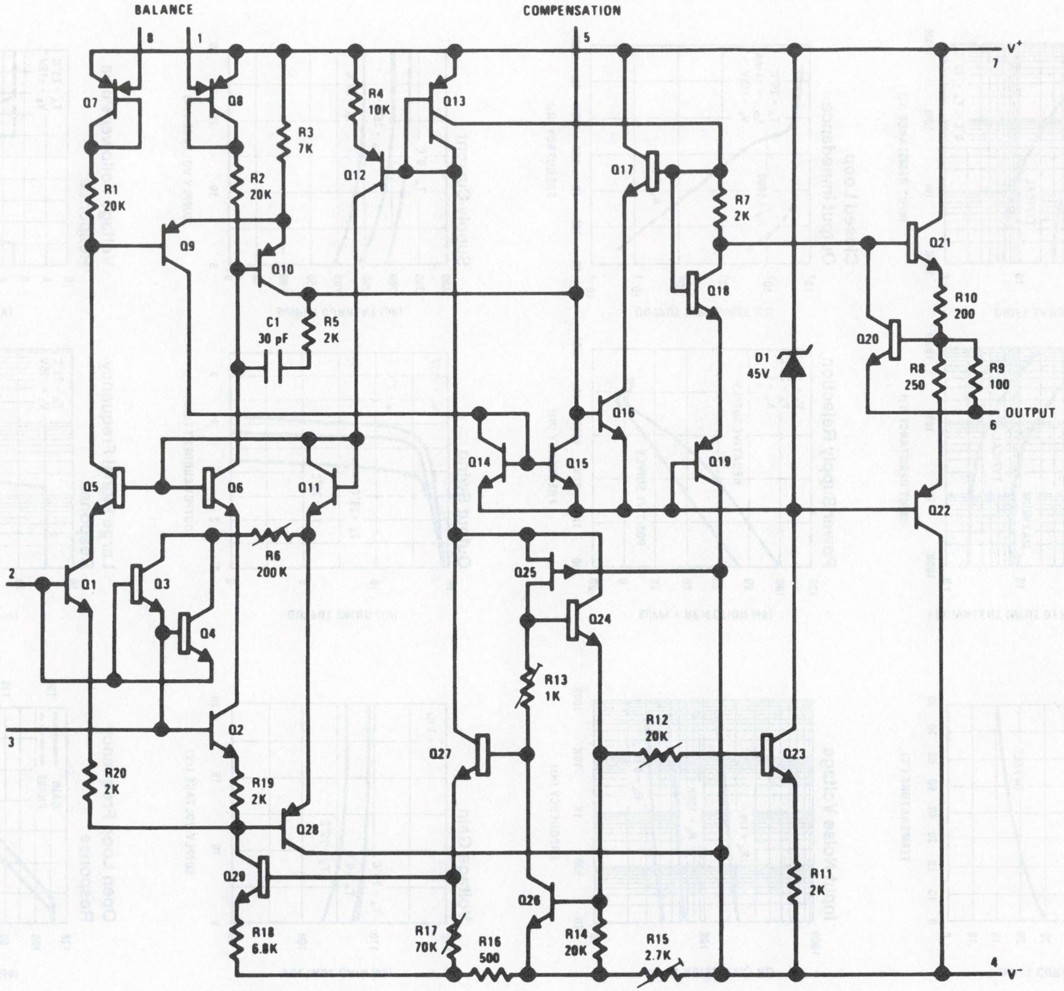

Open Loop Frequency Response


Large Signal Frequency Response


Voltage Follower Pulse Response

TL/H/7751–6

## Schematic Diagram


BALANCE
8
1
COMPENSATION
5
V+
7
Q7
Q8
R1
20K
R2
20K
R3
7K
R4
10K
Q12
Q13
Q9
Q10
C1
30 pF
R5
2K
Q17
R7
2K
Q18
Q21
R10
200
Q20
R8
250
R9
100
OUTPUT
6
D1
45V
Q16
Q14
Q15
Q19
Q22
Q5
Q6
Q11
R6
200K
2
−
Q1
Q3
Q4
INPUTS
+
3
Q2
Q25
Q24
R13
1K
R12
20K
Q27
Q23
R20
2K
R19
2K
Q28
Q29
R11
2K
R18
6.8K
R17
70K
R16
500
Q26
R14
20K
R15
2.7K
4
V−

TL/H/7751–1

**National Semiconductor Corporation**

# LM118/LM218/LM318 Operational Amplifiers

## General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

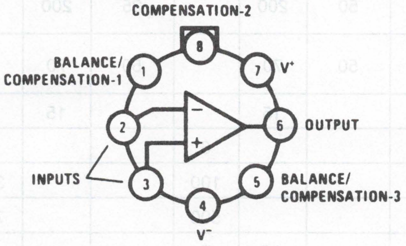
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

## Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

## Connection Diagrams

**Metal Can Package***



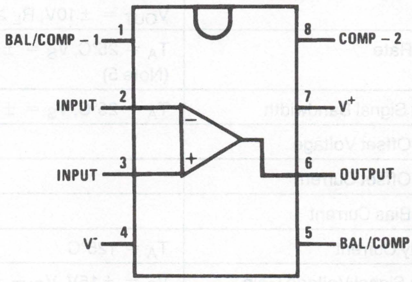
TL/H/7766-2

**Top View**

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

**Order Number LM118H, LM218H or LM318H**
**See NS Package Number H08C**

**Dual-In-Line Package**



TL/H/7766-3

**Top View**

**Order Number LM118J-8, LM318J-8, LM318M or LM318N**
**See NS Package Number J08A, M08A or N08B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**
**(Note 6)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | |
| LM118 | −55°C to +125°C |
| LM218 | −25°C to +85°C |
| LM318 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | |
| Hermetic Package | 300°C |
| Plastic Package | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM118/LM218 | | | LM318 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 2 | 4 | | 4 | 10 | mV |
| Input Offset Current | $T_A = 25°C$ | | 6 | 50 | | 30 | 200 | nA |
| Input Bias Current | $T_A = 25°C$ | | 120 | 250 | | 150 | 500 | nA |
| Input Resistance | $T_A = 25°C$ | 1 | 3 | | 0.5 | 3 | | MΩ |
| Supply Current | $T_A = 25°C$ | | 5 | 8 | | 5 | 10 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = \pm 15V$<br>$V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$ | 50 | 200 | | 25 | 200 | | V/mV |
| Slew Rate | $T_A = 25°C$, $V_S = \pm 15V$, $A_V = 1$<br>(Note 5) | 50 | 70 | | 50 | 70 | | V/μs |
| Small Signal Bandwidth | $T_A = 25°C$, $V_S = \pm 15V$ | | 15 | | | 15 | | MHz |
| Input Offset Voltage | | | | 6 | | | 15 | mV |
| Input Offset Current | | | | 100 | | | 300 | nA |
| Input Bias Current | | | | 500 | | | 750 | nA |
| Supply Current | $T_A = 125°C$ | | 4.5 | 7 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$<br>$R_L \geq 2\ k\Omega$ | 25 | | | 20 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 2\ k\Omega$ | ±12 | ±13 | | ±12 | ±13 | | V |
| Input Voltage Range | $V_S = \pm 15V$ | ±11.5 | | | ±11.5 | | | V |
| Common-Mode Rejection Ratio | | 80 | 100 | | 70 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 70 | 80 | | 65 | 80 | | dB |

**Note 1:** The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

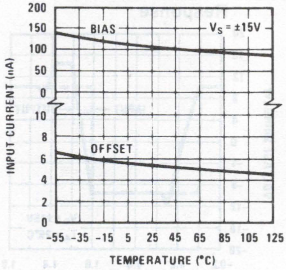
**Note 4:** These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM118), $-25°C \leq T_A \leq +85°C$ (LM218), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

**Note 5:** Slew rate is tested with $V_S = \pm 15V$. The LM118 is in a unity-gain non-inverting configuration. $V_{IN}$ is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

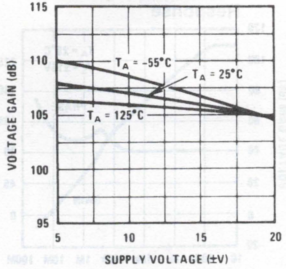
**Note 6:** Refer to RETS118X for LM118H and LM118J-8 military specifications.

## Typical Performance Characteristics LM118, LM218

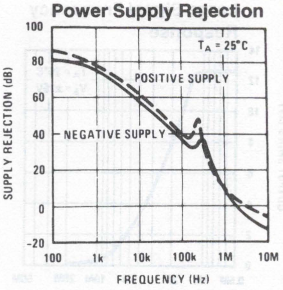
### Input Current



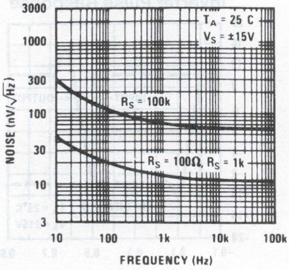
### Voltage Gain



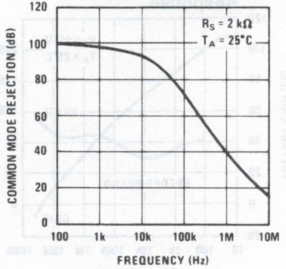
### Power Supply Rejection



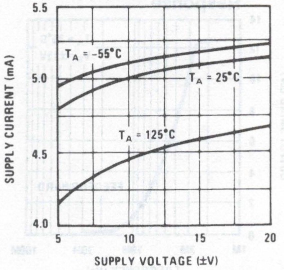
### Input Noise Voltage



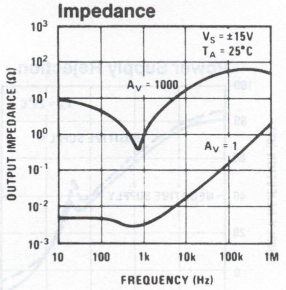
### Common Mode Rejection



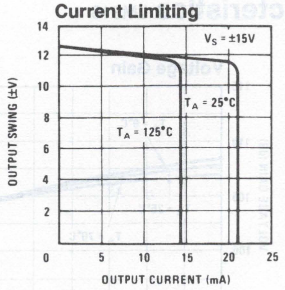
### Supply Current



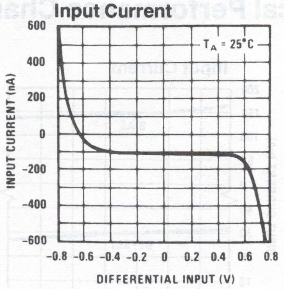
### Closed Loop Output Impedance



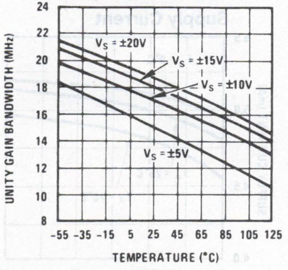
### Current Limiting



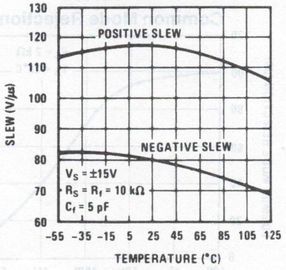
### Input Current



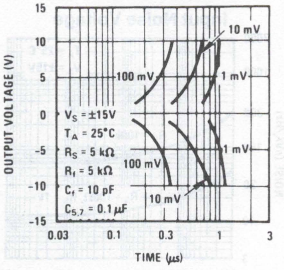
### Unity Gain Bandwidth



### Voltage Follower Slew Rate



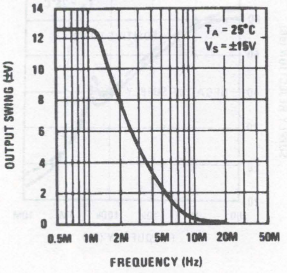
### Inverter Settling Time



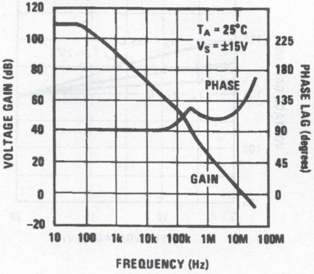
TL/H/7766–4

## Typical Performance Characteristics LM118, LM218 (Continued)

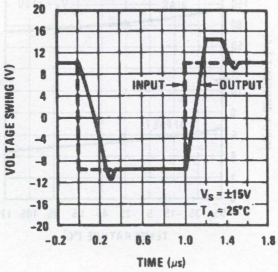
### Large Signal Frequency Response



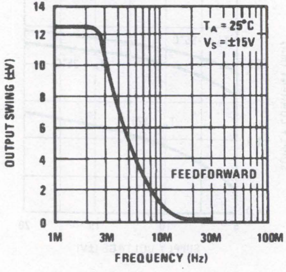
### Open Loop Frequency Response



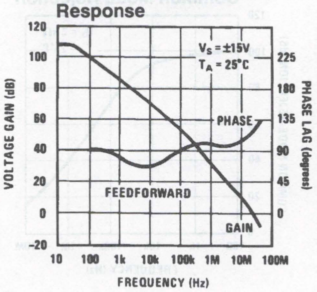
### Voltage Follower Pulse Response



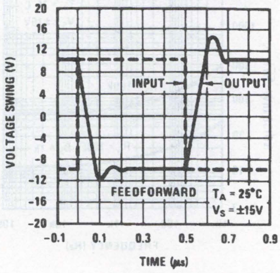
### Large Signal Frequency Response



### Open Loop Frequency Response



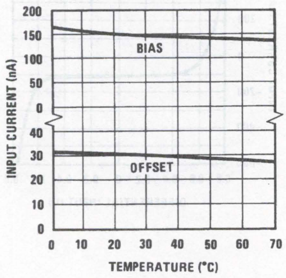
### Inverter Pulse Response



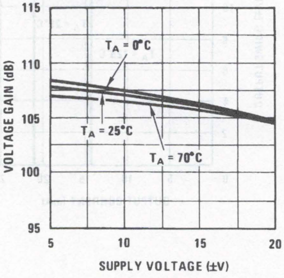
TL/H/7766–5

## Typical Performance Characteristics LM318

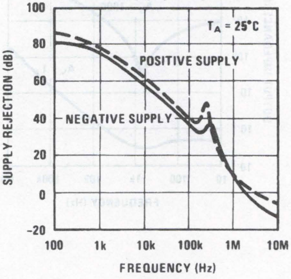
### Input Current



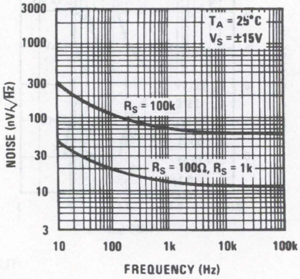
### Voltage Gain



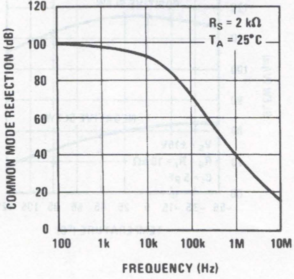
### Power Supply Rejection



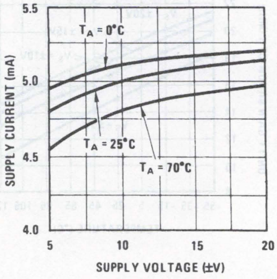
### Input Noise Voltage



### Common Mode Rejection



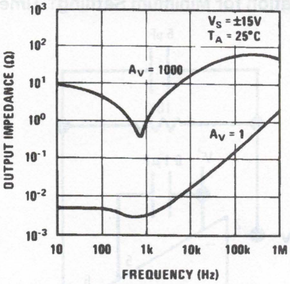
### Supply Current



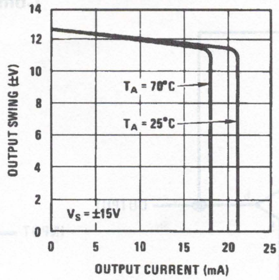
TL/H/7766–6

## Typical Performance Characteristics LM318 (Continued)

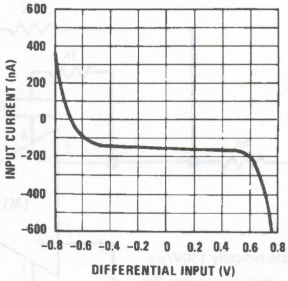
**Closed Loop Output Impedance**



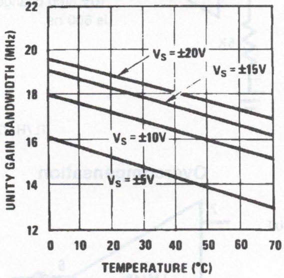
**Current Limiting**



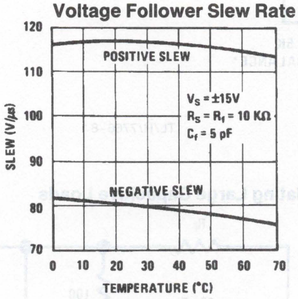
**Input Current**



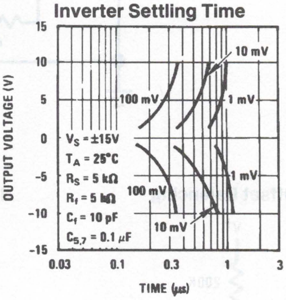
**Unity Gain Bandwidth**



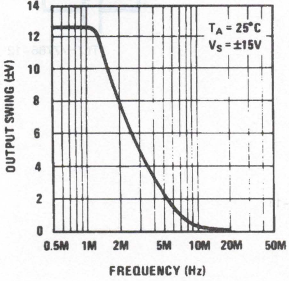
**Voltage Follower Slew Rate**



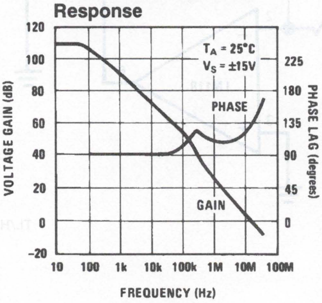
**Inverter Settling Time**



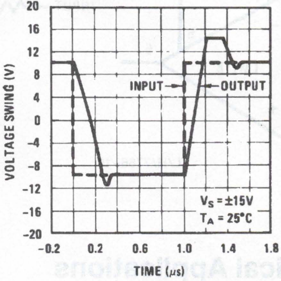
**Large Signal Frequency Response**



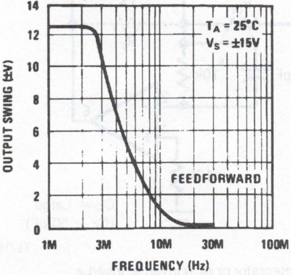
**Open Loop Frequency Response**



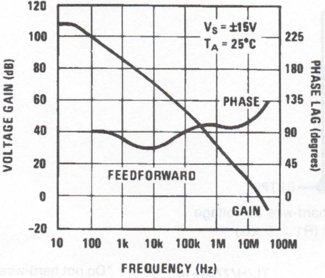
**Voltage Follower Pulse Response**



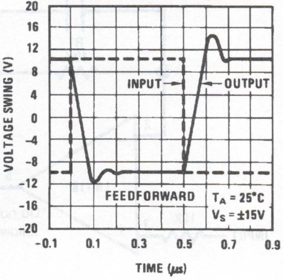
**Large Signal Frequency Response**



**Open Loop Frequency Response**



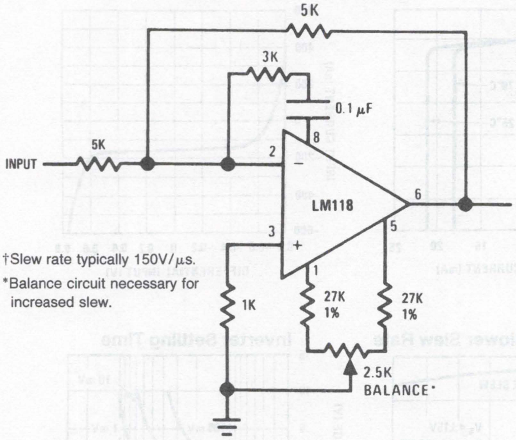
**Inverter Pulse Response**



TL/H/7766–7

# Auxiliary Circuits

### Feedforward Compensation for Greater Inverting Slew Rate†

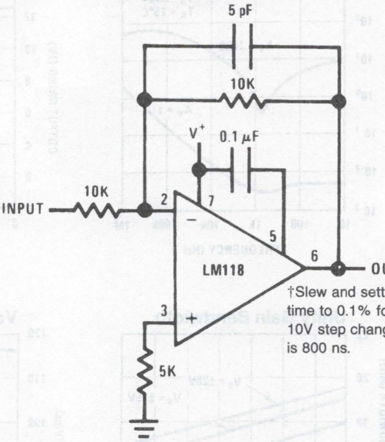

5K
3K
0.1 µF
INPUT
5K
8
2
LM118
6
OUTPUT
3
5
1
1K
27K 1%
27K 1%
2.5K
BALANCE*

†Slew rate typically 150V/µs.

*Balance circuit necessary for increased slew.

TL/H/7766-8

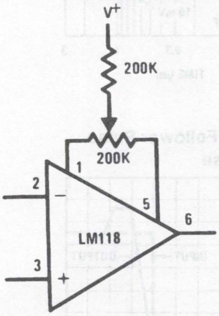
### Compensation for Minimum Settling† Time


5 pF
10K
V+
0.1 µF
10K
INPUT
2
7
5
LM118
6
OUTPUT
3
5K

†Slew and settling time to 0.1% for a 10V step change is 800 ns.

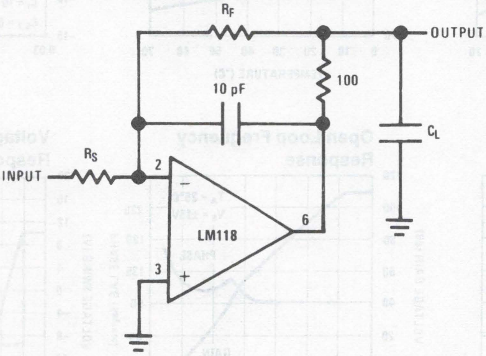
TL/H/7766-9

### Offset Balancing


V+
200K
200K
1
2
5
6
LM118
3

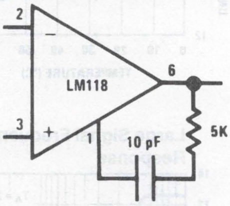
TL/H/7766-10

### Isolating Large Capacitive Loads


$R_F$
OUTPUT
10 pF
100
$C_L$
$R_S$
INPUT
2
6
LM118
3

TL/H/7766-11

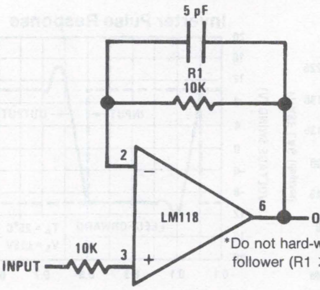
### Overcompensation


2
6
LM118
3
1
5K
10 pF

TL/H/7766-12

# Typical Applications

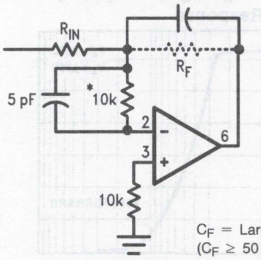
### Fast Voltage Follower*


5 pF
R1
10K
2
LM118
6
OUTPUT
10K
INPUT
3

*Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

TL/H/7766-13

### Integrator or Slow Inverter


$R_{IN}$
$R_F$
5 pF
*
10k
2
6
3
10k

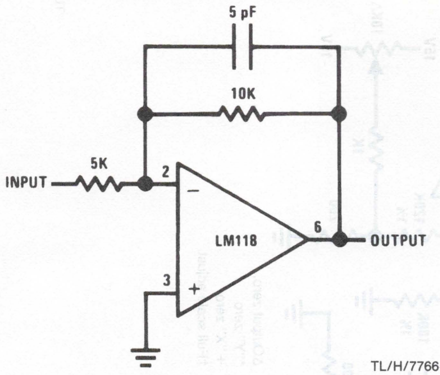
$C_F$ = Large ($C_F \geq 50$ pF)

TL/H/7766-14

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

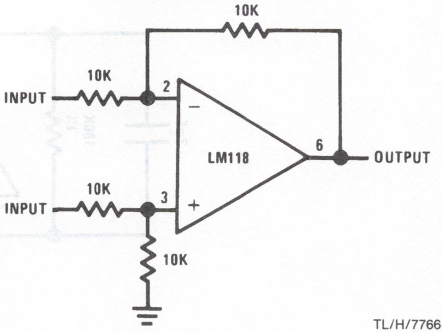
## Typical Applications (Continued)

### Fast Summing Amplifier


5 pF
10K
5K
INPUT
2
3
6
LM118
OUTPUT

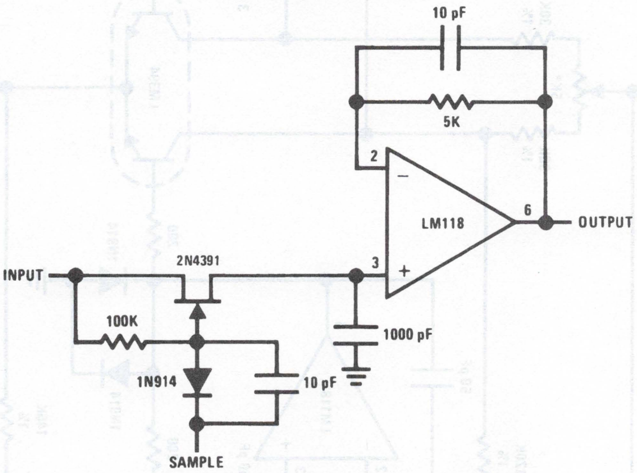
TL/H/7766-15

### Differential Amplifier


10K
10K
INPUT
10K
INPUT
2
3
6
LM118
OUTPUT
10K

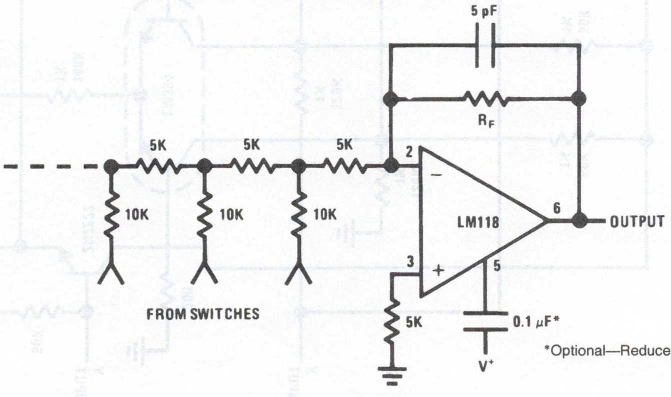
TL/H/7766-16

### Fast Sample and Hold


10 pF
5K
2
3
6
LM118
OUTPUT
INPUT
2N4391
100K
1N914
10 pF
1000 pF
SAMPLE

TL/H/7766-18

### D/A Converter Using Ladder Network

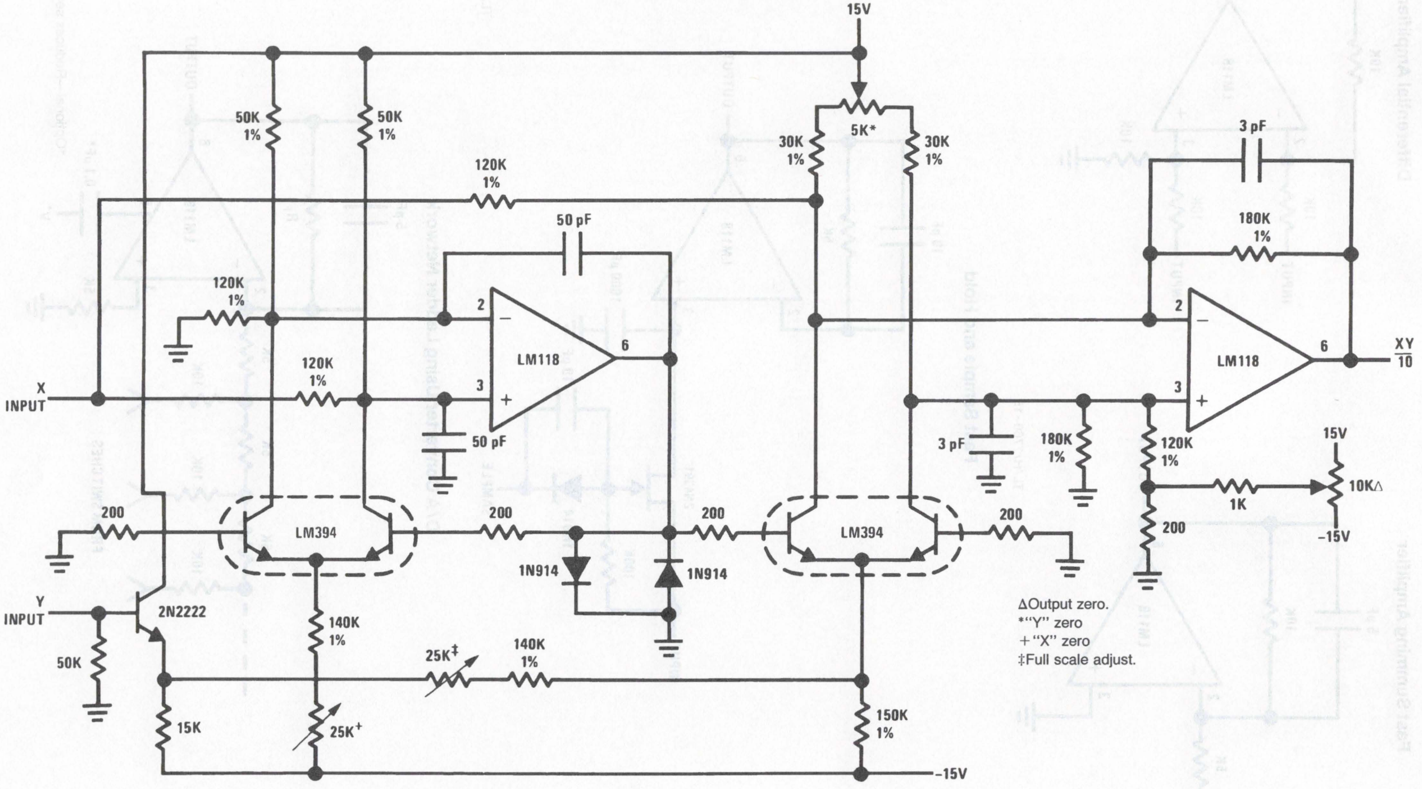

5 pF
$R_F$
5K
5K
5K
10K
10K
10K
FROM SWITCHES
2
3
5
6
LM118
OUTPUT
5K
0.1 μF*
V⁺

*Optional—Reduces settling time.

TL/H/7766-19

## Typical Applications (Continued)

### Four Quadrant Multiplier

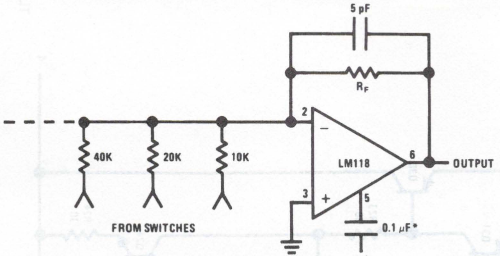

15V
50K
1%
50K
1%
120K
1%
30K
1%
5K*
30K
1%
3 pF
180K
1%
50 pF
120K
1%
2
LM118
6
120K
1%
3
X
INPUT
50 pF
200
LM394
200
200
LM394
200
1N914
1N914
Y
INPUT
2N2222
50K
15K
140K
1%
25K+
25K‡
140K
1%
150K
1%
−15V
2
LM118
6
XY
10
3
3 pF
180K
1%
120K
1%
1K
15V
10KΔ
−15V
200

ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

TL/H/7766–17

## Typical Applications (Continued)

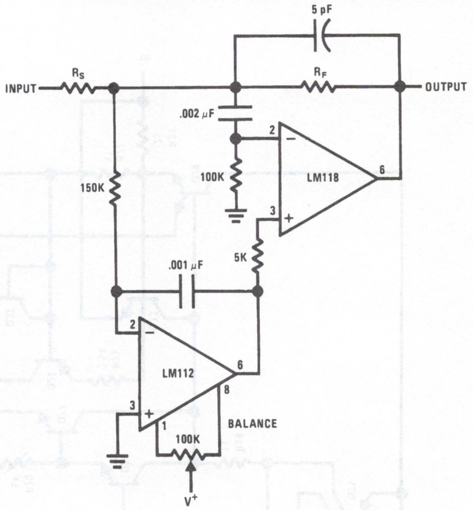
### D/A Converter Using Binary Weighted Network


5 pF
$R_F$
2
3
6
5
LM118
OUTPUT
40K
20K
10K
FROM SWITCHES
0.1 μF*
V⁻

*Optional—Reduces settling time.

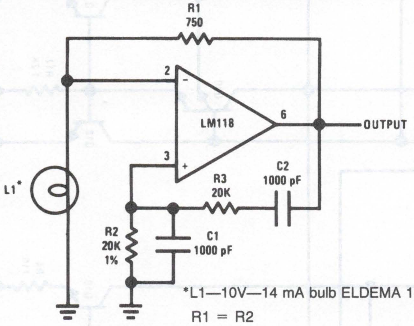
TL/H/7766-20

### Fast Summing Amplifier with Low Input Current


5 pF
$R_S$
$R_F$
INPUT
OUTPUT
.002 μF
100K
LM118
2
3
6
150K
5K
.001 μF
LM112
2
3
6
8
1
BALANCE
100K
V⁺

TL/H/7766-21

### Wein Bridge Sine Wave Oscillator


R1
750
2
3
6
LM118
OUTPUT
L1*
R3
20K
C2
1000 pF
R2
20K
1%
C1
1000 pF

*L1—10V—14 mA bulb ELDEMA 1869

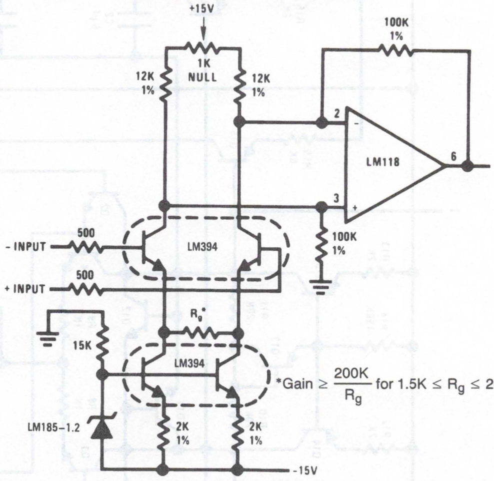
R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\,C1}$$

TL/H/7766-22

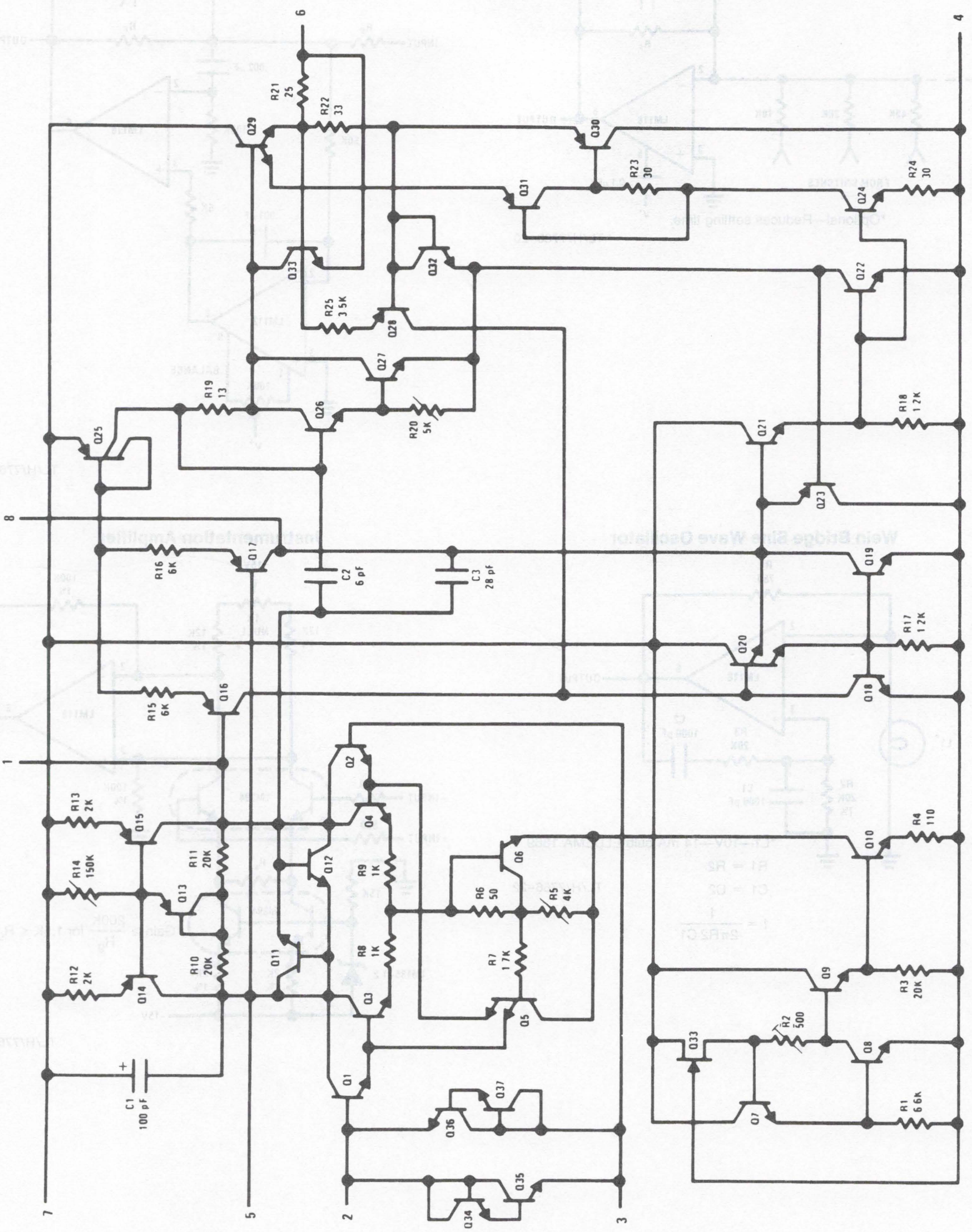
### Instrumentation Amplifier


+15V
1K
NULL
12K
1%
12K
1%
100K
1%
2
3
6
LM118
100K
1%
500
− INPUT
500
+ INPUT
LM394
$R_g$*
15K
LM394
LM185-1.2
2K
1%
2K
1%
−15V

$$\text{*Gain} \geq \frac{200K}{R_g} \text{ for } 1.5K \leq R_g \leq 200K$$

TL/H/7766-23

## Schematic Diagram


Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
R1 6.6k
R2 500
R3 20K
R4 110
R5 4K
R6 50
R7 1.7K
R8 1K
R9 1K
R10 20K
R11 20K
R12 2K
R13 2K
R14 150K
R15 6K
R16 6K
R17 1.2K
R18 1.2K
R19 13
R20 5K
R21 25
R22 33
R23 30
R24 30
R25 3.5K
C1 100 pF
C2 6 pF
C3 28 pF
1
2
3
4
5
6
7
8

TL/H/7766–1

**National Semiconductor Corporation**

# LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

## General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard $+5\ V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15\ V_{DC}$ power supplies.

## Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

## Advantages

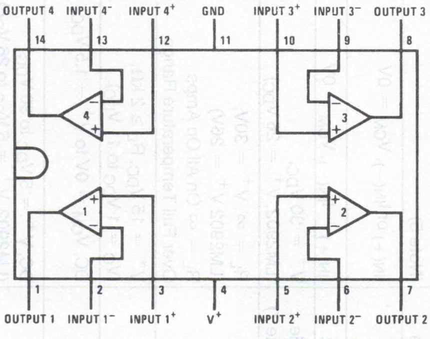
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and $V_{OUT}$ also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

## Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply $3\ V_{DC}$ to $32\ V_{DC}$
  - or dual supplies $\pm 1.5\ V_{DC}$ to $\pm 16\ V_{DC}$
- Very low supply current drain (800 μA)—essentially independent of supply voltage (1 mW/op amp at $+5\ V_{DC}$)
- Low input biasing current $45\ nA_{DC}$ (temperature compensated)
- Low input offset voltage $2\ mV_{DC}$ and offset current $5\ nA_{DC}$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing $0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$

## Connection Diagram

### Dual-In-Line Package



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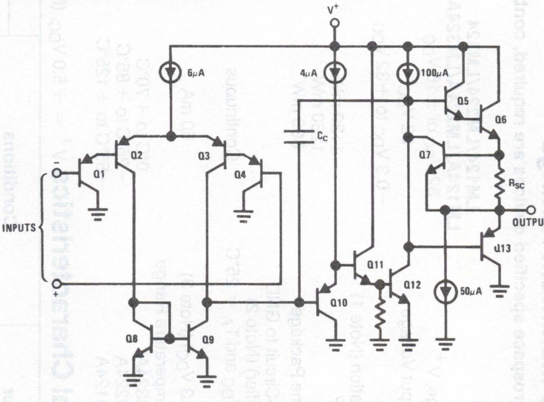
**Top View**

**Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N**
**See NS Package Number J14A, M14A or N14A**

## Schematic Diagram (Each Amplifier)



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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)**

| | LM124/LM224/LM324<br>LM124A/LM224A/LM324A | LM2902 |
|---|---|---|
| Supply Voltage, $V^+$ | $32\ V_{DC}$ or $\pm 16\ V_{DC}$ | $26\ V_{DC}$ or $\pm 13\ V_{DC}$ |
| Differential Input Voltage | $32\ V_{DC}$ | $26\ V_{DC}$ |
| Input Voltage | $-0.3\ V_{DC}$ to $+32\ V_{DC}$ | $-0.3\ V_{DC}$ to $+26\ V_{DC}$ |
| Power Dissipation (Note 1) | | |
| Molded DIP | 1130 mW | 1130 mW |
| Cavity DIP | 1260 mW | 1260 mW |
| Small Outline Package | 800 mW | 800 mW |
| Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \le 15\ V_{DC}$ and $T_A = 25°C$ | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3) | 50 mA | 50 mA |
| Operating Temperature Range | | −40°C to +85°C |
| LM324/LM324A | 0°C to +70°C | |
| LM224/LM224A | −25°C to +85°C | |
| LM124/LM124A | −55°C to +125°C | |

| | LM124/LM224/LM324<br>LM124A/LM224A/LM324A | LM2902 |
|---|---|---|
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics $V^+ = +5.0\ V_{DC}$, (Note 4), unless otherwise stated

| Parameter | Conditions | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 5) | | ±1 | ±2 | | ±1 | ±3 | | ±2 | ±3 | | ±2 | ±5 | | ±2 | ±7 | | ±2 | ±7 | $mV_{DC}$ |
| Input Bias Current (Note 6) | $I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$ | | 20 | 50 | | 40 | 80 | | 45 | 100 | | 45 | 150 | | 45 | 250 | | 45 | 250 | $nA_{DC}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | ±2 | ±10 | | ±2 | ±15 | | ±5 | ±30 | | ±3 | ±30 | | ±5 | ±50 | | ±5 | ±50 | $nA_{DC}$ |
| Input Common-Mode Voltage Range (Note 7) | $V^+ = 30\ V_{DC}$, (LM2902, $V^+ = 26\ V_{DC}$) | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | $V_{DC}$ |
| Supply Current | $R_L = \infty$, $V^+ = 30V$, (LM2902 $V^+ = 26V$)<br>$R_L = \infty$ On All Op Amps Over Full Temperature Range | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | $mA_{DC}$ |
| Large Signal Voltage Gain | $V^+ = 15\ V_{DC}$, $R_L \ge 2\ k\Omega$, ($V_O = 1\ V_{DC}$ to $11\ V_{DC}$) | 50 | 100 | | 50 | 100 | | 25 | 100 | | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |
| Common-Mode Rejection Ratio | DC, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$ | 70 | 85 | | 70 | 85 | | 65 | 85 | | 70 | 85 | | 65 | 85 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2902, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$) | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |

## Electrical Characteristics $V^{+} = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

| Parameter | | Conditions | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Amplifier-to-Amplifier Coupling (Note 8) | | f = 1 kHz to 20 kHz, (Input Referred) | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | dB |
| Output Current | Source | $V_{IN}^{+} = 1\ V_{DC}$, $V_{IN}^{+} = 0\ V_{DC}$, $V^{+} = 15\ V_{DC}$, $V_O = 2\ V_{DC}$ | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | $mA_{DC}$ |
| | Sink | $V_{IN}^{-} = 1\ V_{DC}$, $V_{IN}^{+} = 0\ V_{DC}$, $V^{+} = 15\ V_{DC}$, $V_O = 2\ V_{DC}$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | |
| | | $V_{IN}^{-} = 1\ V_{DC}$, $V_{IN}^{+} = 0\ V_{DC}$, $V^{+} = 15\ V_{DC}$, $V_O = 200\ mV_{DC}$ | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | $\mu A_{DC}$ |
| Short Circuit to Ground | | (Note 2) $V^{+} = 15\ V_{DC}$, $T_A = 25°C$ | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | $mA_{DC}$ |
| Input Offset Voltage | | (Note 5) | | | ±4 | | | ±4 | | | ±5 | | | ±7 | | | ±9 | | | ±10 | $mV_{DC}$ |
| Input Offset Voltage Drift | | $R_S = 0\Omega$ | | ±7 | ±20 | | ±7 | ±20 | | ±7 | ±30 | | ±7 | | | ±7 | | | ±7 | | μV/°C |
| Input Offset Current | | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | | ±30 | | | ±30 | | | ±75 | | | ±100 | | | ±150 | | ±45 | ±200 | $nA_{DC}$ |
| Input Offset Current Drift | | $R_S = 0\Omega$ | | ±10 | ±200 | | ±10 | ±200 | | ±10 | ±200 | | ±10 | | | ±10 | | | ±10 | | $pA_{DC}$/°C |
| Input Bias Current | | $I_{IN(+)}$ or $I_{IN(-)}$ | | 40 | 100 | | 40 | 100 | | 40 | 200 | | 40 | 300 | | 40 | 500 | | 40 | 500 | $nA_{DC}$ |
| Input Common-Mode Voltage Range (Note 7) | | $V^{+} = +30\ V_{DC}$ (LM2902, $V^{+} = 26\ V_{DC}$) | 0 | | $V^{+} - 2$ | 0 | | $V^{+} - 2$ | 0 | | $V^{+} - 2$ | 0 | | $V^{+} - 2$ | 0 | | $V^{+} - 2$ | 0 | | $V^{+} - 2$ | $V_{DC}$ |
| Large Signal Voltage Gain | | $V^{+} = +15\ V_{DC}$ ($V_O$ Swing = 1 $V_{DC}$ to 11 $V_{DC}$) $R_L \geq 2\ k\Omega$ | 25 | | | 25 | | | 15 | | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_{OH}$ | $V^{+} = +30\ V_{DC}$, $R_L = 2\ k\Omega$ | 26 | | | 26 | | | 26 | | | 26 | | | 26 | | | 22 | | | $V_{DC}$ |
| | | $R_L \geq 10\ k\Omega$ (LM2902, $V^{+} = 26\ V_{DC}$) | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 23 | 24 | | |
| | $V_{OL}$ | $V^{+} = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$ | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 100 | $mV_{DC}$ |

## Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

| Parameter | | Conditions | | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Current | Source | $V_O = 2\ V_{DC}$ | $V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | $mA_{DC}$ |
| | Sink | | $V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$ | 10 | 15 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | |

**Note 1:** For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of $V^+$. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

**Note 4:** These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

**Note 5:** $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with $V^+$ from 5 $V_{DC}$ to 30 $V_{DC}$; and over the full input common-mode range (0 $V_{DC}$ to $V^+ - 1.5\ V_{DC}$) at 25°C; for LM2902, $V^+$ from 5 $V_{DC}$ to 26 $V_{DC}$.

**Note 6:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

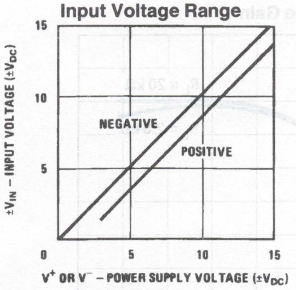
**Note 7:** The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2902), independent of the magnitude of $V^+$.

**Note 8:** Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

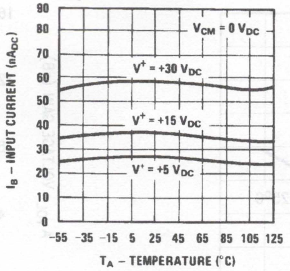
**Note 9:** Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

# Typical Performance Characteristics

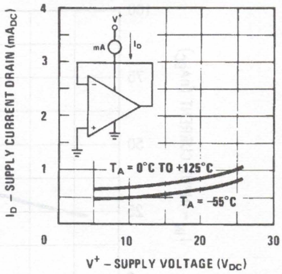
**Input Voltage Range**



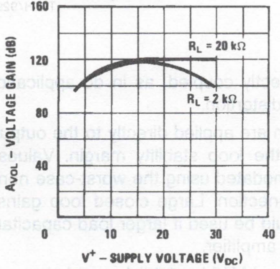
**Input Current**



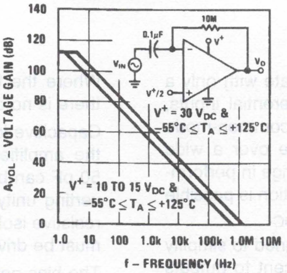
**Supply Current**



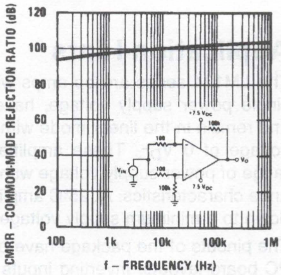
**Voltage Gain**



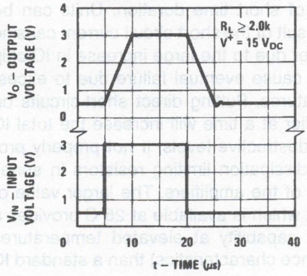
**Open Loop Frequency Response**



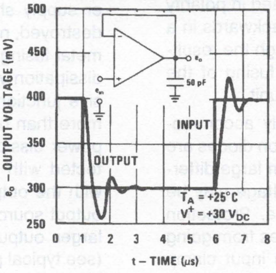
**Common Mode Rejection Ratio**



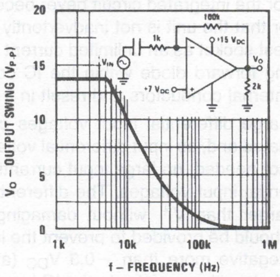
**Voltage Follower Pulse Response**



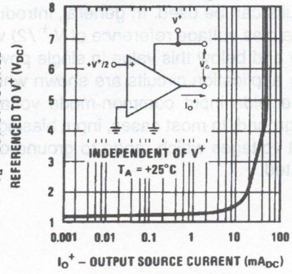
**Voltage Follower Pulse Response (Small Signal)**



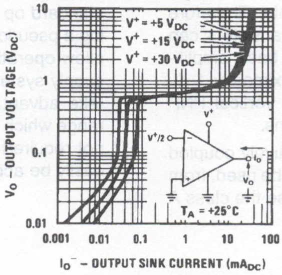
**Large Signal Frequency Response**



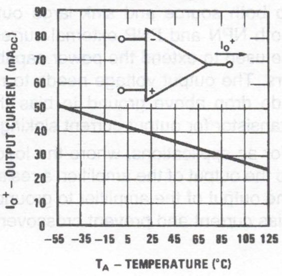
**Output Characteristics Current Sourcing**



**Output Characteristics Current Sinking**



**Current Limiting**



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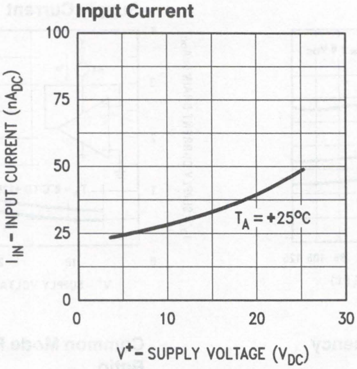
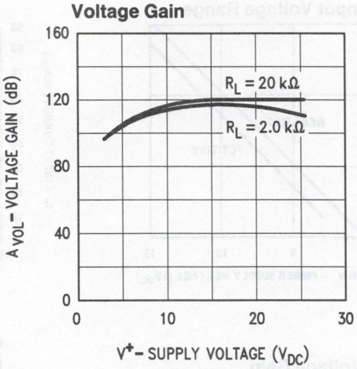
## Typical Performance Characteristics (LM2902 only)





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## Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 $V_{DC}$. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 $V_{DC}$.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than $V^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3$ $V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

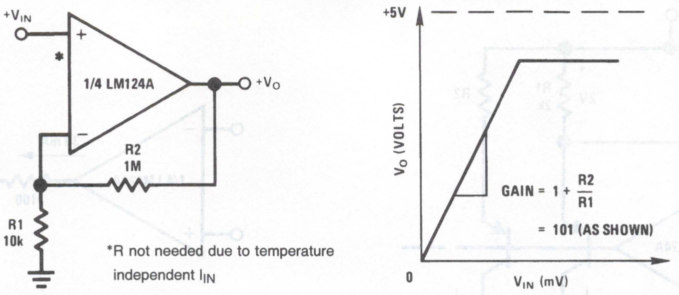
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 $V_{DC}$ to 30 $V_{DC}$.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

### Non-Inverting DC Gain (0V Input = 0V Output)


$+V_{IN}$
*
1/4 LM124A
$+V_O$
R2
1M
R1
10k
+5V
$V_O$ (VOLTS)
GAIN = $1 + \frac{R2}{R1}$
= 101 (AS SHOWN)
0
$V_{IN}$ (mV)

*R not needed due to temperature independent $I_{IN}$

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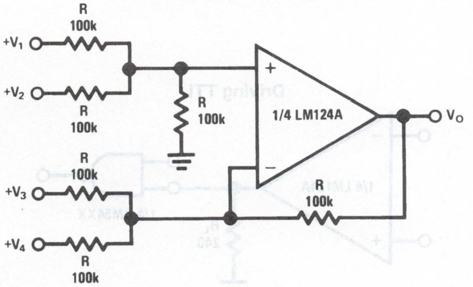
### DC Summing Amplifier ($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)


R
100k
$+V_1$
$+V_2$
R
100k
R
100k
1/4 LM124A
$V_O$
R
100k
$+V_3$
$+V_4$
R
100k
R
100k

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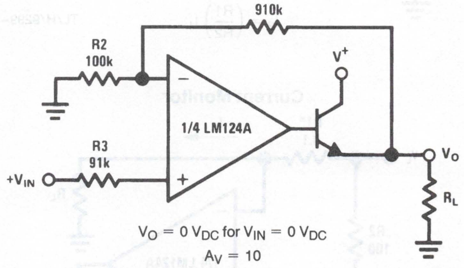
Where: $V_O = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

### Power Amplifier


R1
910k
R2
100k
$V^+$
1/4 LM124A
R3
91k
$+V_{IN}$
$V_O$
$R_L$

$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$

$A_V = 10$

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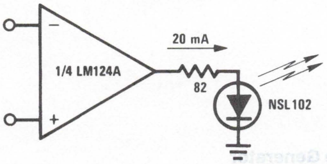
### LED Driver


1/4 LM124A
20 mA
82
NSL102

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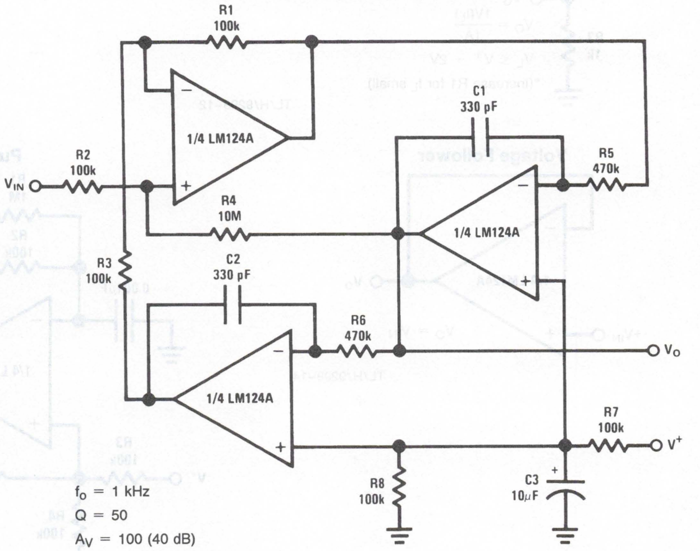
### "BI-QUAD" RC Active Bandpass Filter


R1
100k
1/4 LM124A
C1
330 pF
R2
100k
$V_{IN}$
R5
470k
R4
10M
1/4 LM124A
R3
100k
C2
330 pF
R6
470k
$V_O$
1/4 LM124A
R7
100k
$V^+$
R8
100k
C3
10µF

$f_o = 1$ kHz

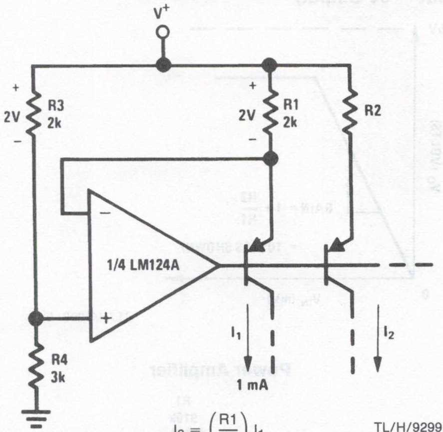
$Q = 50$

$A_V = 100$ (40 dB)

TL/H/9299-9

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

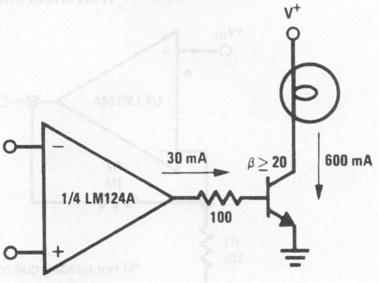
### Fixed Current Sources


V+
+
2V
−
R3
2k
+
2V
−
R1
2k
R2
−
+
1/4 LM124A
R4
3k
I1
I2
1 mA

$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

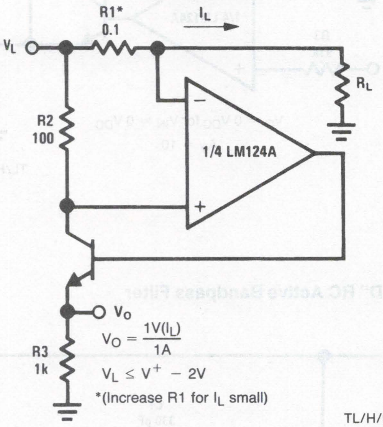
TL/H/9299–10

### Lamp Driver


V+
−
+
1/4 LM124A
30 mA
100
β ≥ 20
600 mA

TL/H/9299–11

### Current Monitor


R1*
0.1
IL
VL
R2
100
RL
−
+
1/4 LM124A
VO
R3
1k

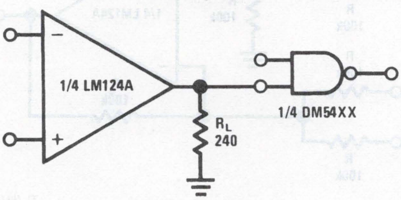
$V_O = \frac{1V(I_L)}{1A}$

$V_L \leq V^+ - 2V$

*(Increase R1 for $I_L$ small)

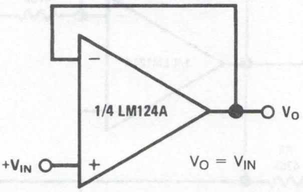
TL/H/9299–12

### Driving TTL


−
+
1/4 LM124A
RL
240
1/4 DM54XX

TL/H/9299–13

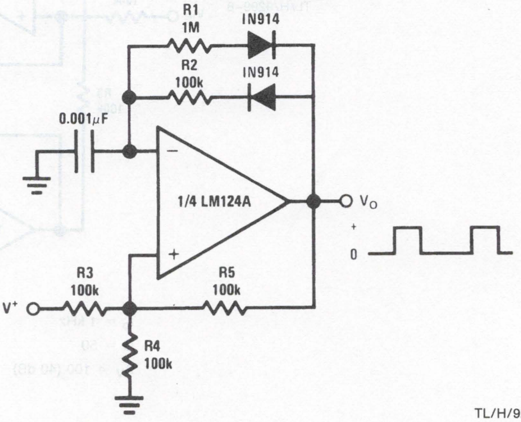
### Voltage Follower


−
+
1/4 LM124A
VO
+VIN

$V_O = V_{IN}$

TL/H/9299–14

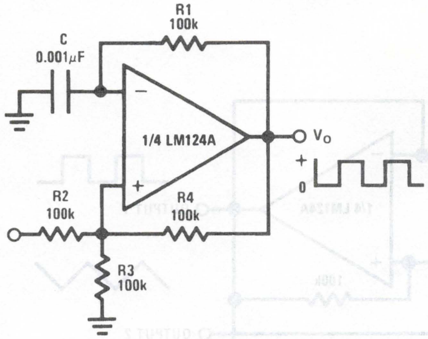
### Pulse Generator


R1
1M
IN914
R2
100k
IN914
0.001μF
−
+
1/4 LM124A
VO
+
0
R3
100k
R5
100k
V+
R4
100k

TL/H/9299–15

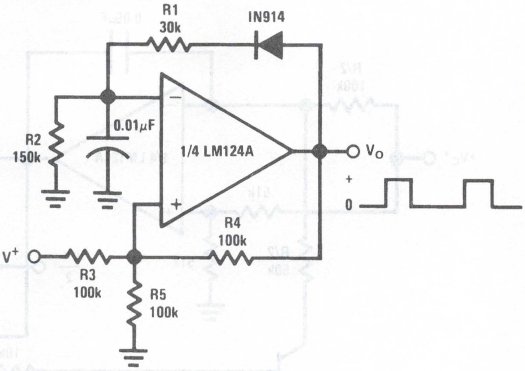
## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### Squarewave Oscillator


R1
100k
C
0.001μF
1/4 LM124A
$V_O$
+
0
R2
100k
R4
100k
$V^+$
R3
100k

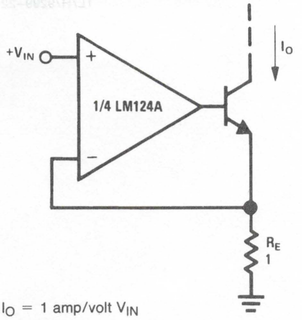
TL/H/9299-16

### Pulse Generator


R1
30k
IN914
R2
150k
0.01μF
1/4 LM124A
$V_O$
+
0
R4
100k
$V^+$
R3
100k
R5
100k

TL/H/9299-17

### High Compliance Current Sink

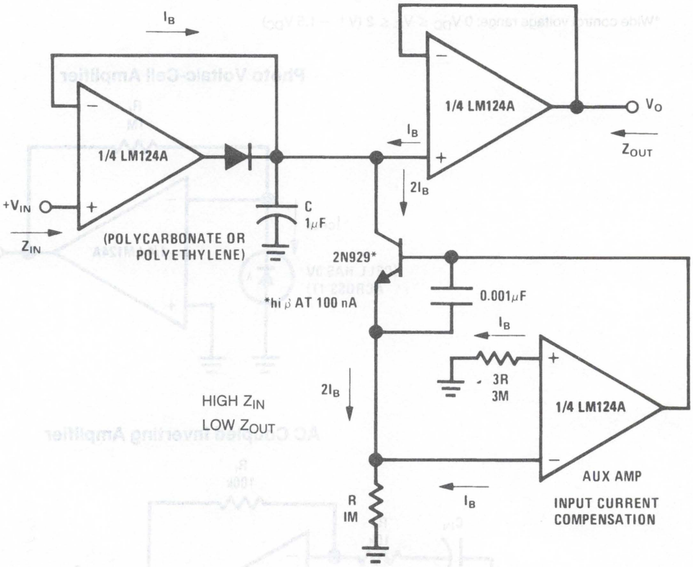

$I_O$
$+V_{IN}$
1/4 LM124A
$R_E$
1

$I_O$ = 1 amp/volt $V_{IN}$

(Increase $R_E$ for $I_o$ small)

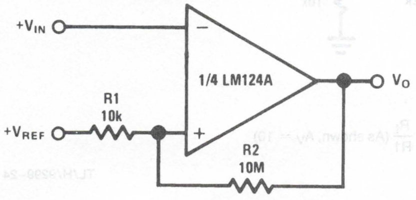
TL/H/9299-18

### Low Drift Peak Detector


$I_B$
1/4 LM124A
$V_O$
$I_B$
$Z_{OUT}$
1/4 LM124A
$+V_{IN}$
$Z_{IN}$
(POLYCARBONATE OR POLYETHYLENE)
C
1μF
$2I_B$
2N929*
*hi β AT 100 nA
0.001μF
$I_B$
3R
3M
1/4 LM124A
HIGH $Z_{IN}$
LOW $Z_{OUT}$
$2I_B$
R
1M
$I_B$
AUX AMP
INPUT CURRENT COMPENSATION

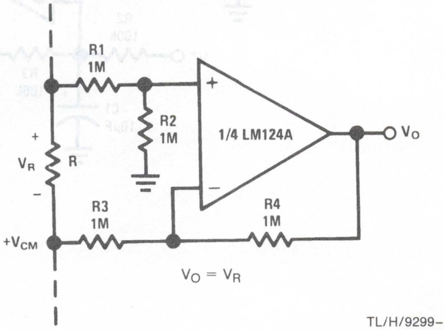
TL/H/9299-19

### Comparator with Hysteresis


$+V_{IN}$
1/4 LM124A
$V_O$
R1
10k
$+V_{REF}$
R2
10M

TL/H/9299-20

### Ground Referencing a Differential Input Signal

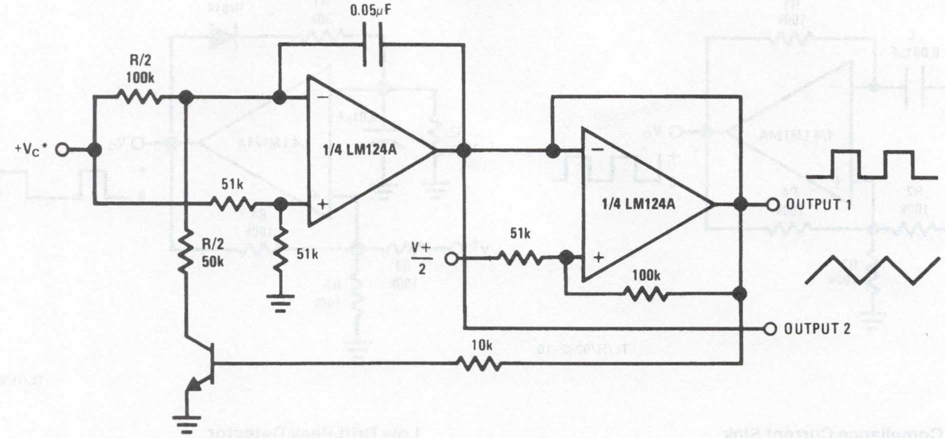

R1
1M
R2
1M
1/4 LM124A
$V_O$
+
$V_R$
R
−
R3
1M
R4
1M
$+V_{CM}$

$V_O = V_R$

TL/H/9299-21

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

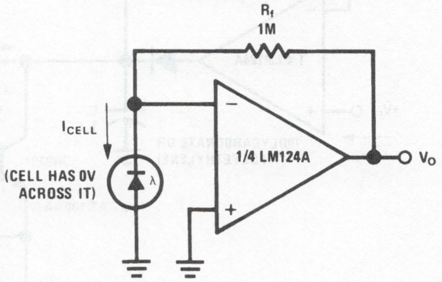
### Voltage Controlled Oscillator Circuit


0.05μF
R/2
100k
+VC*
51k
R/2
50k
51k
1/4 LM124A
1/4 LM124A
V+/2
51k
100k
OUTPUT 1
OUTPUT 2
10k

TL/H/9299–22

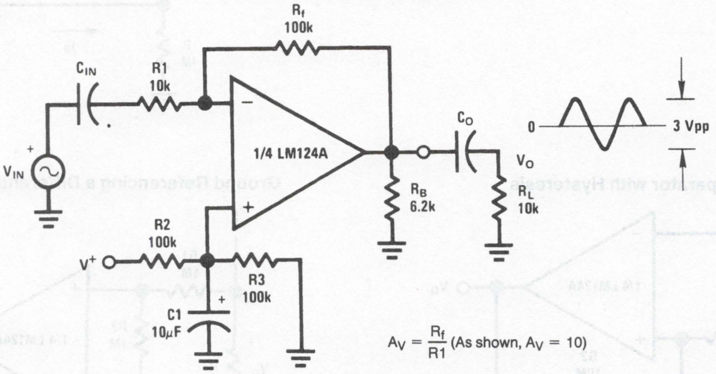
*Wide control voltage range: $0\ V_{DC} \le V_C \le 2\ (V^+ - 1.5\ V_{DC})$

### Photo Voltaic-Cell Amplifier


Rf
1M
ICELL
(CELL HAS 0V ACROSS IT)
λ
1/4 LM124A
VO

TL/H/9299–23

### AC Coupled Inverting Amplifier

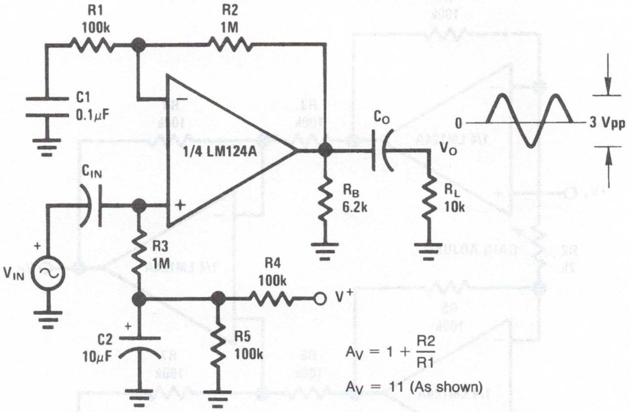

Rf
100k
CIN
R1
10k
VIN
1/4 LM124A
CO
VO
RB
6.2k
RL
10k
0
3 Vpp
R2
100k
V+
R3
100k
C1
10μF

$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/9299–24

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### AC Coupled Non-Inverting Amplifier

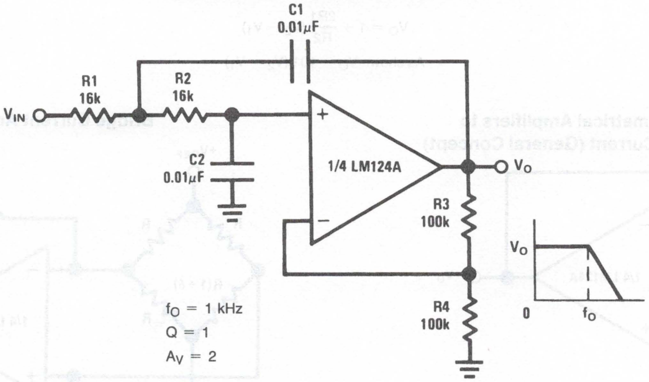

R1
100k
R2
1M
C1
0.1μF
1/4 LM124A
$C_O$
0
$V_O$
3 Vpp
$C_{IN}$
$R_B$
6.2k
$R_L$
10k
+
$V_{IN}$
R3
1M
R4
100k
$V^+$
+
C2
10μF
R5
100k

$$A_V = 1 + \frac{R2}{R1}$$

$A_V = 11$ (As shown)

TL/H/9299–25

### DC Coupled Low-Pass RC Active Filter


C1
0.01μF
$V_{IN}$
R1
16k
R2
16k
C2
0.01μF
1/4 LM124A
$V_O$
R3
100k
R4
100k
$V_O$
0
$f_O$

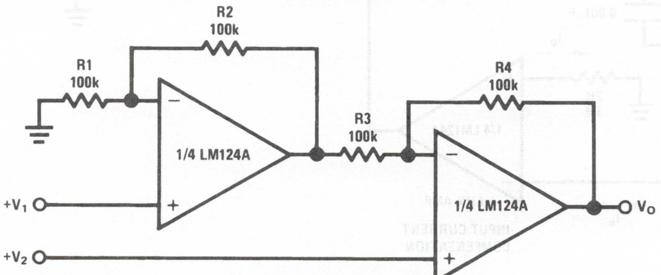
$f_O = 1$ kHz

$Q = 1$

$A_V = 2$

TL/H/9299–26

### High Input Z, DC Differential Amplifier


R2
100k
R1
100k
1/4 LM124A
R3
100k
R4
100k
1/4 LM124A
$+V_1$
$+V_2$
$V_O$

TL/H/9299–27

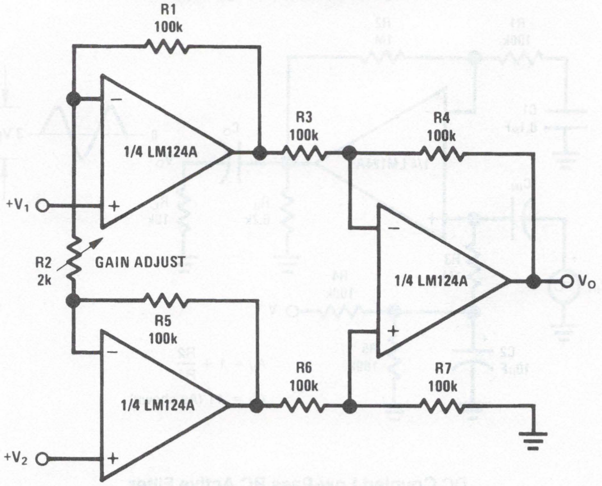
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

## Typical Single-Supply Applications $(V^+ = 5.0\ V_{DC})$ (Continued)

### High Input Z Adjustable-Gain DC Instrumentation Amplifier


R1
100k
−
+
1/4 LM124A
$+V_1$
R2
2k
GAIN ADJUST
R3
100k
R4
100k
−
+
1/4 LM124A
$V_O$
R5
100k
−
+
1/4 LM124A
$+V_2$
R6
100k
R7
100k

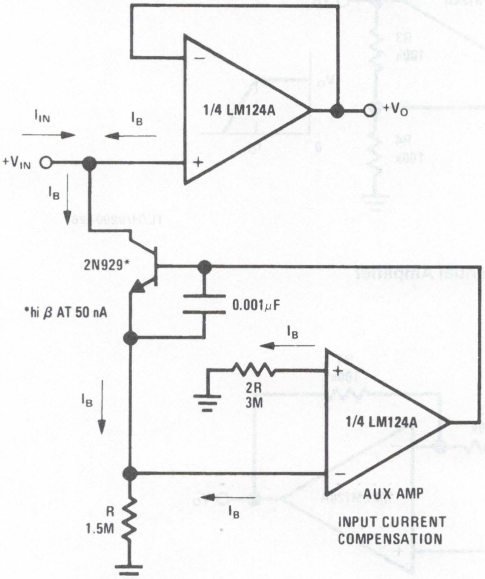
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

TL/H/9299-28

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

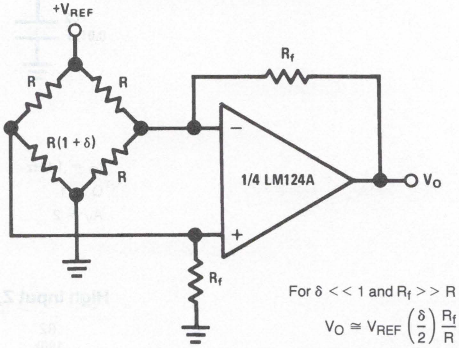
As shown $V_O = 101\ (V_2 - V_1)$

### Using Symmetrical Amplifiers to Reduce Input Current (General Concept)


−
+
1/4 LM124A
$+V_O$
$I_{IN}$
$I_B$
$+V_{IN}$
$I_B$
2N929*
*hi β AT 50 nA
0.001μF
$I_B$
+
−
2R
3M
1/4 LM124A
AUX AMP
INPUT CURRENT
COMPENSATION
$I_B$
$I_B$
R
1.5M

TL/H/9299-29

### Bridge Current Amplifier


$+V_{REF}$
R
R
$R(1 + \delta)$
R
$R_f$
−
+
1/4 LM124A
$V_O$
$R_f$

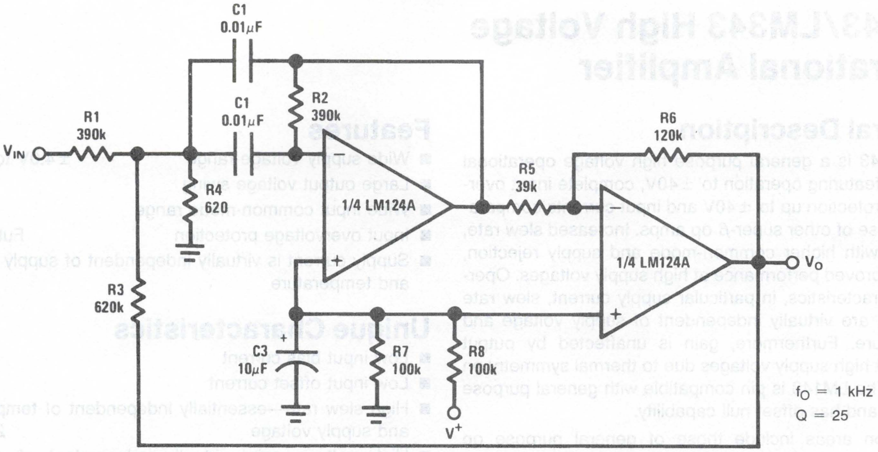
For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299-30

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

**Bandpass Active Filter**


C1
0.01µF
R2
390k
C1
0.01µF
R1
390k
V_IN
R4
620
1/4 LM124A
R6
120k
R5
39k
1/4 LM124A
V_O
R3
620k
C3
10µF
R7
100k
R8
100k
V+
f_O = 1 kHz
Q = 25

TL/H/9299–31

**National Semiconductor Corporation**

# LM143/LM343 High Voltage Operational Amplifier

## General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-$\beta$ op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

## Features

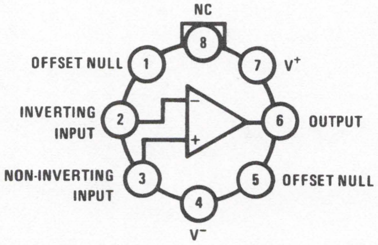
| | |
|---|---|
| ■ Wide supply voltage range | ±4.0V to ±40V |
| ■ Large output voltage swing | ±37V |
| ■ Wide input common-mode range | ±38V |
| ■ Input overvoltage protection | Full ±40V |
| ■ Supply current is virtually independent of supply voltage and temperature | |

## Unique Characteristics

| | |
|---|---|
| ■ Low input bias current | 8.0 nA |
| ■ Low input offset current | 1.0 nA |
| ■ High slew rate—essentially independent of temperature and supply voltage | 2.5V/µs |
| ■ High voltage gain—virtually independent of resistive loading, temperature, and supply voltage | 100k min |
| ■ Internally compensated for unity gain | |
| ■ Output short circuit protection | |
| ■ Pin compatible with general purpose op amps | |

## Connection Diagram

**Metal Can Package**
**Top View**



TL/H/7783-1

**Order Number LM143H or LM343H**
**See NS Package Number H08C**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 4)**

| | LM143 | LM343 |
|---|---|---|
| Supply Voltage | ±40V | ±34V |
| Power Dissipation (Note 1) | 680 mW | 680 mW |
| Differential Input Voltage (Note 2) | 80V | 68V |
| Input Voltage (Note 2) | ±40V | ±34V |
| Operating Temperature Range | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Output Short Circuit Duration | 5 seconds | 5 seconds |
| Lead Temperature (Soldering, 10 sec.) | 300°C | 300°C |
| ESD rating to be determined. | | |

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM143 | | | LM343 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 2.0 | 5.0 | | 2.0 | 8.0 | mV |
| Input Offset Current | $T_A = 25°C$ | | 1.0 | 3.0 | | 1.0 | 10 | nA |
| Input Bias Current | $T_A = 25°C$ | | 8.0 | 20 | | 8.0 | 40 | nA |
| Supply Voltage Rejection Ratio | $T_A = 25°C$ | | 10 | 100 | | 10 | 200 | μV/V |
| Output Voltage Swing | $T_A = 25°C$, $R_L \geq 5\ k\Omega$ | 22 | 25 | | 20 | 25 | | V |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$ | 100k | 180k | | 70k | 180k | | V/V |
| Common-Mode Rejection Ratio | $T_A = 25°C$ | 80 | 90 | | 70 | 90 | | dB |
| Input Voltage Range | $T_A = 25°C$ | 24 | 26 | | 22 | 26 | | V |
| Supply Current (Note 5) | $T_A = 25°C$ | | 2.0 | 4.0 | | 2.0 | 5.0 | mA |
| Short Circuit Current | $T_A = 25°C$ | | 20 | | | 20 | | mA |
| Slew Rate | $T_A = 25°C$, $A_V = 1$ | | 2.5 | | | 2.5 | | V/μs |
| Power Bandwidth | $T_A = 25°C$, $V_{OUT} = 40\ V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤ 1% | | 20k | | | 20k | | Hz |
| Unity Gain Frequency | $T_A = 25°C$ | | 1.0M | | | 1.0M | | Hz |
| Input Offset Voltage | $T_A = Max$<br>$T_A = Min$ | | | 6.0<br>6.0 | | | 10<br>10 | mV |
| Input Offset Current | $T_A = Max$<br>$T_A = Min$ | | 0.8<br>1.8 | 4.5<br>7.0 | | 0.8<br>1.8 | 14<br>14 | nA |
| Input Bias Current | $T_A = Max$<br>$T_A = Min$ | | 5.0<br>16 | 35<br>35 | | 5.0<br>16 | 55<br>55 | nA |
| Large Signal Voltage Gain | $R_L \geq 100\ k\Omega$, $T_A = Max$<br>$R_L \geq 100\ k\Omega$, $T_A = Min$ | 50k<br>50k | 150k<br>220k | | 50k<br>50k | 150k<br>220k | | V/V |
| Output Voltage Swing | $R_L \geq 5.0\ k\Omega$, $T_A = Max$<br>$R_L \geq 5.0\ k\Omega$, $T_A = Min$ | 22<br>22 | 26<br>25 | | 20<br>20 | 26<br>25 | | V |

**Note 1:** Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

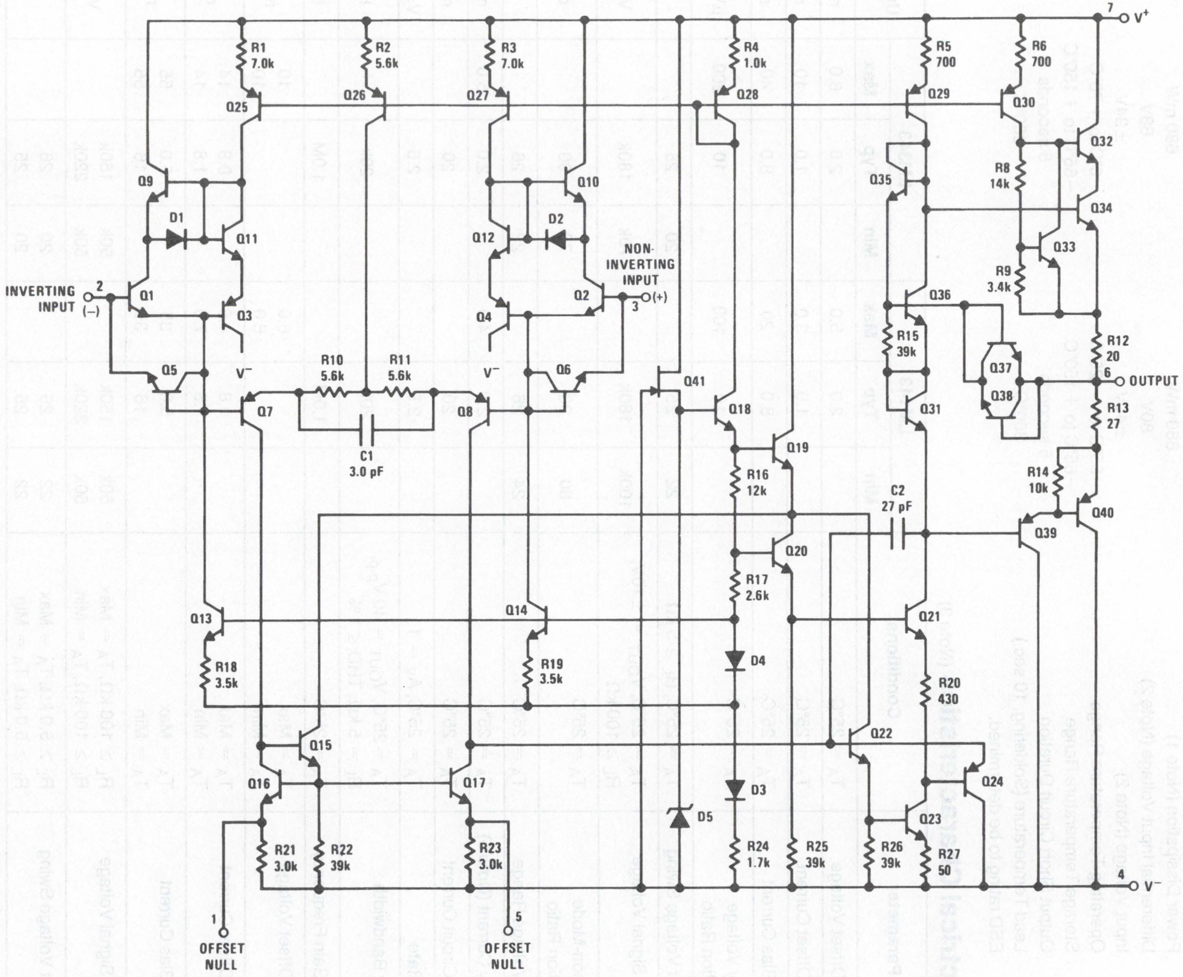
**Note 2:** For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** These specifications apply for $V_S = \pm 28V$. For LM143, $T_A$ = max = 125°C and $T_A$ = min = −55°C. For LM343, $T_A$ = max = 70°C and $T_A$ = min = 0°C.

**Note 4:** Refer to RETS143X for LM143H and LM1536H military specifications.

**Note 5:** The maximum supply currents are guaranteed at $V_S = \pm 40V$ for the LM143 and $V_S = \pm 34V$ for the LM343.

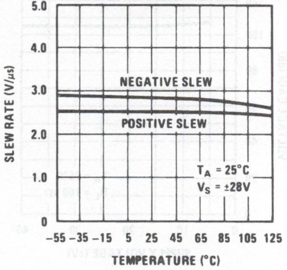
## Schematic Diagram


7
V+
R1
7.0k
R2
5.6k
R3
7.0k
R4
1.0k
R5
700
R6
700
Q25
Q26
Q27
Q28
Q29
Q30
Q32
R8
14k
Q35
Q9
Q10
Q34
D1
D2
Q11
Q12
NON-INVERTING INPUT
Q33
R9
3.4k
INVERTING INPUT
2
(−)
Q1
Q3
Q4
Q2
3
(+)
Q36
R15
39k
R12
20
Q5
V−
R10
5.6k
R11
5.6k
V−
Q6
Q41
Q37
6
OUTPUT
Q38
Q7
Q8
Q18
Q31
R13
27
C1
3.0 pF
Q19
R16
12k
R14
10k
C2
27 pF
Q40
Q39
Q20
R17
2.6k
Q13
Q14
Q21
R18
3.5k
R19
3.5k
D4
R20
430
Q22
Q15
Q16
Q17
Q24
D3
D5
Q23
R21
3.0k
R22
39k
R23
3.0k
R24
1.7k
R25
39k
R26
39k
R27
50
4
V−
1
OFFSET NULL
5
OFFSET NULL

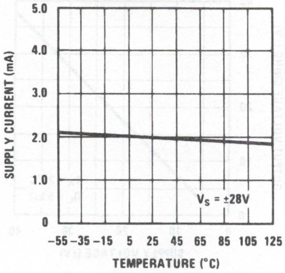
TL/H/7783-2

# Typical Performance Characteristics

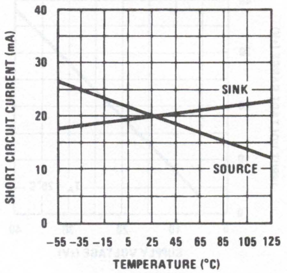
### Voltage Follower Slew Rate



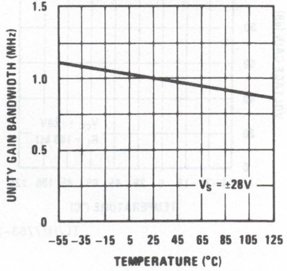
### Supply Current



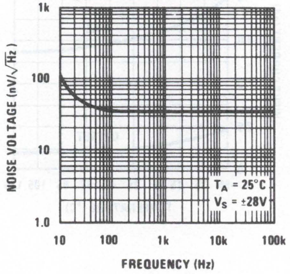
### Short Circuit Current



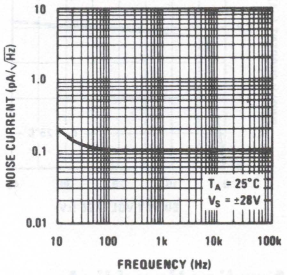
### Unity Gain Bandwidth



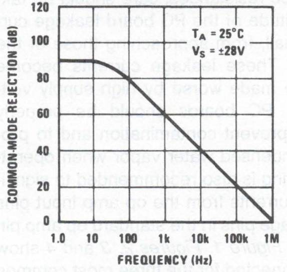
### Input Noise Voltage



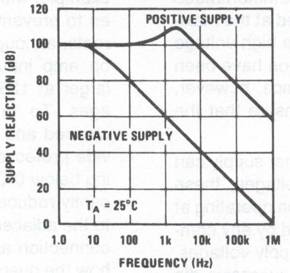
### Input Noise Current



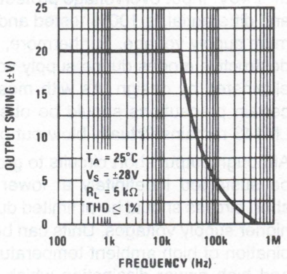
### Common-Mode Rejection



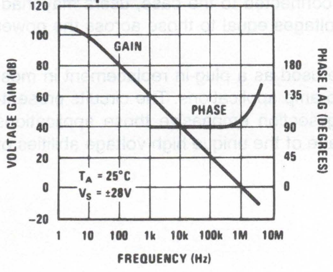
### Power Supply Rejection



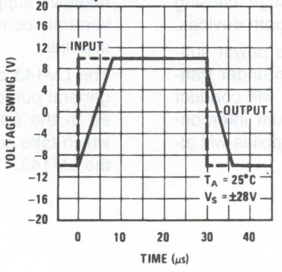
### Large Signal Frequency Response



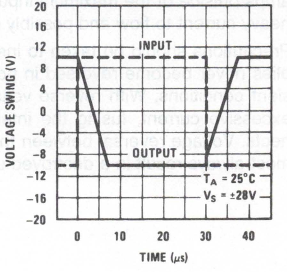
### Open Loop Frequency Response



### Voltage Follower Pulse Response



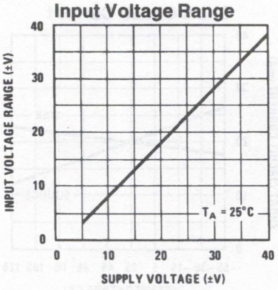
### Inverter Pulse Response



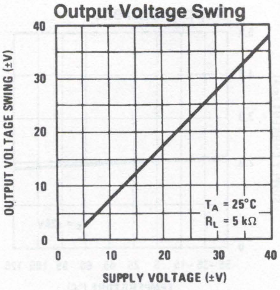
TL/H/7783–4

## Typical Performance Characteristics (Continued)

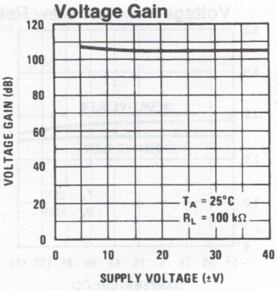
Input Voltage Range



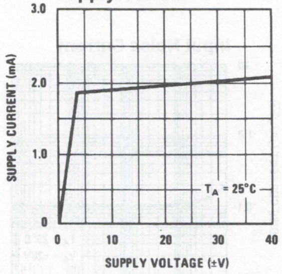
Output Voltage Swing



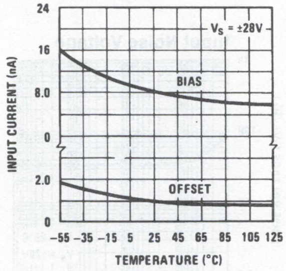
Voltage Gain



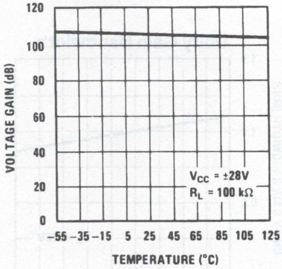
Supply Current



Input Current



Voltage Gain



TL/H/7783-3

## Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

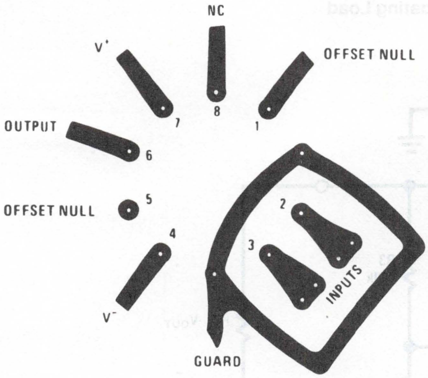
Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3* and *4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage abilities of the LM143.

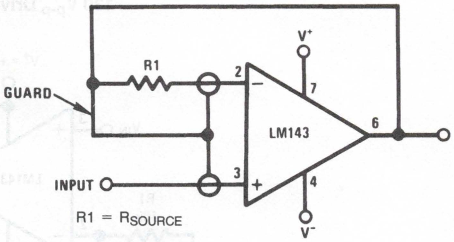
## Application Hints (See AN-127) (Continued)


NC
V+
OFFSET NULL
7
8
1
OUTPUT
6
OFFSET NULL
5
2
3
4
INPUTS
V-
GUARD

TL/H/7783-5

Bottom View

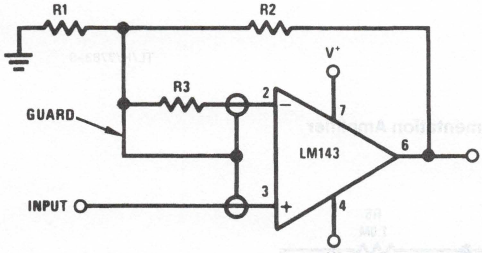
FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package


R1
GUARD
2
V+
7
LM143
6
INPUT
3
4
V-

$R1 = R_{SOURCE}$

TL/H/7783-6

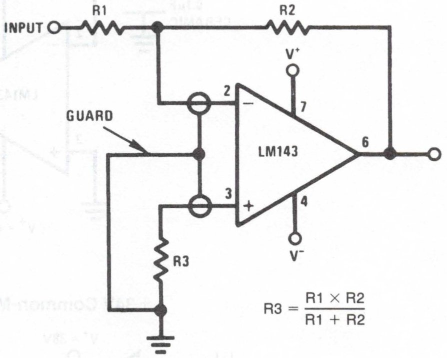
FIGURE 2. Guarded Voltage Follower


R1
R2
R3
V+
GUARD
2
7
LM143
6
INPUT
3
4
V-

$$R3 + \frac{R1 \times R2}{R1 + R2} = R_{SOURCE}$$

TL/H/7783-7

FIGURE 3. Guarded Non-Inverting Amplifier


R1
R2
INPUT
V+
2
7
GUARD
LM143
6
3
4
V-
R3

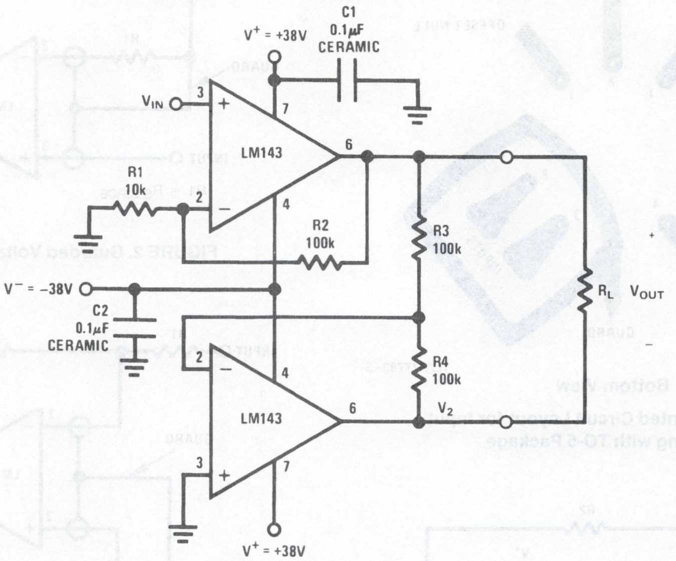
$$R3 = \frac{R1 \times R2}{R1 + R2}$$

TL/H/7783-8

FIGURE 4. Guarded Inverting Amplifier

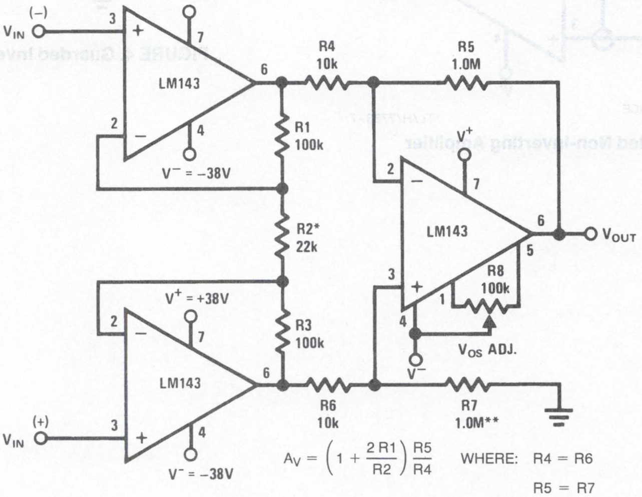
## Typical Applications ‡ (For more detail see AN-127)

### 130 $V_{p-p}$ Drive Across a Floating Load


V+ = +38V
C1
0.1μF
CERAMIC
VIN
3
7
LM143
6
R1
10k
2
4
R2
100k
R3
100k
V− = −38V
C2
0.1μF
CERAMIC
RL
VOUT
R4
100k
2
4
LM143
6
V2
3
7
V+ = +38V

TL/H/7783-9

### ±34V Common-Mode Instrumentation Amplifier


V+ = 38V
(−)
VIN
3
7
LM143
6
2
4
V− = −38V
R4
10k
R5
1.0M
R1
100k
V+
2
7
LM143
6
VOUT
5
R2*
22k
R8
100k
3
1
4
V+ = +38V
2
7
R3
100k
VOS ADJ.
V−
LM143
6
R6
10k
R7
1.0M**
(+)
VIN
3
4
V− = −38V

$$A_V = \left(1 + \frac{2\,R1}{R2}\right)\frac{R5}{R4}$$

WHERE: R4 = R6

R5 = R7

TL/H/7783-10

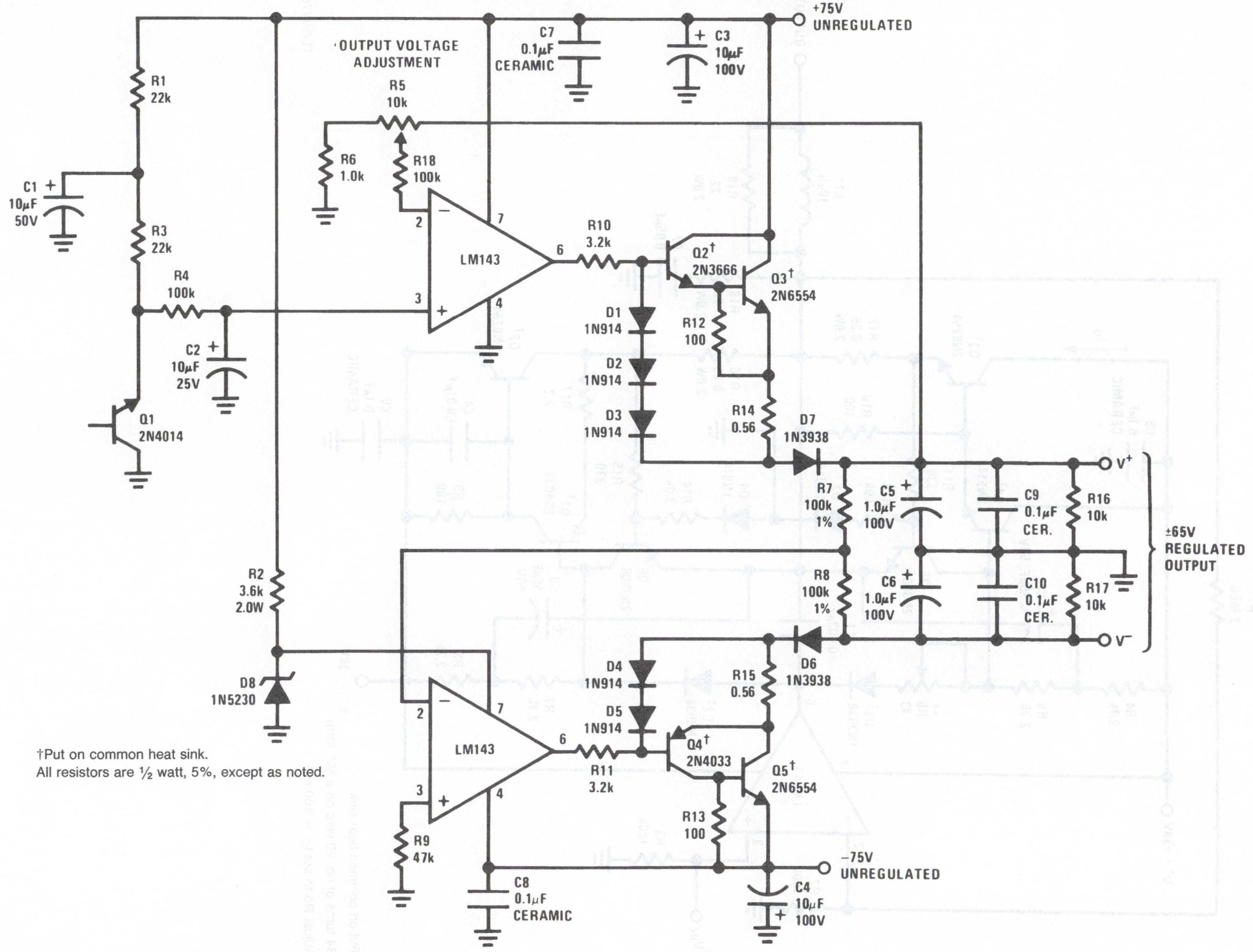
*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

---

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

### Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection


+75V UNREGULATED
OUTPUT VOLTAGE ADJUSTMENT
R5 10k
C7 0.1μF CERAMIC
C3 10μF 100V
R1 22k
C1 10μF 50V
R3 22k
R4 100k
C2 10μF 25V
Q1 2N4014
R6 1.0k
R18 100k
LM143
2
3
7
4
6
R10 3.2k
Q2† 2N3666
Q3† 2N6554
D1 1N914
D2 1N914
D3 1N914
R12 100
R14 0.56
D7 1N3938
V+
R7 100k 1%
C5 1.0μF 100V
C9 0.1μF CER.
R16 10k
±65V REGULATED OUTPUT
R8 100k 1%
C6 1.0μF 100V
C10 0.1μF CER.
R17 10k
V−
R2 3.6k 2.0W
D8 1N5230
D4 1N914
D5 1N914
D6 1N3938
R15 0.56
Q4† 2N4033
Q5† 2N6554
R11 3.2k
R13 100
R9 47k
C8 0.1μF CERAMIC
C4 10μF 100V
−75V UNREGULATED

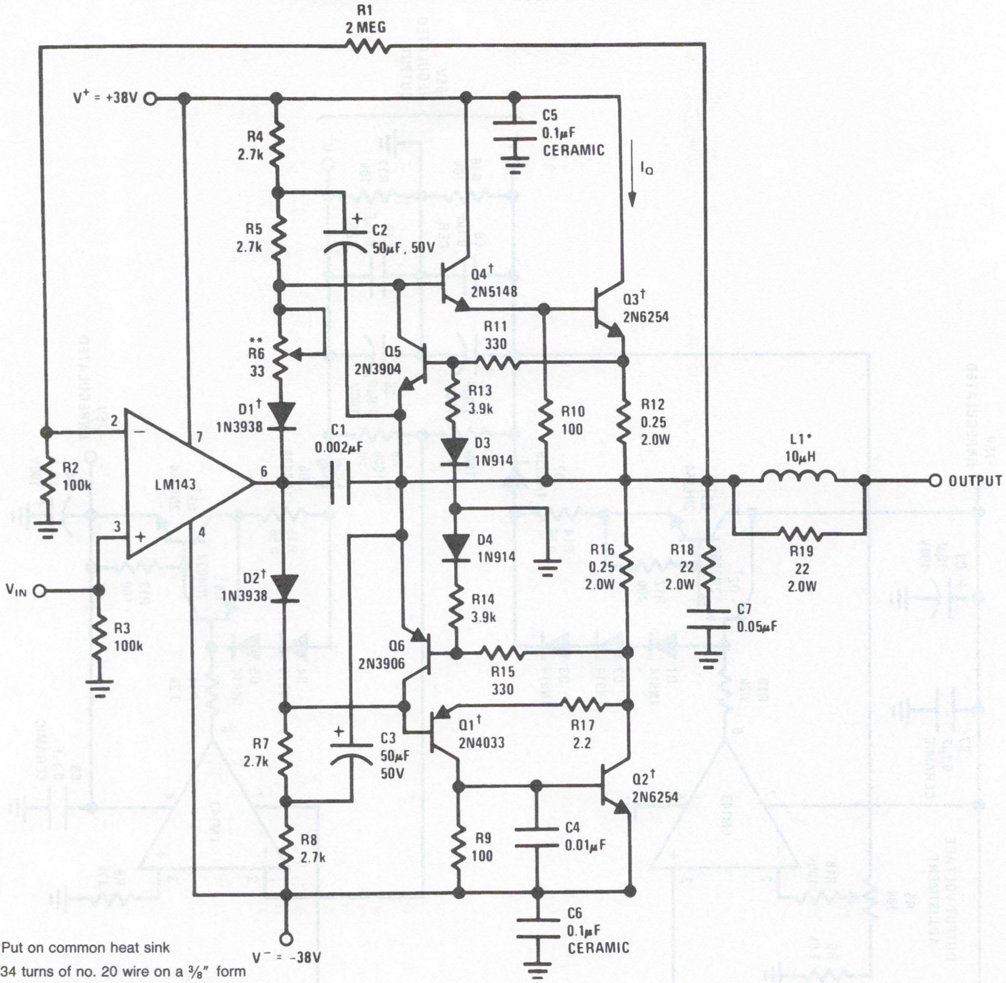
†Put on common heat sink.
All resistors are ½ watt, 5%, except as noted.

TL/H/7783–11

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

## Typical Applications ‡ (Continued) (For more detail see AN-127)

### 90W Audio Power Amplifier with Safe Area Protection


R1
2 MEG
V+ = +38V
R4
2.7k
C5
0.1μF
CERAMIC
IQ
R5
2.7k
C2
50μF, 50V
Q4†
2N5148
Q3†
2N6254
R11
330
**
R6
33
Q5
2N3904
R13
3.9k
R10
100
R12
0.25
2.0W
D1†
1N3938
C1
0.002μF
D3
1N914
L1*
10μH
OUTPUT
R2
100k
LM143
2
7
6
3
4
D4
1N914
R16
0.25
2.0W
R18
22
2.0W
R19
22
2.0W
VIN
D2†
1N3938
R14
3.9k
C7
0.05μF
R3
100k
Q6
2N3906
R15
330
Q1†
2N4033
R17
2.2
R7
2.7k
C3
50μF
50V
Q2†
2N6254
R9
100
C4
0.01μF
R8
2.7k
C6
0.1μF
CERAMIC
V− = −38V

†Put on common heat sink

*34 turns of no. 20 wire on a ⅜″ form

**Adjust R6 to set $I_Q$ = 100 mA

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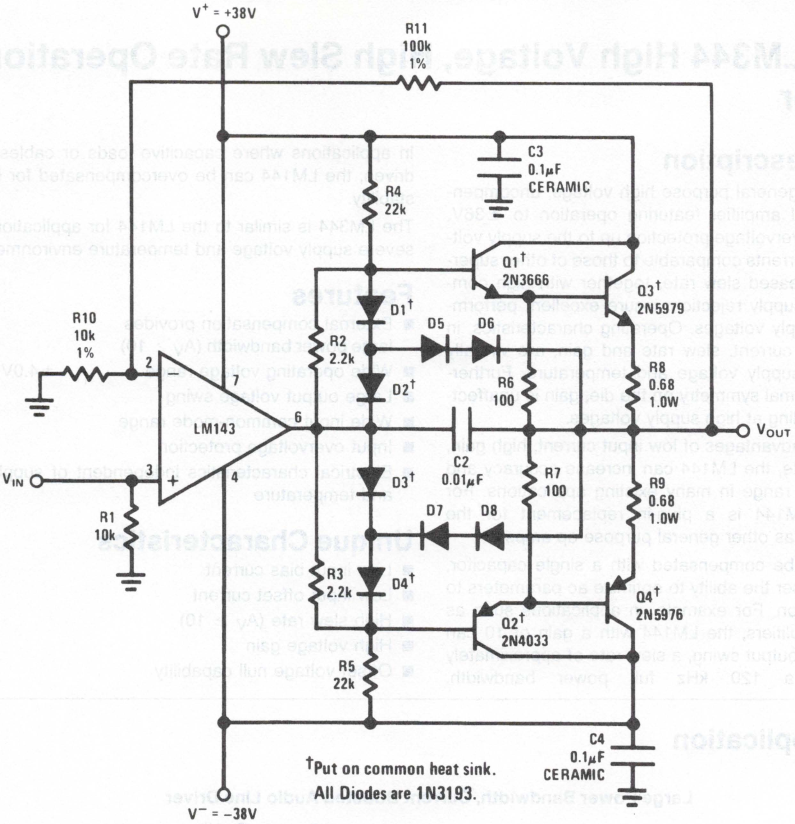
‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

## Typical Applications ‡ (Continued) (For more detail see AN-127)

### 1 Amp Power Amplifier with Short Circuit Protection


V⁺ = +38V
R11
100k
1%
C3
0.1μF
CERAMIC
R4
22k
Q1†
2N3666
Q3†
2N5979
D1†
R10
10k
1%
R2
2.2k
D5
D6
2
7
LM143
D2†
R6
100
R8
0.68
1.0W
6
C2
0.01μF
R7
100
V_OUT
V_IN
3
4
D3†
R9
0.68
1.0W
R1
10k
D7
D8
R3
2.2k
D4†
Q4†
2N5976
Q2†
2N4033
R5
22k
C4
0.1μF
CERAMIC
V⁻ = −38V

†Put on common heat sink.
All Diodes are 1N3193.

TL/H/7783-13

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

National
Semiconductor
Corporation

# LM144/LM344 High Voltage, High Slew Rate Operational Amplifier

## General Description

The LM144 is a general purpose high voltage, uncompensated operational amplifier featuring operation to ±36V, complete input overvoltage protection up to the supply voltages and input currents comparable to those of other super-$\beta$ op amps. Increased slew rate, together with high common-mode and supply rejection, insure excellent performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, due to thermal symmetry on the die, gain is unaffected by output loading at high supply voltages.

With the unique advantages of low input current, high gain, and high slew rate, the LM144 can increase accuracy and useful frequency range in many existing applications. For example, the LM144 is a plug-in replacement for the LM101A, as well as other general purpose op amps.

The LM144 can be compensated with a single capacitor, thus giving the user the ability to optimize ac parameters to suit the application. For example, in applications such as audio power amplifiers, the LM144 with a gain of 10 can provide a ±30V output swing, a slew rate of approximately 30V/µs, and a 120 kHz full power bandwidth. In applications where capacitive loads or cables must be driven, the LM144 can be overcompensated for increased stability.

The LM344 is similar to the LM144 for applications in less severe supply voltage and temperature environments.

## Features

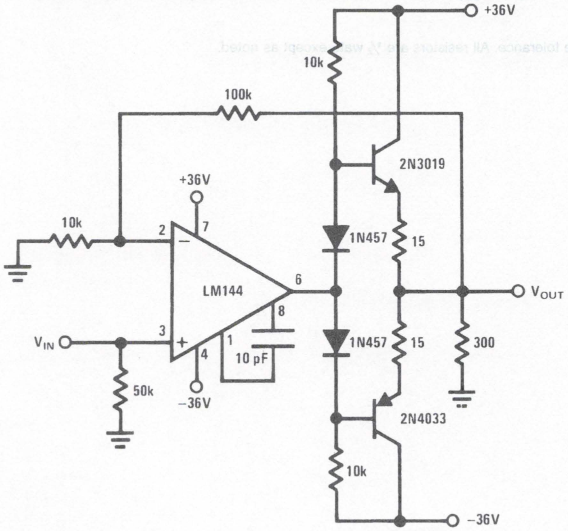
| | |
|---|---|
| External compensation provides large power bandwidth ($A_V \geq 10$) | 120 kHz |
| Wide operating voltage range | ±4.0V to ±36V |
| Large output voltage swing | ±30V |
| Wide input common-mode range | |
| Input overvoltage protection | |
| Electrical characteristics independent of supply voltage and temperature | |

## Unique Characteristics

| | |
|---|---|
| Low input bias current | 8.0 nA |
| Low input offset current | 1.0 nA |
| High slew rate ($A_V \geq 10$) | 30V/µs |
| High voltage gain | 100k min |
| Offset voltage null capability | |

## Typical Application

**Large Power Bandwidth, Current Boosted Audio Line Driver**



TL/H/7784–1

## Absolute Maximum Ratings (These ratings are not concurrent)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 4)**

| | **LM144** | **LM344** |
|---|---|---|
| Supply Voltage | ±40V | ±34V |
| Power Dissipation (Note 1) | 680 mW | 680 mW |
| Differential Input Voltage (Note 2) | 80V | 68V |
| Input Voltage (Note 2) | ±40V | ±34V |
| Operating Temperature Range | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Output Short Circuit Duration | 5 seconds | 5 seconds |
| Lead Temperature (Soldering, 10 sec) | 300°C | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM144 | | | LM344 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ C$ | | 2.0 | 5.0 | | 2.0 | 8.0 | mV |
| Input Offset Current | $T_A = 25^\circ C$ | | 1.0 | 3.0 | | 1.0 | 10 | nA |
| Input Bias Current | $T_A = 25^\circ C$ | | 8.0 | 20 | | 8.0 | 40 | nA |
| Supply Voltage Rejection Ratio | $T_A = 25^\circ C$ | | 10 | 100 | | 10 | 200 | μV/V |
| Output Voltage Swing | $T_A = 25^\circ C$, $R_L \geq 5\ k\Omega$ | 22 | 25 | | 20 | 25 | | V |
| Large Signal Voltage Gain | $T_A = 25^\circ C$, $V_{OUT} = \pm 10V$,<br>$R_L \geq 100\ k\Omega$ | 100k | 180k | | 70k | 180k | | V/V |
| Common-Mode Rejection Ratio | $T_A = 25^\circ C$ | 80 | 90 | | 70 | 90 | | dB |
| Input Voltage Range | $T_A = 25^\circ C$ | 24 | 26 | | 22 | 26 | | V |
| Supply Current | $T_A = 25^\circ C$ | | 2.0 | 4.0 | | 2.0 | 5.0 | mA |
| Short Circuit Current | $T_A = 25^\circ C$ | | 20 | | | 20 | | mA |
| Slew Rate | $T_A = 25^\circ C$, $A_V = 1$<br>$T_A = 25^\circ C$, $A_V = 10$, C1 = 3 pF | | 2.5<br>30 | | | 2.5<br>30 | | V/μs<br>V/μs |
| Power Bandwidth | $T_A = 25^\circ C$, $V_{OUT} = 40\ V_{p\text{-}p}$,<br>$R_L = 5\ k\Omega$, THD ≤ 1%, $A_V = 1$ | | 20k | | | 20k | | Hz |
| Unity Gain Frequency | $T_A = 25^\circ C$ | | 1.0M | | | 1.0M | | Hz |
| Input Offset Voltage | $T_A$ = Max<br>$T_A$ = Min | | | 6.0<br>6.0 | | | 10<br>10 | mV<br>mV |
| Input Offset Current | $T_A$ = Max<br>$T_A$ = Min | | 0.8<br>1.8 | 4.5<br>7.0 | | 0.8<br>1.8 | 14<br>14 | nA<br>nA |
| Input Bias Current | $T_A$ = Max<br>$T_A$ = Min | | 5.0<br>16 | 35<br>35 | | 5.0<br>16 | 55<br>55 | nA<br>nA |
| Large Signal Voltage Gain | $R_L \geq 100\ k\Omega$, $T_A$ = Max<br>$R_L \geq 100\ k\Omega$, $T_A$ = Min | 50k<br>50k | 150k<br>220k | | 50k<br>50k | 150k<br>220k | | V/V<br>V/V |
| Output Voltage Swing | $R_L \geq 5.0\ k\Omega$, $T_A$ = Max<br>$R_L \geq 5.0\ k\Omega$, $T_A$ = Min | 22<br>22 | 26<br>25 | | 20<br>20 | 26<br>25 | | V<br>V |

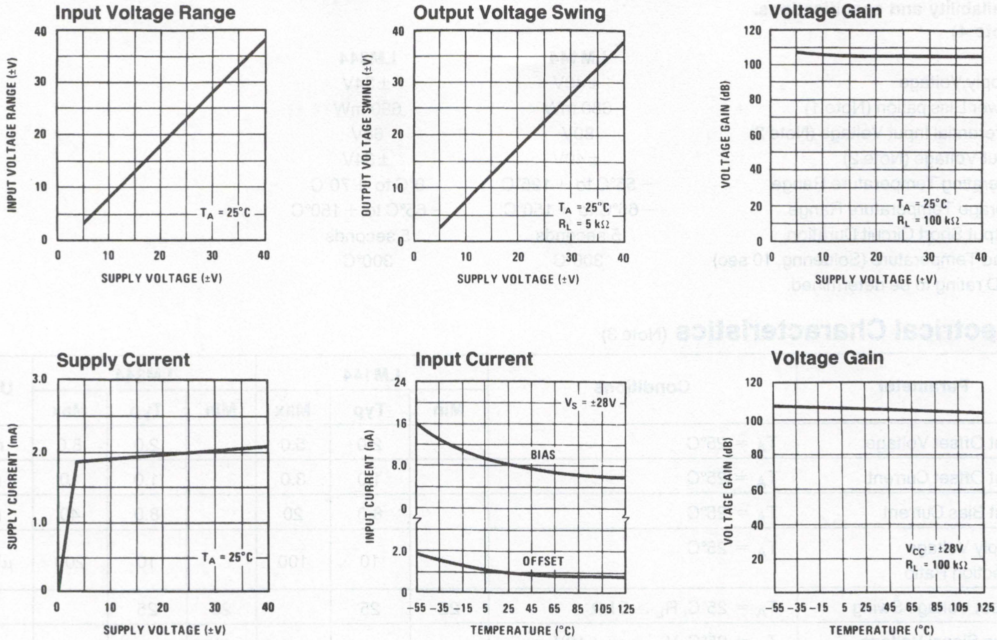
**Note 1:** The maximum junction temperature of the LM144 is 150°C, while that of the LM344 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

**Note 2:** For supply voltage less than ±40V for the LM144 and less than ±34V for the LM344, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** These specifications apply for $V_S = \pm 28V$. For the LM144, $T_A$ = max = 125°C and $T_A$ = min = −55°C. For the LM344, $T_A$ = max = 70°C and $T_A$ = min = 0°C.

**Note 4:** Refer to RETS144X for LM144H specifications.

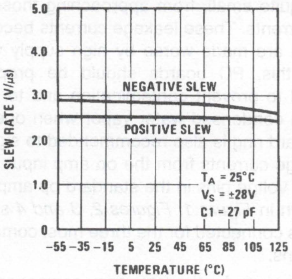
## Typical Performance Characteristics



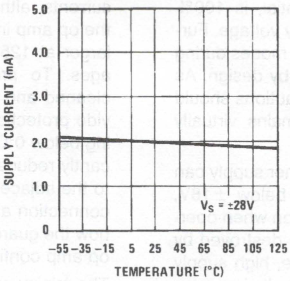
TL/H/7784-3

## Typical Performance Characteristics (Continued)

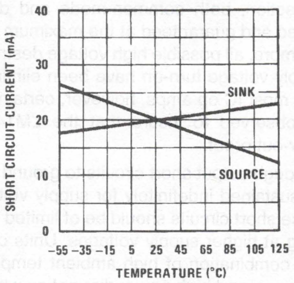
### Voltage Follower Slew Rate



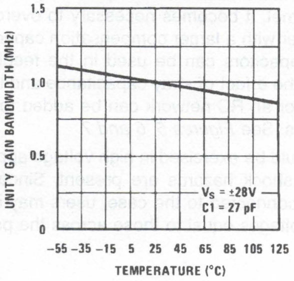
### Supply Current



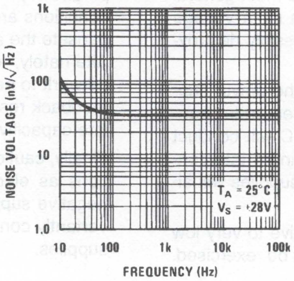
### Short Circuit Current



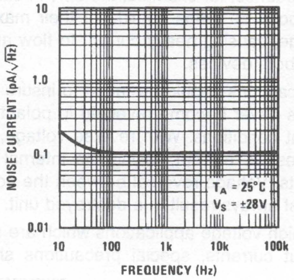
### Unity Gain Bandwidth



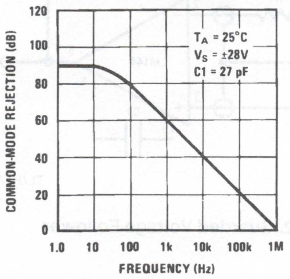
### Input Noise Voltage



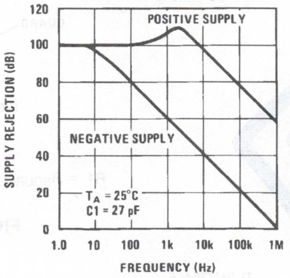
### Input Noise Current



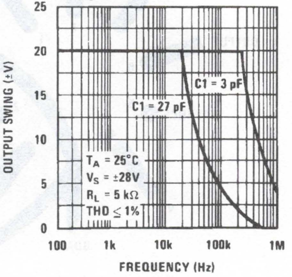
### Common-Mode Rejection



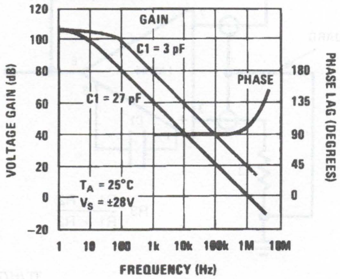
### Power Supply Rejection



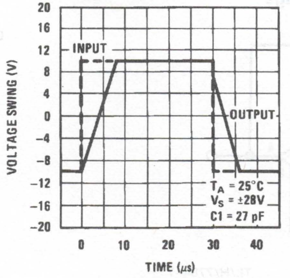
### Large Signal Frequency Response



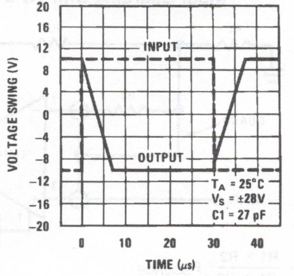
### Open Loop Frequency Response



### Voltage Follower Pulse Response



### Inverter Pulse Response



TL/H/7784–4

## Application Hints (See Also AN-127)

The LM144 is designed for trouble-free operation at any supply voltage up to a maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM144 remains virtually blow-out proof.

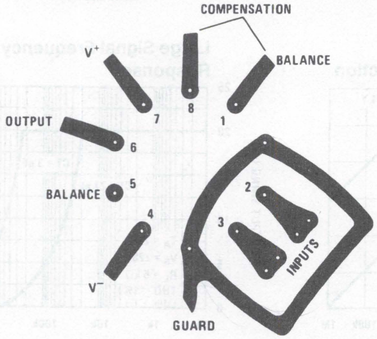
Although output short circuits to ground or either supply can be sustained indefinitely for supply voltages, below ±18V, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM144 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltge pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads. See *Figures 5, 6 and 7.*

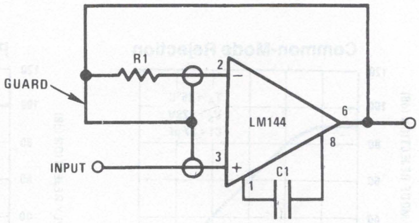
Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.



TL/H/7784-5

**Bottom View**

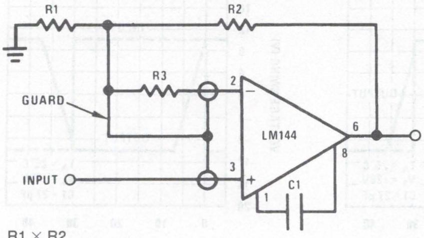
**FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package**



R1 = R$_{SOURCE}$

TL/H/7784-6

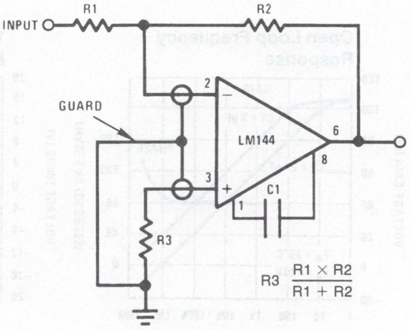
**FIGURE 2. Guarded Voltage Follower**



$R3 \times \frac{R1 \times R2}{R1 + R2}$ R$_{SOURCE}$

TL/H/7784-7

**FIGURE 3. Guarded Non-Inverting Amplifier**

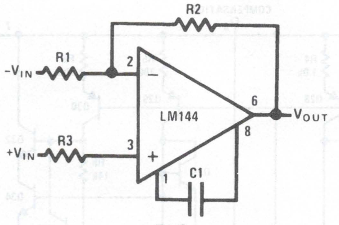


$R3 \frac{R1 \times R2}{R1 + R2}$

TL/H/7784-8

**FIGURE 4. Guarded Inverting Amplifier**

## Application Hints (Continued)


R2
R1
$-V_{IN}$
2
−
LM144
6
$V_{OUT}$
R3
$+V_{IN}$
3
+
8
1
C1

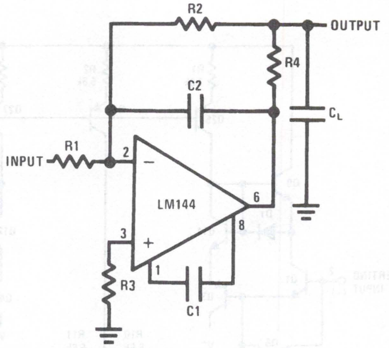
$$C1 = \frac{R1\,C_C}{R1 + R2} \quad \text{NON-INVERTING}$$

$$C1 = \frac{R1\,C_C}{R2} \quad \text{INVERTING}$$

$$C_C = 27\text{ PF}$$

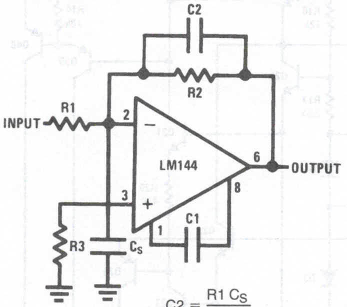
TL/H/7784-9

**FIGURE 5. Single Pole Compensation**


R2
OUTPUT
R4
C2
$C_L$
R1
INPUT
2
−
LM144
6
3
+
8
1
R3
C1

TL/H/7784-10

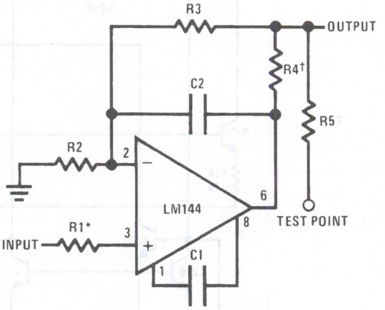
**FIGURE 6. Isolating Large Capacitive Loads**


C2
R2
R1
INPUT
2
−
LM144
6
OUTPUT
3
+
8
1
C1
R3
$C_S$

$$C2 = \frac{R1\,C_S}{R2}$$

TL/H/7784-11

**FIGURE 7. Compensating For Stray Input Capacitances or Large Feedback Resistor**


R3
OUTPUT
R4†
C2
R5∴
R2
2
−
LM144
6
TEST POINT
R1*
INPUT
3
+
8
1
C1

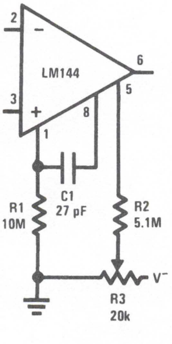
*Protects input

†Protects output

∴Protects output—not needed when R4 is used

TL/H/7784-12

**FIGURE 8. Protecting Against Gross Fault Conditions**

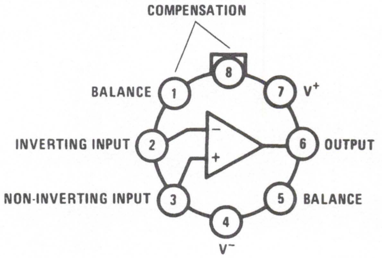

2
−
LM144
6
5
3
+
8
1
C1
27 pF
R1
10M
R2
5.1M
V⁻
R3
20k

TL/H/7784-13

**FIGURE 9. Balancing Circuit**

## Connection Diagram

### Metal Can Package


COMPENSATION
8
BALANCE
1
7
V⁺
INVERTING INPUT
2
−
+
6
OUTPUT
NON-INVERTING INPUT
3
5
BALANCE
4
V⁻

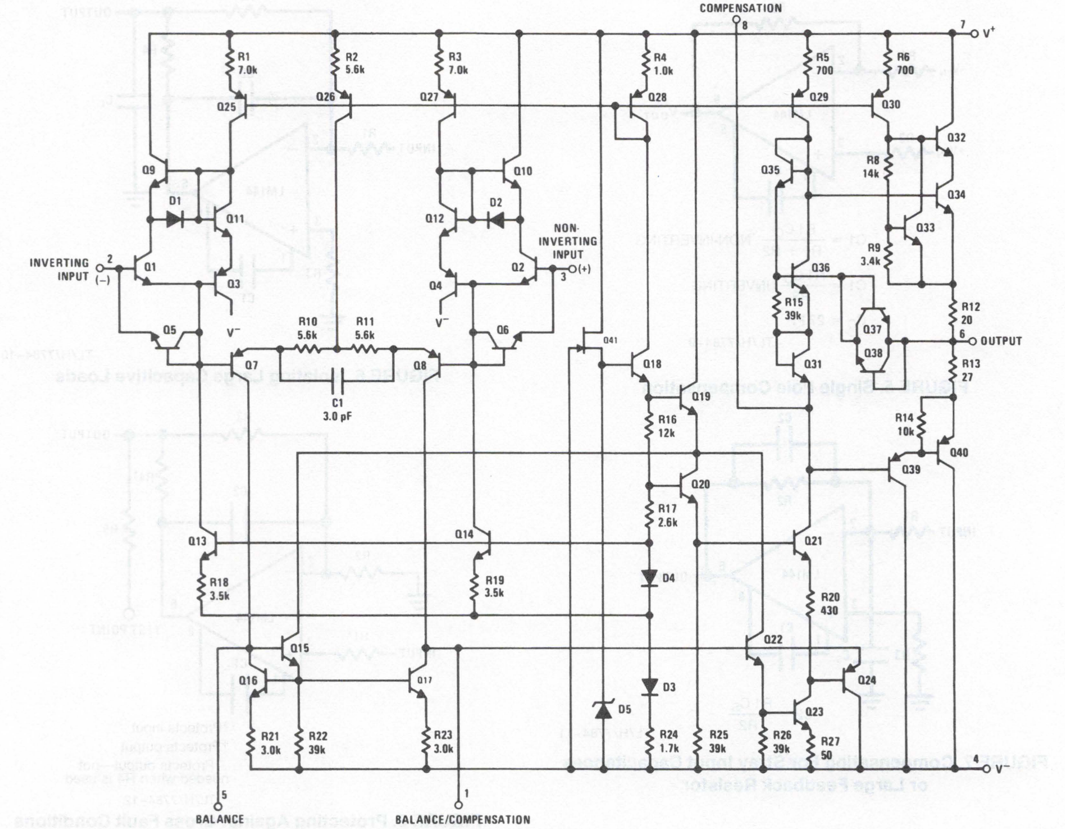
TL/H/7784-14

**Top View**

Pin 4 is connected to case

**Order Number LM144H or LM344H**
**See NS Package Number H08C**

## Schematic Diagram


COMPENSATION
8
7
V+
R1
7.0k
R2
5.6k
R3
7.0k
R4
1.0k
R5
700
R6
700
Q25
Q26
Q27
Q28
Q29
Q30
Q32
Q9
Q10
Q35
R8
14k
Q34
D1
Q11
Q12
D2
Q33
NON-INVERTING INPUT
3
(+)
R9
3.4k
INVERTING INPUT
2
(−)
Q1
Q3
Q4
Q2
Q36
R15
39k
R12
20
Q37
6
OUTPUT
Q38
Q5
V−
R10
5.6k
R11
5.6k
V−
Q6
Q41
Q7
Q8
Q18
Q31
R13
27
C1
3.0 pF
Q19
R16
12k
R14
10k
Q40
Q20
Q39
R17
2.6k
Q13
Q14
Q21
D4
R18
3.5k
R19
3.5k
R20
430
Q15
Q22
Q16
Q17
Q24
D3
D5
Q23
R21
3.0k
R22
39k
R23
3.0k
R24
1.7k
R25
39k
R26
39k
R27
50
4
V−
5
BALANCE
1
BALANCE/COMPENSATION

TL/H/7784-2

**National Semiconductor Corporation**

# LM146/LM246/LM346 Programmable Quad Operational Amplifiers

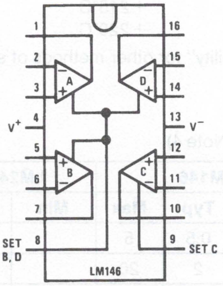
## General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors ($R_{SET}$) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

## Features ($I_{SET} = 10\ \mu A$)

| | |
|---|---|
| ■ Programmable electrical characteristics | |
| ■ Battery-powered operation | |
| ■ Low supply current | 350 μA amplifier |
| ■ Guaranteed gain bandwidth product | 0.8 MHz min |
| ■ Large DC voltage gain | 120 dB |
| ■ Low noise voltage | 28 nV/$\sqrt{Hz}$ |
| ■ Wide power supply range | ±1.5V to ±22V |
| ■ Class AB output stage–no crossover distortion | |
| ■ Ideal pin out for Biquad active filters | |
| ■ Input bias currents are temperature compensated | |

## Connection Diagram (Dual-In-Line Package, Top View)


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A
B
C
D
V+
V−
SET A, B, D
SET C
LM146

TL/H/5654-1

**Order Number LM146J, LM246J, LM346J, LM346M or LM346N**
**See NS Package Number J16A, M16A or N16A**

**PROGRAMMING EQUATIONS**

Total Supply Current = 1.4 mA ($I_{SET}$/10 μA)

Gain Bandwidth Product = 1 MHz ($I_{SET}$/10 μA)

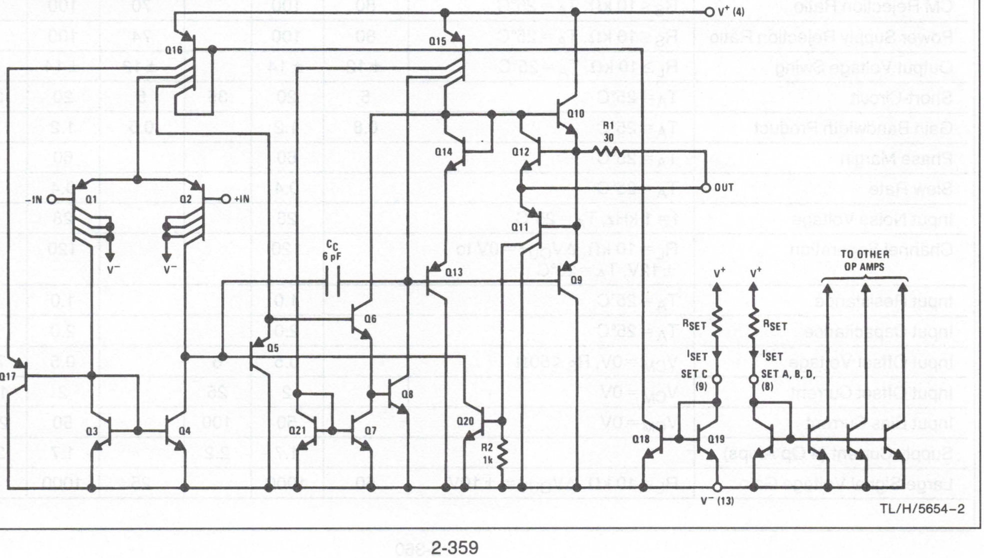
Slew Rate = 0.4/μs ($I_{SET}$/10 μA)

Input Bias Current ≅ 50 nA ($I_{SET}$/10 μA)

$I_{SET}$ = Current into pin 8, pin 9 (see schematic diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

## Schematic Diagram


V+ (4)
Q16
Q15
Q10
R1
30
Q14
Q12
OUT
Q11
−IN
Q1
Q2
+IN
V−
V−
CC
6 pF
Q13
Q9
Q6
Q5
Q17
Q8
Q3
Q4
Q21
Q7
Q20
R2
1k
V+
V+
RSET
RSET
ISET
ISET
SET C
(9)
SET A, B, D,
(8)
TO OTHER OP AMPS
Q18
Q19
V− (13)

TL/H/5654-2

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 5)**

| | | LM146 | LM246 | LM346 |
|---|---|---|---|---|
| Supply Voltage | | ±22V | ±18V | ±18V |
| Differential Input Voltage (Note 1) | | ±30V | ±30V | ±30V |
| CM Input Voltage (Note 1) | | ±15V | ±15V | ±15V |
| Power Dissipation (Note 2) | | 900 mW | 500 mW | 500 mW |
| Output Short-Circuit Duration (Note 3) | | Indefinite | Indefinite | Indefinite |
| Operating Temperature Range | | −55°C to +125°C | −25°C to +85°C | 0°C to +70°C |
| Maximum Junction Temperature | | 150°C | 110°C | 100°C |
| Storage Temperature Range | | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | | 260°C | 260°C | 260°C |
| Thermal Resistance ($\theta_{jA}$), (Note 2) | | | | |
| Cavity DIP (J) | Pd | 900 mW | 900 mW | 900 mW |
| | $\theta_{jA}$ | 100°C/W | 100°C/W | 100°C/W |
| Small Outline (M) | $\theta_{jA}$ | | | 115°C/W |
| Molded DIP (N) | Pd | | | 500 mW |
| | $\theta_{jA}$ | | | 90°C/W |
| Soldering Information | | | | |
| Dual-In-Line Package | | | | |
| Soldering (10 seconds) | | +260°C | +260°C | +260°C |
| Small Outline Package | | | | |
| Vapor Phase (60 seconds) | | +215°C | +215°C | +215°C |
| Infrared (15 seconds) | | +220°C | +220°C | +220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

## DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$ | | 0.5 | 5 | | 0.5 | 6 | mV |
| Input Offset Current | $V_{CM} = 0V$, $T_A = 25°C$ | | 2 | 20 | | 2 | 100 | nA |
| Input Bias Current | $V_{CM} = 0V$, $T_A = 25°C$ | | 50 | 100 | | 50 | 250 | nA |
| Supply Current (4 Op Amps) | $T_A = 25°C$ | | 1.4 | 2.0 | | 1.4 | 2.5 | mA |
| Large Signal Voltage Gain | $R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$, $T_A = 25°C$ | 100 | 1000 | | 50 | 1000 | | V/mV |
| Input CM Range | $T_A = 25°C$ | ±13.5 | ±14 | | ±13.5 | ±14 | | V |
| CM Rejection Ratio | $R_S \leq 10\ k\Omega$, $T_A = 25°C$ | 80 | 100 | | 70 | 100 | | dB |
| Power Supply Rejection Ratio | $R_S \leq 10\ k\Omega$, $T_A = 25°C$ | 80 | 100 | | 74 | 100 | | dB |
| Output Voltage Swing | $R_L \geq 10\ k\Omega$, $T_A = 25°C$ | ±12 | ±14 | | ±12 | ±14 | | V |
| Short-Circuit | $T_A = 25°C$ | 5 | 20 | 35 | 5 | 20 | 35 | mA |
| Gain Bandwidth Product | $T_A = 25°C$ | 0.8 | 1.2 | | 0.5 | 1.2 | | MHz |
| Phase Margin | $T_A = 25°C$ | | 60 | | | 60 | | Deg |
| Slew Rate | $T_A = 25°C$ | | 0.4 | | | 0.4 | | V/µs |
| Input Noise Voltage | $f = 1\ kHz$, $T_A = 25°C$ | | 28 | | | 28 | | $nV/\sqrt{Hz}$ |
| Channel Separation | $R_L = 10\ k\Omega$, $\Delta V_{OUT} = 0V$ to $\pm 12V$, $T_A = 25°C$ | | 120 | | | 120 | | dB |
| Input Resistance | $T_A = 25°C$ | | 1.0 | | | 1.0 | | MΩ |
| Input Capacitance | $T_A = 25°C$ | | 2.0 | | | 2.0 | | pF |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$ | | 0.5 | 6 | | 0.5 | 7.5 | mV |
| Input Offset Current | $V_{CM} = 0V$ | | 2 | 25 | | 2 | 100 | nA |
| Input Bias Current | $V_{CM} = 0V$ | | 50 | 100 | | 50 | 250 | nA |
| Supply Current (4 Op Amps) | | | 1.7 | 2.2 | | 1.7 | 2.5 | mA |
| Large Signal Voltage Gain | $R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$ | 50 | 1000 | | 25 | 1000 | | V/mV |

## DC Electrical Characteristics (Continued) ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input CM Range | | ±13.5 | ±14 | | ±13.5 | ±14 | | V |
| CM Rejection Ratio | $R_S \leq 50\Omega$ | 70 | 100 | | 70 | 100 | | dB |
| Power Supply Rejection Ratio | $R_S \leq 50\Omega$ | 76 | 100 | | 74 | 100 | | dB |
| Output Voltage Swing | $R_L \geq 10\ k\Omega$ | ±12 | ±14 | | ±12 | ±14 | | V |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$ | | 0.5 | 5 | | 0.5 | 7 | mV |
| Input Bias Current | $V_{CM} = 0V$, $T_A = 25°C$ | | 7.5 | 20 | | 7.5 | 100 | nA |
| Supply Current (4 Op Amps) | $T_A = 25°C$ | | 140 | 250 | | 140 | 300 | μA |
| Gain Bandwidth Product | $T_A = 25°C$ | 80 | 100 | | 50 | 100 | | kHz |

## DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$ | | 0.5 | 5 | | 0.5 | 7 | mV |
| Input CM Range | $T_A$ 25°C | ±0.7 | | | ±0.7 | | | V |
| CM Rejection Ratio | $R_S \leq 50\Omega$, $T_A = 25°C$ | | 80 | | | 80 | | dB |
| Output Voltage Swing | $R_L \geq 10\ k\Omega$, $T_A = 25°C$ | ±0.6 | | | ±0.6 | | | V |

**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{jMAX}$, $\theta_{jA}$, and the ambient temperature, $T_A$. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C $P_{dMAX}$, whichever is less.

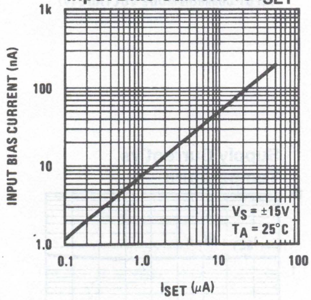
**Note 3:** Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 4:** These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

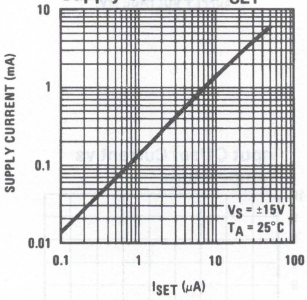
**Note 5:** Refer to RETS146X for LM146J military specifications.

## Typical Performance Characteristics

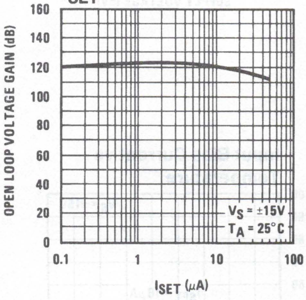
### Input Bias Current vs $I_{SET}$



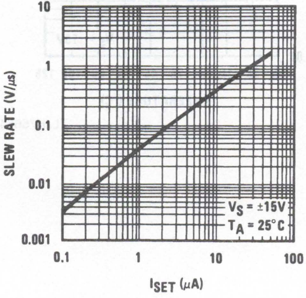
### Supply Current vs $I_{SET}$



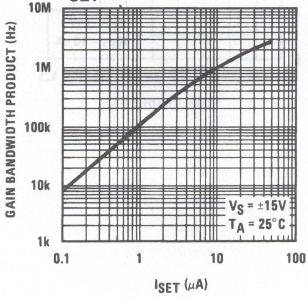
### Open Loop Voltage Gain vs $I_{SET}$



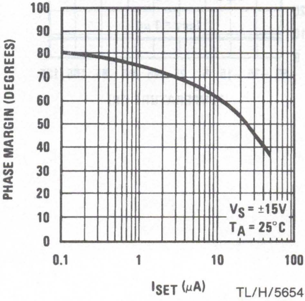
### Slew Rate vs $I_{SET}$



### Gain Bandwidth Product vs $I_{SET}$



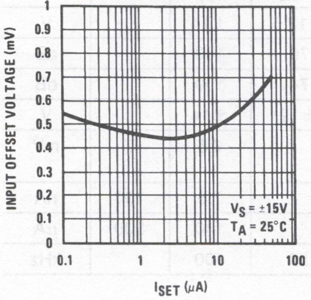
### Phase Margin vs $I_{SET}$



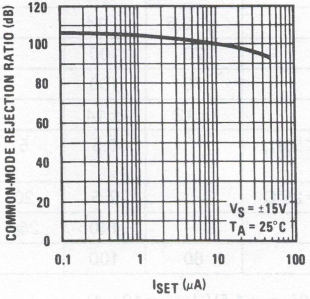
TL/H/5654–3

## Typical Performance Characteristics (Continued)

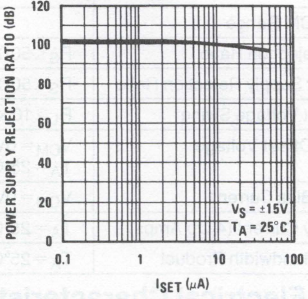
**Input Offset Voltage vs $I_{SET}$**



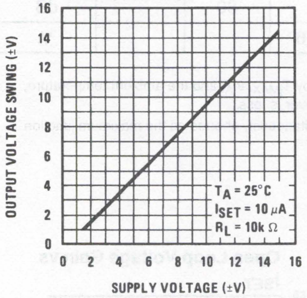
**Common-Mode Rejection Ratio vs $I_{SET}$**



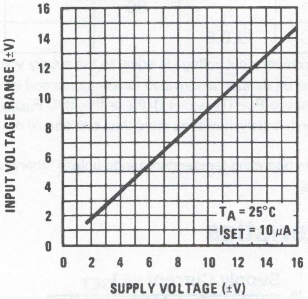
**Power Supply Rejection Ratio vs $I_{SET}$**



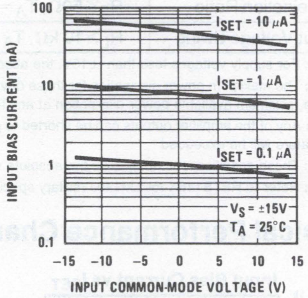
**Output Voltage Swing vs Supply Voltage**



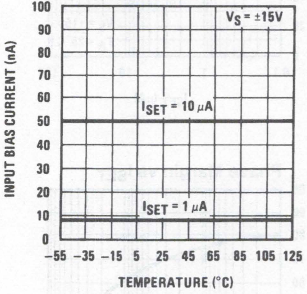
**Input Voltage Range vs Supply Voltage**



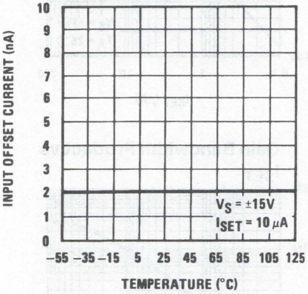
**Input Bias Current vs Input Common-Mode Voltage**



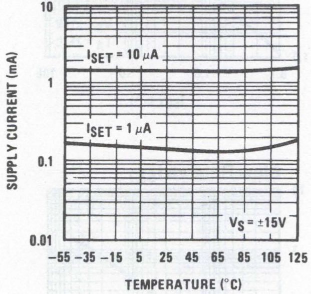
**Input Bias Current vs Temperature**



**Input Offset Current vs Temperature**



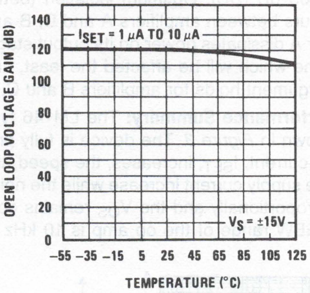
**Supply Current vs Temperature**



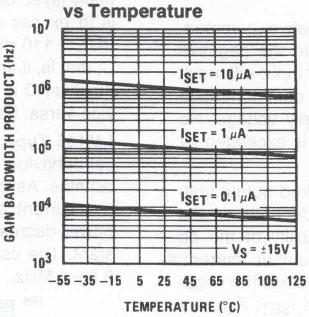
TL/H/5654-4

## Typical Performance Characteristics (Continued)

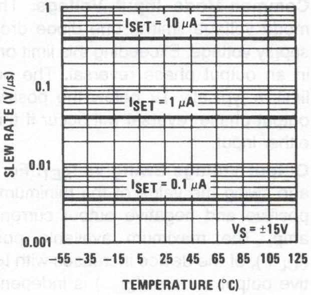
### Open Loop Voltage Gain vs Temperature



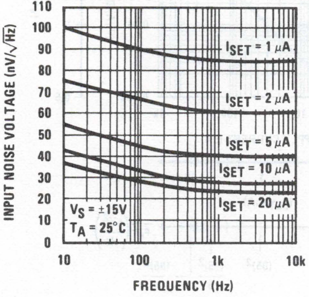
### Gain Bandwidth Product vs Temperature



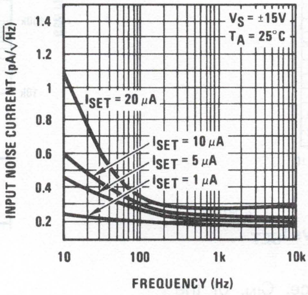
### Slew Rate vs Temperature



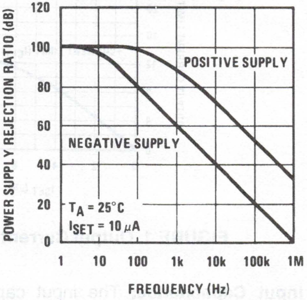
### Input Noise Voltage vs Frequency



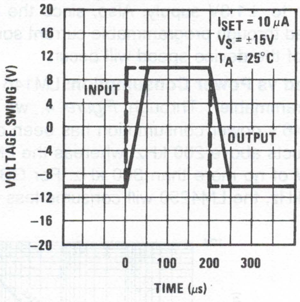
### Input Noise Current vs Frequency



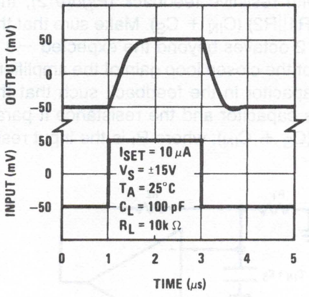
### Power Supply Rejection Ratio vs Frequency



### Voltage Follower Pulse Response

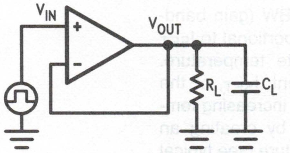


### Voltage Follower Transient Response



TL/H/5654–5

### Transient Response Test Circuit



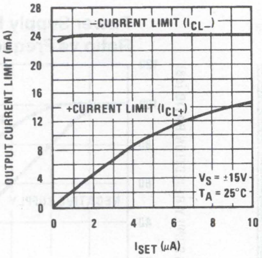
TL/H/5654–6

## Application Hints

Avoid reversing the power supply polarity; the device will fail.

**Common-Mode Input Voltage:** The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

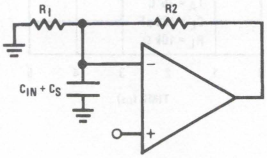
**Output Voltage Swing vs $I_{SET}$:** For a desired output voltage swing the value of the minimum load depends on the positive and negative output current capability of the op amp. The maximum available positive output current, ($I_{CL}+$), of the device increases with $I_{SET}$ whereas the negative output current ($I_{CL}-$) is independent of $I_{SET}$. *Figure 1* illustrates the above.



TL/H/5654-7

FIGURE 1. Output Current Limit vs $I_{SET}$

**Input Capacitance:** The input capacitance, $C_{IN}$, of the LM146 is approximately 2 pF; any stray capacitance, $C_S$, (due to external circuit circuit layout) will add to $C_{IN}$. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback (*Figure 2*), this pole occurs at $\frac{1}{2}\pi$ (R1||R2) ($C_{IN}$ + $C_S$). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where $R_I$ is the input resistance of the circuit.



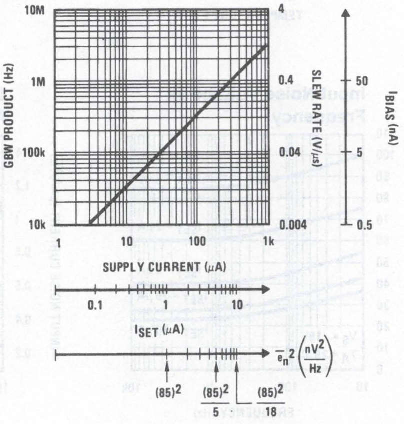
TL/H/5654-9

FIGURE 2

**Temperature Effect on the GBW:** The GBW (gain bandwidth product), of the LM146 is directly proportional to $I_{SET}$ and inversely proportional to the absolute temperature. When using resistors to set the bias current, $I_{SET}$, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an $I_{SET}$ current directly proportional to temperature (see typical applications).

**Isolation Between Amplifiers:** The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

**LM146 Typical Performance Summary:** The LM146 typical behaviour is shown in *Figure 3*. The device is fully predictable. As the set current, $I_{SET}$, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the $V_{OS}$ remains constant. The usable GBW range of the op amp is 10 kHz to 3.5−4 MHz.

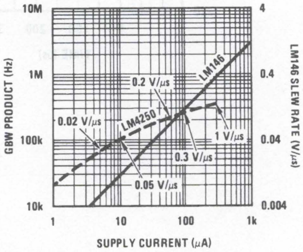


TL/H/5654-8

FIGURE 3. LM146 Typical Characteristics

**Low Power Supply Operation:** The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

**Speed vs Power Consumption:** LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz. For GBW products below 200 kHz, the LM4250 will consume less power.

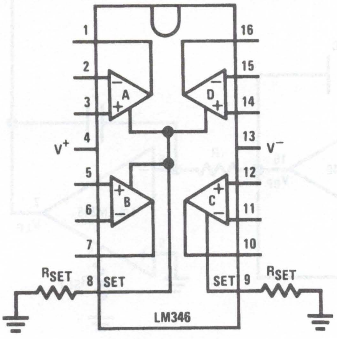


TL/H/5654-10

FIGURE 4. LM146 vs LM4250

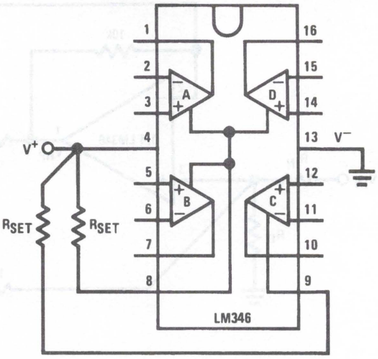
# Typical Applications

## Dual Supply or Negative Supply Biasing


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A
B
C
D
V+
V−
RSET
RSET
SET
SET
LM346

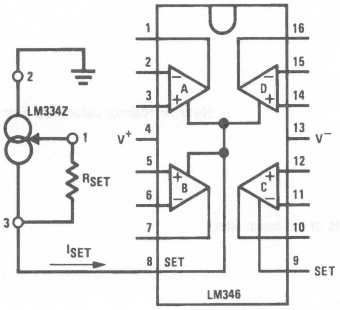
$$I_{SET} \cong \frac{|V^-| - 0.6V}{R_{SET}}$$

## Single (Positive) Supply Biasing


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A
B
C
D
V+
13 V−
RSET
RSET
LM346

$$I_{SET} \cong \frac{V^+ - 0.6V}{R_{SET}}$$

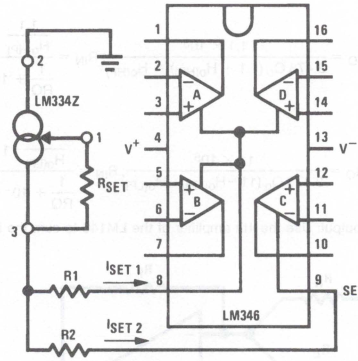
## Current Source Biasing with Temperature Compensation


2
LM334Z
1
3
RSET
ISET
V+
V−
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A
B
C
D
SET
SET
LM346

$$I_{SET} = \frac{67.7\text{ mV}}{R_{SET}}$$

- The LM334 provides an $I_{SET}$ directly proportional to absolute temperature. This cancels the slight GBW product Temperature coefficient of the LM346.

## Biasing all 4 Amplifiers with Single Current Source


2
LM334Z
1
3
RSET
R1
R2
ISET 1
ISET 2
V+
V−
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
A
B
C
D
SET
LM346

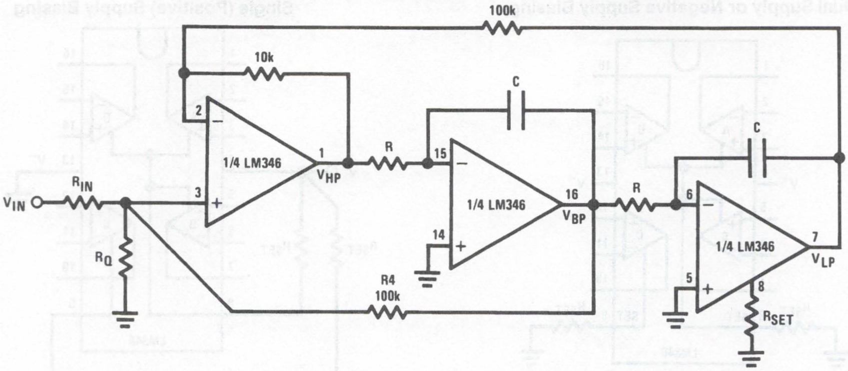
TL/H/5654–11

$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\text{ mV}}{R_{SET}}$$

- For $I_{SET1} \cong I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

## Active Filters Applications

### Basic (Non-Inverting "State Variable") Active Filter Building Block



TL/H/5654-12

- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

**Circuit synthesis equations** (for circuit analysis equations, consult with the LM148 data sheet).

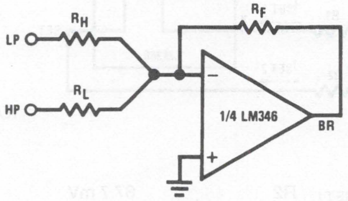
Need to know desired: $f_o$ = center frequency measured at the BP output

$Q_o$ = quality factor measured at the BP output

$H_o$ = gain at the output of interest (BP or HP or LP or all of them)

- Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$
- $R \times C = \frac{5.033 \times 10^{-2}}{f_o}$ (sec)
- For BP output: $R_Q = \left( \frac{3.478\, Q_o - H_{o(BP)}}{10^5} - \frac{H_{o(BP)}}{10^5 \times 3.748 \times Q_o} \right)^{-1}$; $R_{IN} = \frac{\left( \frac{3.478\, Q_o}{H_{o(BP)}} - 1 \right)}{\frac{1}{RQ} + 10^{-5}}$
- For HP ouput: $R_Q = \frac{1.1 \times 10^5}{3.478\, Q_o\, (1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \frac{\frac{1.1}{H_{o(HP)}} - 1}{\frac{1}{RQ} + 10^{-5}}$
- For LP output: $R_Q = \frac{11 \times 10^5}{3.478\, Q_o\, (11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \frac{\frac{11}{H_{o(LP)}} - 1}{\frac{1}{RQ} + 10^{-5}}$
- For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.

Note. All resistor values are given in ohms.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\, \frac{f_{notch}}{f_o}$$

TL/H/5654-13

Determine $R_F$ according to the desired gains: $H_{o(BR)} \Big|_{f << f_{notch}} = \frac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)} \Big|_{f >> f_{notch}} = \frac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (**$V_{HP}$, $V_{BP}$, $V_{LP}$), that is:**

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\, \mu A} \times \frac{1}{f_o \times H_o} \text{ (Volts)}$$

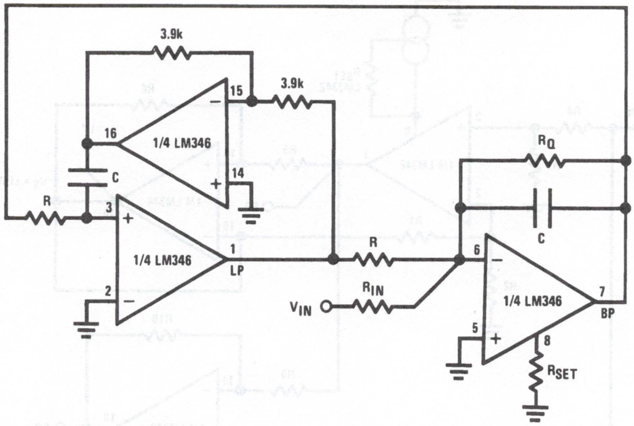
If necessary, use amplifier C, biased at higher $I_{SET}$, where you get the largest output swing.

**Deviation from Theoretical Predictions:** Due to the finite GBW products of the op amps the $f_o$, $Q_o$ will be slightly different from the theoretical predictions.

$$f_{real} \cong \frac{f_o}{1 + \frac{2\, f_o}{GBW}},\quad Q_{real} \cong \frac{Q_o}{1 - \frac{3.2\, f_o \times Q_o}{GBW}}$$

# Active Filters Applications (Continued)

## A Simple-to-Design BP, LP Filter Building Block


3.9k
3.9k
15
16
1/4 LM346
14
C
R
3
1/4 LM346
1
LP
2
R
RIN
VIN
RQ
C
6
1/4 LM346
7
BP
5
8
RSET

TL/H/5654–14

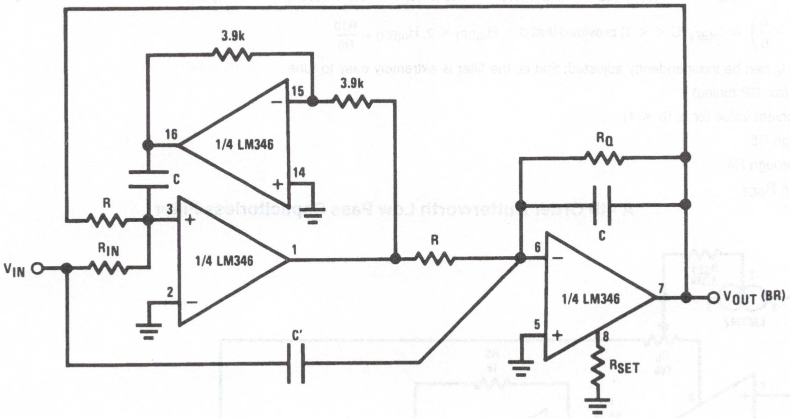
- If resistive biasing is used to set the LM346 performance, the $Q_o$ of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

### Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

## A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)


3.9k
3.9k
15
16
1/4 LM346
14
C
R
3
RIN
VIN
1/4 LM346
1
2
C′
R
RQ
C
6
1/4 LM346
7
VOUT (BR)
5
8
RSET

TL/H/5654–15

### Circuit Synthesis Equations

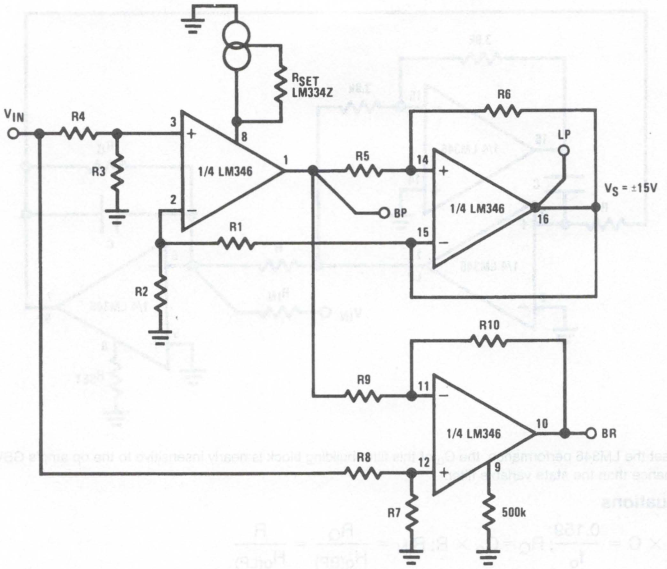
$$R \times C = \frac{0.159}{f_o};\ R_o = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f<<f_{notch}} = \frac{R}{R_{IN}}\ H_{o(BR)}\Big|_{f>>f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

## Active Filters Applications (Continued)

### Capacitorless Active Filters (Basic Circuit)


RSET
LM334Z
VIN
R4
3
+
8
R3
1/4 LM346
1
2
−
R1
R2
R6
R5
14
+
LP
BP
1/4 LM346
16
15
−
VS = ±15V
R10
R9
11
−
1/4 LM346
10
BR
R8
12
+
9
R7
500k

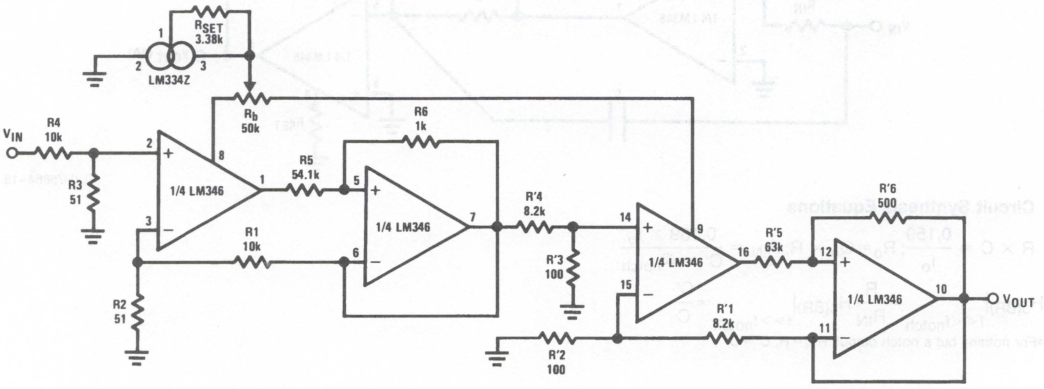
TL/H/5654–16

- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $\text{Vpeak(out)} \le \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}(\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R( + R10}$, $f_{o(BP)} = f_u\sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$, $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

$f_{o(BR)} = f_{o(BP)}, \left(1 - \frac{c}{b}\right) \cong f_{o(BP)}$ $(C < < 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.

- Advantage: $f_oQ_o$, $H_o$ can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust $Q_o$ through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust $f_o$ through $R_{SET}$

### A 4th Order Butterworth Low Pass Capacitorless Filter


RSET
3.38k
1
2
3
LM334Z
Rb
50k
VIN
R4
10k
R3
51
2
+
8
1/4 LM346
1
3
−
R1
10k
R2
51
R6
1k
R5
54.1k
5
+
1/4 LM346
7
6
−
R'4
8.2k
R'3
100
R'2
100
14
+
9
1/4 LM346
16
15
−
R'1
8.2k
R'5
63k
R'6
500
12
+
1/4 LM346
10
11
−
VOUT

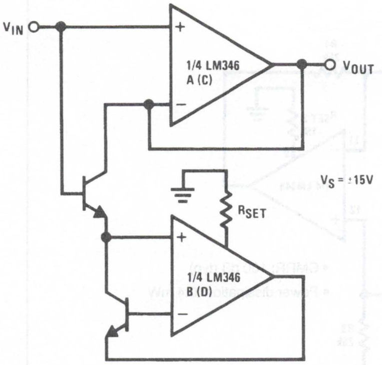
TL/H/5654–17

Ex: $f_c = 20$ kHz, $H_o$ (gain of the filter) $= 1$, $Q_{01} = 0.541$, $Q_{02} = 1.306$.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through $R_b$.

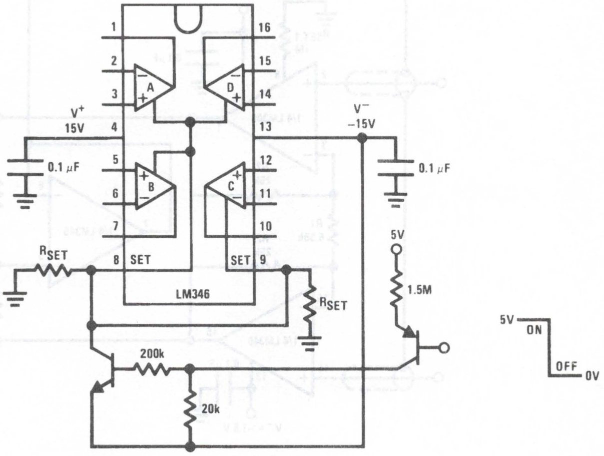
# Miscellaneous Applications

## A Unity Gain Follower with Bias Current Reduction


V_IN
V_OUT
1/4 LM346
A (C)
1/4 LM346
B (D)
R_SET
V_S = ±15V

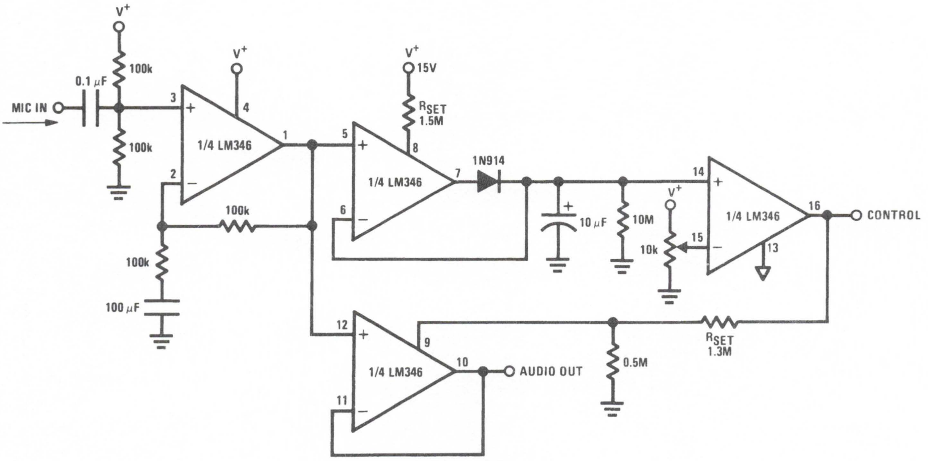
- For better performance, use a matched NPN pair.

## Circuit Shutdown


1
2
3
4
5
6
7
8
SET
16
15
14
13
12
11
10
9
SET
A
B
C
D
V+
15V
V−
−15V
0.1 µF
0.1 µF
R_SET
R_SET
LM346
200k
20k
5V
1.5M
5V
ON
OFF
0V

- By pulling the SET pin(s) to V− the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

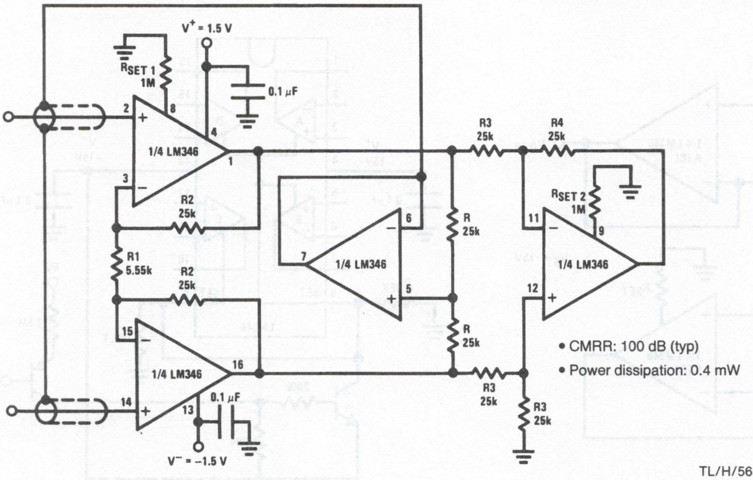
## Voice Activated Switch and Amplifier


V+
100k
0.1 µF
MIC IN
100k
V+
3
4
1/4 LM346
1
2
100k
100k
100 µF
V+
15V
R_SET
1.5M
5
8
1/4 LM346
7
6
1N914
10 µF
10M
V+
10k
14
15
1/4 LM346
16
13
CONTROL
12
9
1/4 LM346
10
11
AUDIO OUT
0.5M
R_SET
1.3M

TL/H/5654–18

## Miscellaneous Applications (Continued)

### X10 Micropower Instrumentation Amplifier with Buffered Input Guarding


V+ = 1.5 V
RSET 1
1M
0.1 μF
2
3
8
4
1
1/4 LM346
R2
25k
R1
5.55k
R2
25k
15
14
16
13
1/4 LM346
0.1 μF
V− = −1.5 V
6
7
5
1/4 LM346
R
25k
R
25k
R3
25k
R4
25k
R3
25k
R3
25k
RSET 2
1M
11
12
9
1/4 LM346

- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW

TL/H/5654–19

National Semiconductor Corporation

# LM148/LM149 Series Quad 741 Op Amp

## LM148/LM248/LM348 Quad 741 Op Amps

## LM149/LM249/LM349 Wide Band Decompensated ($A_{V\,(MIN)} = 5$)

## General Description

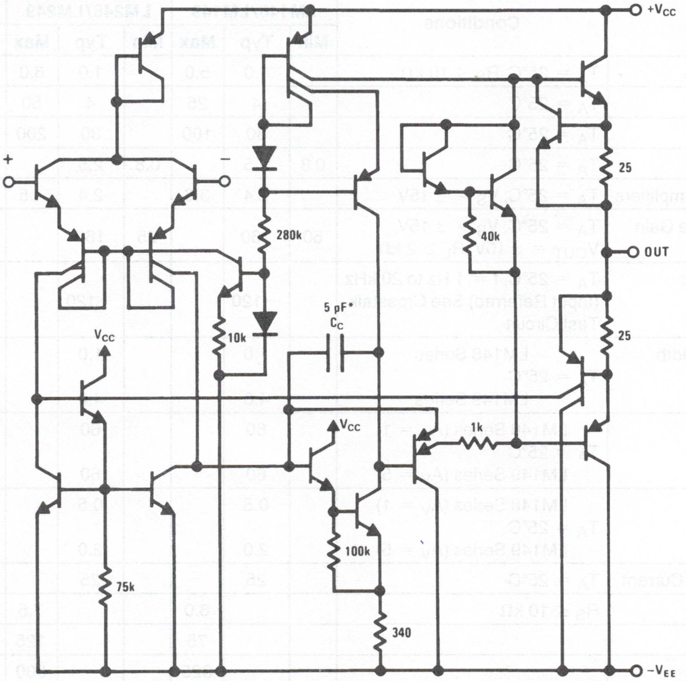
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

## Features

| | |
|---|---|
| ■ 741 op amp operating characteristics | |
| ■ Low supply current drain | 0.6 mA/Amplifier |
| ■ Class AB output stage—no crossover distortion | |
| ■ Pin compatible with the LM124 | |
| ■ Low input offset voltage | 1 mV |
| ■ Low input offset current | 4 nA |
| ■ Low input bias current | 30 nA |
| ■ Gain bandwidth product | |
| LM148 (unity gain) | 1.0 MHz |
| LM149 ($A_V \geq 5$) | 4 MHz |
| ■ High degree of isolation between amplifiers | 120 dB |
| ■ Overload protection for inputs and outputs | |

## Schematic Diagram



TL/H/7786-1

*1 pF in the LM149

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 4)**

| | LM148/LM149 | LM248/LM249 | LM348/LM349 |
|---|---|---|---|
| Supply Voltage | ±22V | ±18V | ±18V |
| Differential Input Voltage | ±44V | ±36V | ±36V |
| Output Short Circuit Duration (Note 1) | Continuous | Continuous | Continuous |
| Power Dissipation ($P_d$ at 25°C) and Thermal Resistance ($\theta_{jA}$), (Note 2) | | | |
| Molded DIP (N) $P_d$ | — | — | 750 mW |
| $\theta_{jA}$ | — | — | 100°C/W |
| Cavity DIP (J) $P_d$ | 1100 mW | 800 mW | 700 mW |
| $\theta_{JA}$ | 110°C/W | 110°C/W | 110°C/W |
| Maximum Junction Temperature ($T_{jMAX}$) | 150°C | 110°C | 100°C |
| Operating Temperature Range | $-55°C \le T_A \le +125°C$ | $-25°C \le T_A \le +85°C$ | $0°C \le T_A \le +70°C$ |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) Ceramic | 300°C | 300°C | 300°C |
| Lead Temperature (Soldering, 10 sec.) Plastic | | | 260°C |
| Soldering Information | | | |
| Dual-In-Line Package | | | |
| Soldering (10 seconds) | 260°C | 260°C | 260°C |
| Small Outline Package | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM148/LM149 | | | LM248/LM249 | | | LM348/LM349 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C, R_S \le 10\ k\Omega$ | | 1.0 | 5.0 | | 1.0 | 6.0 | | 1.0 | 6.0 | mV |
| Input Offset Current | $T_A = 25°C$ | | 4 | 25 | | 4 | 50 | | 4 | 50 | nA |
| Input Bias Current | $T_A = 25°C$ | | 30 | 100 | | 30 | 200 | | 30 | 200 | nA |
| Input Resistance | $T_A = 25°C$ | 0.8 | 2.5 | | 0.8 | 2.5 | | 0.8 | 2.5 | | MΩ |
| Supply Current All Amplifiers | $T_A = 25°C, V_S = \pm 15V$ | | 2.4 | 3.6 | | 2.4 | 4.5 | | 2.4 | 4.5 | mA |
| Large Signal Voltage Gain | $T_A = 25°C, V_S = \pm 15V$<br>$V_{OUT} = \pm 10V, R_L \ge 2\ k\Omega$ | 50 | 160 | | 25 | 160 | | 25 | 160 | | V/mV |
| Amplifier to Amplifier Coupling | $T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit | | −120 | | | −120 | | | −120 | | dB |
| Small Signal Bandwidth | $T_A = 25°C$ LM148 Series | | 1.0 | | | 1.0 | | | 1.0 | | MHz |
| | $T_A = 25°C$ LM149 Series | | 4.0 | | | 4.0 | | | 4.0 | | MHz |
| Phase Margin | $T_A = 25°C$ LM148 Series ($A_V = 1$) | | 60 | | | 60 | | | 60 | | degrees |
| | $T_A = 25°C$ LM149 Series ($A_V = 5$) | | 60 | | | 60 | | | 60 | | degrees |
| Slew Rate | $T_A = 25°C$ LM148 Series ($A_V = 1$) | | 0.5 | | | 0.5 | | | 0.5 | | V/µs |
| | $T_A = 25°C$ LM149 Series ($A_V = 5$) | | 2.0 | | | 2.0 | | | 2.0 | | V/µs |
| Output Short Circuit Current | $T_A = 25°C$ | | 25 | | | 25 | | | 25 | | mA |
| Input Offset Voltage | $R_S \le 10\ k\Omega$ | | | 6.0 | | | 7.5 | | | 7.5 | mV |
| Input Offset Current | | | | 75 | | | 125 | | | 100 | nA |
| Input Bias Current | | | | 325 | | | 500 | | | 400 | nA |

## Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM148/LM149 | | | LM248/LM249 | | | LM348/LM349 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$ | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$<br>$R_L = 2\ k\Omega$ | ±12<br>±10 | ±13<br>±12 | | ±12<br>±10 | ±13<br>±12 | | ±12<br>±10 | ±13<br>±12 | | V<br>V |
| Input Voltage Range | $V_S = \pm 15V$ | ±12 | | | ±12 | | | ±12 | | | V |
| Common-Mode Rejection Ratio | $R_S \leq 10\ k\Omega$ | 70 | 90 | | 70 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection | $R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$ | 77 | 96 | | 77 | 96 | | 77 | 96 | | dB |

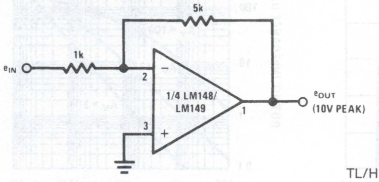
**Note 1:** Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 2:** The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by $T_{jMAX}$, $\theta_{jA}$, and the ambient temperature, $T_A$. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C $P_{dMAX}$, whichever is less.

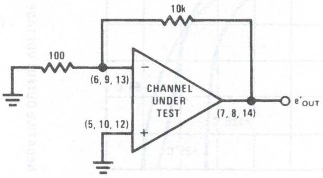
**Note 3:** These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

**Note 4:** Refer to RETS 148X for LM148 military specifications.

## Cross Talk Test Circuit



TL/H/7786-6



TL/H/7786-7

$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$V_S = \pm 15V$

## Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

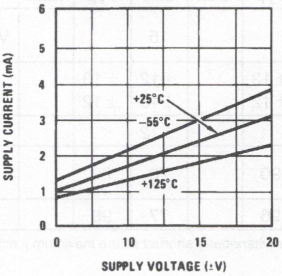
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

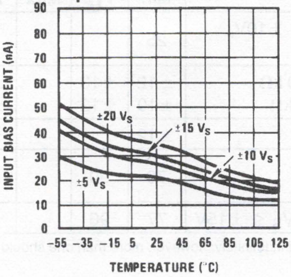
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Performance Characteristics

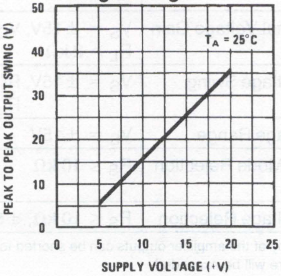
### Supply Current



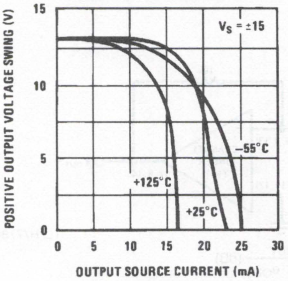
### Input Bias Current



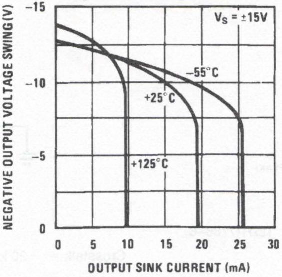
### Voltage Swing



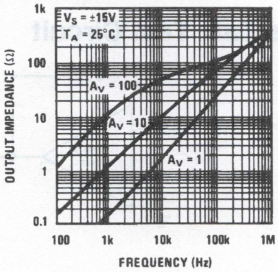
### Positive Current Limit



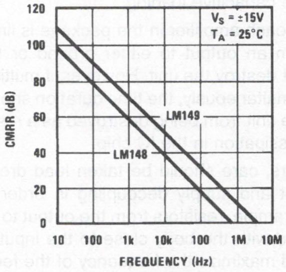
### Negative Current Limit



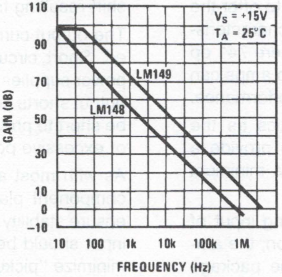
### Output Impedance



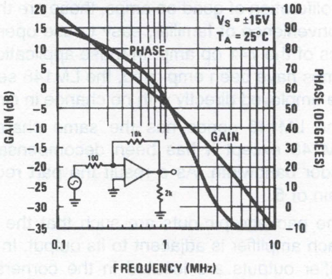
### Common-Mode Rejection Ratio



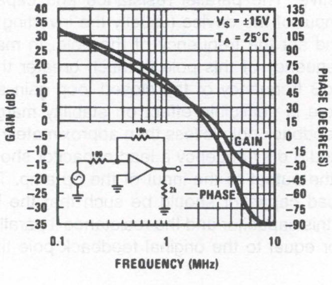
### Open Loop Frequency Response



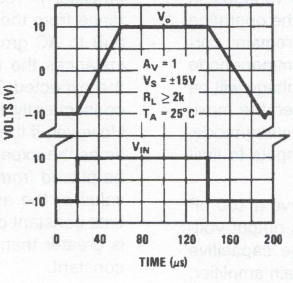
### Bode Plot LM148



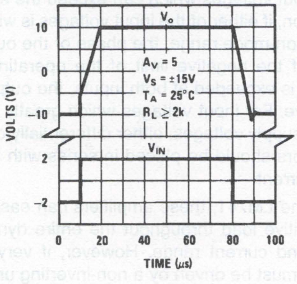
### Bode Plot LM149



### Large Signal Pulse Response (LM148)



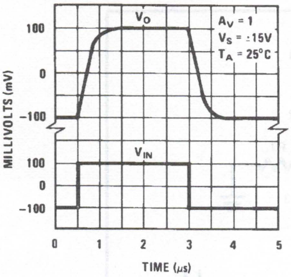
### Large Signal Pulse Response (LM149)



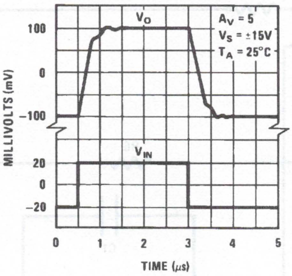
TL/H/7786–3

# Typical Performance Characteristics (Continued)

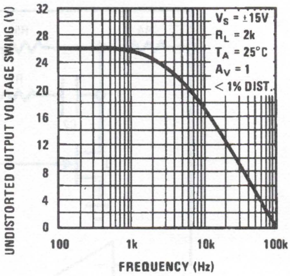
### Small Signal Pulse Response (LM148)



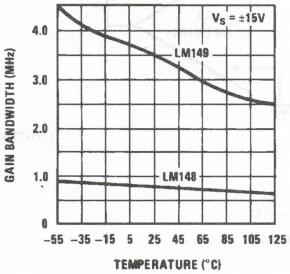
### Small Signal Pulse Response (LM149)



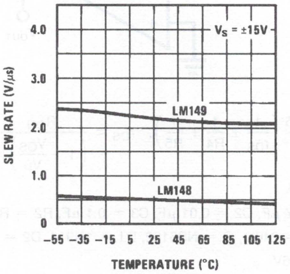
### Undistorted Output Voltage Swing



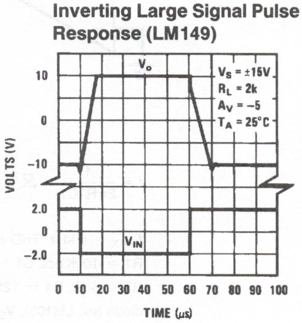
### Gain Bandwidth



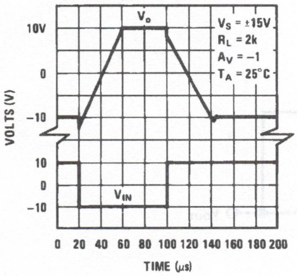
### Slew Rate



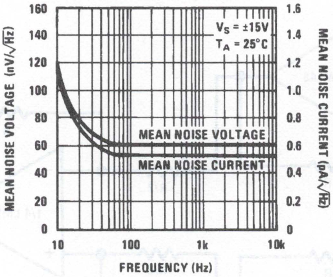
### Inverting Large Signal Pulse Response (LM149)



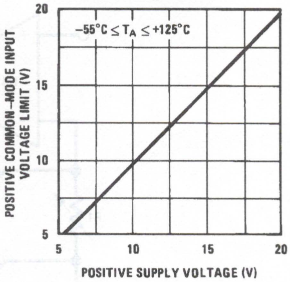
### Inverting Large Signal Pulse Response (LM148)



### Input Noise Voltage and Noise Current

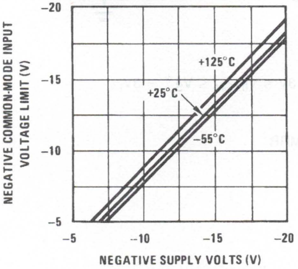


### Positive Common-Mode Input Voltage Limit



TL/H/7786–4

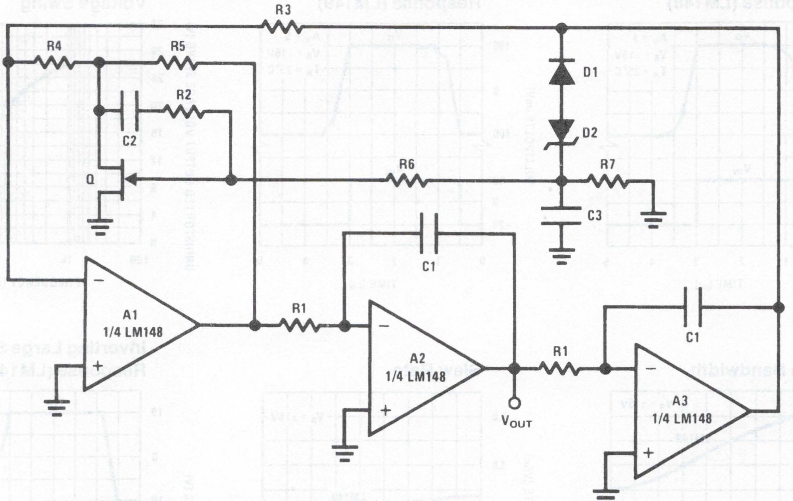
### Negative Common-Mode Input Voltage Limit



TL/H/7786–5

## Typical Applications—LM148

### One Decade Low Distortion Sinewave Generator


R3
R4
R5
R2
C2
Q
R6
D1
D2
R7
C3
C1
A1
1/4 LM148
R1
A2
1/4 LM148
V_OUT
R1
C1
A3
1/4 LM148

TL/H/7786-8

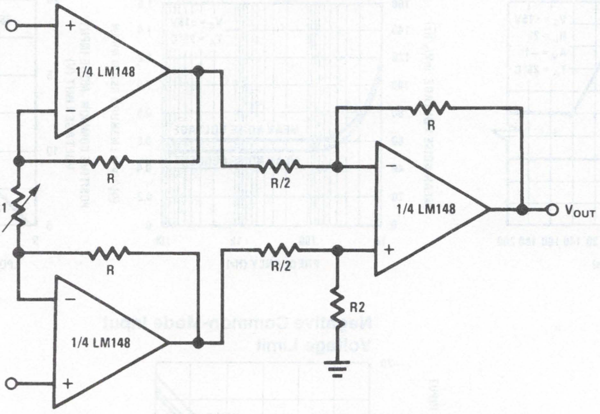
$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

$f_{MAX} = 5$ kHz, THD $\leq 0.03\%$

R1 = 100k pot. C1 = 0.0047 $\mu$F, C2 = 0.01 $\mu$F, C3 = 0.1 $\mu$F, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12$\Omega$, R5 = 240$\Omega$, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), $V_S = \pm 15V$

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

### Low Cost Instrumentation Amplifier


1/4 LM148
R
R1
R
R/2
R
R/2
1/4 LM148
V_OUT
R2
1/4 LM148

TL/H/7786-9

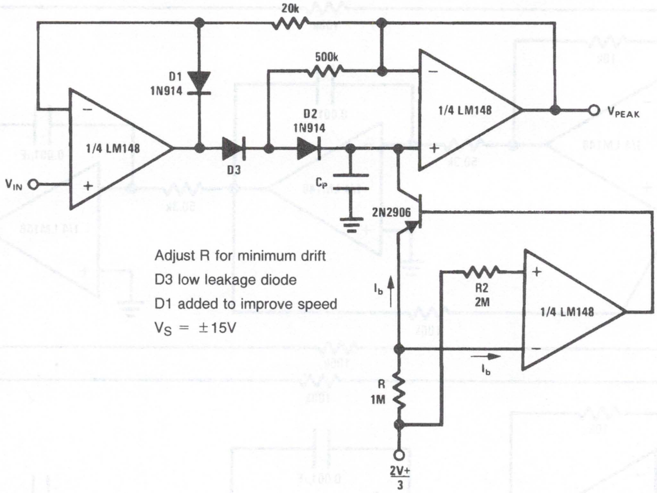
$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \leq V_{IN\,CM} \leq V_S^+ - 3V,$$

$V_S = \pm 15V$

R = R2, trim R2 to boost CMRR

# Typical Applications—LM148 (Continued)

## Low Drift Peak Detector with Bias Current Compensation


20k
500k
D1
1N914
D2
1N914
D3
1/4 LM148
1/4 LM148
1/4 LM148
$V_{IN}$
$V_{PEAK}$
$C_P$
2N2906
$I_b$
$I_b$
R2
2M
R
1M
2V+
3

Adjust R for minimum drift

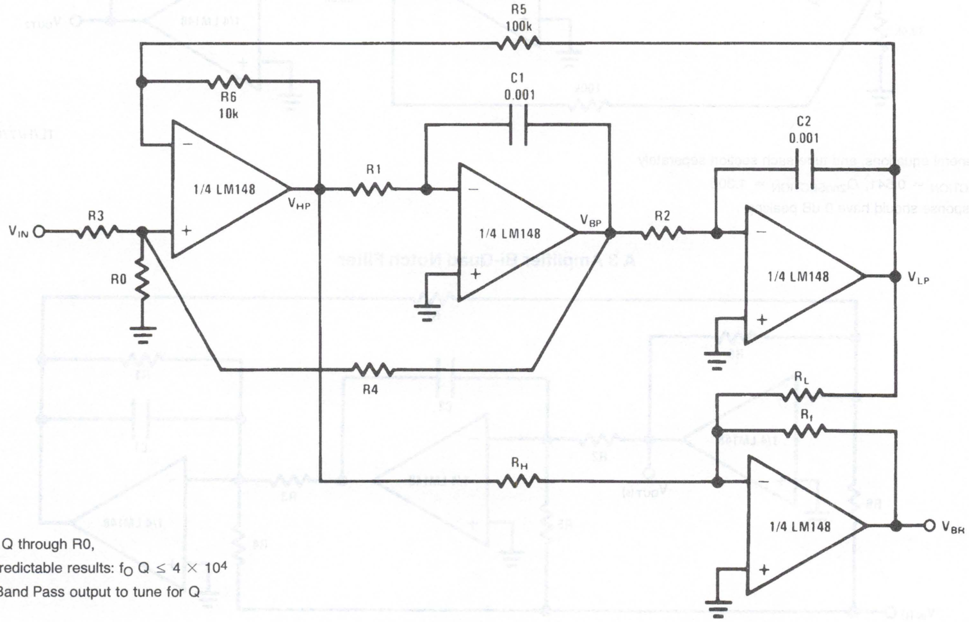
D3 low leakage diode

D1 added to improve speed

$V_S = \pm 15V$

TL/H/7786-10

## Universal State-Space Filter


R5
100k
R6
10k
C1
0.001
C2
0.001
R1
R2
R3
R0
R4
$R_L$
$R_f$
$R_H$
$V_{IN}$
$V_{HP}$
$V_{BP}$
$V_{LP}$
$V_{BR}$
1/4 LM148
1/4 LM148
1/4 LM148
1/4 LM148

Tune Q through R0,

For predictable results: $f_O \, Q \le 4 \times 10^4$

Use Band Pass output to tune for Q

TL/H/7786-11

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o{}^2$$

$$N_{HP(s)} = S^2 H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O H_{OBP}}{Q} \quad N_{LP} = \omega_o{}^2 H_{OLP}.$$

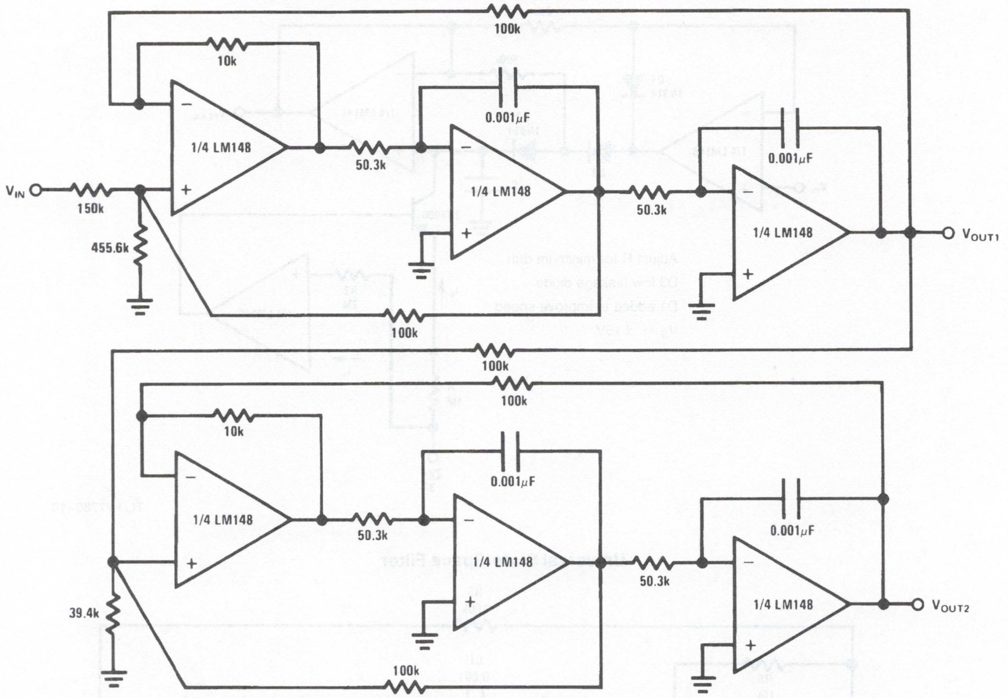
$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\, t_1\, t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

## Typical Applications—LM148 (Continued)

### A 1 kHz 4 Pole Butterworth


100k
10k
1/4 LM148
0.001μF
50.3k
1/4 LM148
0.001μF
$V_{IN}$
150k
455.6k
50.3k
1/4 LM148
$V_{OUT1}$
100k
100k
100k
10k
0.001μF
1/4 LM148
50.3k
1/4 LM148
0.001μF
39.4k
50.3k
1/4 LM148
$V_{OUT2}$
100k

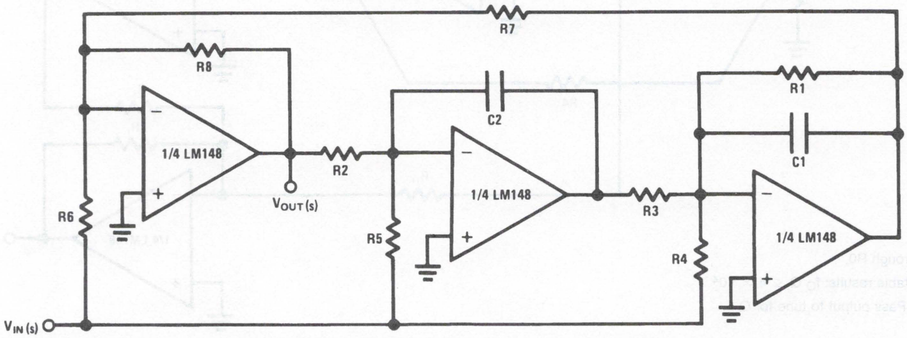
TL/H/7786–12

Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

### A 3 Amplifier Bi-Quad Notch Filter


R7
R8
1/4 LM148
$V_{OUT(s)}$
R2
C2
1/4 LM148
R3
R1
C1
1/4 LM148
R6
R5
R4
$V_{IN(s)}$

TL/H/7786–13

$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\ f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\ f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

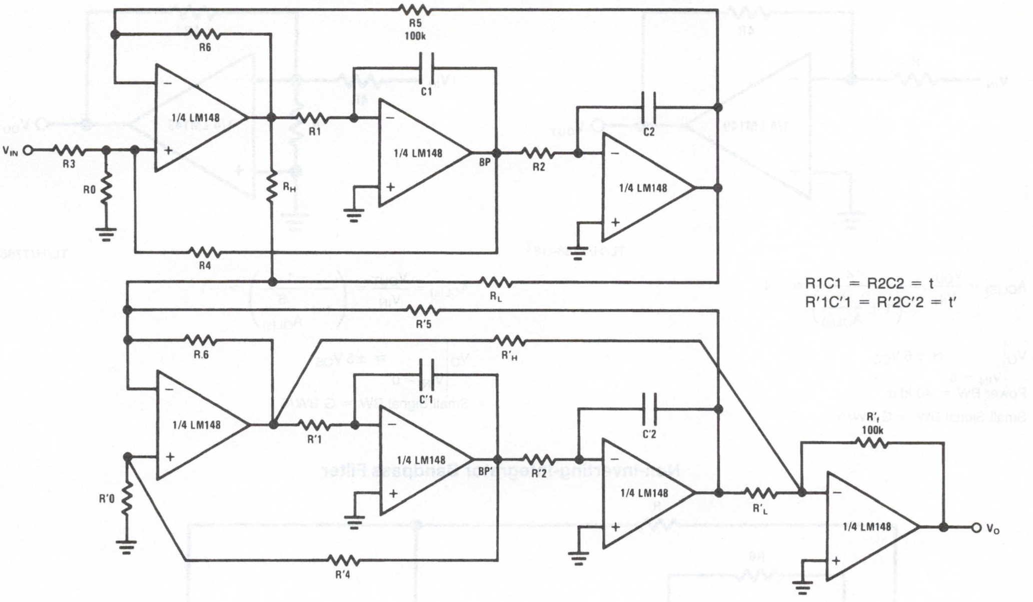
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: $f_{NOTCH} = 3$ kHz, $Q = 5$, $R1 = 270k$, $R2 = R3 = 20k$, $R4 = 27k$, $R5 = 20k$, $R6 = R8 = 10k$, $R7 = 100k$, $C1 = C2 = 0.001\ \mu F$

Better noise performance than the state-space approach.

## Typical Applications—LM148 (Continued)

### A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)


R5
100k
R6
C1
1/4 LM148
R1
V_IN
R3
R0
R_H
BP
R2
C2
R4
R_L
R'5
R.6
R'_H
C'1
R'1
BP'
R'2
C'2
R'0
R'4
R'_L
R'_f
100k
V_O

R1C1 = R2C2 = t
R'1C'1 = R'2C'2 = t'

TL/H/7786–14

$f_C$ = 1 kHz, $f_S$ = 2 kHz, $f_p$ = 0.543, $f_Z$ = 2.14, Q = 0.841, $f'_P$ = 0.987, $f'_Z$ = 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t'},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

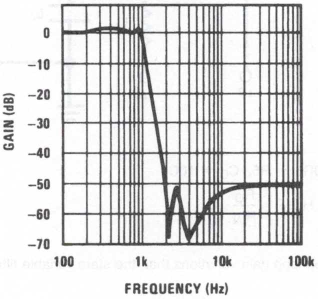
$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, $R_L$ = 100k, $R_H$ = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, $R'_L$ = 100k, $R'_H$ = 248.12k, R'f = 100k. All capacitors are 0.001 μF.

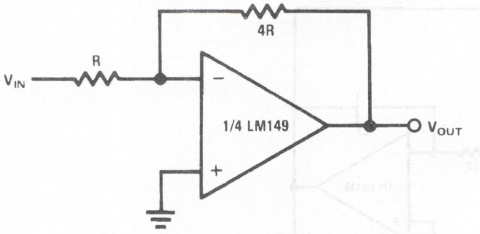
**Lowpass Response**



TL/H/7786–15

## Typical Applications—LM149

### Minimum Gain to Insure LM149 Stability


4R
R
V_IN
−
+
1/4 LM149
V_OUT

TL/H/7786-16

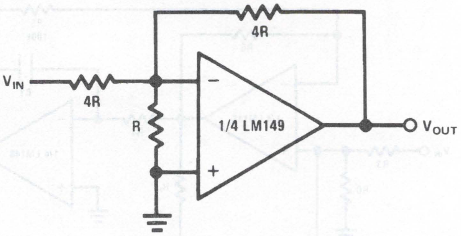
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL(s)}}\right)} \cong -4$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\,V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

### The LM149 as a Unity Gain Inverter


4R
V_IN
4R
R
−
+
1/4 LM149
V_OUT

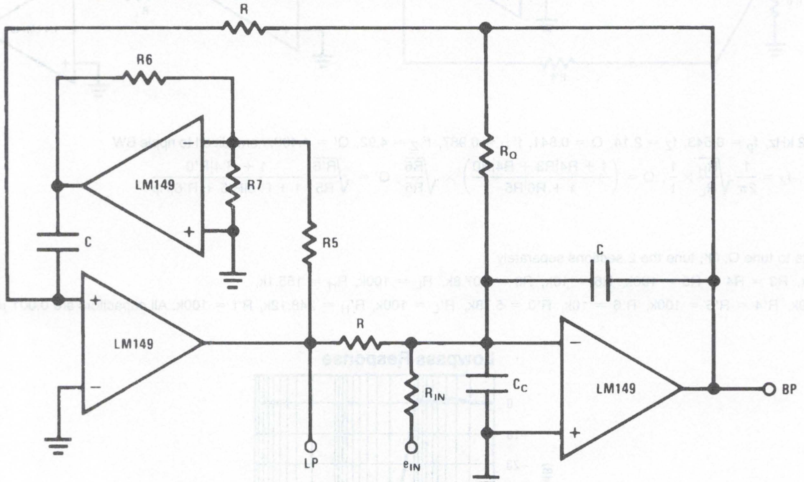
TL/H/7786-17

$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1 + \frac{6}{A_{OL(s)}}}\right) \cong -1$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\,V_{OS}$$

Small Signal BW = G BW/5

### Non-inverting-Integrator Bandpass Filter


R
R6
LM149
R7
C
R5
LM149
R
LP
R_IN
e_IN
R_Q
C
C_C
LM149
BP

TL/H/7786-18

For stability purposes: R7 = R6/4, 10R6 = R5, $C_C$ = 10C

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6}} \times \frac{1}{RC},\quad Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}},\quad Ho_{BP} = \frac{R_Q}{R_{IN}}$$

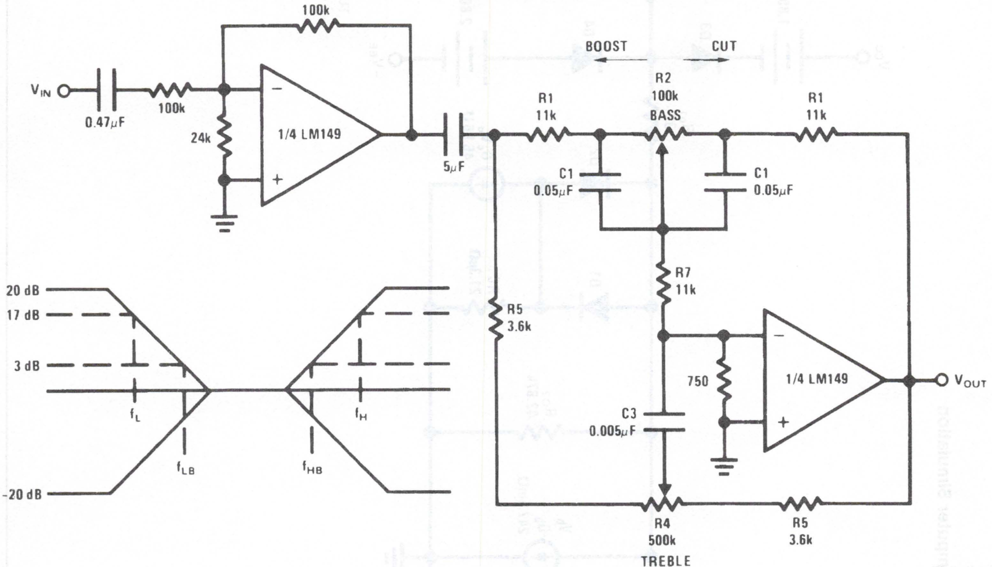
$f_{O(MAX)}$, $Q_{MAX}$ = 20 kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, $C_C$ added for compensation

## Typical Applications—LM149 (Continued)

### Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)


100k
$V_{IN}$
0.47µF
100k
24k
1/4 LM149
5µF
BOOST
CUT
R1 11k
R2 100k BASS
R1 11k
C1 0.05µF
C1 0.05µF
R7 11k
R5 3.6k
750
1/4 LM149
$V_{OUT}$
C3 0.005µF
R4 500k TREBLE
R5 3.6k
20 dB
17 dB
3 dB
-20 dB
$f_L$
$f_{LB}$
$f_{HB}$
$f_H$

TL/H/7786-19

$V_S = \pm 15V$, $V_{OUT(MAX)} = 9.1\ V_{RMS}$,

$f_{MAX} = 20$ kHz, THD $\leq$ 1%

Duplicate the above circuit for stereo

$f_L = \frac{1}{2\pi R2C1}$, $f_{LB} = \frac{1}{2\pi R1C1}$

$f_H = \frac{1}{2\pi R5C3}$, $f_{HB} = \frac{1}{2\pi (R1 + 2R7)\,C3}$

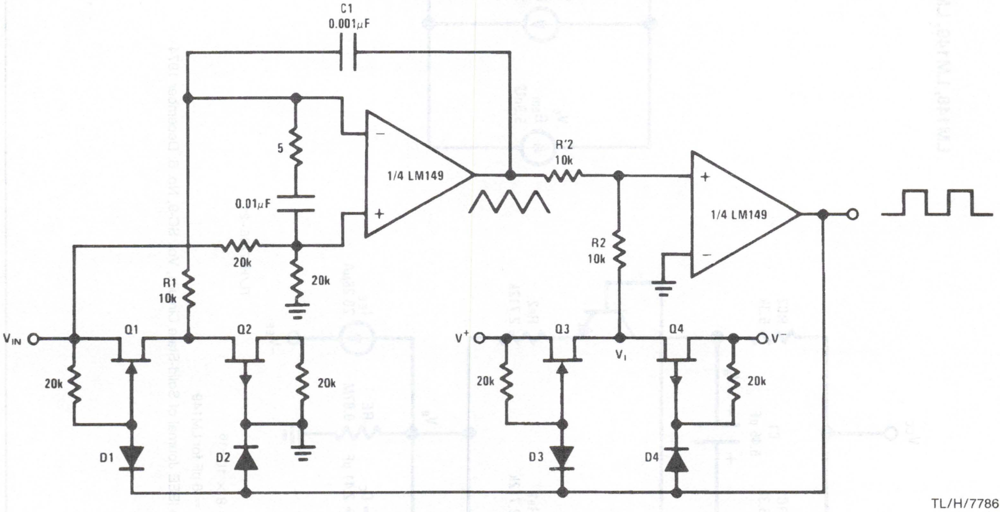
Max Bass Gain $\cong$ (R1 + R2)/R1

Max Treble Gain $\cong$ (R1 + 2R7)/R5

as shown: $f_L \cong 32$ Hz, $f_{LB} \cong 320$ Hz

$f_H \cong 11$ kHz, $f_{HB} \cong 1.1$ Hz

### Triangular Squarewave Generator


C1 0.001µF
5
0.01µF
1/4 LM149
R'2 10k
1/4 LM149
20k
20k
R1 10k
R2 10k
$V_{IN}$
Q1
Q2
Q3
Q4
$V^+$
$V^-$
$V_I$
20k
20k
20k
20k
D1
D2
D3
D4

TL/H/7786-20

$f = \frac{K \times V_{IN}}{8V^+C1R1}$, $K = R2/R'2$, $\frac{2V_I}{K} \leq 25V$, $V^+ = V^-$, $V_S = \pm 15V$

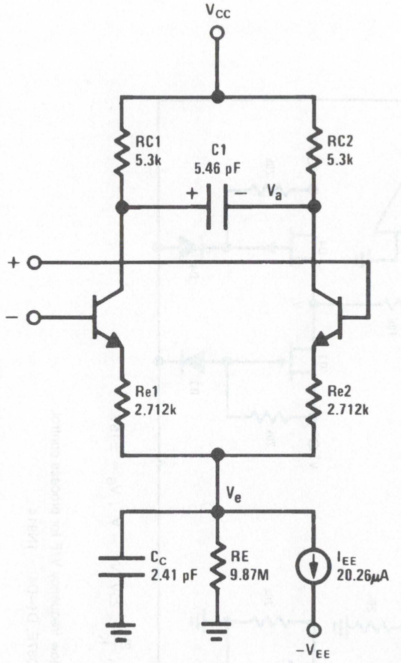
Use LM125 for ±15V supply

The circuit can be used as a low frequency V/F for process control.

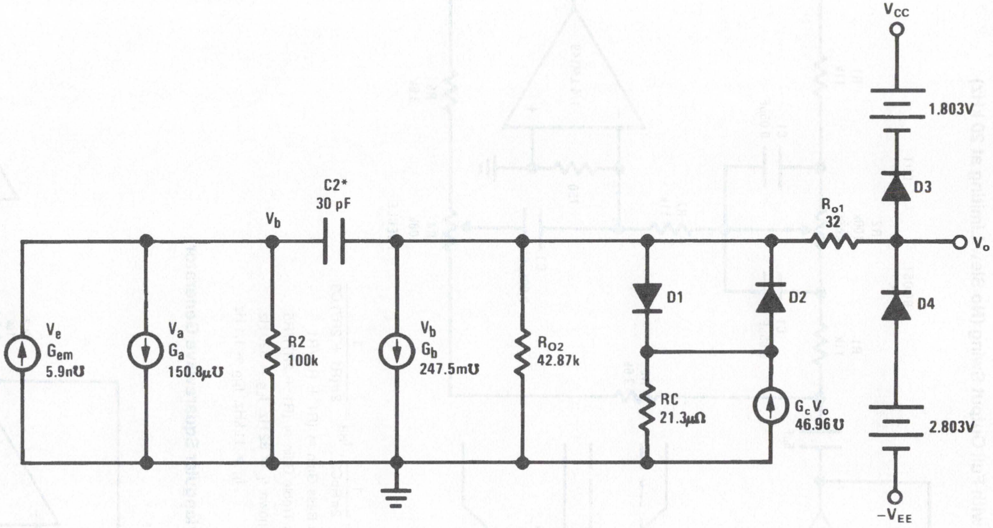
Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

## Typical Simulation

### LM148, LM149, LM741 Macromodel for Computer Simulation


V_CC
RC1
5.3k
C1
5.46 pF
+
−
V_a
RC2
5.3k
+
−
Re1
2.712k
Re2
2.712k
V_e
C_C
2.41 pF
RE
9.87M
I_EE
20.26μA
−V_EE

TL/H/7786-21


V_b
C2*
30 pF
V_e
G_em
5.9n℧
V_a
G_a
150.8μ℧
R2
100k
V_b
G_b
247.5m℧
R_O2
42.87k
D1
RC
21.3μΩ
D2
G_cV_o
46.96℧
V_CC
1.803V
D3
R_o1
32
V_o
D4
2.803V
−V_EE

TL/H/7786-22

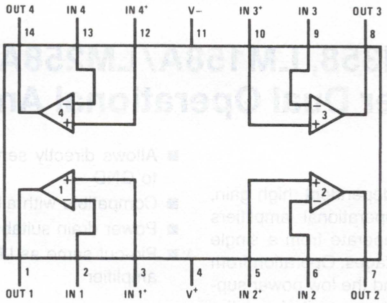
$\beta_{o1} = 112$ $\quad I_S = 8 \times 10^{-16}$

$\beta_{o2} = 144$ $\quad$ *C2 = 6 pF for LM149

For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

## Connection Diagram

**Dual-In-Line Package**


OUT 4
IN 4⁻
IN 4⁺
V⁻
IN 3⁺
IN 3⁻
OUT 3
14
13
12
11
10
9
8
4
3
1
2
1
2
3
4
5
6
7
OUT 1
IN 1⁻
IN 1⁺
V⁺
IN 2⁺
IN 2⁻
OUT 2

TL/H/7786–2

**Top View**

**Order Number LM148J, LM248J, LM348J, LM149J, LM249J, LM349J, LM348M, LM348N or LM349N**
**See NS Package Number J14A, M14A or N14A**

**National Semiconductor Corporation**

# LM158/LM258/LM358, LM158A/LM258A/LM358A, LM2904 Low Power Dual Operational Amplifiers

## General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard $+5\ V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm15\ V_{DC}$ power supplies.

## Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

## Advantages

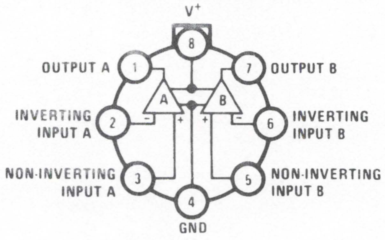
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package
- Allows directly sensing near GND and $V_{OUT}$ also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

## Features

| | |
|---|---|
| Internally frequency compensated for unity gain | |
| Large dc voltage gain | 100 dB |
| Wide bandwidth (unity gain)<br>(temperature compensated) | 1 MHz |
| Wide power supply range: | |
| Single supply | $3\ V_{DC}$ to $32\ V_{DC}$ |
| or dual supplies | $\pm1.5\ V_{DC}$ to $\pm16\ V_{DC}$ |
| Very low supply current drain (500 μA)—essentially independent of supply voltage (1 mW/op amp at $+5\ V_{DC}$) | |
| Low input biasing current<br>(temperature compensated) | $45\ nA_{DC}$ |
| Low input offset voltage | $2\ mV_{DC}$ |
| and offset current | $5\ nA_{DC}$ |
| Input common-mode voltage range includes ground | |
| Differential input voltage range equal to the power supply voltage | |
| Large output voltage swing | $0\ V_{DC}$ to $V^{+} - 1.5\ V_{DC}$ |

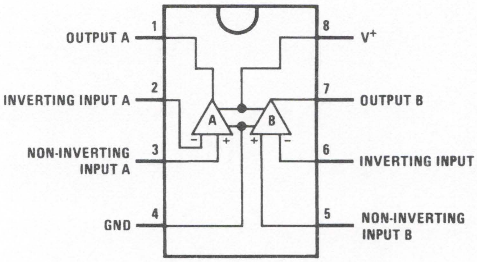
## Connection Diagrams (Top Views)

**Metal Can Package**



TL/H/7787-1

**Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H**
**See NS Package Number H08C**



TL/H/7787-2

**Order Number LM158J, LM158AJ or LM358J**
**See NS Package Number J08A**
**Order Number LM358M, LM358AM or LM2904M**
**See NS Package Number M08A**
**Order Number LM358AN, LM358N or LM2904N**
**See NS Package Number N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 9)**

| | LM158/LM258/LM358<br>LM158A/LM258A/LM358A | LM2904 |
|---|---|---|
| Supply Voltage, $V^+$ | 32 $V_{DC}$ or ±16 $V_{DC}$ | 26 $V_{DC}$ or ±13 $V_{DC}$ |
| Differential Input Voltage | 32 $V_{DC}$ | 26 $V_{DC}$ |
| Input Voltage | $-0.3$ $V_{DC}$ to $+32$ $V_{DC}$ | $-0.3$ $V_{DC}$ to $+26$ $V_{DC}$ |
| Power Dissipation (Note 1) | | |
| Molded DIP (LM358N) | 830 mW | 830 mW |
| Metal Can (LM158H/ LM258H/LM358H) | 550 mW | |
| Small Outline Package | 530 mW | 530 mW |
| Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15$ $V_{DC}$ and $T_A = 25°C$ | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3$ $V_{DC}$) (Note 3) | 50 mA | 50 mA |

| | LM158/LM258/LM358<br>LM158A/LM258A/LM358A | LM2904 |
|---|---|---|
| Operating Temperature Range | | |
| LM358 | 0°C to +70°C | −40°C to +85°C |
| LM258 | −25°C to +85°C | |
| LM158 | −55°C to +125°C | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) DIP | 260°C | 260°C |
| ESD rating to be determined. | | |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 300°C |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics $V^+ = +5.0$ $V_{DC}$, $T_A = 25°C$, unless otherwise stated

| Parameter | Conditions | LM158A | | | LM258A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 5) | | ±1 | ±2 | | ±1 | ±3 | | ±2 | ±3 | | ±2 | ±5 | | ±2 | ±7 | | ±2 | ±7 | $mV_{DC}$ |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, (Note 6) | | 20 | 50 | | 40 | 80 | | 45 | 100 | | 45 | 150 | | 45 | 250 | | 45 | 250 | $nA_{DC}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | ±2 | ±10 | | ±2 | ±15 | | ±5 | ±30 | | ±3 | ±30 | | ±5 | ±50 | | ±5 | ±50 | $nA_{DC}$ |
| Input Common-Mode Voltage Range | $V^+ = 30$ $V_{DC}$, (Note 7) (LM2904, $V^+ = 26V$) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | $V_{DC}$ |
| Supply Current | $R_L = \infty$, $V^+ = 30V$ (LM2904 $V^+ = 26V$) | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | | 1 | 2 | $mA_{DC}$ |
| | $R_L = \infty$ on all Op Amps Over Full Temperature Range | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | $mA_{DC}$ |

## Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

| Parameter | Conditions | LM158A | | | LM258A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $V^+ = 15\ V_{DC}$ $R_L \geq 2\ k\Omega$, (For $V_O = 1\ V_{DC}$ to $11\ V_{DC}$) | 50 | 100 | | 50 | 100 | | 25 | 100 | | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |
| Common-Mode Rejection Ratio | DC, $V_{CM} = 0V$ to $V^+ -1.5\ V_{DC}$ | 70 | 85 | | 70 | 85 | | 65 | 85 | | 70 | 85 | | 65 | 70 | | 50 | | 70 | dB |
| Power Supply Rejection Ratio | DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2904, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$), $T_A = 25°C$ | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |
| Amplifier-to-Amplifier Coupling | f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8) | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | dB |
| Output Current Source | $V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$ | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | $mA_{DC}$ |
| Sink | $V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $V^+ = 15\ V_{DC}$, $T_A = 25°C$, $V_O = 2\ V_{DC}$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | $mA_{DC}$ |
| | $V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $T_A = 25°C$, $V_O = 200\ mV_{DC}$, $V^+ = 15\ V_{DC}$ | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | $\mu A_{DC}$ |
| Short Circuit to Ground | $T_A = 25°C$, (Note 2), $V^+ = 15\ V_{DC}$ | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | $mA_{DC}$ |
| Input Offset Voltage | (Note 5) | | | ±4 | | | ±4 | | | ±5 | | | ±7 | | | ±9 | | | ±10 | $mV_{DC}$ |
| Input Offset Voltage Drift | $R_S = 0\Omega$ | | 7 | 15 | | 7 | 15 | | 7 | 20 | | 7 | | | 7 | | | 7 | | μV/°C |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$ | | | ±30 | | | ±30 | | | ±75 | | | ±100 | | | ±150 | | ±45 | ±200 | $nA_{DC}$ |
| Input Offset Current Drift | $R_S = 0\Omega$ | | 10 | 200 | | 10 | 200 | | 10 | 300 | | 10 | | | 10 | | | 10 | | $pA_{DC}/°C$ |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ | | 40 | 100 | | 40 | 100 | | 40 | 200 | | 40 | 300 | | 40 | 500 | | 40 | 500 | $nA_{DC}$ |

## Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

| Parameter | Conditions | LM158A | | | LM258A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Common-Mode Voltage Range | $V^+ = 30\ V_{DC}$, (Note 7)<br>(LM2904, $V^+ = 26\ V_{DC}$) | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | $V_{DC}$ |
| Large Signal Voltage Gain | $V^+ = +15\ V_{DC}$<br>($V_O = 1\ V_{DC}$ to $11\ V_{DC}$)<br>$R_L \geq 2\ k\Omega$ | 25 | | | 25 | | | 15 | | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing<br>$V_{OH}$ | $V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$ | 26 | | | 26 | | | 26 | | | 26 | | | 26 | | | 22 | | | $V_{DC}$ |
| | $R_L \geq 10\ k\Omega$<br>(LM2904, $V^+ = 26\ V_{DC}$) | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 23 | 24 | | $V_{DC}$ |
| $V_{OL}$ | $V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$ | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 100 | $mV_{DC}$ |
| Output Current<br>Source | $V_O = 2\ V_{DC}$<br>$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$,<br>$V^+ = 15\ V_{DC}$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | $mA_{DC}$ |
| Sink | $V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$,<br>$V^+ = 15\ V_{DC}$ | 10 | 15 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | $mA_{DC}$ |

**Note 1:** For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short cirucits to ground, the maximum output current is approximately 40 mA independent of the magnitude of $V^+$. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

**Note 4:** These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

**Note 5:** $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with $V^+$ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$) at 25°C. For LM2904, $V^+$ from $5\ V_{DC}$ to $26\ V_{DC}$.

**Note 6:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

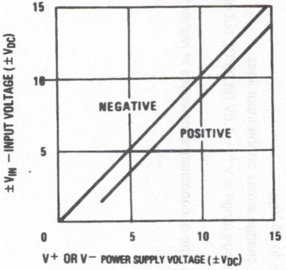
**Note 7:** The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2904), independent of the magnitude of $V^+$.

**Note 8:** Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

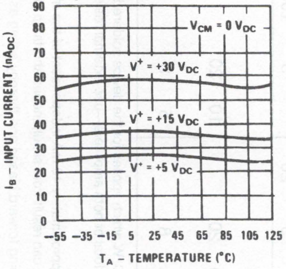
**Note 9:** Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

# Typical Performance Characteristics

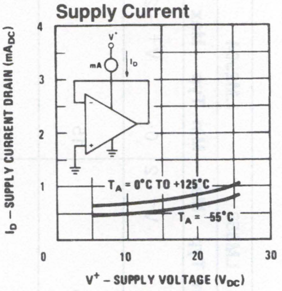
### Input Voltage Range



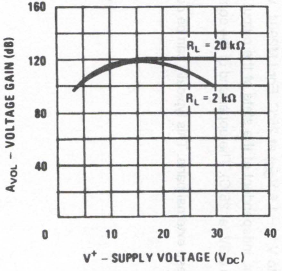
### Input Current



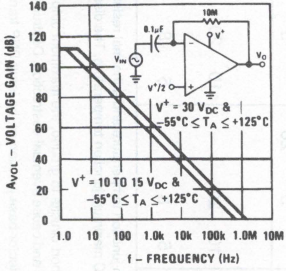
### Supply Current



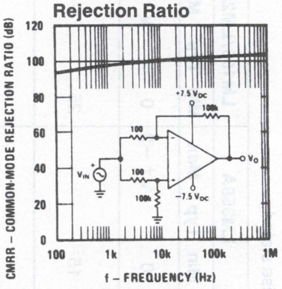
### Voltage Gain



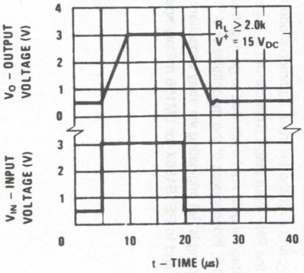
### Open Loop Frequency Response



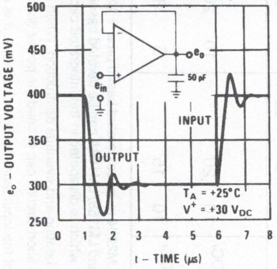
### Common-Mode Rejection Ratio



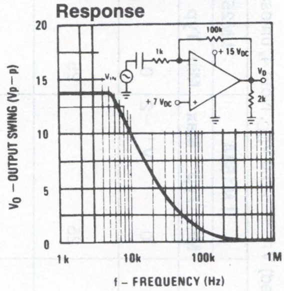
### Voltage Follower Pulse Response



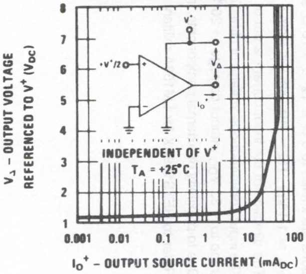
### Voltage Follower Pulse Response (Small Signal)



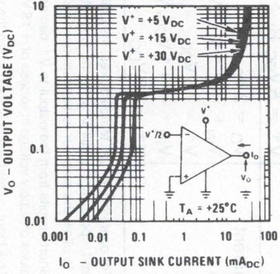
### Large Signal Frequency Response



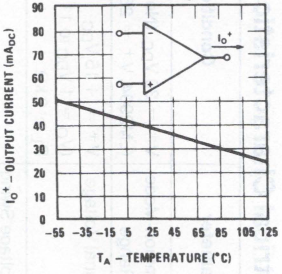
### Output Characteristics Current Sourcing



### Output Characteristics Current Sinking



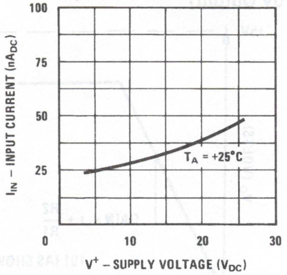
### Current Limiting



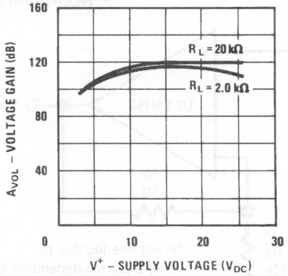
TL/H/7787-4

## Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



TL/H/7787–5

## Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 $V_{DC}$. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 $V_{DC}$.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than $V^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3$ $V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

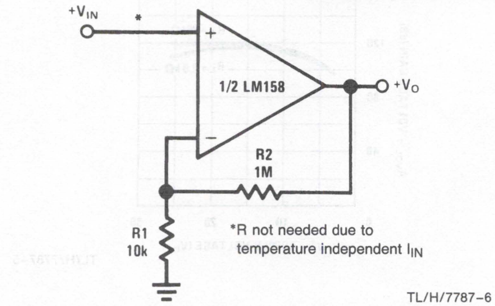
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 $V_{DC}$ to 30 $V_{DC}$.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

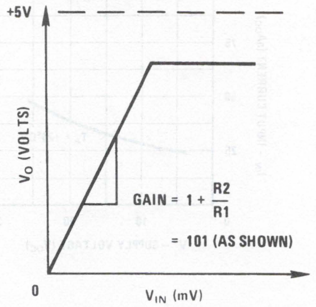
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

# Typical Single-Supply Applications $(V^+ = 5.0\ V_{DC})$

## Non-Inverting DC Gain (0V Input = 0V Output)

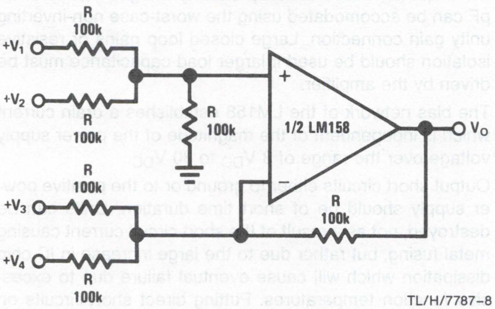

+VIN
*
+
−
1/2 LM158
+VO
R2
1M
R1
10k
*R not needed due to temperature independent IIN

TL/H/7787-6



TL/H/7787-7

## DC Summing Amplifier $(V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq 0\ V_{DC})$

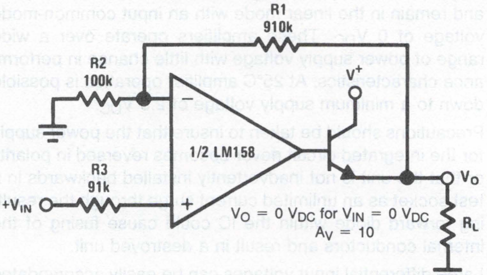

R
100k
+V1
+V2
R
100k
R
100k
+V3
+V4
R
100k
R
100k
R
100k
R
100k
+
−
1/2 LM158
VO

TL/H/7787-8

Where: $V_O = V_1 + V_2 - V_3 - V_4$

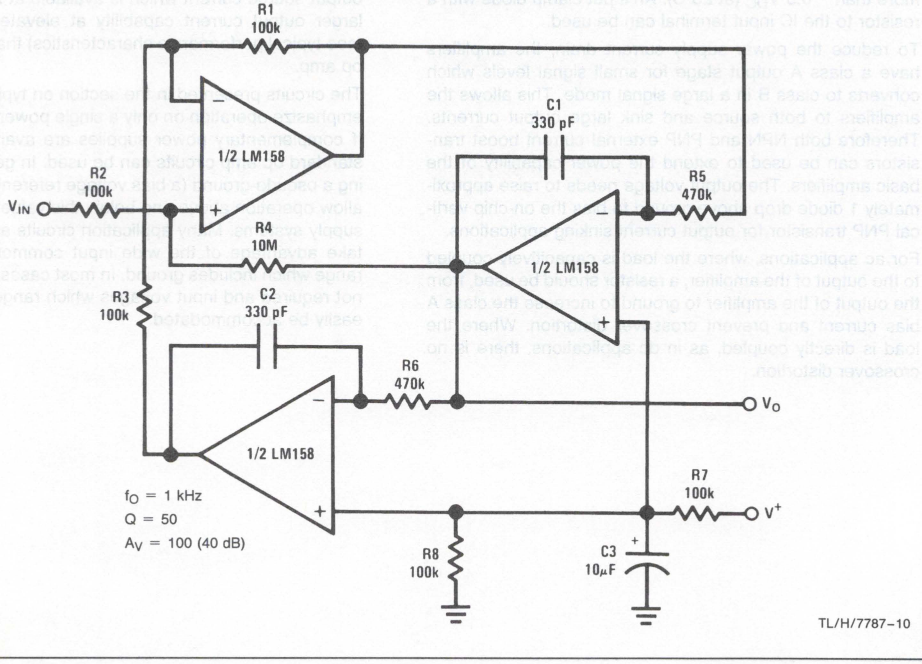
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

## Power Amplifier


R1
910k
R2
100k
V+
1/2 LM158
R3
91k
+VIN
+
−
VO
RL
VO = 0 VDC for VIN = 0 VDC
AV = 10

TL/H/7787-9

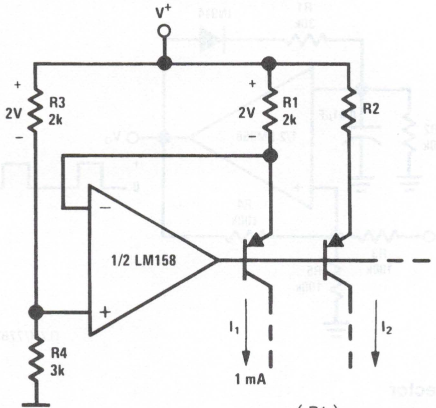
## "BI-QUAD" RC Active Bandpass Filter


R1
100k
1/2 LM158
−
+
R2
100k
VIN
R4
10M
R3
100k
C2
330 pF
C1
330 pF
R5
470k
1/2 LM158
−
+
R6
470k
VO
1/2 LM158
−
+
fO = 1 kHz
Q = 50
AV = 100 (40 dB)
R7
100k
V+
R8
100k
C3
10μF
+

TL/H/7787-10

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

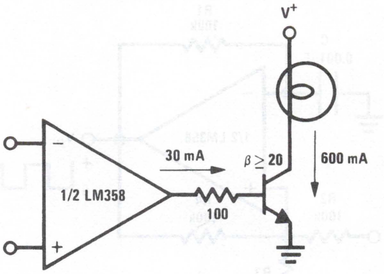
### Fixed Current Sources


V+
+
2V
−
R3
2k
+
2V
−
R1
2k
R2
1/2 LM158
−
+
R4
3k
I1
1 mA
I2

$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

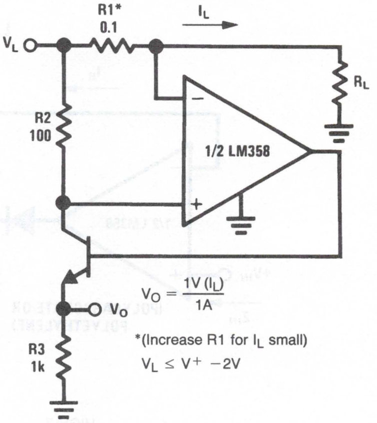
TL/H/7787–11

### Lamp Driver


V+
−
+
1/2 LM358
30 mA
100
β ≥ 20
600 mA

TL/H/7787–12

### Current Monitor


R1*
0.1
IL
VL
R2
100
RL
−
+
1/2 LM358
Vo
R3
1k

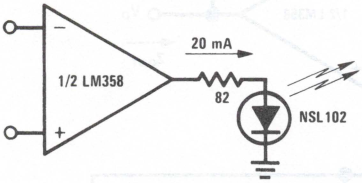
$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for $I_L$ small)

$V_L \le V^+ - 2V$

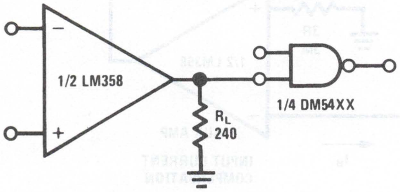
TL/H/7787–14

### LED Driver


−
+
1/2 LM358
20 mA
82
NSL102

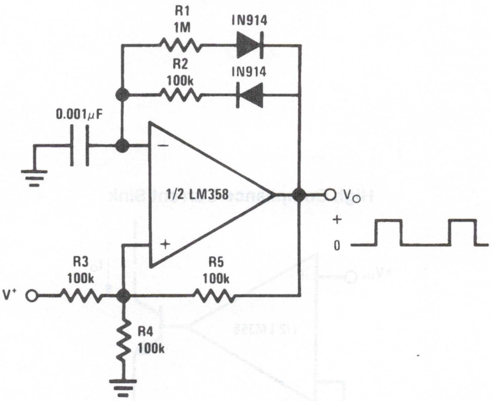
TL/H/7787–13

### Driving TTL


−
+
1/2 LM358
RL
240
1/4 DM54XX

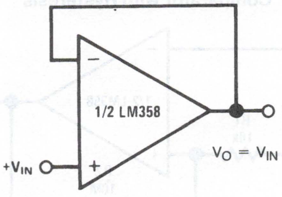
TL/H/7787–15

### Pulse Generator


R1
1M
IN914
R2
100k
IN914
0.001μF
−
+
1/2 LM358
VO
+
0
R3
100k
R5
100k
V+
R4
100k

TL/H/7787–16

### Voltage Follower

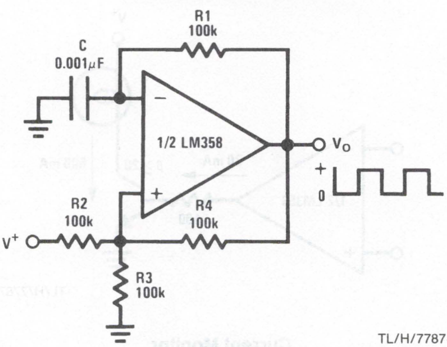

−
+
1/2 LM358
VO
+VIN

$V_O = V_{IN}$

TL/H/7787–17

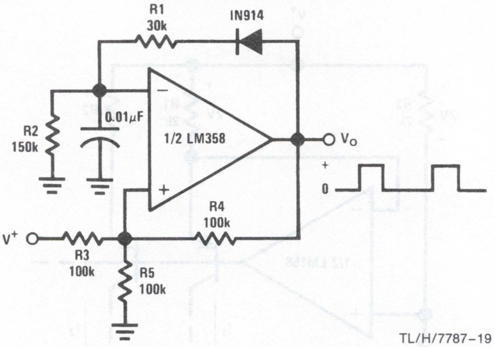
## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### Squarewave Oscillator


R1
100k
C
0.001μF
1/2 LM358
$V_O$
+
0
R2
100k
R4
100k
$V^+$
R3
100k

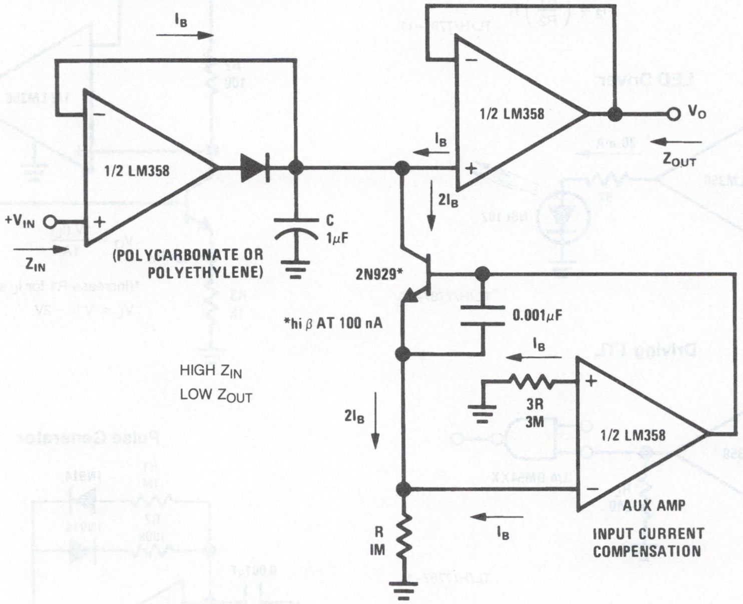
TL/H/7787-18

### Pulse Generator


R1
30k
IN914
R2
150k
0.01μF
1/2 LM358
$V_O$
+
0
R4
100k
$V^+$
R3
100k
R5
100k

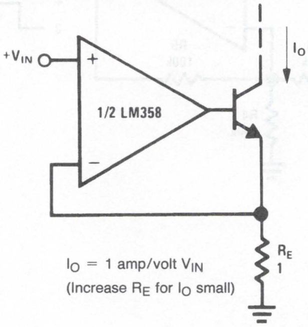
TL/H/7787-19

### Low Drift Peak Detector


$I_B$
1/2 LM358
$+V_{IN}$
$Z_{IN}$
C
1μF
(POLYCARBONATE OR POLYETHYLENE)
1/2 LM358
$V_O$
$Z_{OUT}$
$I_B$
$2I_B$
2N929*
*hi β AT 100 nA
0.001μF
$I_B$
3R
3M
1/2 LM358
HIGH $Z_{IN}$
LOW $Z_{OUT}$
$2I_B$
R
IM
$I_B$
AUX AMP
INPUT CURRENT COMPENSATION

TL/H/7787-20

### High Compliance Current Sink

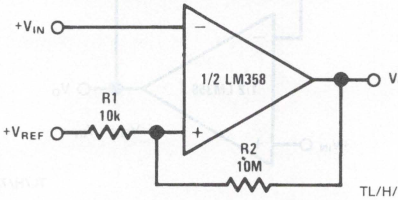

$+V_{IN}$
1/2 LM358
$I_O$
$R_E$
1

$I_O = 1$ amp/volt $V_{IN}$

(Increase $R_E$ for $I_O$ small)

TL/H/7787-21

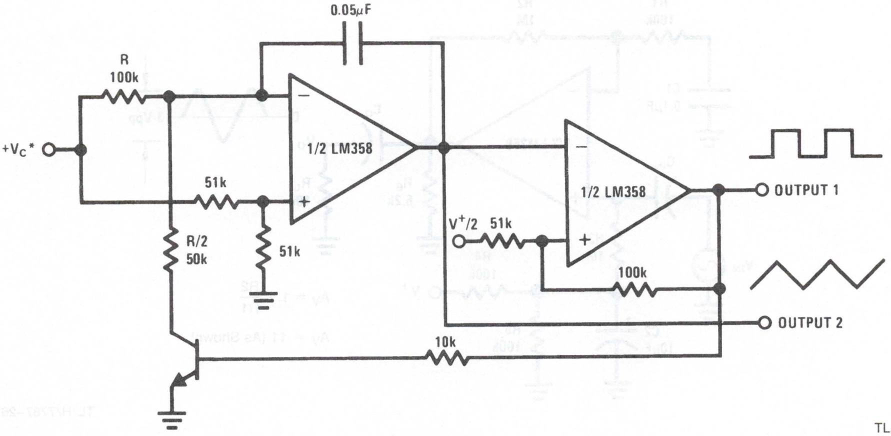
### Comparator with Hysteresis


$+V_{IN}$
1/2 LM358
$V_O$
R1
10k
$+V_{REF}$
R2
10M

TL/H/7787-22

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

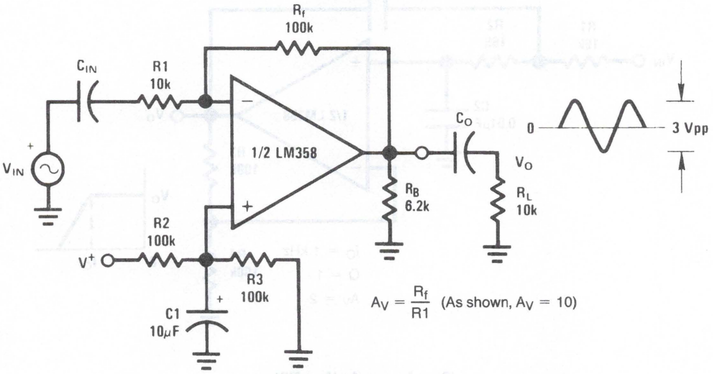
### Voltage Controlled Oscillator (VCO)


0.05μF
R
100k
+V_C*
1/2 LM358
51k
R/2
50k
51k
V+/2
51k
1/2 LM358
100k
OUTPUT 1
OUTPUT 2
10k

TL/H/7787-23

*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

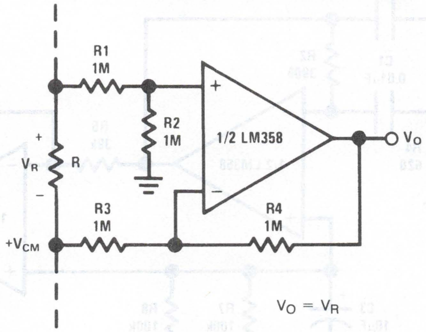
### AC Coupled Inverting Amplifier


R_f
100k
C_IN
R1
10k
V_IN
1/2 LM358
C_O
0
3 Vpp
V_O
R_B
6.2k
R_L
10k
R2
100k
V+
R3
100k
C1
10μF

$$A_V = \frac{R_f}{R1}$$ (As shown, $A_V = 10$)

TL/H/7787-24

### Ground Referencing a Differential Input Signal

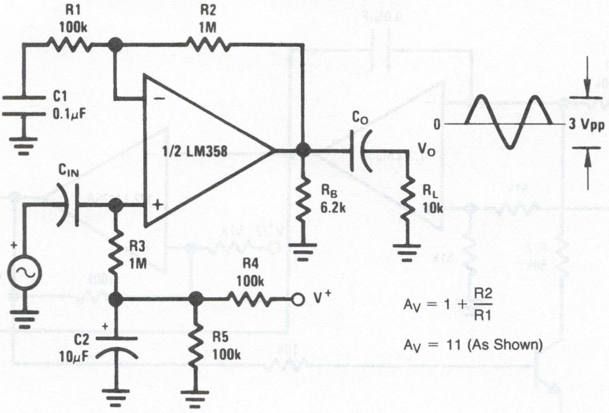

R1
1M
R2
1M
1/2 LM358
V_O
V_R
R
R3
1M
R4
1M
+V_CM

$V_O = V_R$

TL/H/7787-25

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### AC Coupled Non-Inverting Amplifier

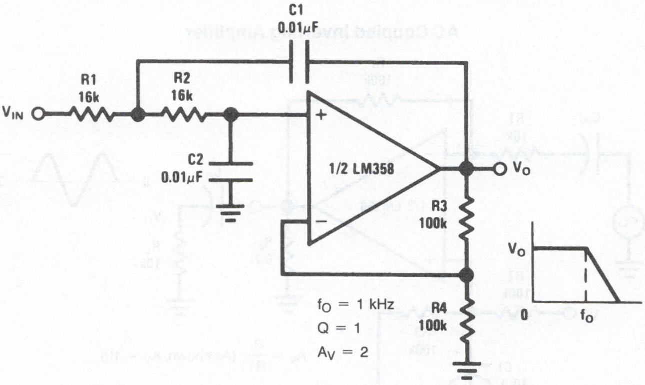

R1
100k
R2
1M
C1
0.1μF
1/2 LM358
$C_{IN}$
$V_{IN}$
R3
1M
R4
100k
$V^+$
C2
10μF
R5
100k
$C_O$
$V_O$
$R_B$
6.2k
$R_L$
10k
0
3 Vpp

$A_V = 1 + \frac{R2}{R1}$

$A_V = 11$ (As Shown)

TL/H/7787–26

### DC Coupled Low-Pass RC Active Filter


C1
0.01μF
R1
16k
R2
16k
$V_{IN}$
C2
0.01μF
1/2 LM358
$V_O$
R3
100k
R4
100k
$V_O$
0
$f_O$

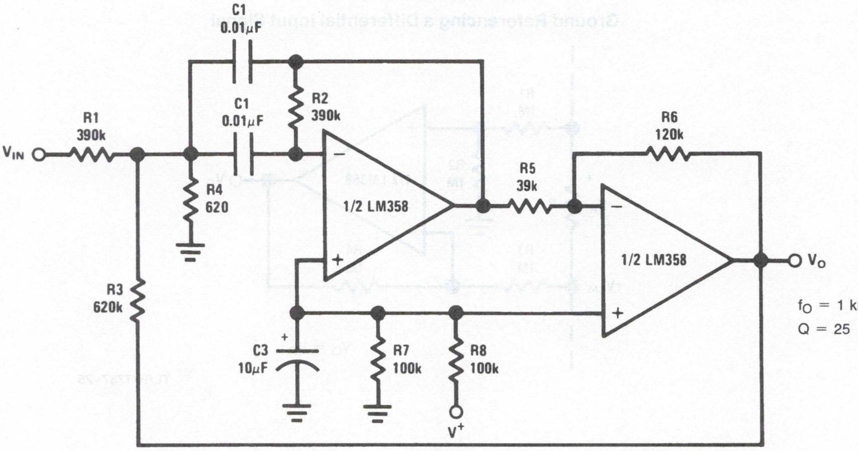
$f_O = 1$ kHz

$Q = 1$

$A_V = 2$

TL/H/7787–27

### Bandpass Active Filter


C1
0.01μF
R2
390k
C1
0.01μF
R1
390k
$V_{IN}$
R4
620
R3
620k
1/2 LM358
R5
39k
R6
120k
1/2 LM358
$V_O$
C3
10μF
R7
100k
R8
100k
$V^+$

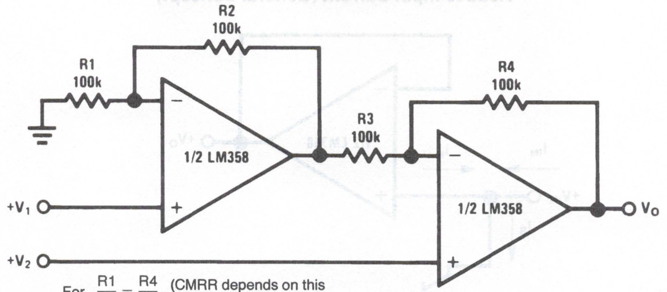
$f_O = 1$ kHz

$Q = 25$

TL/H/7787–28

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### High Input Z, DC Differential Amplifier


R2
100k
R1
100k
R4
100k
R3
100k
1/2 LM358
1/2 LM358
+V₁
+V₂
V₀
−
+
−
+

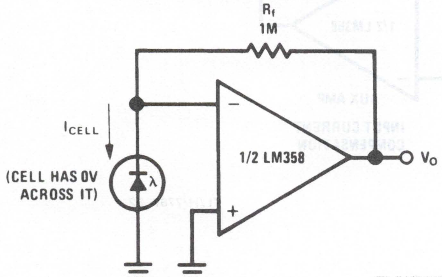
TL/H/7787-29

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

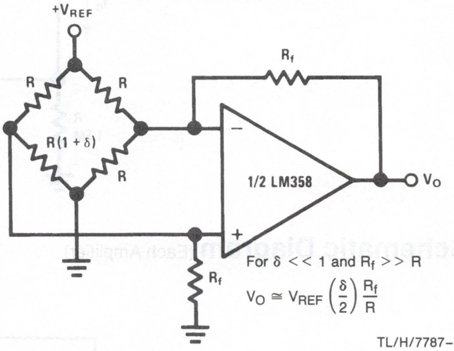
As Shown: $V_O = 2(V_2 - V_1)$

### Photo Voltaic-Cell Amplifier


Rf
1M
ICELL
(CELL HAS 0V
ACROSS IT)
λ
1/2 LM358
V₀
−
+

TL/H/7787-30

### Bridge Current Amplifier

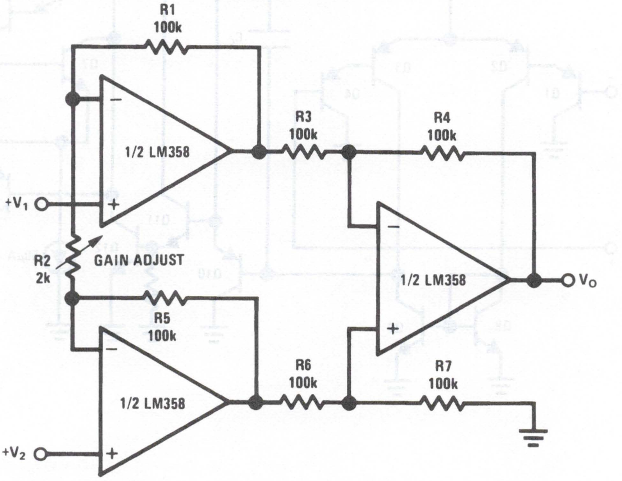

+VREF
R
R
R(1 + δ)
R
Rf
Rf
1/2 LM358
V₀
−
+

For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/7787-33

### High Input Z Adjustable-Gain DC Instrumentation Amplifier


R1
100k
1/2 LM358
+V₁
R2
2k
GAIN ADJUST
R5
100k
1/2 LM358
+V₂
R3
100k
R4
100k
1/2 LM358
V₀
R6
100k
R7
100k
−
+
−
+
−
+

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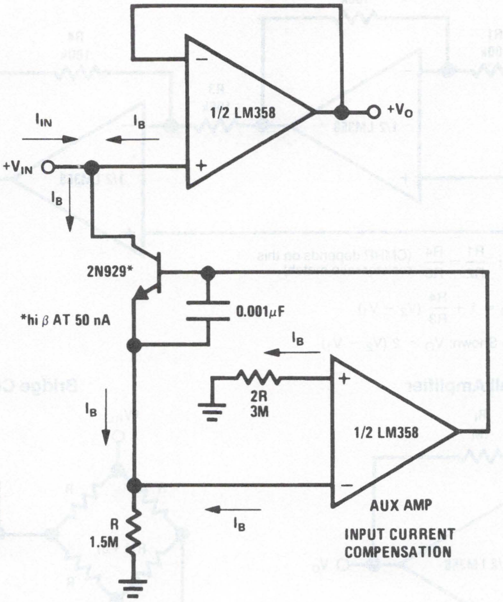
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

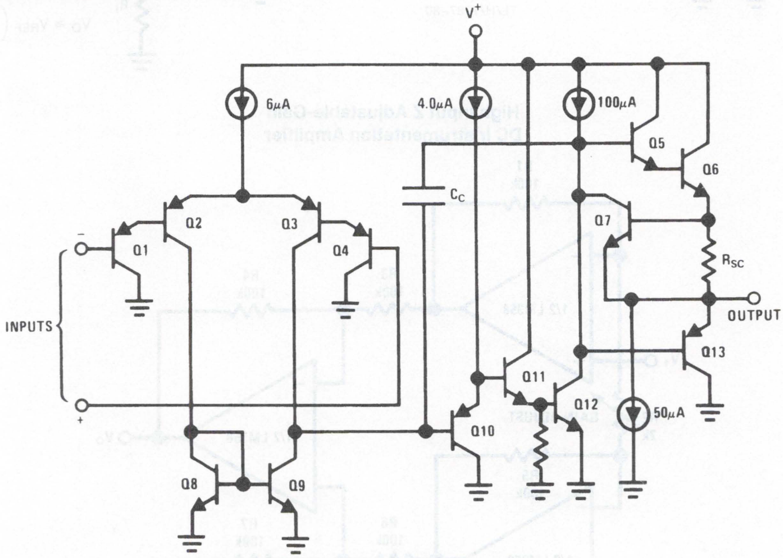
## Typical Single-Supply Applications (V+ = 5.0 $V_{DC}$) (Continued)

### Using Symmetrical Amplifiers to Reduce Input Current (General Concept)


1/2 LM358
+V_O
I_IN
I_B
+V_IN
I_B
2N929*
*hi β AT 50 nA
0.001μF
I_B
2R
3M
I_B
1/2 LM358
R
1.5M
I_B
AUX AMP
INPUT CURRENT
COMPENSATION

TL/H/7787–32

## Schematic Diagram (Each Amplifier)


V+
6μA
4.0μA
100μA
Q5
Q6
C_C
Q7
Q2
Q3
Q1
Q4
R_SC
OUTPUT
INPUTS
−
+
Q13
Q11
Q12
50μA
Q10
Q8
Q9

TL/H/7787–3

**National Semiconductor Corporation**

# LM192/LM392, LM2924 Low Power Operational Amplifier/Voltage Comparator

## General Description

The LM192 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 $V_{DC}$ power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM192 extremely useful in the design of portable equipment.

## Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM158 dual op amp and the LM193 dual comparator

## Features

- Wide power supply voltage range
  - Single supply 3V to 32V
  - Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 µA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

### ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to $V^+ - 1.5V$

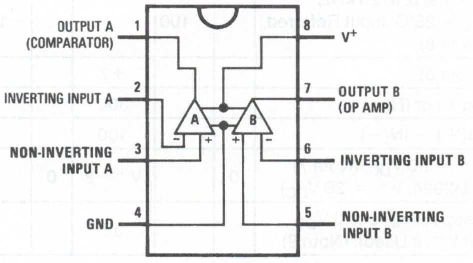
### ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

## Connection Diagram (Top View)

**(Amplifier A = Comparator)**
**(Amplifier B = Operational Amplifier)**

**Dual-In-Line Package**



TL/H/7793–1

**Order Number LM192J or LM2924J**
**See NS Package Number J08A**
**Order Number LM392M**
**See NS Package Number M08A**
**Order Number LM392N or LM2924N**
**See NS Package Number N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | LM192/LM392 | LM2924 |
|---|---|---|
| Supply Voltage, V+ | 32V or ±16V | 26V or ±13V |
| Differential Input Voltage | 32V | 26V |
| Input Voltage | −0.3V to +32V | −0.3V to +26V |
| Power Dissipation (Note 1) | | |
| Molded DIP (LM392N, LM2924N) | 820 mW | 820 mW |
| Metal Can (LM192H/LM392H) | 680 mW | |
| Small Outline Package | 530 mW | 530 mW |
| Output Short-Circuit to Ground (Note 2) | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3) | 50 mA | 50 mA |
| Operating Temperature Range | | |
| LM392 | 0°C to +70°C | −40°C to +85°C |
| LM192 | −55°C to +125°C | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |
| ESD rating to be determined. | | |
| Soldering Information | | |
| Dual-in-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

| Parameter | Conditions | LM192 | | | LM392 | | | LM2924 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$, (Note 5) | | ±2 | ±5 | | ±2 | ±5 | | ±2 | ±7 | mV |
| Input Bias Current | IN(+) or IN(−), $T_A = 25°C$, (Note 6), $V_{CM} = 0V$ | | 50 | 150 | | 50 | 250 | | 50 | 250 | nA |
| Input Offset Current | IN(+) − IN(−), $T_A = 25°C$ | | ±3 | ±25 | | ±5 | ±50 | | ±5 | ±50 | nA |
| Input Common-Mode Voltage Range | $V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Supply Current | $R_L = \infty$, $V^+ = 30V$, (LM2924, $V^+ = 26V$) | | 1 | 2 | | 1 | 2 | | 1 | 2 | mA |
| Supply Current | $R_L = \infty$, $V^+ = 5V$ | | 0.5 | 1 | | 0.5 | 1 | | 0.5 | 1 | mA |
| Amplifier-to-Amplifier Coupling | f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8) | | −100 | | | −100 | | | −100 | | dB |
| Input Offset Voltage | (Note 5) | | | ±7 | | | ±7 | | | ±10 | mV |
| Input Bias Current | IN(+) or IN(−) | | | 300 | | | 400 | | | 500 | nA |
| Input Offset Current | IN(+) − IN(−) | | | 100 | | | 150 | | | 200 | nA |
| Input Common-Mode Voltage Range | $V^+ = 30\ V_{DC}$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$) | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | V |
| Differential Input Voltage | Keep All $V_{IN}$'s $\geq 0\ V_{DC}$ (or $V^-$, if Used), (Note 9) | | | 32 | | | 32 | | | 26 | V |
| **OP AMP ONLY** | | | | | | | | | | | |
| Large Signal Voltage Gain | $V^+ = 15\ V_{DC}$, $V_o$ swing = $1\ V_{DC}$ to $11\ V_{DC}$, $R_L = 2\ k\Omega$, $T_A = 25°C$ | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |

## Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4) (Continued)

| Parameter | Conditions | LM192 | | | LM392 | | | LM2924 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **OP AMP ONLY** | | | | | | | | | | | |
| Output Voltage Swing | $R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Common-Mode Rejection Ratio | DC, $T_A = 25°C$, $V_{CM} =$ 0 $V_{DC}$ to $V^+ - 1.5\ V_{DC}$ | 70 | 85 | | 65 | 70 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | DC, $T_A = 25°C$ | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |
| Output Current Source | $V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ 2 $V_{DC}$, $T_A = 25°C$ | 20 | 40 | | 20 | 40 | | 20 | 40 | | mA |
| Output Current Sink | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ 2 $V_{DC}$, $T_A = 25°C$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o =$ 200 mV, $T_A = 25°C$ | 12 | 50 | | 12 | 50 | | 12 | 50 | | μA |
| Input Offset Voltage Drift | $R_S = 0\Omega$ | | 7 | | | 7 | | | 7 | | μV/°C |
| Input Offset Current Drift | $R_S = 0\Omega$ | | 10 | | | 10 | | | 10 | | $pA_{DC}$/°C |
| **COMPARATOR ONLY** | | | | | | | | | | | |
| Voltage Gain | $R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$ | 50 | 200 | | 50 | 200 | | 25 | 100 | | V/mV |
| Large Signal Response Time | $V_{IN}$ = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$ | | 300 | | | 300 | | | 300 | | ns |
| Response Time | $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 10) | | 1.3 | | | 1.3 | | | 1.5 | | μs |
| Output Sink Current | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V_o \geq 1.5\ V_{DC}$, $T_A = 25°C$ | 6 | 16 | | 6 | 16 | | 6 | 16 | | mA |
| Saturation Voltage | $V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$ | | 250 | 400 | | 250 | 400 | | | 400 | mV |
| | $V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$ | | | 700 | | | 700 | | | 700 | mV |
| Output Leakage Current | $V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 5\ V_{DC}$, $T_A = 25°C$ | | 0.1 | | | 0.1 | | | 0.1 | | nA |
| | $V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 30\ V_{DC}$ | | | 1.0 | | | 1.0 | | | 1.0 | μA |

**Note 1:** For operating at temperatures above 25°C, the LM392N and the LM2924N must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The LM192H/LM392H must be derated based on a 150°C maximum junction temperature and a thermal resistance of 184°C/W. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of $V^+$. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

**Note 4:** These specifications apply for $V^+ = 5V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. For the LM392, temperature specifications are limited to $0°C \leq T_A \leq +70°C$ and the LM2924 temperature specifications are limited to $-40°C \leq T_A \leq +85°C$.

**Note 5:** At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with $V^+$ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).

**Note 6:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

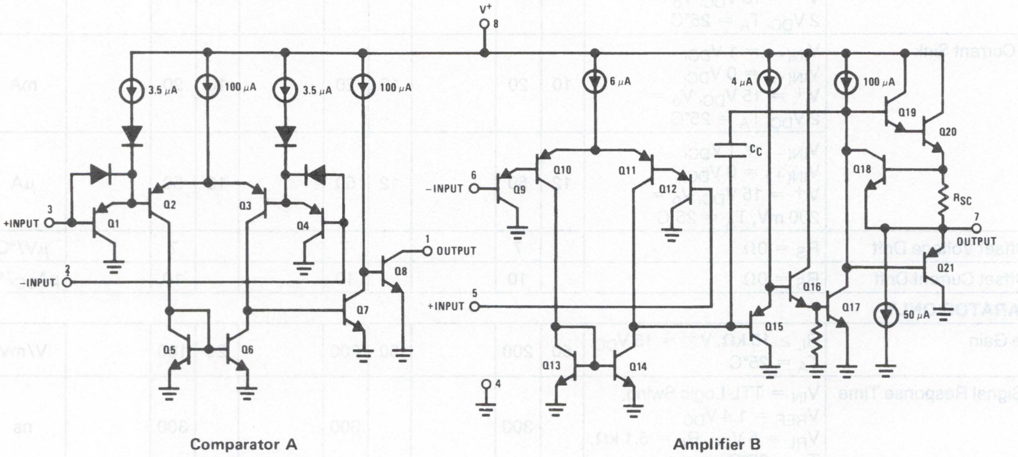
**Note 7:** The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

**Note 8:** Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

**Note 9:** Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

**Note 10:** The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

## Schematic Diagram



TL/H/7793-2

## Application Hints

Please refer to the application hints section of the LM193 and the LM158 datasheets.

**National Semiconductor Corporation**

# LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

## General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

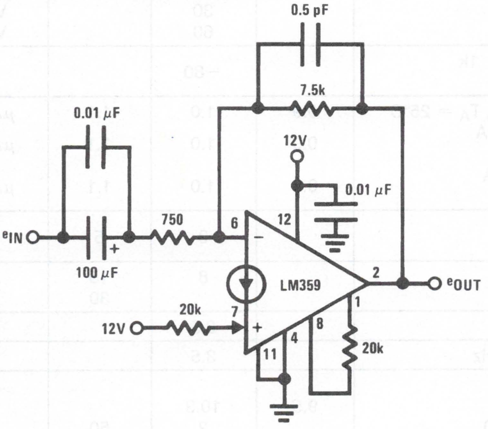
## Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

## Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product ($I_{SET} = 0.5$ mA)
  400 MHz for $A_V = 10$ to 100
  30 MHz for $A_V = 1$
- High slew rate ($I_{SET} = 0.5$ mA)
  60 V/µs for $A_V = 10$ to 100
  30 V/µs for $A_V = 1$
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to $V_{CC} - 2V$
- Low spot noise, 6 nV/$\sqrt{Hz}$, for f > 1 kHz

## Typical Application

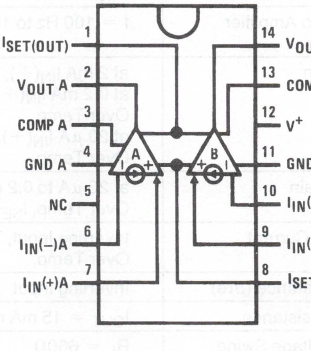


TL/H/7788–1

- $A_V$ = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

## Connection Diagram

**Dual-In-Line Package**



TL/H/7788–2

**Top View**

**Order Number LM359J, LM359M or LM359N**
**See NS Package Number J14A, M14A or N14A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 22 $V_{DC}$<br>or ±11 $V_{DC}$ |
| Power Dissipation (Note 1) | |
| J Package | 1W |
| N Package | 750 mW |
| Maximum $T_J$ | |
| J Package | +150°C |
| N Package | +125°C |

Thermal Resistance

J Package

$\theta_{jA}$ 147°C/W still air

110°C/W with 400 linear feet/min air flow

N Package

$\theta_{jA}$ 100°C/W still air

75°C/W with 400 linear feet/min air flow

| | |
|---|---|
| Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$ | 10 $mA_{DC}$ |
| Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$ | 2 $mA_{DC}$ |
| Operating Temperature Range | |
| LM359 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25°C$ unless otherwise noted

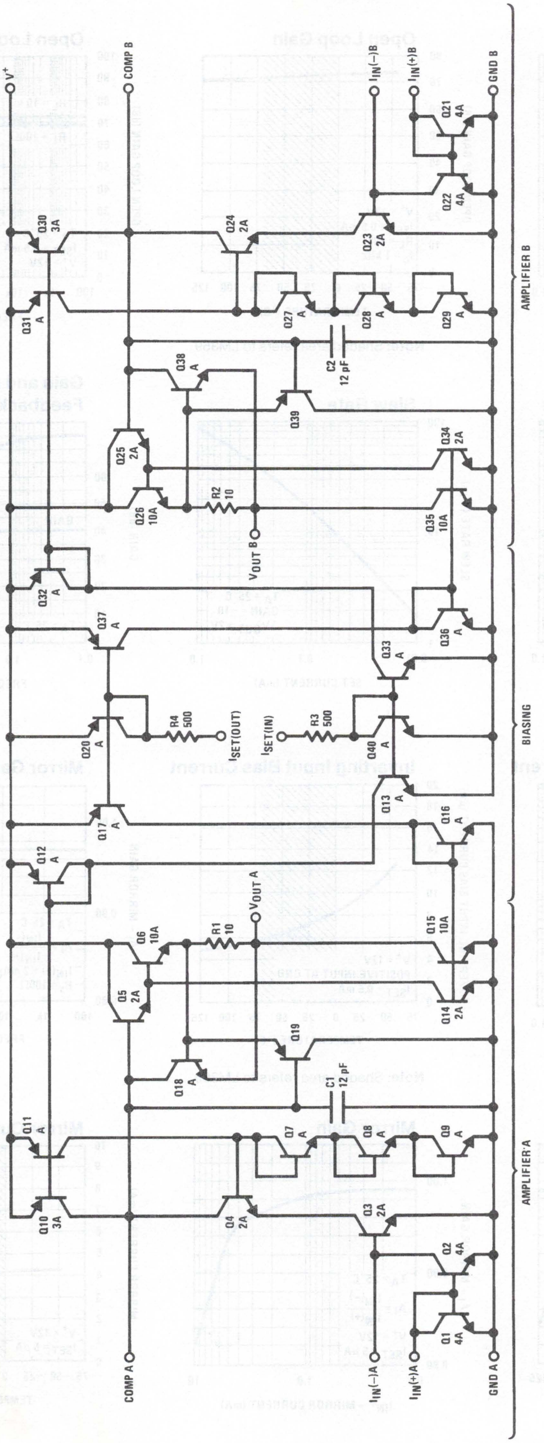
| Parameter | Conditions | LM359 | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Open Loop Voltage Gain | $V_{supply} = 12V$, $R_L = 1k$, f = 100 Hz<br>$T_A = 125°C$ | 62 | 72<br>68 | | dB<br>dB |
| Bandwidth<br>Unity Gain | $R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF | 15 | 30 | | MHz |
| Gain Bandwidth Product<br>Gain of 10 to 100 | $R_{IN} = 50\Omega$ to $200\Omega$ | 200 | 400 | | MHz |
| Slew Rate<br>Unity Gain<br>Gain of 10 to 100 | <br>$R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF<br>$R_{IN} < 200\Omega$ | | <br>30<br>60 | | <br>V/μs<br>V/μs |
| Amplifier to Amplifier Coupling | f = 100 Hz to 100 kHz, $R_L = 1k$ | | −80 | | dB |
| Mirror Gain (Note 2) | at 2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$, $T_A = 25°C$<br>at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp.<br>at 20 μA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp. | 0.9<br>0.9<br>0.9 | 1.0<br>1.0<br>1.0 | 1.1<br>1.1<br>1.1 | μA/μA<br>μA/μA<br>μA/μA |
| ΔMirror Gain (Note 2) | at 20 μA to 0.2 mA $I_{IN}(+)$<br>Over Temp, $I_{SET} = 5\ \mu A$ | | 3 | 5 | % |
| Input Bias Current | Inverting Input, $T_A = 25°C$<br>Over Temp. | | 8 | 15<br>30 | μA<br>μA |
| Input Resistance (βre) | Inverting Input | | 2.5 | | kΩ |
| Output Resistance | $I_{OUT} = 15$ mA rms, f = 1 MHz | | 3.5 | | Ω |
| Output Voltage Swing<br>$V_{OUT}$ High<br>$V_{OUT}$ Low | $R_L = 600\Omega$<br>$I_{IN}(-)$ and $I_{IN}(+)$ Grounded<br>$I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$ | <br>9.5 | <br>10.3<br>2 | <br><br>50 | <br>V<br>mV |
| Output Currents<br>Source<br>Sink (Linear Region)<br>Sink (Overdriven) | <br>$I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100\Omega$<br>$V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$<br>$I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$, $V_{OUT}$ Force = 1V | <br>16<br><br>1.5 | <br>40<br>4.7<br>3 | | <br>mA<br>mA<br>mA |
| Supply Current | Non-Inverting Input Grounded, $R_L = \infty$ | | 18.5 | 22 | mA |
| Power Supply Rejection (Note 3) | f = 120 Hz, $I_{IN}(+)$ Grounded | 40 | 50 | | dB |

**Note 1:** See Maximum Power Dissipation graph.

**Note 2:** Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in $A_I$ for two different mirror currents at any given temperature.

**Note 3:** See Supply Rejection graphs.

## Schematic Diagram


V+
COMP B
COMP A
IIN(−)B
IIN(+)B
GND B
IIN(−)A
IIN(+)A
GND A
VOUT B
VOUT A
ISET(OUT)
ISET(IN)
AMPLIFIER B
BIASING
AMPLIFIER A
Q1 4A
Q2 4A
Q3 2A
Q4 2A
Q5 2A
Q6 10A
Q7 A
Q8 A
Q9 A
Q10 3A
Q11 A
Q12 A
Q13 A
Q14 2A
Q15 10A
Q16 A
Q17 A
Q18 A
Q19
Q20 A
Q21 4A
Q22 4A
Q23 2A
Q24 2A
Q25 2A
Q26 10A
Q27 A
Q28 A
Q29 A
Q30 3A
Q31 A
Q32 A
Q33 A
Q34 2A
Q35 10A
Q36 A
Q37 A
Q38 A
Q39
Q40 A
R1 10
R2 10
R3 500
R4 500
C1 12 pF
C2 12 pF

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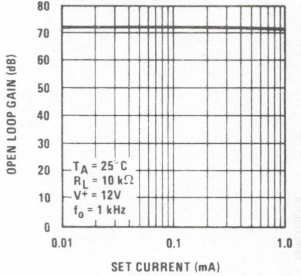
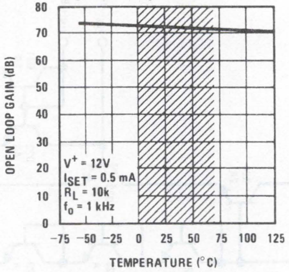
## Typical Performance Characteristics

### Open Loop Gain

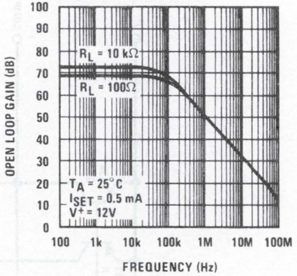


### Open Loop Gain

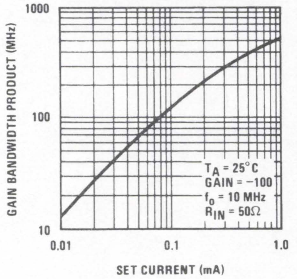


**Note:** Shaded area refers to LM359

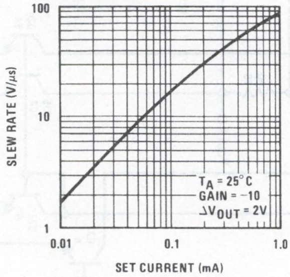
### Open Loop Gain



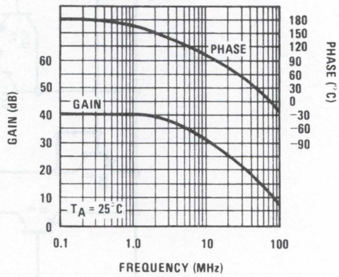
### Gain Bandwidth Product



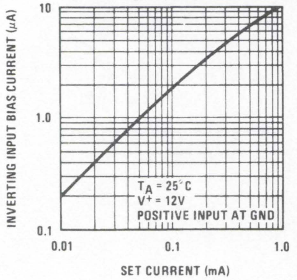
### Slew Rate



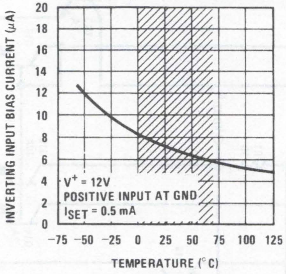
### Gain and Phase Feedback Gain = −100



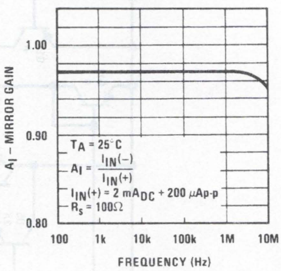
### Inverting Input Bias Current



### Inverting Input Bias Current

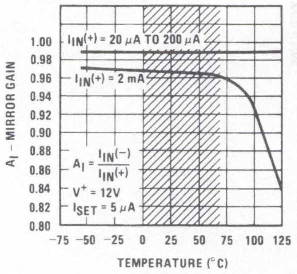


### Mirror Gain

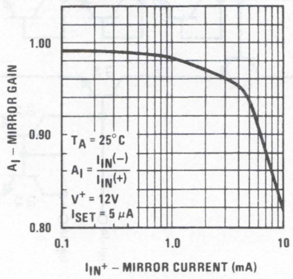


**Note:** Shaded area refers to LM359

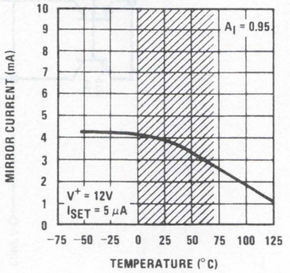
### Mirror Gain



### Mirror Gain



### Mirror Current



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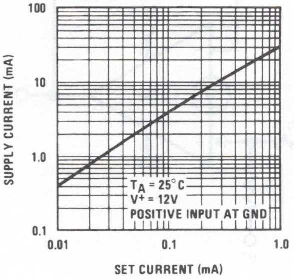
**Note:** Shaded area refers to LM359

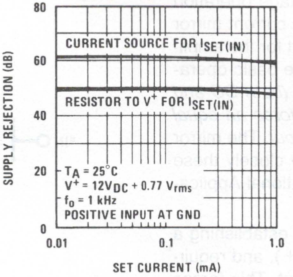
**Note:** Shaded area refers to LM359

## Typical Performance Characteristics (Continued)

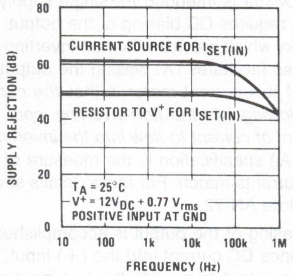
**Supply Current**



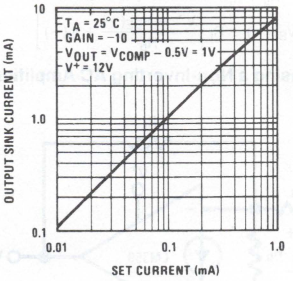
**Supply Rejection**



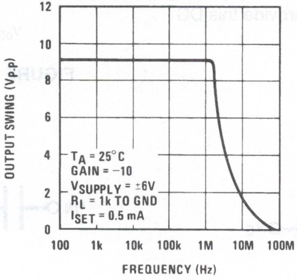
**Supply Rejection**



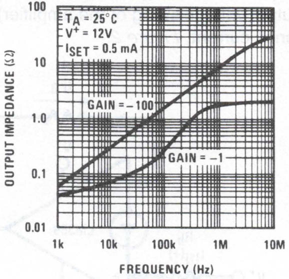
**Output Sink Current**



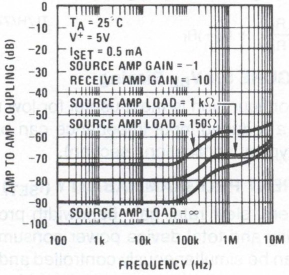
**Output Swing**



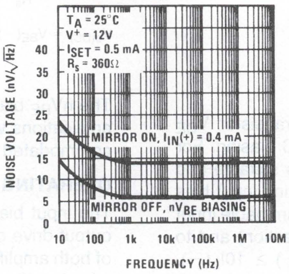
**Output Impedance**



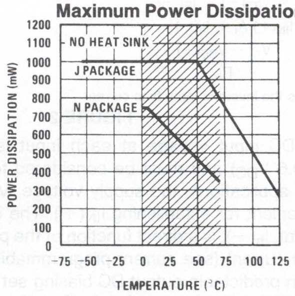
**Amplifier to Amplifier Coupling (Input Referred)**



**Noise Voltage**



**Maximum Power Dissipation**



**Note:** Shaded area refers to LM359J/LM359N

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## Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

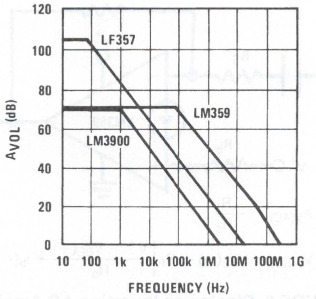

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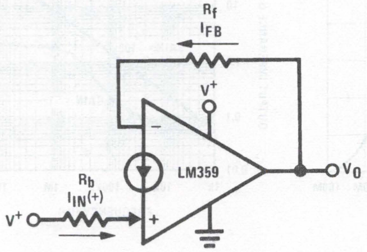
**FIGURE 1**

## Application Hints (Continued)

### DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and DC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input.* The mirror gain ($A_I$) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2*.



$$V_{o(DC)} = V_{BE}(-) + I_{FB}\,R_f$$

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$$I_{FB} = I_{IN}(+)\,A_I + I_b(-)$$

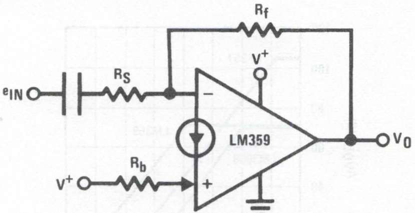
$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

$I_b(-)$ is the inverting input bias current

**FIGURE 2**

The DC input voltage at each input is a transistor $V_{BE}$ ($\cong 0.6\ V_{DC}$) and must be considered for DC biasing. For most applications, the supply voltage, $V^+$, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$.

The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

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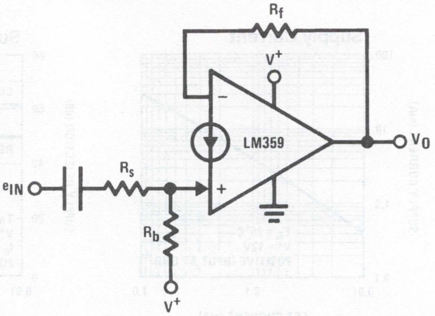
$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

**FIGURE 3. Biasing an Inverting AC Amplifier**



$$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$$

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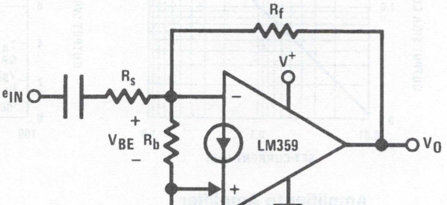
$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

**FIGURE 4. Biasing a Non-Inverting AC Amplifier**



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$$

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**FIGURE 5. nV$_{BE}$ Biasing**

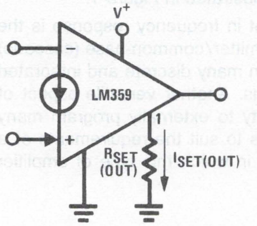
The nV$_{BE}$ biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

### OPERATING CURRENT PROGRAMMABILITY ($I_{SET}$)

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

### $I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6*, this current is equal to:



$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

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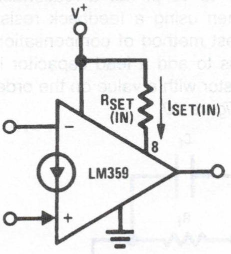
**FIGURE 6. Establishing the Output Set Current**

## Application Hints (Continued)

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to $V^+$. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$.* This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

### $I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to $V^+$ sets this current to be:



$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

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**FIGURE 7. Establishing the Input Set Current**

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\,(10^{-6})}{C_{comp}}\ (V/\mu s)$$

$$\begin{matrix}\text{frequency of} \\ \text{dominant pole}\end{matrix} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\,(0.026V)}\ (Hz)$$

$$\text{input resistance} = \beta re \cong \frac{150\,(0.026V)}{3I_{SET(IN)}}\ (\Omega)$$

where $C_{comp}$ is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, $A_{VOL}$ is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed ($KT/q = 26$ mV and $\beta_{typ} = 150$). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

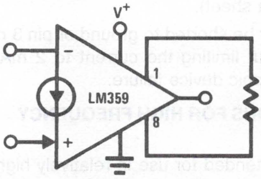
$$I_{supply} \cong 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

### PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as $I_{SET}$ and it is created by connecting a resistor from pin 1 to pin 8 *(Figure 8)*.

$$I_{SET} = \frac{V^+ - 2\,V_{BE}}{R_{SET} + 1\,k\Omega} \text{ where } V_{BE} \cong 0.6V$$



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$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

**FIGURE 8. Single Resistor Programming of $I_{SET}$**

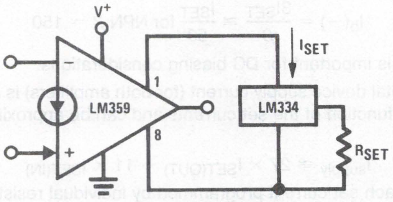
This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \cong 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

## Application Hints (Continued)

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9*.



$I_{SET} = \frac{67.7\text{ mV}}{R_{SET}}$ @25°C

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**FIGURE 9. Current Source Programming of $I_{SET}$**

This circuit allows $I_{SET}$ to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to $V^+$ without limiting the current to 2 mA or less to prevent catastrophic device failure.

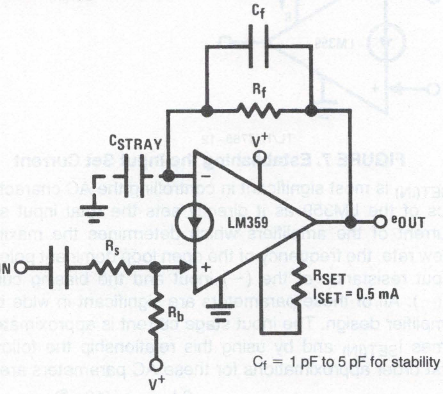
### CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2″) but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

### COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10*.



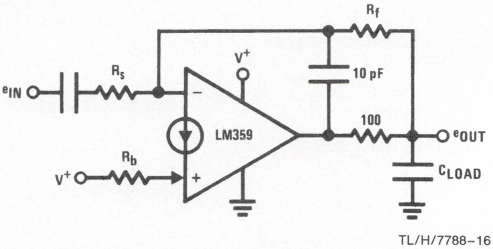
$C_f$ = 1 pF to 5 pF for stability

TL/H/7788–15

**FIGURE 10. Best Method of Compensation**

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11*. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.



TL/H/7788–16

**FIGURE 11. Isolating Large Capacitive Loads**

## Application Hints (Continued)

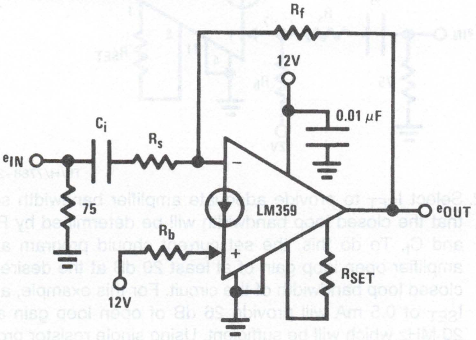
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

### AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 $V_{DC}$ and single resistor programming of the operating current, $I_{SET}$, will be used for simplicity.

### AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



TL/H/7788–17

2. Determine the required $I_{SET}$ from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\ \text{MHz} = 100\ \text{MHz}$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

Actual GBW = 10 × 40 MHz = 400 MHz

$I_{SET}$ required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\ \text{k}\Omega = \frac{10.8\text{V}}{0.5\ \text{mA}} - 1\ \text{k}\Omega = 20.6\ \text{k}\Omega$$

3. Determine maximum value for $R_f$ to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3\,I_{SET}}{\beta} = \begin{array}{c}100\ \mu\text{A minimum DC}\\ \text{feedback current}\end{array}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$\approx \frac{(V^+ - 3\,V_{BE}) - 2\ \text{mV}}{2}$$

$$V_{oDC(opt)} \cong \frac{12 - 1.8\text{V}}{2} = \frac{10.2\text{V}}{2} = 5.1\ V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE}(-)}{I_{f(MIN)}} = \frac{5.1\text{V} - 0.6\text{V}}{100\ \mu\text{A}} = 45\ \text{k}\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select $R_s$ to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega \text{ Let } R_s = 750\Omega$$

5. Select $R_f$ for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10\ R_s = 7.5\ \text{k}\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since $R_f$ = 7.5k, for the output to be biased to 5.1 $V_{DC}$, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1\text{V} - V_{BE}(-)}{R_f} = \frac{5.1\text{V} - 0.6\text{V}}{7.5\ \text{k}\Omega} = 600\ \mu\text{A}$$

Now $R_b$ can be found by:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{600\ \mu\text{A}} = 19\ \text{k}\Omega$$

7. Select $C_i$ to provide the proper gain for the 8 Hz minimum input frequency:

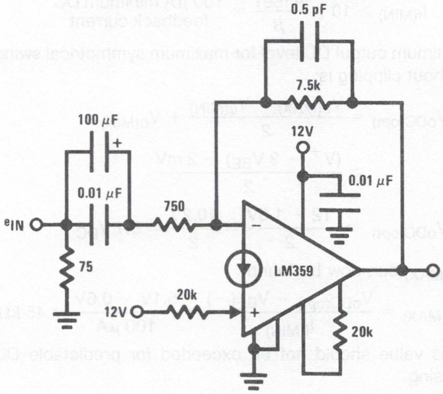
$$C_i \geq \frac{1}{2\pi\,R_s\,(f_{low})} = \frac{1}{2\pi\,(750\Omega)\,(8\ \text{Hz})} = 26\ \mu\text{F}$$

A larger value of $C_i$ will allow a flat frequency response down to 8 Hz and a 0.01 μF ceramic capacitor in parallel with $C_i$ will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

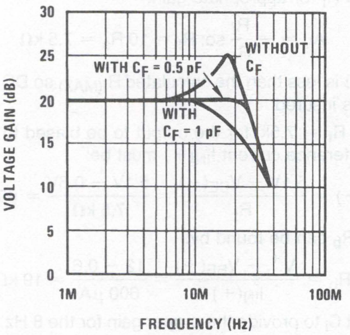
## Application Hints (Continued)

**Final Circuit Using Standard 5% Tolerance Resistor Values:**



TL/H/7788–18

**Circuit Performance:**



TL/H/7788–19

$V_{O(DC)} = 5.1V$

Differential phase error < 1° for 3.58 MHz $f_{IN}$

Differential gain error < 0.5% for 3.58 MHz $f_{IN}$

$f_{-3\ dB}$ low = 2.5 Hz

### A NON-INVERTING VIDEO AMPLIFIER

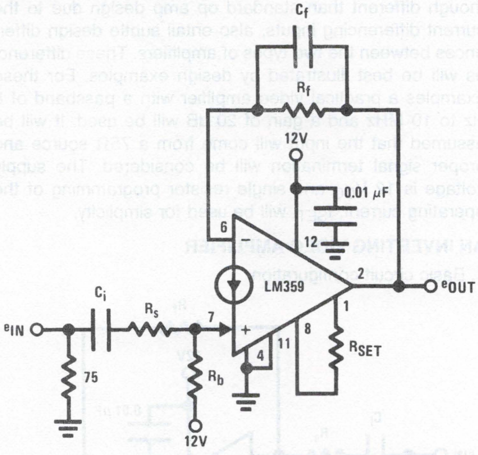
For this case several design considerations must be dealt with.

- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the $V_{BE}$ diode clamp at the (−) input.

**DESIGN EXAMPLE:**

$e_{IN}$ = 50 mV (MAX), $f_{IN}$ = 10 MHz (MAX), desired circuit BW = 20 MHz, $A_V$ = 20 dB, driving source impedance = 75Ω, $V^+$ = 12V.

1. Basic circuit configuration:



TL/H/7788–20

2. Select $I_{SET}$ to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by $R_f$ and $C_f$. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an $I_{SET}$ of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for $I_{SET}$:

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = 20.6\,k\Omega$$

3. Since the closed loop bandwidth will be determined by

$$R_f \text{ and } C_f \left( f_{-3\ dB} = \frac{1}{2\pi\, R_f\, C_f} \right)$$

## Application Hints (Continued)

to obtain a 20 MHz bandwidth, both $R_f$ and $C_f$ should be kept small. It can be assumed that $C_f$ can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of $R_f$ to be within the range of:

$$\frac{1}{2\pi\ 5\ \text{pF}\ 20\ \text{MHz}} \leq R_f \leq \frac{1}{2\pi\ 1\ \text{pF}\ 20\ \text{MHz}}$$

$$\text{or } 1.6\ \text{k}\Omega \leq R_f \leq 7.96\ \text{k}\Omega$$

Also, for a closed loop gain of +10, $R_f$ must be 10 times $R_s + r_e$ where $r_e$ is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω.
5. For $A_v = 10$; $R_f$ is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4\ V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE}(-)}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640\ \mu A = I_{IN}(+)$$

DC biasing predictability will be insured because 640 µA is greater than the minimum of $I_{SET}/5$ or 100 µA.

For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be;

$$\frac{\pm e_{in\ peak}}{R_s + r_e} = \frac{\pm 50\ \text{mV}}{750\Omega} = \pm 66\ \mu A$$

therefore the total mirror current range will be 574 µA to 706 µA which will insure gain accuracy.

8. $R_b$ can now be found:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{640\ \mu A} = 17.8\ \text{k}\Omega$$

9. Since $R_s + r_e$ will be 750Ω and $r_e$ is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\ I_{IN(+)}} = \frac{26\ \text{mV}}{640\ \mu A} \cong 40\Omega \text{ at } 25°C$$

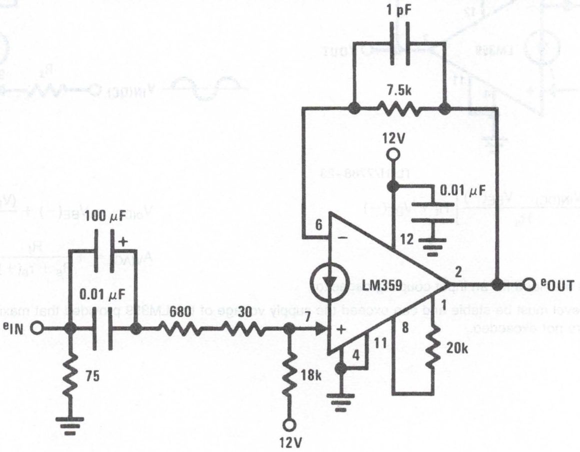
$R_s$ must be 750Ω−40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

10. As a final design step, $C_i$ must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\ (R_s + r_e)\ f_{low}} = \frac{1}{2\pi\ (750\Omega)\ (8\ \text{Hz})} = 26.5\ \mu F$$

A larger value may be used and a 0.01 µF ceramic capacitor in parallel with $C_i$ will maintain high frequency gain accuracy.

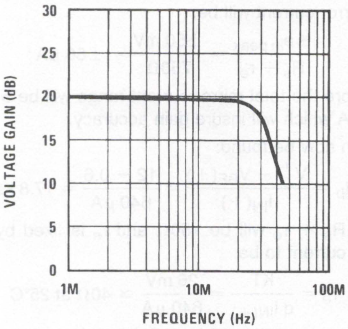
**Final Circuit Using Standard 5% Tolerance Resistor Values**



TL/H/7788–21

## Application Hints (Continued)

### Circuit Performance



TL/H/7788-22

$V_{o(DC)} = 5.4V$

Differential phase error < 0.5°

Differential gain error < 2%

$f_{-3\ dB}$ low = 2.5 Hz

**GENERAL PRECAUTIONS**

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

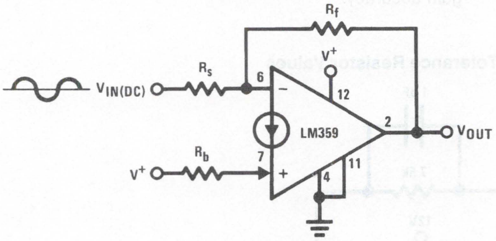
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, $I_{SET}$, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure

## Typical Applications

### DC Coupled Inputs

**Inverting**

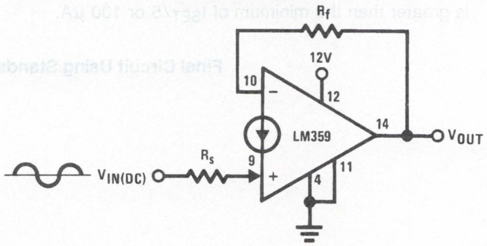


TL/H/7788-23

$$V_{o(DC)} = \left[\frac{V^+ - V_{BE}(+)}{R_b} - \frac{V_{IN(DC)} - V_{BE}(-)}{R_s}\right] R_f + V_{BE}(-)$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

**Non-Inverting**



TL/H/7788-24

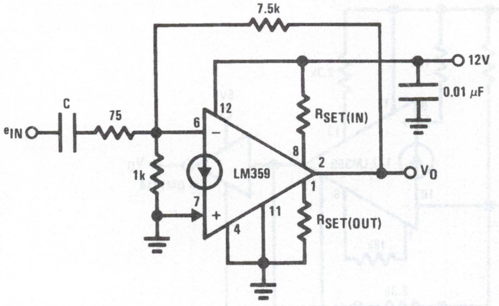
$$V_{o(DC)} = V_{BE}(-) + \frac{(V_{IN(DC)} - V_{BE}(+))\,R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_e(+)}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

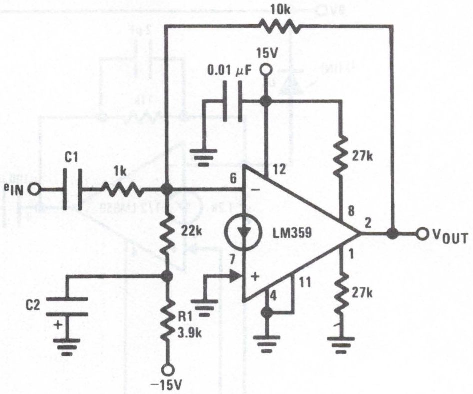
## Application Hints (Continued)

### Noise Reduction using $nV_{BE}$ Biasing


7.5k
12V
0.01 µF
C
75
$e_{IN}$
6
12
$R_{SET(IN)}$
8
2
$V_O$
1k
LM359
1
7
11
$R_{SET(OUT)}$
4

TL/H/7788-25

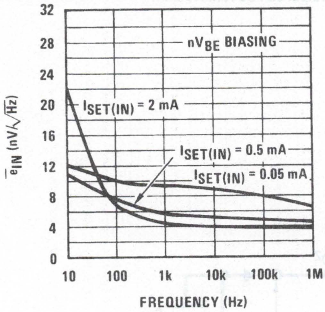
### $nV_{BE}$ Biasing with a Negative Supply


10k
15V
0.01 µF
C1
1k
$e_{IN}$
6
12
27k
22k
LM359
8
2
$V_{OUT}$
1
7
11
27k
C2
4
R1
3.9k
−15V

TL/H/7788-26

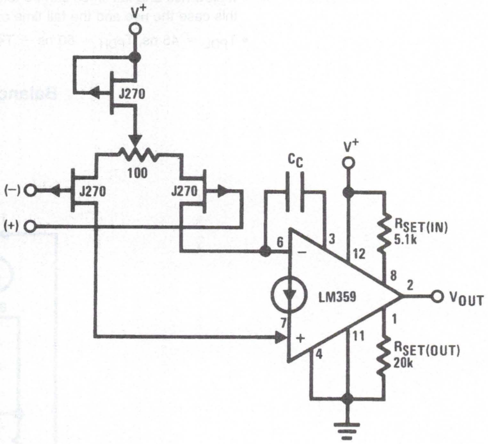
- R1 and C2 provide additional filtering of the negative biasing supply

### Typical Input Referred Noise Performance



TL/H/7788-27

### Adding a JFET Input Stage

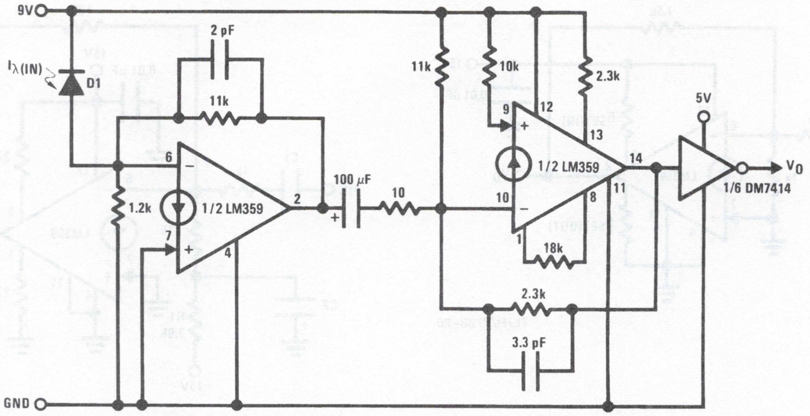

V+
J270
100
(−)
J270
J270
(+)
$C_C$
V+
6
3
12
$R_{SET(IN)}$
5.1k
8
2
LM359
$V_{OUT}$
7
1
11
4
$R_{SET(OUT)}$
20k

TL/H/7788-28

- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, $S_r = 60\ V/\mu s$; $C_C = 51$ pF
- For $A_V = +11$; BW = 24 MHz, $S_r = 130\ V/\mu s$; $C_C = 5$ pF
- For $A_V = +100$; BW = 4.5 MHz, $S_r = 150\ V/\mu s$; $C_C = 2$ pF
- $V_{OS}$ is typically <25 mV; 100Ω potentiometer allows a $V_{OS}$ adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

## Typical Applications (Continued)

**Photo Diode Amplifier**

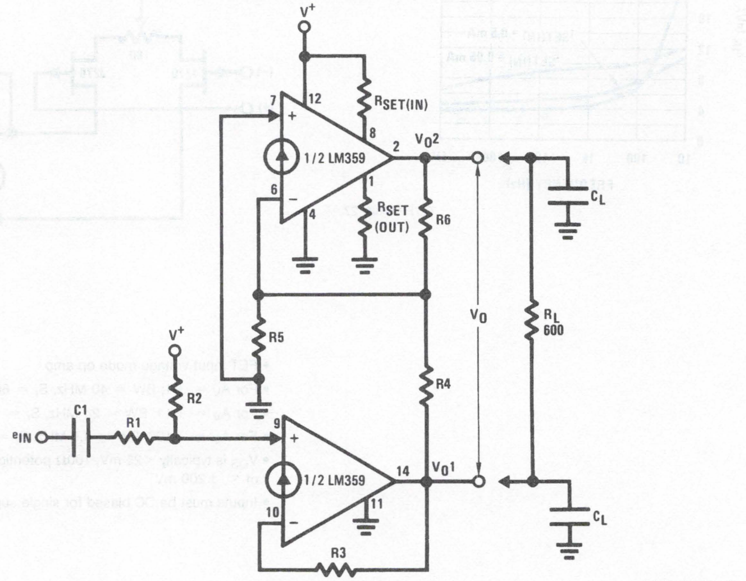

9V
$I_\lambda$(IN)
D1
2 pF
11k
6
1.2k
1/2 LM359
2
7
4
100 μF
10
11k
10k
2.3k
9
12
13
1/2 LM359
14
10
8
11
1
18k
2.3k
3.3 pF
5V
$V_O$
1/6 DM7414
GND

TL/H/7788–29

D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- $T_{PDL}$ = 45 ns, $T_{PDH}$ = 50 ns – $T^2L$ output

**Balanced Line Driver**


V+
7
12
$R_{SET(IN)}$
8
2
$V_O2$
1/2 LM359
6
1
4
$R_{SET}$ (OUT)
R6
$C_L$
R5
$V_O$
$R_L$ 600
R4
V+
R2
C1
R1
$e_{IN}$
9
1/2 LM359
14
$V_O1$
11
10
R3
$C_L$

TL/H/7788–30

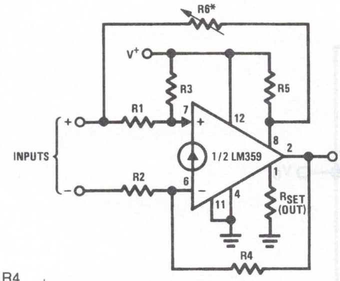
For $V_O1 = V_O2 = \frac{V^+}{2}$, $\frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive $C_L$ = 1500 pF with no additional compensation, ±0.01 μF with $C_{comp}$ = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

## Typical Applications (Continued)

### Difference Amplifier


R6*
V+
R3
R5
R1
7
12
+
INPUTS
8
2
1/2 LM359
Vo
R2
6
1
−
4
11
RSET (OUT)
R4

TL/H/7788-31

$V_{o(DC)} = \frac{R4}{R3}(V^+ - \phi)$ where $\phi = 0.6V$

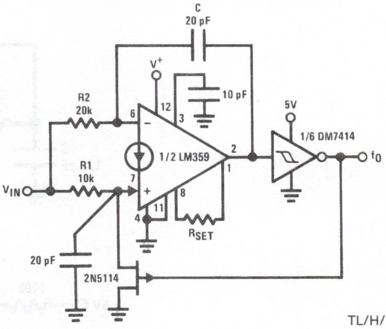
$A_V = \frac{R4}{R1}$ for $R1 = R2$

*CMRR is adjusted for max at expected CM input signal

$R6 \approx \frac{R5}{5}$, for $R5 = 100\ k\Omega$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

### Voltage Controlled Oscillator


C
20 pF
V+
10 pF
5V
R2
20k
6
12
3
1/6 DM7414
fo
−
2
1/2 LM359
R1
10k
1
VIN
7
+
8
4
11
RSET
20 pF
2N5114

TL/H/7788-32

$f_o = \frac{V_{IN} - \phi}{4\ C \Delta V\ R1}$

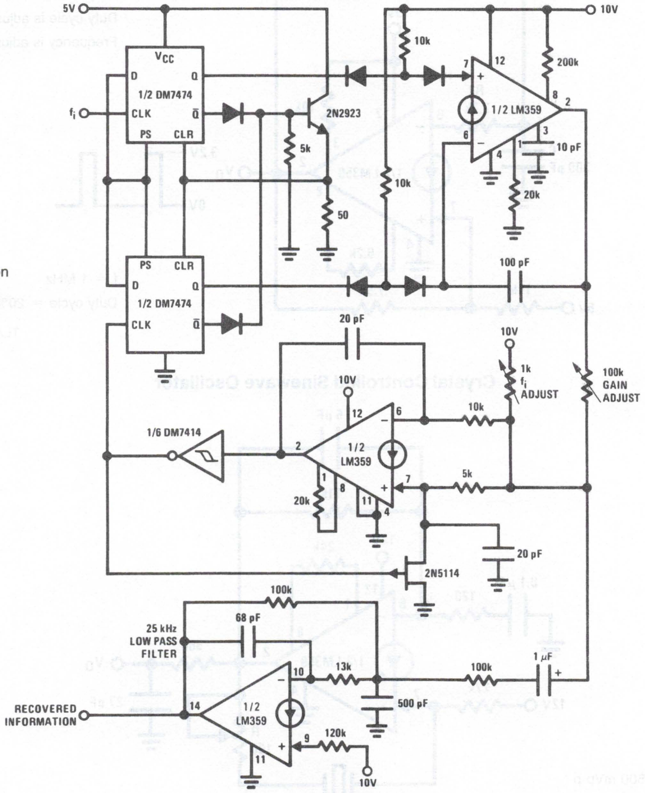
where: $R2 = 2R1$

$\phi$ = amplifier input voltage = 0.6V

$\Delta V$ = DM7414 hysteresis, typ 1V

- 5 MHz operation
- $T^2L$ output

### Phase Locked Loop


5V
10V
VCC
10k
200k
D
Q
7
12
1/2 DM7474
+
8
2
fi
CLK
Q̄
2N2923
1/2 LM359
PS
CLR
6
−
3
5k
1
10 pF
4
10k
20k
50
PS
CLR
100 pF
D
Q
1/2 DM7474
CLK
Q̄
20 pF
10V
1k
fi
ADJUST
100k
GAIN
ADJUST
10V
12
−
6
10k
1/6 DM7414
2
1/2
LM359
1
8
+
7
5k
20k
11
4
20 pF
2N5114
100k
25 kHz
LOW PASS
FILTER
68 pF
100k
1 µF
10
13k
+
−
RECOVERED
INFORMATION
14
1/2
LM359
500 pF
+
9
120k
11
10V

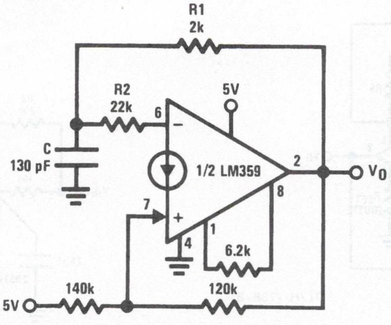
- Up to 5 MHz operation
- $T^2L$ compatible input

All diodes = 1N914

TL/H/7788-33

## Typical Applications (Continued)

### Squarewave Generator


R1
2k
R2
22k
6
5V
C
130 pF
1/2 LM359
2
V_O
8
7
4
1
6.2k
5V
140k
120k

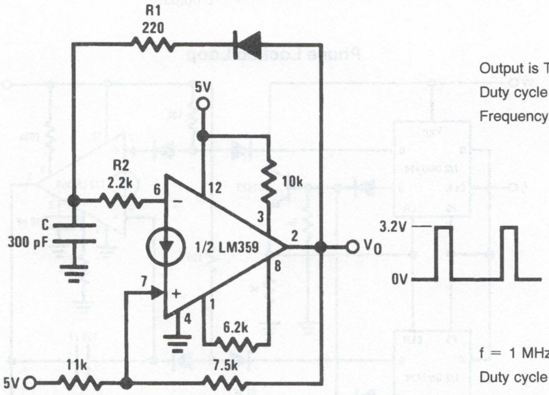
TL/H/7788-34

f = 1 MHz

Output is TTL compatible

Frequency is adjusted by R1 & C (R1 ≪ R2)

### Pulse Generator


R1
220
5V
10k
R2
2.2k
6
12
3
C
300 pF
1/2 LM359
2
V_O
8
7
1
4
6.2k
5V
11k
7.5k
3.2V
0V

Output is TTL compatible

Duty cycle is adjusted by R1

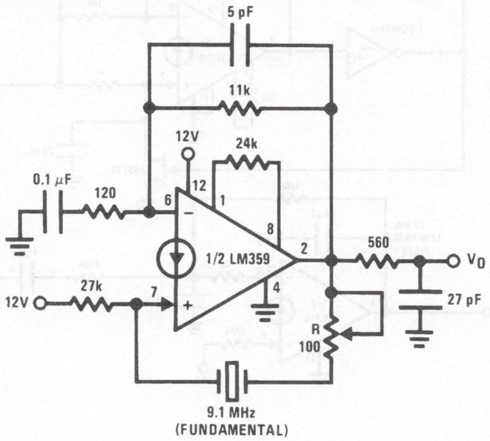
Frequency is adjusted by C

f = 1 MHz

Duty cycle = 20%

TL/H/7788-36

### Crystal Controlled Sinewave Oscillator


5 pF
11k
12V
24k
0.1 μF
120
6
12
1
8
1/2 LM359
2
560
V_O
12V
27k
7
4
27 pF
R
100
9.1 MHz
(FUNDAMENTAL)

$V_O$ = 500 mVp-p

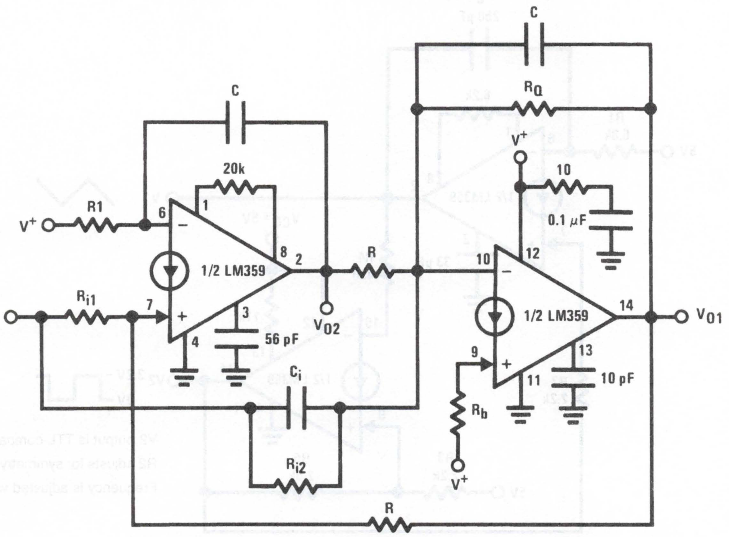
f = 9.1 MHz

THD < 2.5%

TL/H/7788-37

## Typical Applications (Continued)

### High Performance 2 Amplifier Biquad Filter(s)



TL/H/7788-35

- The high speed of the LM359 allows the center frequency $Q_o$ product of the filter to be: $f_o \times Q_o \leq 5$ MHz
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

### DC Biasing Equations for $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+/2$

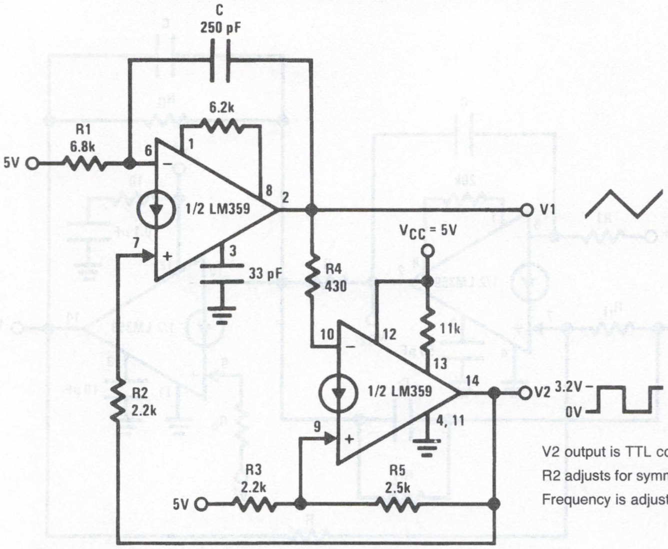
| | |
|---|---|
| Type I | $\frac{2\,V_{IN(DC)}}{V^+\,(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R |
| Type II | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R |
| Type III | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; $\frac{1}{R1} = \frac{V_{IN(DC)}}{V^+\,(R_{i1})} + \frac{1}{2R}$ |

### Analysis and Design Equations

| Type | $V_{O1}$ | $V_{O2}$ | $C_i$ | $R_{i2}$ | $R_{i1}$ | $f_o$ | $Q_o$ | $f_Z$(notch) | $H_{o(LP)}$ | $H_{o(BP)}$ | $H_{o(HP)}$ | $H_{o(BR)}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I | BP | LP | O | $R_{i2}$ | ∞ | $½\,\pi RC$ | $R_Q/R$ | — | $R/R_{i2}$ | $R_Q/R_{i2}$ | — | — |
| II | HP | BP | $C_i$ | ∞ | ∞ | $½\,\pi RC$ | $R_Q/R$ | — | — | $R_QC_i/RC$ | $C_i/C$ | — |
| III | Notch/ BR | — | $C_i$ | ∞ | $R_{i1}$ | $½\,\pi RC$ | $R_Q/R$ | $½\pi\,\sqrt{RR_iCC_i}$ | — | — | — | $H_o\big\rvert_{f \to \infty} = C_i/C$<br>$H_o\big\rvert_{f \to O} = C/R_i$ |

## Typical Applications (Continued)

### Triangle Waveform Generator


C
250 pF
6.2k
R1
6.8k
5V
6
1
−
8
2
1/2 LM359
V1
7
+
3
33 pF
R4
430
V$_{CC}$ = 5V
11k
10
12
13
−
14
1/2 LM359
V2
3.2V
0V
9
+
4, 11
R2
2.2k
R3
2.2k
5V
R5
2.5k

V2 output is TTL compatible

R2 adjusts for symmetry of the triangle waveform

Frequency is adjusted with R5 and C

TL/H/7788-38

**National Semiconductor Corporation**

# LM604A/LM604 4 Channel Mux-Amp

## General Description

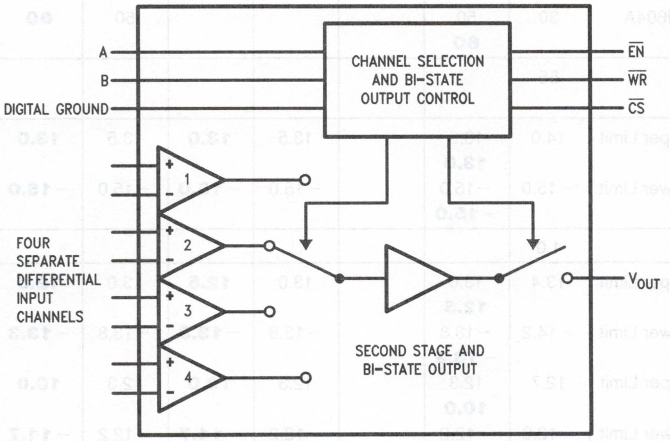
The LM604 Mux-Amp is an op-amp with four selectable differential inputs, combining the functions of a multiplexer with an op-amp. The LM604 can select, buffer, and amplify one of four different input signals, providing a complete system for multiplexing analog signals. It also has the unique Bi-State output which allows two or more Mux-Amps to be connected together at their outputs to increase the number of multiplexed channels. Channel selection and the Bi-State output are controlled by internal logic that interfaces directly to a microprocessor. Besides these unique features, the LM604 has excellent AC and DC op-amp specifications and is internally compensated.

Applications include signal multiplexing and linear circuits that are controlled by digital signals (i.e., programmable gain blocks, filters, and other op-amp circuits).

## Features

- Multiplexes four differential input channels to a single op-amp
- Easy to interface to microprocessor, or operates "stand alone"
- Bi-State output: Operates in two states, Active and Disabled. When disabled, it becomes a high impedance.
- Wide operating voltage range
  - single supply 4V to 32V
  - split supply ±2V to ±16V
- Wide input common mode range $V^- \text{ to } V^+ - 1V$
- Fast channel to channel switching time 5 μs
- Output will drive a 600Ω load

## Block Diagram


A
B
DIGITAL GROUND
CHANNEL SELECTION AND BI-STATE OUTPUT CONTROL
EN
WR
CS
+
−
1
2
3
4
FOUR SEPARATE DIFFERENTIAL INPUT CHANNELS
SECOND STAGE AND BI-STATE OUTPUT
V_OUT

TL/H/9131-10

**Channel Selection**

| A | B | $\overline{\text{WR}}$ | $\overline{\text{CS}}$ | Channel |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 2 |
| 1 | 0 | 0 | 0 | 3 |
| 1 | 1 | 0 | 0 | 4 |
| X | X | X | 1 | Unchanged |
| X | X | 1 | X | Unchanged |

**Bi-State Output Control**

| $\overline{\text{EN}}$ | $\overline{\text{WR}}$ | $\overline{\text{CS}}$ | Output State |
|---|---|---|---|
| 0 | 0 | 0 | Enabled |
| 1 | 0 | 0 | Disabled, High Z |
| X | X | 1 | Unchanged |
| X | 1 | X | Unchanged |

**Order Number LM604AMJ, LM604IJ, LM604IN, LM604ACN, LM604CN, LM604ACM, or LM604CM**
**See NS Package Number J18A, N18A or M20B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 36V or ±18V |
| Differential Input Voltage | ±Supply Voltage |
| Input Voltage Range | ±Supply Voltage |
| Output Short Circuit to Gnd | Continuous (Note 1) |
| ESD Tolerance ($C_{ZAP}$ = 120 pF, $R_{ZAP}$ = 1500Ω) | 2,000V |
| Lead Temperature (Soldering, 5 sec.) | 300°C |
| Storage Temperature Range | −65°C to 150°C |

Operating Ambient Temperature Range

| | |
|---|---|
| LM604AM | $-55°C \leq T_A \leq 125°C$ |
| LM604I | $-40°C \leq T_A \leq 85°C$ |
| LM604AC, LM604C | $0°C \leq T_A \leq 70°C$ |

| | J Pkg. | M Pkg. | N Pkg. |
|---|---|---|---|
| Power Dissipation (Note 2) | 1,600 mW | 1,500 mW | 1,900 mW |
| $T_{JMAX}$ | 150°C | 150°C | 150°C |
| $\theta_{JA}$ (Typical, Board Mounted) | 75°C/W | 83°C/W | 65°C/W |

## DC Electrical Characteristics $V_{SUPPLY}$ = ±15V (Note 3)

| Parameter | Conditions | | Typical | LM604AM | | LM604I | | LM604AC<br>LM604C | | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Input Offset Voltage ($V_{OS}$) | $R_S$ = 10 kΩ | LM604<br>LM604A | 1.0<br>0.5 | 1.0<br>**3.0** | | 3.0 | **5.0** | 3.0<br>1.0 | **5.0**<br>**3.0** | mV (Max) |
| $V_{OS}$ Temperature Drift | | | 5.5 | | | | | | | μV/°C |
| Input Offset Current ($I_{OS}$) | | | 2 | 10<br>**12** | | 10 | **12** | 10 | **12** | nA (Max) |
| $I_{OS}$ Temperature Drift | | | 10 | | | | | | | pA/°C |
| Input Bias Current ($I_B$) | | LM604<br>LM604A | 50<br>30 | 50<br>**60** | | 80 | **100** | 80<br>50 | **100**<br>**60** | nA (Max) |
| $I_B$ Temperature Drift | | | 55 | | | | | | | pA/°C |
| Input Common Mode Voltage Range | | Upper Limit | 14.0 | 13.5<br>**13.0** | | 13.5 | **13.0** | 13.5 | **13.0** | V (Min) |
| | | Lower Limit | −15.0 | −15.0<br>**−15.0** | | −15.0 | **−15.0** | −15.0 | **−15.0** | V (Max) |
| Input Resistance | | | 1.0 | | | | | | | Meg Ω |
| Output Voltage Swing | $R_L$ = 10 kΩ | Upper Limit | 13.4 | 13.0<br>**12.5** | | 13.0 | **12.5** | 13.0 | **12.5** | V (Min) |
| | | Lower Limit | −14.2 | −13.8<br>**−13.3** | | −13.8 | **−13.3** | −13.8 | **−13.3** | V (Max) |
| | $R_L$ = 600Ω | Upper Limit | 12.7 | 12.3<br>**10.0** | | 12.3 | **10.0** | 12.3 | **10.0** | V (Min) |
| | | Lower Limit | −12.6 | −12.2<br>**−11.7** | | −12.2 | **−11.7** | −12.2 | **−11.7** | V (Max) |
| Large Signal Voltage Gain | $V_{OUT}$ = ±10V | $R_L$ = 2 kΩ | 200 | 50<br>**25** | | 50 | **25** | 50 | **25** | V/mV (Min) |
| | | $R_L$ = 600Ω | 200 | 50<br>**25** | | 50 | **25** | 50 | **25** | |
| Common Mode Rejection Ratio | $V_{CM}$ = −15.0V to 13.5V | | 100 | 80<br>**70** | | 80 | **70** | 80 | **70** | dB (Min) |

## DC Electrical Characteristics $V_{SUPPLY}$ = ±15V (Note 3)

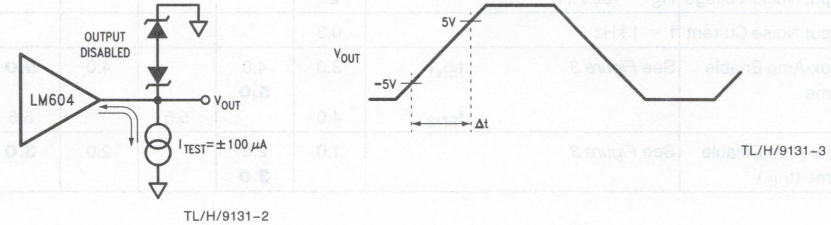
| Parameter | Conditions | Typical | LM604AM | | LM604I | | LM604AC<br>LM604C | | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Power Supply Rejection Ratio | $V_{SUPPLY}$ = ±5.0V to ±16.0V | 100 | 80<br>**70** | | 80 | **70** | 80 | **70** | dB (Min) |
| Output Short Circuit Current | | ±35 | ±50<br>**±60** | | ±50 | **±60** | ±50 | **±60** | mA (Max) |
| Output Leakage Current | $V_{OUT}$ = −13.5V to 13.0V<br>Bi-State Output Disabled | 4.0 | 10.0<br>**20.0** | | 10.0 | **20.0** | 10.0 | **20.0** | μA (Max) |
| Output Capacitance | Bi-State Output Disabled<br>See *Figure 1* | 10 | | | | | | | pF |
| Supply Current | | 7.0 | 9.0<br>**10.0** | | 9.0 | **10.0** | 9.0 | **10.0** | mA (Max) |

## AC Electrical Characteristics $V_{SUPPLY}$ = ±15V (Note 3)

| Parameter | Conditions | Typical | LM604AM | | LM604I | | LM604AC<br>LM604C | | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Slew Rate | $A_V = 1, R_L = 2\ k\Omega$ | 3.0 | 2.0<br>**1.5** | | 2.0 | **1.5** | 2.0 | **1.5** | V/μs (Min) |
| Gain Bandwidth Product | f = 100 kHz | 7.0 | 6.0<br>**3.0** | | 6.0 | **3.0** | 6.0 | **3.0** | MHz (Min) |
| Unity Gain Frequency | | 3.0 | | 2.5 | | 2.5 | | 2.5 | MHz (Min) |
| Phase Margin | $R_L = 2\ k\Omega, C_L = 200\ pF$ | 50 | | | | | | | Degrees |
| Settling Time to 0.1% of Final Value | $A_V = -1, V_{OUT} = -5.0V$ to $5.0V$<br>$R_L = 2\ k\Omega$ | 4.0 | | | | | | | μs |
| Channel Switching Time | See *Figure 2* $t_{SW1}$ | 4.0 | 5.5<br>**6.5** | | 5.5 | **6.5** | 5.5 | **6.5** | μs (Max) |
| | $t_{SW2}$ | 5.0 | | 6.5 | | 6.5 | | 6.5 | |
| Channel to Channel Isolation | $R_S = 10\ k\Omega$, f = 10 kHz<br>$V_{IN} = 10.0V_{p\text{-}p}$ | 100 | | | | | | | dB |
| Input Noise Voltage | $R_S = 100\ \Omega$, f = 1 kHz | 20 | | | | | | | nV/$\sqrt{Hz}$ |
| Input Noise Current | f = 1 kHz | 0.3 | | | | | | | pA/$\sqrt{Hz}$ |
| Mux-Amp Enable Time | See *Figure 3* $t_{EN1}$ | 3.0 | 4.0<br>**5.0** | | 4.0 | **5.0** | 4.0 | **5.0** | μs (Max) |
| | $t_{EN2}$ | 4.0 | | 5.5 | | 5.5 | | 5.5 | |
| Mux-Amp Disable Time ($t_{DIS}$) | See *Figure 3* | 1.0 | 2.0<br>**3.0** | | 2.0 | **3.0** | 2.0 | **3.0** | μs (Max) |

## DC Electrical Characteristics $V_{SUPPLY} = 5V$ (Note 3)

| Parameter | Conditions | | Typical | LM604AM Tested Limit (Note 4) | LM604AM Design Limit (Note 5) | LM604I Tested Limit (Note 4) | LM604I Design Limit (Note 5) | LM604AC LM604C Tested Limit (Note 4) | LM604AC LM604C Design Limit (Note 5) | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $R_S = 10\ k\Omega$ | LM604 | 1.0 | | | 3.0 | **5.0** | 3.0 | **5.0** | mV |
| | $V_{OUT} = 2.0V$ | LM604A | 0.5 | 1.0<br>**3.0** | | | | 1.0 | **3.0** | (Max) |
| Input Offset Current | $V_{OUT} = 2.0V$ | | 3.0 | 10<br>**18** | | 10 | **18** | 10 | **18** | nA<br>(Max) |
| Input Bias Current | $V_{OUT} = 2.0V$ | LM604 | 70 | | | 130 | **150** | 130 | **150** | nA |
| | | LM604A | 50 | 80<br>**110** | | | | 80 | **110** | (Max) |
| Input Common Mode Voltage Range | $V_{OUT} = 2.0V$ | Upper Limit | 4.0 | 3.5<br>**3.0** | | 3.5 | **3.0** | 3.5 | **3.0** | V<br>(Min) |
| | | Lower Limit | 0 | 0<br>**0** | | 0 | **0** | 0 | **0** | |
| Output Voltage Swing | $R_L = 10\ k\Omega$ | Upper Limit | 3.5 | 3.2<br>**3.0** | | 3.2 | **3.0** | 3.2 | **3.0** | V<br>(Min) |
| | | Lower Limit | 0.5 | 0.7<br>**0.8** | | 0.7 | **0.8** | 0.7 | **0.8** | V<br>(Max) |
| | $R_L = 600\Omega$ | Upper Limit | 3.3 | 3.0<br>**2.8** | | 3.0 | **2.8** | 3.0 | **2.8** | V<br>(Min) |
| | | Lower Limit | 0.4 | 0.6<br>**0.7** | | 0.6 | **0.7** | 0.6 | **0.7** | V<br>(Max) |
| Large Signal Voltage Gain | $V_{OUT} = 0.8V$ to 2.8V | $R_L = 2\ k\Omega$ | 200 | | 50<br>**25** | | 50<br>**25** | | 50<br>**25** | V/mV<br>(Min) |
| | | $R_L\ 600\Omega$ | 200 | | 50<br>**25** | | 50<br>**25** | | 50<br>**25** | |
| Common Mode Rejection Ratio | $V_{CM} = 0V$ to 3.5V<br>$V_{OUT} = 2.0V$ | | 100 | 80<br>**70** | | 80 | **70** | 80 | **70** | dB<br>(Min) |
| Power Supply Rejection Ratio | $V^+ = 4.0V$ to 5.0V<br>$V_{OUT} = 2.0V$ | | 100 | 80<br>**70** | | 80 | **70** | 80 | **70** | dB<br>(Min) |



$$C_{OUT} = \frac{\Delta t}{10V} \times 100\ \mu A$$

FIGURE 1. Output Capacitance Test

## Digital Input Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 6)

| Parameter | Conditions | Typical | LM604AM | | LM604I | | LM604AC<br>LM604C | | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| $V_{INHI}$ | | | 1.8<br>**2.0** | | 1.8 | **2.0** | 1.8 | **2.0** | V<br>(Min) |
| $V_{INLO}$ | | | 1.0<br>**0.8** | | 1.0 | **0.8** | 1.0 | **0.8** | V<br>(Max) |
| $I_{INHI}$ | | | 5.0<br>**10.0** | | 5.0 | **10.0** | 5.0 | **10.0** | µA<br>(Max) |
| $I_{INLO}$ | | | 5.0<br>**10.0** | | 5.0 | **10.0** | 5.0 | **10.0** | µA<br>(Max) |
| Minimum Pulse Width for WR & CS | | | | **100** | | **100** | | **100** | ns<br>(Min) |
| Minimum Set-Up Time ($t_S$) | See *Figures 3* and *5* | | | **100** | | **100** | | **100** | ns<br>(Min) |
| Minimum Hold Time ($t_H$) | See *Figures 3* and *5* | | | **50** | | **50** | | **50** | ns<br>(Min) |
| Input Capacitance | | 5 | | | | | | | pF |

**Note 1:** Applies to both single and split supply operation. Continuous short circuit operation can result in exceeding the maximum allowed junction temperature.

**Note 2:** When operating at $T_A > 25°C$, the maximum power dissipation must be derated based on $\theta_{JA}$.

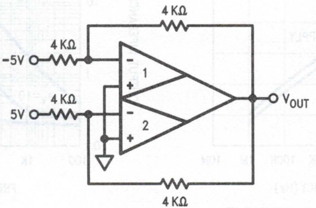
**Note 3:** Unless specified otherwise, all limits are guaranteed for $T_A = T_J = 25°C$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1Meg\Omega$. **Boldface** limits apply at $0°C \le T_J \le 70°C$ for LM604AC and LM604C, $-40°C \le T_J \le 85°C$ for LM604I, and $-55°C \le T_J$ 125°C for LM604AM.

**Note 4:** Guaranteed and 100% production tested.

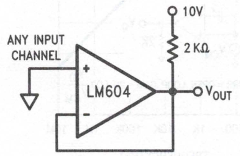
**Note 5:** Guaranteed but not 100% production tested. These numbers are not used to calculate outgoing quality levels.

**Note 6:** Unless specified otherwise, all units are guaranteed at $T_A = T_J = 25°C$. **Boldface** limits apply at the junction temperature extremes specified in note 3. Input voltage levels are with respect to digital ground (pin 4) which must be at least 4.0V below $V^+$.

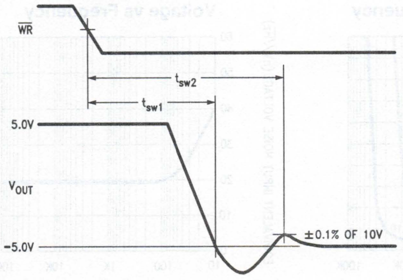
Switching from Channel 1 to 2 with Channel Select preset to $\overline{AB}$ before $\overline{WR}$ = 0. This test applies to all channels.



TL/H/9131-4

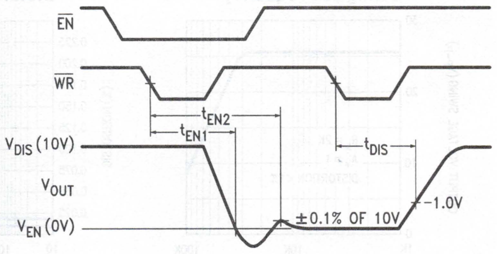


TL/H/9131-8



TL/H/9131-5

**FIGURE 2. Channel Switching Time Test**

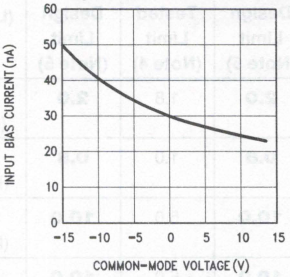


TL/H/9131-9

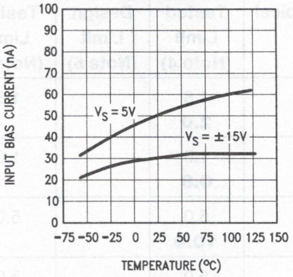
**FIGURE 3. Bi-State Output Enable and Disable Time Test**

## Typical Performance Characteristics (Note 7)

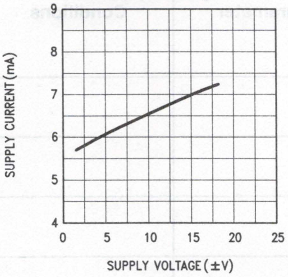
### Input Bias Current vs Input Common-Mode Voltage



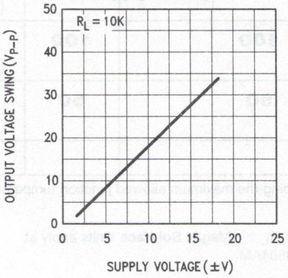
### Input Bias Current vs Temperature



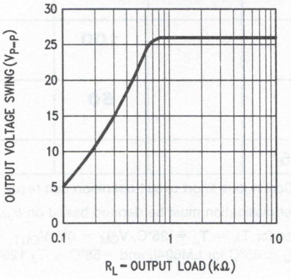
### Supply Current vs Supply Voltage



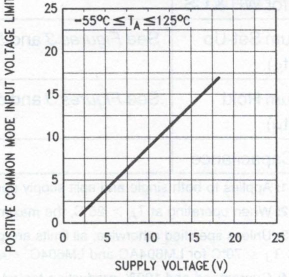
### Output Voltage Swing vs Supply Voltage



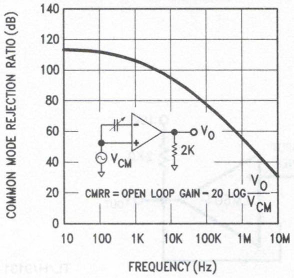
### Output Voltage Swing vs Output Load Resistance



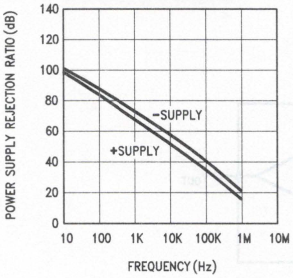
### Upper Common-Mode Voltage Limit vs Positive Supply Voltage



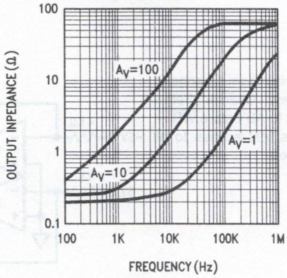
### Common-Mode Rejection Ratio vs Frequency



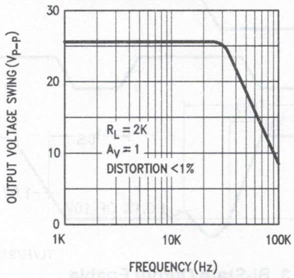
### Power Supply Rejection Ratio vs Frequency



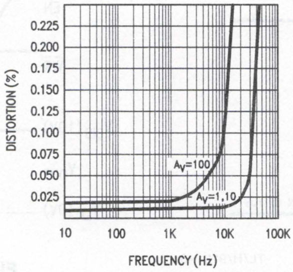
### Output Impedance vs Frequency



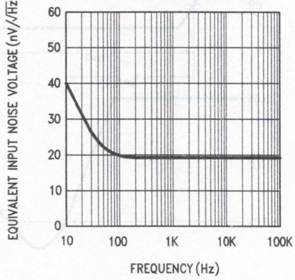
### Undistorted Output Voltage Swing vs Frequency



### Distortion vs Frequency



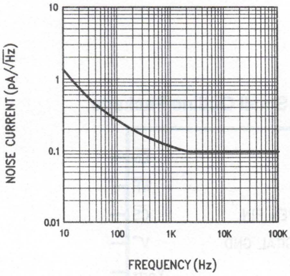
### Equivalent Input Noise Voltage vs Frequency



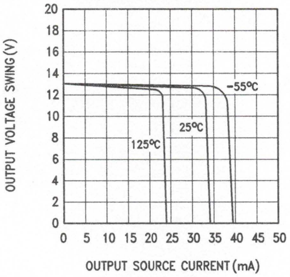
TL/H/9131–6

# Typical Performance Characteristics (Note 7)

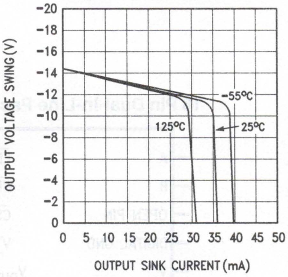
**Equivalent Input Noise Current vs Frequency**



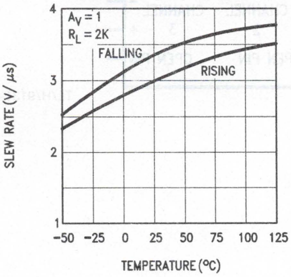
**Positive Current Limit**



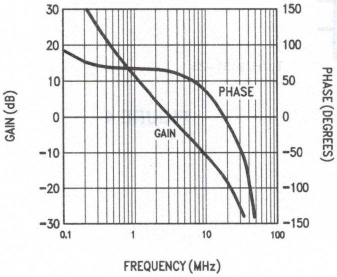
**Negative Current Limit**



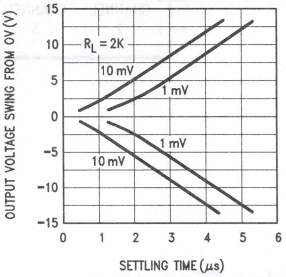
**Slew Rate vs Temperature**



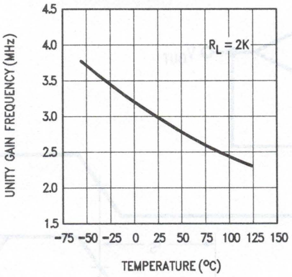
**Bode Plot**



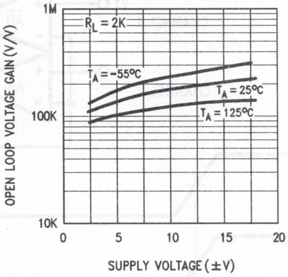
**Inverter Settling Time vs Output Voltage Swing**



**Unity Gain Frequency vs Temperature**



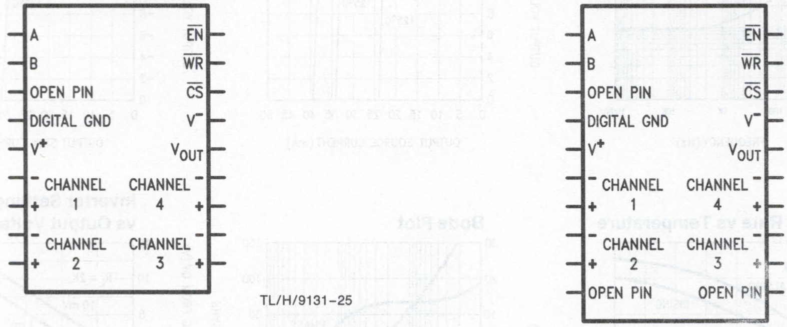
**Open Loop Voltage Gain**



TL/H/9131-7

**Note 7:** Unless specified otherwise, $T_A = T_J = 25°C$, $V_S = \pm 15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1$ Meg.

## Connection Diagrams


A
B
OPEN PIN
DIGITAL GND
$V^+$
CHANNEL 1
CHANNEL 2
$\overline{EN}$
$\overline{WR}$
$\overline{CS}$
$V^-$
$V_{OUT}$
CHANNEL 4
CHANNEL 3
OPEN PIN
OPEN PIN

**18 Pin Dual-In-Line Package**

TL/H/9131-25

**20 Pin Small Outline Package**

TL/H/9131-26

FIGURE 4

## Timing Diagrams

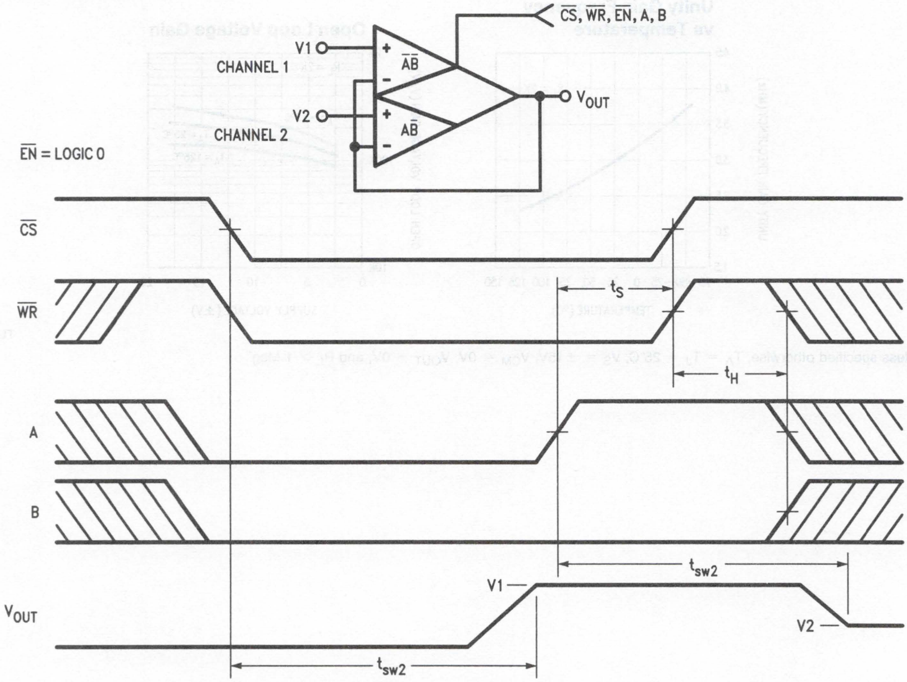

$\overline{CS}$, $\overline{WR}$, $\overline{EN}$, A, B
V1
CHANNEL 1
$\overline{AB}$
V2
CHANNEL 2
$A\overline{B}$
$V_{OUT}$
$\overline{EN}$ = LOGIC 0
$\overline{CS}$
$\overline{WR}$
$t_S$
$t_H$
A
B
$t_{sw2}$
V1
V2
$V_{OUT}$
$t_{sw2}$

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FIGURE 5. Channel Switching Timing Diagram

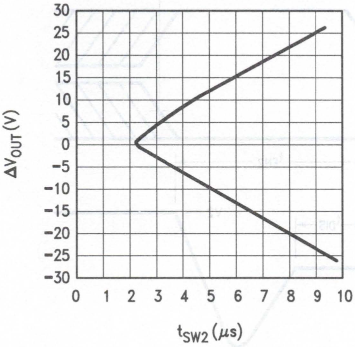
## Functional Description

### INPUT CHANNEL SELECTION

The LM604 contains four differential input channels that are selected one at a time. An input is selected by writing its binary code to pins A and B when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram. The LM604 always has one of its inputs selected. In order to isolate all four channels from the output, the Bi-State output can be disabled.

*Figure 5* illustrates how the LM604 switches from one channel to another. The switching begins on the falling edge of $\overline{WR}$ if A and B are valid before $\overline{WR}$ is a logic 0, or when A and B become valid while $\overline{WR}$ is a logic 0. In either case, the channel switching time ($t_{SW2}$) remains the same. If a channel is to remain selected, its binary code must be valid during the rising edge of $\overline{WR}$ as specified by $t_S$ and $t_H$.

Channel switching time is specified by $t_{SW1}$ and $t_{SW2}$ as shown in *Figure 2*. $t_{SW1}$ is the time it takes the output to first reach its new value, and $t_{SW2}$ is the time it takes the output to settle to within 0.1% of its new value. Clearly, $t_{SW2}$ is a more useful parameter for specifying switching time, but it is difficult to test on a production basis. Therefore, $t_{SW1}$ is tested and this allows $t_{SW2}$ to be guaranteed. Channel switching time will vary as a function of how far the output swings to reach its new value. This is shown in *Figure 6* where $t_{SW2}$ is plotted as a function of output voltage swing ($\Delta V_{OUT}$).



TL/H/9131-12

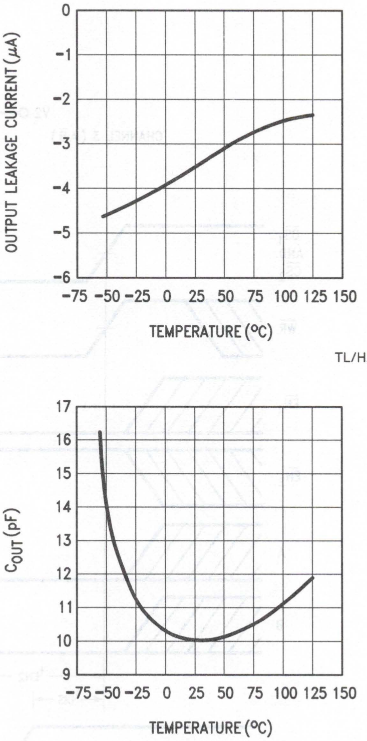
$\Delta V_{OUT} = V_{OUT}$ (Selected Channel) $- V_{OUT}$ (Previous Channel)

**FIGURE 6. $t_{SW2}$ vs $\Delta V_{OUT}$**

### BI-STATE OUTPUT

The Bi-State output can be either enabled (on) or disabled (off). When disabled, the output becomes a high impedance load that can be driven by another output stage. This allows several Mux-Amps to be connected together at their outputs by having only one output enabled at one time. Thus, several Mux-Amps can be in parallel to the same output to increase the number of multiplexed channels. The Bi-State output is controlled by $\overline{EN}$ when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram.

When the output is disabled and driven by another output, it behaves like a small capacitive load with a few microamps of leakage current. The data sheet specifies this with the parameters "Output Capacitance" and "Output Leakage Current". Both parameters vary with temperature, as shown in *Figure 7*.



TL/H/9131-13

TL/H/9131-14

**FIGURE 7. $I_{LEAKAGE}$ and $C_{OUT}$ vs Temperature**

*Figure 8* illustrates switching between two Mux-Amps that are connected in parallel to the same output. Switching begins on the falling edge of $\overline{WR}$ if the $\overline{EN}$ signals are correctly set before $\overline{WR}$ is a logic 0, or when the $\overline{EN}$ signals become valid while $\overline{WR}$ is a logic 0. The Bi-State output takes less time to become disabled than it does to become enabled, and this insures the outputs are switched in a "break before make" method. If an in output is to remain enabled or disabled after $\overline{WR}$ becomes a logic 1, $\overline{EN}$ must be valid during the rising edge of $\overline{WR}$ as specified by $t_S$ and $t_H$. Note that when a Mux-Amp has its output enabled, the binary code for the selected input channel must also be written.

Bi-State output enable time ($t_{EN1}$ and $t_{EN2}$) and disable time ($t_{DIS}$) are defined in *Figure 3*. $t_{EN1}$ is the time it takes the output to first reach its enabled value ($V_{EN}$), and $t_{EN2}$ is the time it takes the output to settle to within 0.1% of $V_{EN}$. As with channel switching time, $t_{EN1}$ is a tested parameter that allows $t_{EN2}$ to be guaranteed. $t_{DIS}$ is the time it takes the output to become a high impedance. Output enable time will vary according to how far the output swings from $V_{DIS}$ to $V_{EN}$, and this is plotted in *Figure 9*.

## Functional Description (Continued)

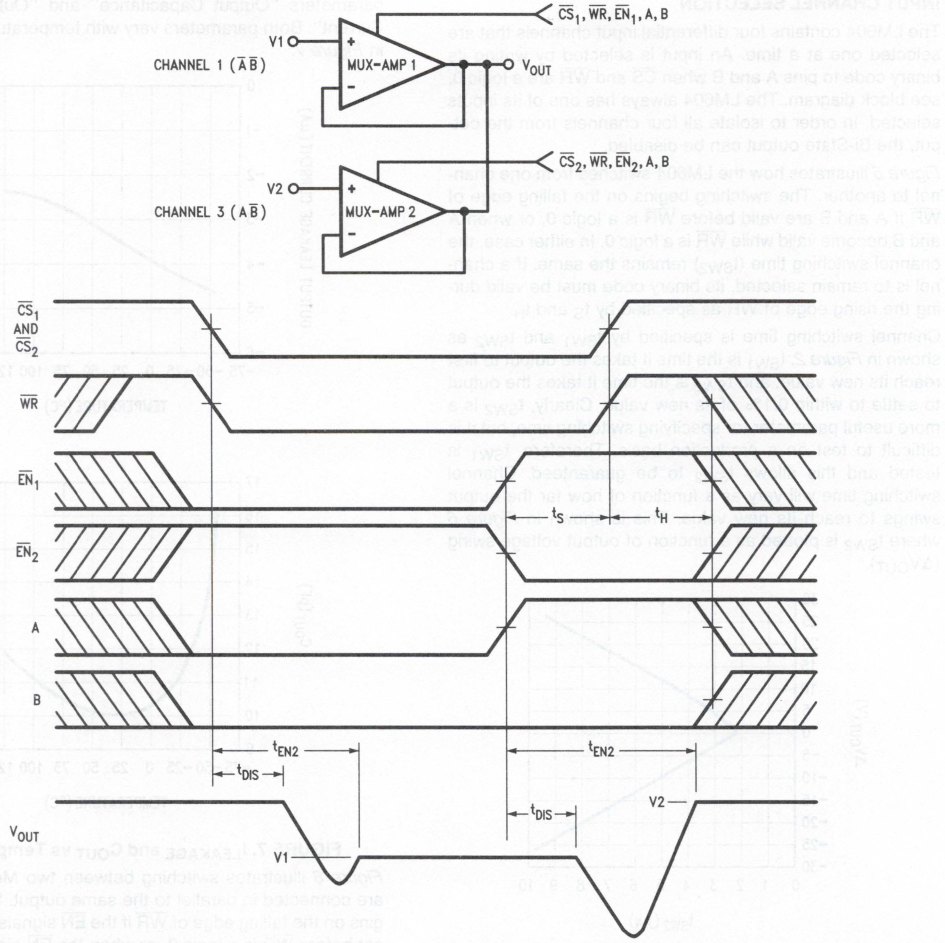

CS1, WR, EN1, A, B
V1
CHANNEL 1 (A B̄)
MUX-AMP 1
VOUT
CS2, WR, EN2, A, B
V2
CHANNEL 3 (A B̄)
MUX-AMP 2
+
−
CS1 AND CS2
WR
EN1
EN2
A
B
tS
tH
tEN2
tDIS
tEN2
tDIS
VOUT
V1
V2

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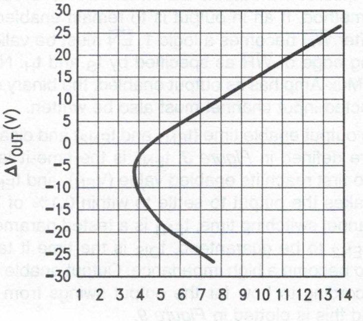
**FIGURE 8. Timing Diagram for Switching Bi-State Outputs**



TL/H/9131-16

$\Delta V_{OUT} = V_{EN} - V_{DIS}$

**FIGURE 9. $t_{EN2}$ vs $\Delta V_{OUT}$**

### DIGITAL CONTROL

As mentioned in the previous sections, the input channels and Bi-State output are controlled by logic levels on pins A, B, and $\overline{EN}$. There are two ways to apply logic levels to these pins. 1) Hardwire $\overline{WR}$ and $\overline{CS}$ directly to digital ground so that the LM604 operates in a "stand alone" mode. This allows input logic levels to directly control the LM604. 2) Write digital signals to A, B, and $\overline{EN}$ as shown in the timing diagrams of *Figures 5* and *8*. This method is used when the LM604 interfaces to a microprocessor. Note that $\overline{CS}$ and $\overline{WR}$ can occur simultaneously, so set-up and hold times are not required for $\overline{CS}$. Also, notice that $\overline{WR}$ must remain a logic 1 during the hold time period.

Input logic levels are referenced to a 1.4V threshold voltage, making the LM604 compatible with TTL and CMOS logic. This threshold voltage is referenced to digital ground. The voltage level of digital ground can be as low as $V^-$ (pin 15) and as high as 4V below $V^+$ (pin 5).

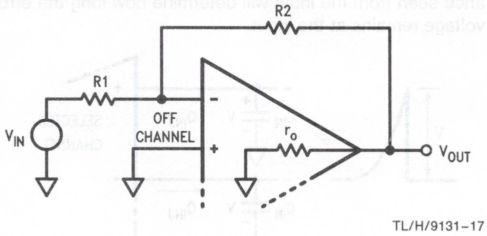
## Application Hints

### USING MULTIPLE FEEDBACK LOOPS

Each input channel of the LM604 is used as a single op-amp with its own feedback loop. Two examples of this are circuits with multiple inverting gain channels and non-inverting gain channels (*Figure 10*). These circuits have multiple feedback loops connected to the same output with one feedback loop connected to a selected channel and the others connected to "off" channels. The feedback loop of the selected channel determines the gain of these circuits. The off channel feedback loops affect these circuits in two ways. 1) They create an additional load at the output. 2) Feedback loops for inverting gain channels provide feedthrough paths from the inputs of the off channels to the output.

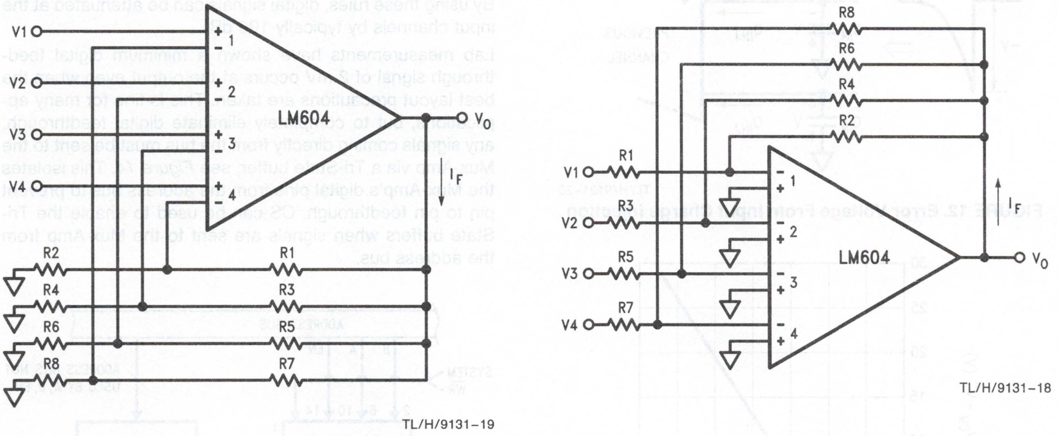
In *Figure 10*, the loading affect of multiple feedback loops is given in terms of current flowing through the feedback loops ($I_F$). In circuits with non-inverting gain channels, $I_F$ is a function of $V_{OUT}$ and the resistance of the feedback loops. In circuits with inverting gain channels, $I_F$ is different for each channel selected because it is also a function of the off channel input voltages. This additional loading must be accounted for when designing Mux-Amp circuits. Otherwise, the output load resistance will be less than anticipated.

*Figure 11* illustrates feedthrough in an off inverting gain channel. Feedthrough occurs because the feedback resistors and the Mux-Amp output impedance ($r_o$) form a voltage divider. This divider allows a portion of the off channel's input signal to appear at the output. The amount of signal that feeds through depends on the ratio of output impedance to feedback loop resistance. Output impedance varies according to Mux-Amp gain (gain of the selected channel) and the frequency of the feedthrough signal. This variation must be considered when calculating feedthrough, and it is plotted in the "Typical Device Characteristics" section.



$$V_{OUT} = V_{IN}\left(\frac{r_o}{R1 + R2 + r_o}\right)$$

**FIGURE 11. Inverting Gain Channel Feedthrough**



| Channel | $V_O$ |
|---|---|
| 1 | $V1\left(1 + \frac{R7}{R8}\right)$ |
| 2 | $V2\left(1 + \frac{R5}{R6}\right)$ |
| 3 | $V3\left(1 + \frac{R3}{R4}\right)$ |
| 4 | $V4\left(1 + \frac{R1}{R2}\right)$ |

$$I_F = V_O\left(\frac{1}{R1 + R2} + \frac{1}{R3 + R4} + \frac{1}{R5 + R6} + \frac{1}{R7 + R8}\right)$$

Multiple Non-Inverting Gain Channels

| Channel | $V_O$ | $I_F$ |
|---|---|---|
| 1 | $-V1\left(\frac{R2}{R1}\right)$ | $\frac{V_O}{R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V3}{R5 + R6} + \frac{V_O - V4}{R7 + R8}$ |
| 2 | $-V2\left(\frac{R4}{R3}\right)$ | $\frac{V_O}{R4} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V3}{R5 + R6} + \frac{V_O - V4}{R7 + R8}$ |
| 3 | $-V3\left(\frac{R6}{R5}\right)$ | $\frac{V_O}{R6} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V4}{R7 + R8}$ |
| 4 | $-V4\left(\frac{R8}{R7}\right)$ | $\frac{V_O}{R8} + \frac{V_O - V1}{R1 + R2} + \frac{V_O - V2}{R3 + R4} + \frac{V_O - V3}{R5 + R6}$ |

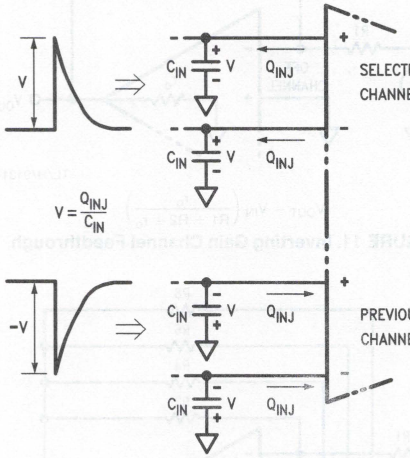
Multiple Inverting Gain Channels

**FIGURE 10. Circuits Using Multiple Inverting and Non-Inverting Gain Channels**

## Application Hints (Continued)

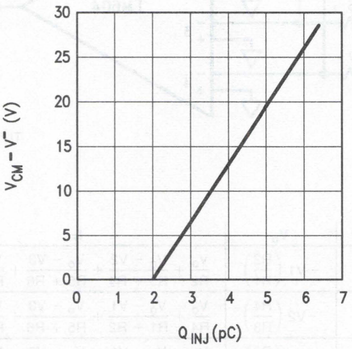
### INPUT CHARGE INJECTION

When the Mux-Amp switches channels, charge is injected from the inputs of the selected and previous channels, see *Figure 12*. This causes a positive error voltage at the input of the selected channel and a negative voltage at the previous channel. The amplitude of this error voltage equals $Q_{INJ}/C_{IN}$, where $C_{IN}$ is the total capacitance at the input and $Q_{INJ}$ is the charge injected. As plotted in *Figure 13*, $Q_{INJ}$ increases proportionally with the difference in voltage between a channel's input common mode voltage and the negative supply. The RC time constant of $C_{IN}$ times resistance seen from the input will determine how long the error voltage remains at the input.



TL/H/9131-20

**FIGURE 12. Error Voltage From Input Charge Injection**



TL/H/9131-21

**FIGURE 13. $Q_{INJ}$ vs $V_{CM} - V^-$**

### MAXIMUM OUTPUT LOAD CONDITIONS

The Mux-Amp is guaranteed to drive a 600Ω load as specified over its entire operating range. Reducing the load resistance below this value may cause the output to current limit. It may also cause the junction temperature limit to be exceeded when operating the part near its maximum ambient temperature.

The Mux-Amp is unconditionally stable with as much as 500 pF connected from the output to ground. If the output is required to drive a larger capacitive load, the Mux-Amp may need to operate with at least a gain of 10. Otherwise, it may become unstable when sinking current.

### DIGITAL FEEDTHROUGH

When interfacing the Mux-Amp to a microprocessor, pins A, B, $\overline{\text{EN}}$, and $\overline{\text{WR}}$ are connected to an address bus where high frequency digital signals are present. The fast edges of these signals can propagate into the Mux-Amp's analog signal path, causing fast transients to appear at the output. To avoid this problem, the following precautions should be taken.

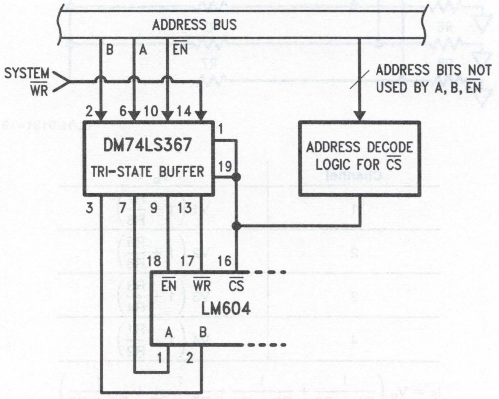
1) Analog and digital ground must be kept separate. They can only be connected together back at the power supply or supply bus.

2) Bypass capacitors should have low inductance to prevent noise spikes on the voltage supply pins. A ceramic disc capacitor of 0.1 $\mu$F is usually sufficient.

3) All lead lengths should be kept short to prevent them from picking up digital signals.

By using these rules, digital signals can be attenuated at the input channels by typically 100 dB.

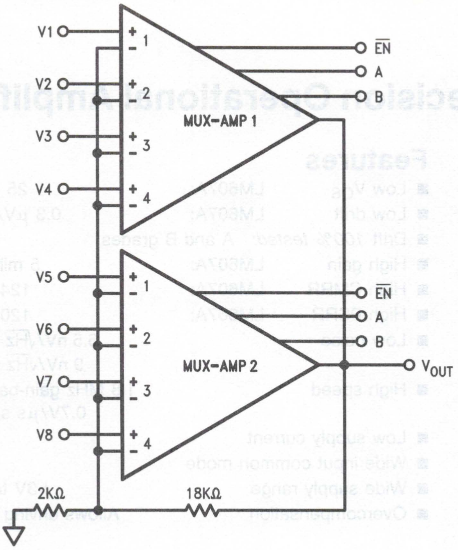
Lab measurements have shown a minimum digital feedthrough signal of 2 mV occurs at the output even when the best layout precautions are taken. This is fine for many applications, but to completely eliminate digital feedthrough, any signals coming directly from the bus must be sent to the Mux-Amp via a Tri-State buffer, see *Figure 14*. This isolates the Mux-Amp's digital pins from the address bus to prevent pin to pin feedthrough. CS can be used to enable the Tri-State buffers when signals are sent to the Mux-Amp from the address bus.



TL/H/9131-22

**FIGURE 14. Isolating Mux-Amp from Address Bus by Using a Tri-State Buffer**

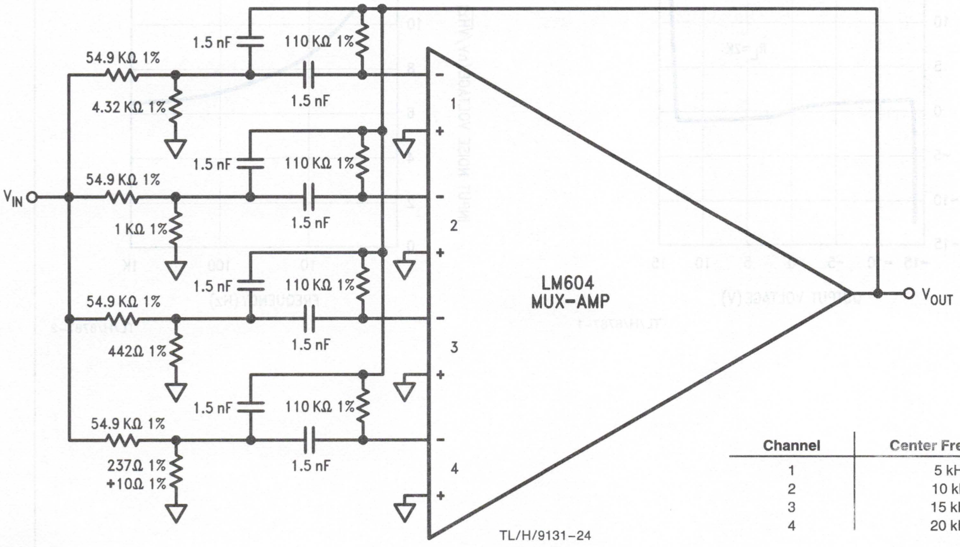
## Typical Applications


V1
V2
V3
V4
V5
V6
V7
V8
+ 1 -
+ 2 -
+ 3 -
+ 4 -
MUX-AMP 1
MUX-AMP 2
EN
A
B
EN
A
B
$V_{OUT}$
2KΩ
18KΩ

| Mux-Amp 1 A | Mux-Amp 1 B | Mux-Amp 1 $\overline{EN}$ | Mux-Amp 2 A | Mux-Amp 2 B | Mux-Amp 2 $\overline{EN}$ | Input |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | X | X | 1 | V1 |
| 0 | 1 | 0 | X | X | 1 | V2 |
| 1 | 0 | 0 | X | X | 1 | V3 |
| 1 | 1 | 0 | X | X | 1 | V4 |
| X | X | 1 | 0 | 0 | 0 | V5 |
| X | X | 1 | 0 | 1 | 0 | V6 |
| X | X | 1 | 1 | 0 | 0 | V7 |
| X | X | 1 | 1 | 1 | 0 | V8 |

TL/H/9131-23

**Eight Channel Multiplexer and Amplifier with a Gain of 10**


$V_{IN}$
54.9 KΩ 1%
4.32 KΩ 1%
54.9 KΩ 1%
1 KΩ 1%
54.9 KΩ 1%
442Ω 1%
54.9 KΩ 1%
237Ω 1%
+10Ω 1%
1.5 nF
110 KΩ 1%
1.5 nF
1.5 nF
110 KΩ 1%
1.5 nF
1.5 nF
110 KΩ 1%
1.5 nF
1.5 nF
110 KΩ 1%
1.5 nF
- 1 +
- 2 +
- 3 +
- 4 +
LM604
MUX-AMP
$V_{OUT}$

| Channel | Center Frequency |
|---|---|
| 1 | 5 kHz |
| 2 | 10 khz |
| 3 | 15 kHz |
| 4 | 20 kHz |

TL/H/9131-24

**Programmable Bandpass Filter:** Each channel has a 2 kHz bandwidth and a gain of 1 at the center frequency

National
Semiconductor
Corporation

# LM607/LM607A/LM607B Precision Operational Amplifier

## General Description

The LM607 series of precision operational amplifiers are trimmed at wafer sort to extremely low values of offset voltage. Advanced circuit design and testing techniques allow guaranteed drift specifications as low as 0.3 μV/°C with offsets as low as 25 μV.

Other input parameters are equally impressive. The typical open loop voltage gain of 5 Million yields extremely low error in high-gain applications. CMRR and PSRR are typically 140 dB.

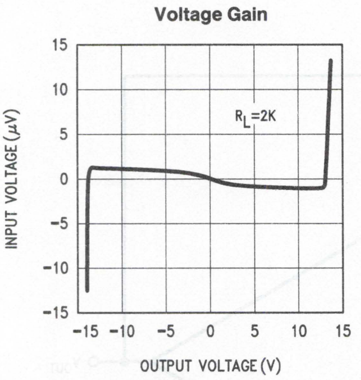
Using Super-Beta transistors in the front end enables the LM607 to operate at high input stage current while maintaining low values of input bias current (1 nA typ.) This gives the part its low input voltage noise: 6.5 nV/$\sqrt{\text{Hz}}$.

High operating currents also help give the LM607 its high gain-bandwidth product of 1.8 MHz and slew rate of 0.7V/μs. Despite its higher speed, the LM607 draws less supply current than OP-07 types: only 1 mA at ±15V supplies.

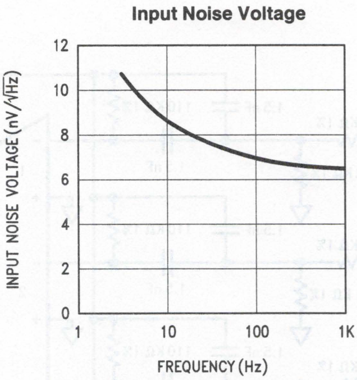
## Features

| | | |
|---|---|---|
| ■ Low $V_{OS}$ | LM607A: | 25 μV max |
| ■ Low drift | LM607A: | 0.3 μV/°C max |
| ■ Drift *100% tested:* | A and B grades | |
| ■ High gain | LM607A: | 5 million min |
| ■ High CMRR | LM607A: | 124 dB min |
| ■ High PSRR | LM607A: | 120 dB min |
| ■ Low noise | | 6.5 nV/$\sqrt{\text{Hz}}$ @ 1 kHz<br>9 nV/$\sqrt{\text{Hz}}$ @ 10 Hz |
| ■ High speed | | 1.8 MHz gain-bandwidth<br>0.7V/μs slew rate |
| ■ Low supply current | | 1 mA |
| ■ Wide input common mode | | ±13V |
| ■ Wide supply range | | ±3V to ±18V |
| ■ Overcompensation | | Allows driving high $C_L$ |

## Typical Performance Characteristics



TL/H/8787-1



TL/H/8787-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Differential Input Overdrive Current (Note 7) | ±25 mA |
| Supply Voltage | 44V |
| Input Voltage | Supply Voltage |
| Output Short Circuit to Gnd | Continuous |
| Power Dissipation | 500 mW |
| Storage Temperature Range | −65°C to 150°C |
| Operating Junction Temperature Range (Note 9) | |
| LM607AM/LM607BM | −55°C to 125°C |
| LM607C/LM607AC/LM607BC | 0°C to 70°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| ESD Tolerance $C_{ZAP}$ = 100 pF<br>$R_{ZAP}$ = 1.5 kΩ | 2000V |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | Typ | LM607AM Tested Limit (Note 5) | LM607AM Design Limit (Note 6) | LM607BM Tested Limit (Note 5) | LM607BM Design Limit (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| Input Offset Voltage | (Note 2) | 15 | 25<br>**80** | | 60<br>**120** | | μV<br>Max |
| Input Offset Voltage Drift | (Note 3) | 0.2 | **0.3** | | **0.6** | | μV/°C<br>Max |
| Input Offset Voltage Long Term Stability | (Note 4) | 0.2 | | | | | μV/mo<br>Max |
| Input Bias Current | | 1 | 2<br>**4** | | 3<br>**6** | | nA<br>Max |
| Input Offset Current | | 0.5 | 2<br>**4** | | 2.8<br>**5.6** | | nA<br>Max |
| Input Noise Voltage | 0.1 to 10 Hz | 0.2 | | 0.5 | | 0.5 | μV p-p<br>Max |
| Input Noise Voltage Density | f = 10 Hz<br>f = 100 Hz<br>f = 1 kHz | 9<br>7<br>6.5 | | 18<br>10<br>8 | | 18<br>10<br>8 | nV/√Hz<br>Max |
| Input Noise Current | 0.1 to 10 Hz | 14 | | | | | pA p-p<br>Max |
| Input Noise Current Density | f = 10 Hz<br>f = 100 Hz<br>f = 1 kHz | 0.32<br>0.14<br>0.12 | | | | | pA/√Hz<br>Max |
| Input Resistance | Differential Mode<br>Common Mode | 2<br>100 | | | | | MΩ<br>GΩ |
| Input Voltage Range | | ±13.5 | ±13<br>**±12.5** | | ±13<br>**±12.5** | | V<br>Min |
| Common-Mode Rejection Ratio | $V_{CM}$ = ±13V<br>**$V_{CM}$ = ±12.5V** | 140 | 124<br>**120** | | 116<br>**112** | | dB<br>Min |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V<br>(Note 8) | 140 | 120<br>**117** | | 114<br>**112** | | dB<br>Min |
| Large-Signal Voltage Gain | $V_O$ = ±10V<br>$R_L$ ≥ 2 kΩ | 10000 | 5000<br>**2000** | | 2000<br>**1500** | | V/mV<br>Min |
| | $R_L$ ≥ 1 kΩ | 5000 | 1500 | | 1000 | | |

## Electrical Characteristics (Note 1) (Continued)

| Parameter | Conditions | Typ | LM607AM |  | LM607BM |  | Units |
|---|---|---|---|---|---|---|---|
|  |  |  | Tested Limit (Note 5) | Design Limit (Note 6) | Tested Limit (Note 5) | Design Limit (Note 6) |  |
| Output Voltage Swing | $R_L \geq 2\ k\Omega$<br>$R_L \geq 1\ k\Omega$ | ±13.8 | ±13<br>**±12.5**<br>±12.5 |  | ±13<br>**±12.5**<br>±12.5 |  | V<br>Min |
| Slew Rate |  | 0.7 |  | 0.4 |  | 0.4 | V/µs<br>Min |
| Gain-Bandwidth Product | f = 100 kHz | 1.8 |  | 1.0 |  | 1.0 | MHz<br>Min |
| Open-Loop Output Resistance |  | 50 |  |  |  |  | Ω |
| Supply Current |  | 1 | 1.5<br>**2.0** |  | 1.5<br>**2.0** |  | mA<br>Max |
| Offset Adjust Range |  | 1.5 |  |  |  |  | mV |

## Electrical Characteristics (Note 1)

| Parameter | Conditions | Typ | LM607AC |  | LM607BC |  | LM607C |  | Units |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Tested Limit (Note 5) | Design Limit (Note 6) | Tested Limit (Note 5) | Design Limit (Note 6) | Tested Limit (Note 5) | Design Limit (Note 6) |  |
| Input Offset Voltage | (Note 2) | 15 | 25<br>**40** |  | 60<br>**90** |  | 150 | **250** | µV<br>Max |
| Input Offset Voltage Drift | (Note 3) | 0.2 | **0.3** |  | **0.6** |  |  | **2.5** | µV/°C<br>Max |
| Input Offset Voltage Long Term Stability | (Note 4) | 0.2 |  |  |  |  |  |  | µV/mo<br>Max |
| Input Bias Current |  | 1 | 2 | **4** | 3 | **6** | 10 | **14** | nA<br>Max |
| Input Offset Current |  | 0.5 | 2 | **4** | 2.8 | **5.6** | 6 | **10** | nA<br>Max |
| Input Noise Voltage | 0.1 to 10 Hz | 0.2 |  | 0.5 |  | 0.5 | 0.5 |  | µV p-p<br>Max |
| Input Voltage Noise Density | f = 10 Hz<br>f = 100 Hz<br>f = 1 kHz | 9<br>7<br>6.5 |  | 18<br>10<br>8 |  | 18<br>10<br>8 |  | 20<br>13.5<br>11.5 | nV/$\sqrt{Hz}$<br>Max |
| Input Noise Current | 0.1 to 10 Hz | 14 |  |  |  |  |  |  | pA p-p<br>Max |
| Input Noise Current Density | f = 10 Hz<br>f = 100 Hz<br>f = 1 kHz | 0.32<br>0.14<br>0.12 |  |  |  |  |  |  | pA/$\sqrt{Hz}$<br>Max |
| Input Resistance | Differential Mode<br>Common Mode | 2<br>100 |  |  |  |  |  |  | MΩ<br>GΩ |
| Input Voltage Range |  | ±13.5 | ±13 | **±12.5** | ±13 | **±12.5** | ±13 | **±12.5** | V<br>Min |
| Common-Mode Rejection Ratio | $V_{CM}$ = ±13V<br>**$V_{CM}$ = ±12.5 V** | 140 | 124 | **120** | 116 | **112** | 110 | **108** | dB<br>Min |
| Power Supply Rejection Ratio | $V_S$ = ±3V to ±18V<br>(Note 8) | 140 | 120 | **117** | 114 | **112** | 110 | **108** | dB<br>Min |

## Electrical Characteristics (Note 1) (Continued)

| Parameter | Conditions | Typ | LM607AC | | LM607BC | | LM607C | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 5) | Design Limit (Note 6) | Tested Limit (Note 5) | Design Limit (Note 6) | Tested Limit (Note 5) | Design Limit (Note 6) | |
| Large-Signal Voltage Gain | $V_O = \pm 10V$<br>$R_L \geq 2 k\Omega$<br>$R_L \geq 1 k\Omega$ | 10000<br>5000 | 5000<br>1500 | **2000** | 2000<br>1000 | **1500** | 1500<br>1000 | **1000** | V/mV Min |
| Output Voltage Swing | $R_L \geq 2 k\Omega$<br>$R_L \geq 1 k\Omega$ | ±13.8 | ±13<br>±12.5 | **±12.5** | ±13<br>±12.5 | **±12.5** | ±12.5<br>±12 | **±12** | V Min |
| Slew Rate | | 0.7 | | 0.4 | | 0.4 | | 0.4 | V/μs Min |
| Gain-Bandwidth Product | f = 100 kHz | 1.8 | | 1.0 | | 1.0 | | 1.0 | MHz Min |
| Open-Loop Output Resistance | | 50 | | | | | | | Ω |
| Supply Current | | 1 | 1.5 | **2.0** | 1.5 | **2.0** | 1.8 | **2.2** | mA Max |
| Offset Adjust Range | | 1.5 | | | | | | | mV |

**Note 1:** All limits guaranteed for $T_J = 25°C$, $V_{CM} = 0$, $V_O = 0$ and ±15V supplies unless otherwise specified. **Boldface limits apply at temperature extremes.**

**Note 2:** Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 3 μV settling out in 5 minutes. The LM607C offset voltage is measured by automated test equipment within 200 ms of applying power.

**Note 3:** Input offset voltage drift is defined as $[V_{OS}(70°C) - V_{OS}(-5°C)]/75°C$ for the commercial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $[V_{OS}(25°C) - V_{OS}(-55°C)]/80°C$ and $[V_{OS}(125°C) - V_{OS}(25°C)]/100°C$.

**Note 4:** Input offset voltage long term stability refers to the average trend line of $V_{OS}$ vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in $V_{OS}$ during the first 30 days are typically 2 μV.

**Note 5:** Guaranteed and 100% production tested.

**Note 6:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

**Note 7:** Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

**Note 8:** Power Supply Rejection Ratio is tested by moving both power supplies together from their minimum to maximum values.

**Note 9:** Typical thermal resistance of the molded package is 95°C/W junction-to-ambient. Typical thermal resistance of the metal can package is 150°C/W junction-to-ambient and 17°C/W junction-to-case.

## Application Hints

### OFFSET VOLTAGE

Offset voltage of the LM607 is internally trimmed to a very low value. The data sheet $V_{OS}$ specification applies at $T_J = 25°C$, $V_{CM} = 0$ and ±15V supplies. For other conditions, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Although the LM607C is specified as $T_J = 25°C$, the 3 μV typical warmup drift is a small fraction of its 100 μV max offset. For the 25 μV LM607A and 50 μV LM607B grades, the offset voltage is measured fully warmed up with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure $V_{OS}$ with high accuracy, gain must be taken right at the device as shown, otherwise the offset voltage would get swamped out by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimized airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal emf. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

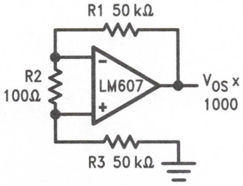


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**FIGURE 1. Offset Voltage Test Circuit**

### OFFSET NULLING

This is usually not required on the LM607 family since its offset voltage is internally trimmed. An offset adjust range of

## Application Hints (Continued)

approximately ±1.5 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2*. With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiometer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. For example the circuit of *Figure 3* has an adjustment range of ±150 μV.

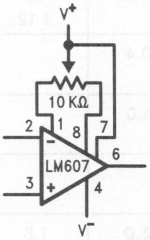

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**FIGURE 2. Offset Adjust Circuit**

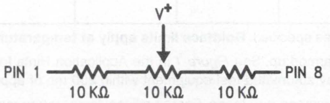

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**FIGURE 3. Improved Sensitivity Offset Adjust**

Because adjusting the offset voltage of an LM607 will alter its offset voltage temperature drift, caution is advised. Every 100 μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM607C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

### OVERCOMPENSATION

Without any external compensation, the LM607 is stable at unity gain and up to 750 pF load capacitance. It has a slew rate of 0.7V/μs and a gain-bandwidth product of 1.8 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4*. This increases maximum capacitive loading to 0.01 μF while decreasing slew rate to 0.13V/μs and bandwidth to 200 kHz. If overcompensation is not desired, pin 5 should be left open.

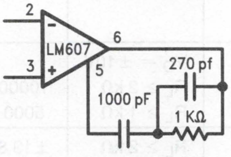

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**FIGURE 4. Overcompensation**

### NOISE

The LM607 achieves lower voltage noise than the OP-07 primarily by operating at higher input stage current. Its superbeta input transistors and trimmed bias-current compensation prevent the bias current from increasing. When measuring spot noise, a circuit as shown in *Figure 5* is recommended. The DUT runs at a gain of 100 will not roll off until approximately 15 kHz. Another gain of 100 amplifier following brings total DUT-input-referred gain up to 10,000 to minimize sensitivity to EMI in the environment. When measuring spot noise at 100 Hz, it is recommended that the bandwidth be 20 Hz or less to minimize pickup of 120 Hz, the second harmonic of line frequency.

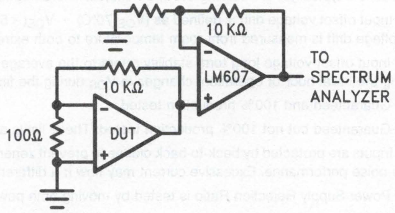

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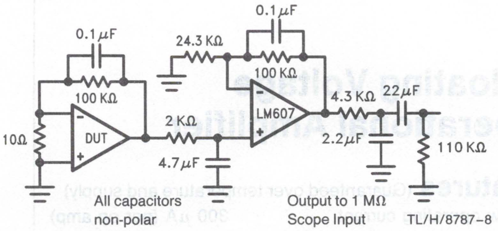
**FIGURE 5. Spot Noise Test Circuit**

The circuit used to measure peak-to-peak noise in the 0.1 to 10 Hz range is shown in *Figure 6*. The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, in addition to the single zero rolloff. The measuring equipment must be flat beyond this bandwidth. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.

## Application Hints (Continued)



All capacitors non-polar

Output to 1 MΩ Scope Input

TL/H/8787-8

Gain = 50,000

**FIGURE 6. 0.1 to 10 Hz Noise Test Circuit**

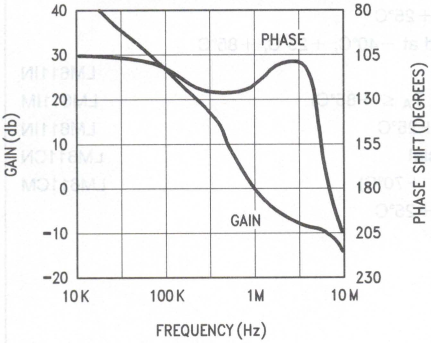
## Input Overdrive

The LM607's input-protection diodes prevent zener breakdown of the input transistors and the ensuing degradation of input DC parameters. Current limiting resistors have not been included as they would degrade input noise voltage. Input current should be limited to ±25 mA to avoid potential damage to the IC metallization.

In voltage follower applications, large input voltage steps may be coupled directly to the op amp's output via the protection diodes. If the input and feedback resistances are low in value, the output stage may be driven temporarily into current limit. The resulting output waveform exhibits an initial fast step when the diodes are conducting followed by a slight glitch as the amplifier comes out of current limit before true slewing is observed. For best results, use input and feedback resistors of 2 kΩ each in parallel with 30 pF capacitors. The capacitors eliminate input and feedback poles which respectively cause signal rolloff and instabilities.

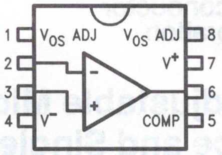
## Typical Performance Characteristics

### Gain and Phase vs. Frequency



TL/H/8787-9

### Top Views



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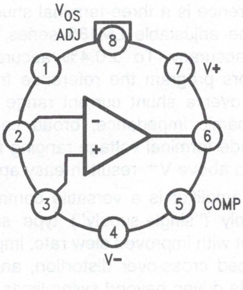
**Cerdip and Molded DIP**



TL/H/8787-11

**TO-99 Can**

## Order Information

| Package | Temperature Range | | NSC Drawing |
|---|---|---|---|
| | Military | Commercial | |
| TO-99 | LM607AMH<br>LM607BMH | LM607ACH<br>LM607BCH<br>LM607CH | H08C |
| 8-Pin Cerdip | LM607AMJ<br>LM607BMJ | LM607ACJ<br>LM607CJ<br>LM607CJ | J08A |
| 8-Pin Molded DIP | | LM607ACN<br>LM607BCN<br>LM607CN | N08E |
| 8-Pin SO | | LM607CM | M08A |

**National Semiconductor Corporation**

**ADVANCED INFORMATION**

# LM611 Adjustable Micropower Floating Voltage Reference and Single-Supply Operational Amplifier

## General Description

The voltage reference is a three-terminal shunt-type band-gap similar to the adjustable LM185 series, but with improved voltage accuracy. To ±0.4% accuracy by wafer trim. Two resistors program the reference from 1.24V to 6.3V. Operation over a shunt current range of 16 $\mu$A to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below $V^-$ to above $V^+$ result in easy application.

The operational amplifier is a versatile common-mode-to-the-negative-supply ("single-supply") type similar to the LM124 series, but with improved slew rate, improved power bandwidth, reduced cross-over distortion, and low supply current even while driven beyond swing limits. Lateral PNP input transistors enable low input currents for large differential input voltages and swings above $V^+$.

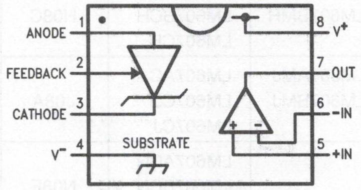
## Features (Guaranteed over temperature and supply)

| | |
|---|---|
| ■ Low operating current | 300 $\mu$A (per op amp)<br>16 $\mu$A (ref) |
| ■ Large supply voltage range | 3V to 36V |
| ■ Large output swing (10k load) | $(V^- + 1V)$ to $(V^+ - 1.8V)$ |
| ■ Input common-mode range includes | $V^-$ to $(V^+ - 1.4V)$ |
| ■ Op amps match LM124 pin-out | |
| ■ Wide input differential voltage | ±36V |
| ■ Reference voltage adjustable | 1.2V to 6.3V |
| ■ Reference initial tolerance | ±0.4% |
| ■ Reference temp. coefficient | ±20 ppm/°C |
| ■ Reference load capacitance | 0 to ∞ |
| ■ Cost effective | |

## Applications

- Power supplies
- Signal conditioning

## Connection Diagrams



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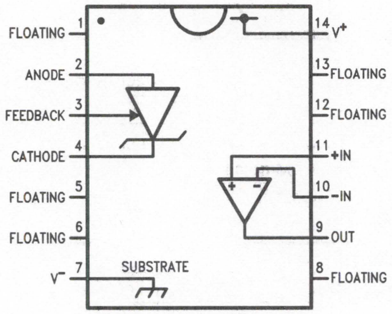
**Top View**

**See NS Package Number J08A or N08E**



TL/H/9221–2

**Top View**

**See NS Package Number M14A**

**M Narrow (0.15")**

## Order Number

| | |
|---|---|
| **Prime Military** | LM611MJ |
| $(-55°C \leq T_A \leq +125°C)$ | |
| tested at −55°C, +25°C, +125°C | |
| drift tested at −55°C, +25°C, +125°C | |
| **Prime Industrial** | LM611AIN |
| $(-40°C \leq T_A \leq +85°C)$ | |
| tested at +25°C | |
| drift tested at −40°C, +25°C, +85°C | |
| **Industrial** | LM611IN |
| $(-40°C \leq T_A \leq +85°C)$ | LM611IM |
| tested at +25°C | LM611IN |
| **Commercial** | LM611CN |
| $(0 \leq T_A \leq +70°C)$ | LM611CM |
| tested at +25°C | |

**National Semiconductor Corporation**

**ADVANCED INFORMATION**

# LM614 Adjustable Micropower Floating Voltage Reference and Four Single-Supply Operational Amplifiers

## General Description

The voltage reference is a three-terminal shunt-type design similar to the adjustable LM185 series, but with improved voltage tolerance and temperature coefficient. It is adjustable from 1.23 to 6.3V and operates over a wide shunt current range of 12 μA to 20 mA. Trimming provides accuracy to ±⅓%. The low dynamic impedance and wide capacitive load range result in easy application.

The four operational amplifiers are versatile single-supply types similar to the LM124 series, but with improved slew rate (0.8V/μs typ.) and power bandwidth, reduced crossover distortion, and low current consumption even while driven beyond swing limits.

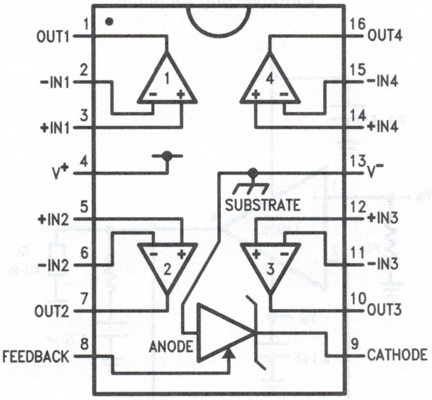
## Features

| | |
|---|---|
| ■ Low operating current | 185 μA (per op amp)<br>12 μA (reference) |
| ■ Wide supply voltage range | 3V to 36V |
| ■ Large output swing | ($V^-$ + 0.9V) to ($V^+$ − 1.7V) |
| ■ Input common-mode range includes | $V^-$ |
| ■ Reference voltage adjustable | 1.2V to 6.3V |
| ■ Reference initial tolerance | ±0.33% |
| ■ Reference temp coefficient | ±20 PPM/C |
| ■ Reference tolerant of capacitive loads | |

## Applications

- Instrumentation
- Switching power supplies
- Battery operated devices

## Connection Diagram



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**Top View**
**M Narrow (0.15″), N, or J**
**Order Number LM614M, LM614N or LM614J**
**See NS Package J16A, M16A or N16A**

## Order Number

| | |
|---|---|
| **Prime Military** | LM614MJ |
| (−55°C ≤ $T_A$ ≤ +125°C) | |
| tested at −55°C, +25°C, +125°C | |
| drift tested at −55°C, +25°C, +125°C | |
| **Prime Industrial** | LM614AIJ |
| (−40°C ≤ $T_A$ ≤ +85°C) | |
| tested at +25°C | |
| drift tested at −40°C, +25°C, +85°C | |
| **Industrial** | LM614IN |
| (−40°C ≤ $T_A$ ≤ +85°C) | LM614IJ |
| tested at +25°C | LM614IM |
| **Commercial** | LM614CN |
| (0°C ≤ $T_A$ ≤ +70°C) | LM614CM |
| tested at +25°C | |

**National Semiconductor Corporation**

**PRELIMINARY**

# LM675 Power Operational Amplifier

## General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

## Features

- 3A current capability
- $A_{VO}$ typicaly 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/µs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

## Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

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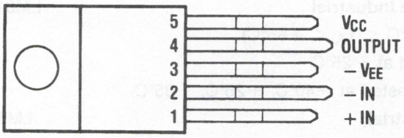
## Connection Diagram

**TO-220 Power Package (T)**



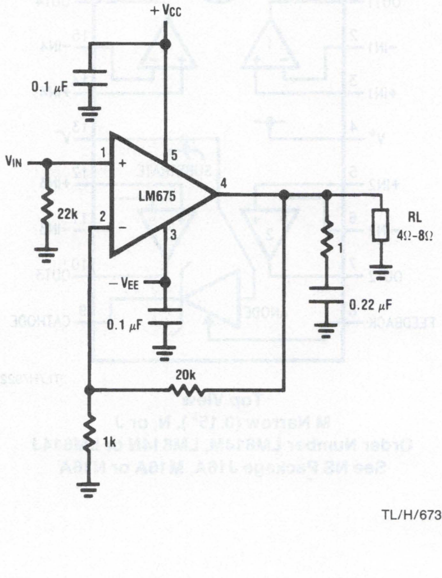
TL/H/6739–1

**Front View**

**Order Number LM675T**
**See NS Package T05B**

## Typical Applications

**Non-Inverting Amplifier**



TL/H/6739–2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±30V |
| Input Voltage | $-V_{EE}$ to $V_{CC}$ |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | −65°C to +150°C |
| Junction Temperature | 150°C |
| Power Dissipation (Note 1) | 30W |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

ESD rating to be determined.

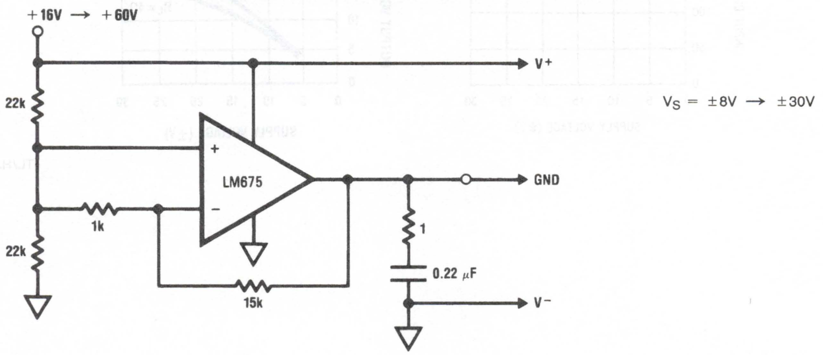
## Electrical Characteristics $V_S = \pm 25V$, $T_A = 25°C$ unless otherwise specified.

| Parameter | Conditions | Typical | Tested Limit | Units |
|---|---|---|---|---|
| Supply Current | $P_{OUT} = 0W$ | 18 | 50 (max) | mA |
| Input Offset Voltage | $V_{CM} = 0V$ | 1 | 10 (max) | mV |
| Input Bias Current | $V_{CM} = 0V$ | 0.2 | 2 (max) | μA |
| Input Offset Current | $V_{CM} = 0V$ | 50 | 500 (max) | nA |
| Open Loop Gain | $R_L = \infty\Omega$ | 90 | 70 (min) | dB |
| PSRR | $\Delta V_S = \pm 5V$ | 90 | 70 (min) | dB |
| CMRR | $V_{IN} = \pm 20V$ | 90 | 70 (min) | dB |
| Output Voltage Swing | $R_L = 8\Omega$ | ±21 | ±18 (min) | V |
| Offset Voltage Drift Versus Temperature | $R_S < 100\ k\Omega$ | 25 | | μV/°C |
| Offset Voltage Drift Versus Output Power | | 25 | | μV/W |
| Output Power | THD = 1%, $f_O = 1$ kHz, $R_L = 8\Omega$ | 25 | 20 | W |
| Gain Bandwidth Product | $f_O = 20$ kHz, $A_{VCL} = 1000$ | 5.5 | | MHz |
| Max Slew Rate | | 8 | | V/μs |
| Input Common Mode Range | | ±22 | ±20 (min) | V |

**Note 1:** Assumes $T_A$ equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

## Typical Applications (Continued)

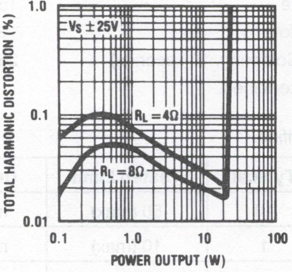
**Generating a Split Supply From a Single Supply**



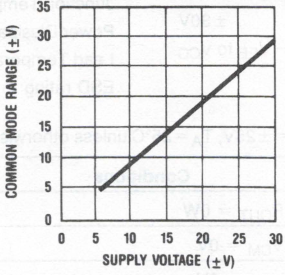
TL/H/6739-3

## Typical Performance Characteristics

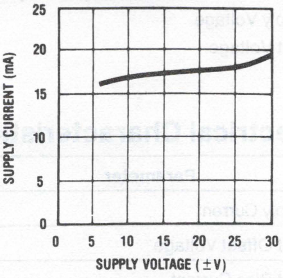
### THD vs Power Output



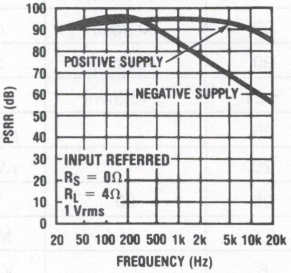
### Input Common Mode Range vs Supply Voltage



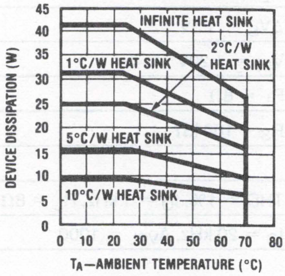
### Supply Current vs Supply Voltage



### PSRR vs Frequency

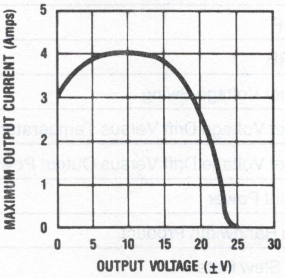


### Device Dissipation vs Ambient Temperature†



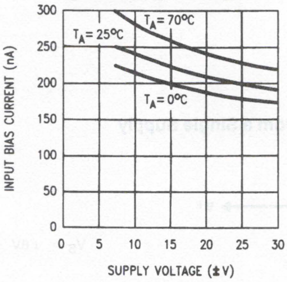
†θ INTERFACE = 1° C/W.
See Application Hints.

### Current Limit vs Output Voltage*

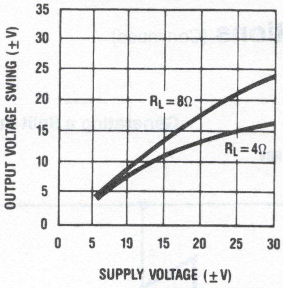


*VS = ±25V

### IB vs Supply Voltage



### Output Voltage Swing vs Supply Voltage



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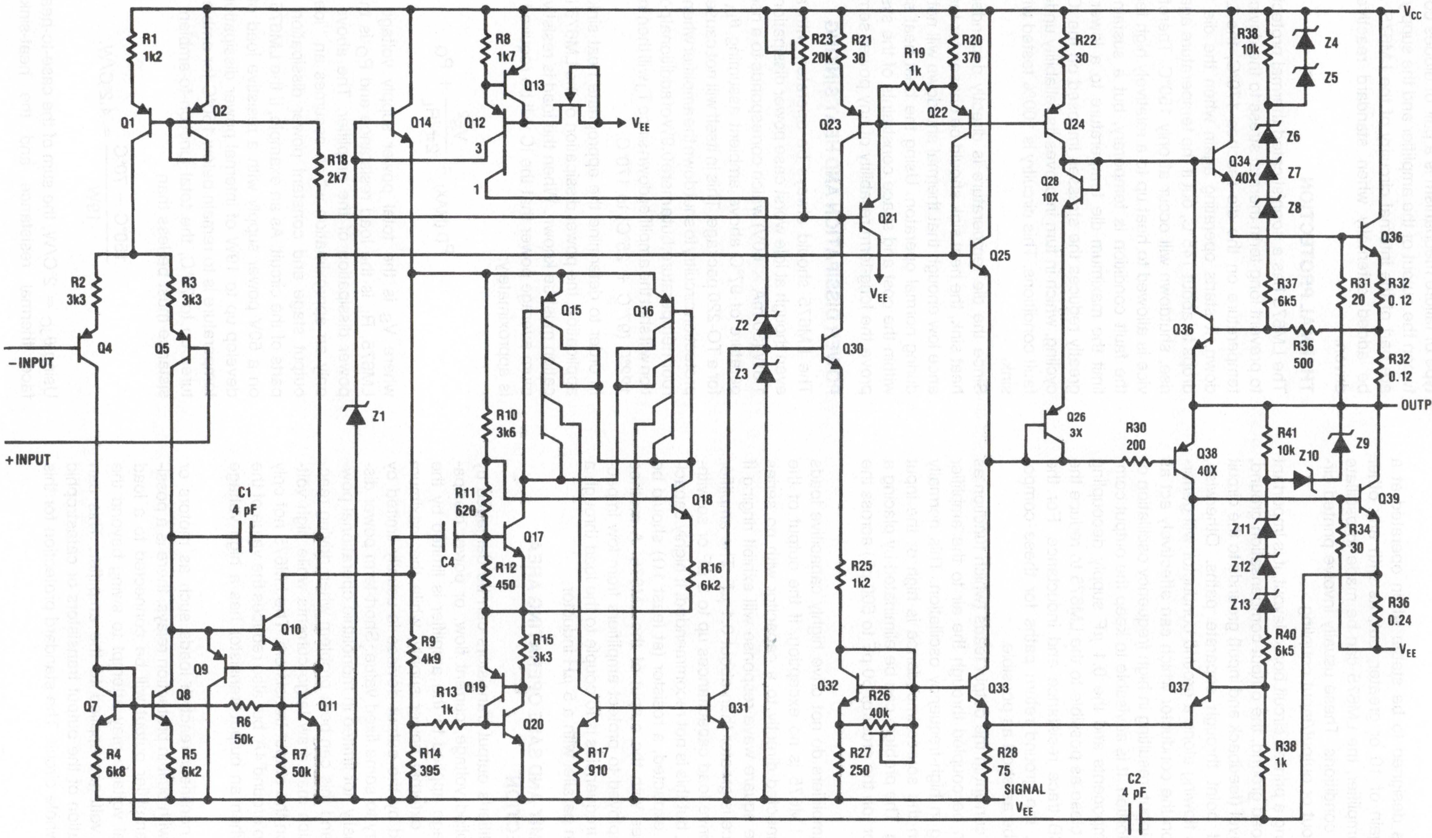
## Schematic Diagram


VCC
VEE
OUTPUT
−INPUT
+INPUT
SIGNAL VEE
R1 1k2
R2 3k3
R3 3k3
R4 6k8
R5 6k2
R6 50k
R7 50k
R8 1k7
R9 4k9
R10 3k6
R11 620
R12 450
R13 1k
R14 395
R15 3k3
R16 6k2
R17 910
R18 2k7
R19 1k
R20 370
R21 30
R22 30
R23 20K
R25 1k2
R26 40k
R27 250
R28 75
R30 200
R31 20
R32 0.12
R32 0.12
R34 30
R36 500
R36 0.24
R37 6k5
R38 10k
R38 1k
R40 6k5
R41 10k
C1 4 pF
C2 4 pF
C4
Q1
Q2
Q4
Q5
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26 3X
Q28 10X
Q30
Q31
Q32
Q33
Q34 40X
Q36
Q36
Q37
Q38 40X
Q39
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
Z13
1
3

TL/H/6739-5

# Application Hints

### STABILITY

The LM675 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM675 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a printed circuit board layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM675 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM675 is no exception. If the output of the LM675 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM675. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

### CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic operational power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM675 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM675, and needn't be added externally when standard reactive loads are driven.

### THERMAL PROTECTION

The LM675 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM675 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. This circuitry is 100% tested without a heat sink.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operaton. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor.

### POWER DISSIPATION AND HEAT SINKING

The LM675 should always be operated with a heat sink, even though at idle worst case power dissipation will be only 1.8W (30 mA × 60V) which corresponds to a rise in die temperature of 97°C above ambient assuming $\theta_{jA} = 54°C/W$ for a TO-220 package. This in itself will not cause the thermal protection circuitry to shut down the amplifier when operating at room temperature, but a mere 0.9W of additional power dissipation will shut the amplifier down since $T_J$ will then increase from 122°C (97°C + 25°C) to 170°C.

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM675 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D\,(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where $V_S$ is the total power supply voltage across the LM675, $R_L$ is the load resistance and $P_Q$ is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. As an example, if the LM675 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat sink interface thermal resistance and the heat-sink-to-ambient

## Application Hints (Continued)

thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

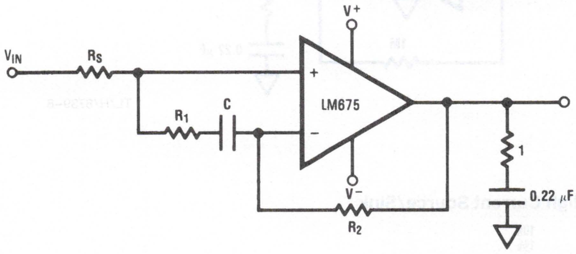
$$4.2°\text{C/W} - 2°\text{C/W} - 1.6°\text{C/W} = 0.6°\text{C/W}.$$

This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be restricted to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load will be roughly that of the same amplifier driving the resistive part of that load. For example, some reactive loads may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 8Ω × cos 60° or 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

## Typical Applications (Continued)

### Non-Inverting Unity Gain Operation



$$R_1C \geq \frac{1}{2\pi 500\ \text{kHz}}$$

$$R_1 \leq \frac{R_S + R_2}{10}$$

$$A_{V(DC)} = 1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

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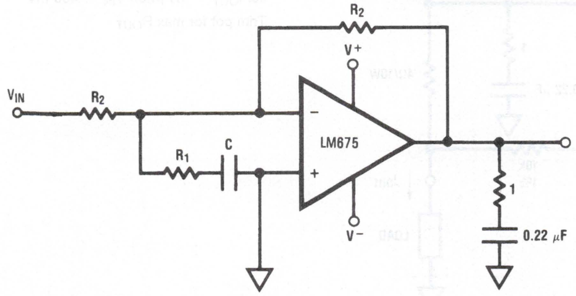
### Inverting Unity Gain Operation



$$R_1C \geq \frac{1}{2\pi 500\ \text{kHz}}$$

$$R_1 \leq \frac{R_2}{10}$$

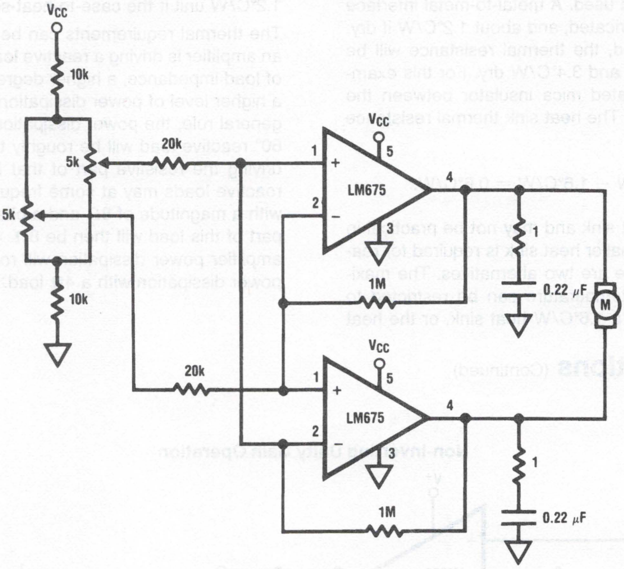
$$A_{V(DC)} = -1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

TL/H/6739-7

## Typical Applications (Continued)

### Servo Motor Control


VCC
10k
5k
20k
5k
10k
20k
1
+
2
−
LM675
5
VCC
4
3
1
0.22 µF
M
1M
1
+
2
−
LM675
5
VCC
4
3
1
0.22 µF
1M

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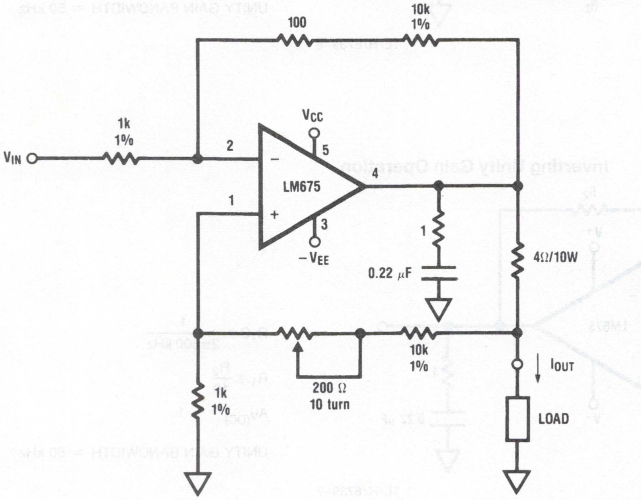
### High Current Source/Sink


100
10k
1%
VIN
1k
1%
2
−
1
+
LM675
VCC
5
4
3
− VEE
1
0.22 µF
4Ω/10W
200 Ω
10 turn
10k
1%
1k
1%
IOUT
LOAD

$I_{OUT} = V_{IN} \times 2.5$ amps/volt

i.e. $I_{OUT} = 1A$ when $V_{IN} = 400$ mV

Trim pot for max $R_{OUT}$

TL/H/6739-9

National Semiconductor Corporation

# LM741/LM741A/LM741C/LM741E Operational Amplifier

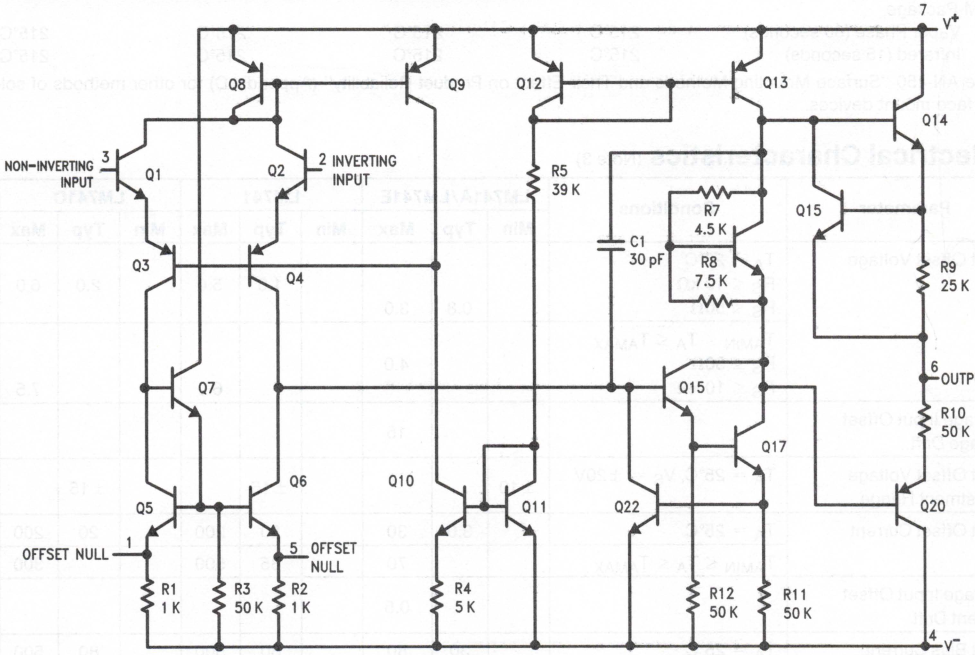
## General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

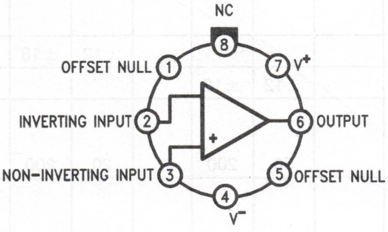
## Schematic and Connection Diagrams (Top Views)



7 V+
Q8
Q9
Q12
Q13
Q14
3 NON-INVERTING INPUT
Q1
Q2
2 INVERTING INPUT
R5 39 K
R7 4.5 K
Q15
C1 30 pF
R8 7.5 K
R9 25 K
Q3
Q4
Q7
Q15
6 OUTPUT
R10 50 K
Q17
Q5
Q6
Q10
Q11
Q22
Q20
1 OFFSET NULL
5 OFFSET NULL
R1 1 K
R3 50 K
R2 1 K
R4 5 K
R12 50 K
R11 50 K
4 V−

TL/H/9341-1

**Metal Can Package**

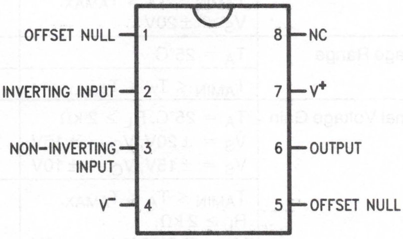


NC
8
OFFSET NULL 1
7 V+
INVERTING INPUT 2
6 OUTPUT
NON-INVERTING INPUT 3
5 OFFSET NULL
4
V−

TL/H/9341-2

**Order Number LM741H, LM741AH, LM741CH or LM741EH**
**See NS Package Number H08C**

**Dual-In-Line or S.O. Package**



OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V− 4
8 NC
7 V+
6 OUTPUT
5 OFFSET NULL

TL/H/9341-3

**Order Number LM741CJ, LM741CM, LM741CN or LM741EN**
**See NS Package Number J08A, M08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 5)**

| | LM741A | LM741E | LM741 | LM741C |
|---|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±22V | ±18V |
| Power Dissipation (Note 1) | 500 mW | 500 mW | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V | ±30V | ±30V |
| Input Voltage (Note 2) | ±15V | ±15V | ±15V | ±15V |
| Output Short Circuit Duration | Indefinite | Indefinite | Indefinite | Indefinite |
| Operating Temperature Range | −55°C to +125°C | 0°C to +70°C | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Junction Temperature | 150°C | 100°C | 150°C | 100°C |
| Soldering Information | | | | |
| N-Package (10 seconds) | 260°C | 260°C | 260°C | 260°C |
| J- or H-Package (10 seconds) | 300°C | 300°C | 300°C | 300°C |
| M-Package | | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 215°C | 215°C | 215°C | 215°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM741A/LM741E | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | | | | | | | | | |
| | $R_S \leq 10\ k\Omega$ | | | | | 1.0 | 5.0 | | 2.0 | 6.0 | mV |
| | $R_S \leq 50\Omega$ | | 0.8 | 3.0 | | | | | | | mV |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | | | | | | | |
| | $R_S \leq 50\Omega$ | | | 4.0 | | | | | | | mV |
| | $R_S \leq 10\ k\Omega$ | | | | | | 6.0 | | | 7.5 | mV |
| Average Input Offset Voltage Drift | | | | 15 | | | | | | | μV/°C |
| Input Offset Voltage Adjustment Range | $T_A = 25°C, V_S = \pm 20V$ | ±10 | | | | ±15 | | | ±15 | | mV |
| Input Offset Current | $T_A = 25°C$ | | 3.0 | 30 | | 20 | 200 | | 20 | 200 | nA |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | 70 | | 85 | 500 | | | 300 | nA |
| Average Input Offset Current Drift | | | | 0.5 | | | | | | | nA/°C |
| Input Bias Current | $T_A = 25°C$ | | 30 | 80 | | 80 | 500 | | 80 | 500 | nA |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | 0.210 | | | 1.5 | | | 0.8 | μA |
| Input Resistance | $T_A = 25°C, V_S = \pm 20V$ | 1.0 | 6.0 | | 0.3 | 2.0 | | 0.3 | 2.0 | | MΩ |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ | 0.5 | | | | | | | | | MΩ |
| Input Voltage Range | $T_A = 25°C$ | | | | | | | ±12 | ±13 | | V |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | ±12 | ±13 | | | | | V |
| Large Signal Voltage Gain | $T_A = 25°C, R_L \geq 2\ k\Omega$ | | | | | | | | | | |
| | $V_S = \pm 20V, V_O = \pm 15V$ | 50 | | | | | | | | | V/mV |
| | $V_S = \pm 15V, V_O = \pm 10V$ | | | | 50 | 200 | | 20 | 200 | | V/mV |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\ k\Omega$, | | | | | | | | | | |
| | $V_S = \pm 20V, V_O = \pm 15V$ | 32 | | | | | | | | | V/mV |
| | $V_S = \pm 15V, V_O = \pm 10V$ | | | | 25 | | | 15 | | | V/mV |
| | $V_S = \pm 5V, V_O = \pm 2V$ | 10 | | | | | | | | | V/mV |

## Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM741A/LM741E | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage Swing | $V_S = \pm 20V$ | | | | | | | | | | |
| | $R_L \geq 10\ k\Omega$ | ±16 | | | | | | | | | V |
| | $R_L \geq 2\ k\Omega$ | ±15 | | | | | | | | | V |
| | $V_S = \pm 15V$ | | | | | | | | | | |
| | $R_L \geq 10\ k\Omega$ | | | | ±12 | ±14 | | ±12 | ±14 | | V |
| | $R_L \geq 2\ k\Omega$ | | | | ±10 | ±13 | | ±10 | ±13 | | V |
| Output Short Circuit Current | $T_A = 25°C$ | 10 | 25 | 35 | | 25 | | | 25 | | mA |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | 10 | | 40 | | | | | | | mA |
| Common-Mode Rejection Ratio | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | | | | | | | |
| | $R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$ | | | | 70 | 90 | | 70 | 90 | | dB |
| | $R_S \leq 50\ k\Omega$, $V_{CM} = \pm 12V$ | 80 | 95 | | | | | | | | dB |
| Supply Voltage Rejection Ratio | $T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$ | | | | | | | | | | |
| | $R_S \leq 50\Omega$ | 86 | 96 | | | | | | | | dB |
| | $R_S \leq 10\ k\Omega$ | | | | 77 | 96 | | 77 | 96 | | dB |
| Transient Response | $T_A = 25°C$, Unity Gain | | | | | | | | | | |
| Rise Time | | | 0.25 | 0.8 | | 0.3 | | | 0.3 | | µs |
| Overshoot | | | 6.0 | 20 | | 5 | | | 5 | | % |
| Bandwidth (Note 4) | $T_A = 25°C$ | 0.437 | 1.5 | | | | | | | | MHz |
| Slew Rate | $T_A = 25°C$, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/µs |
| Supply Current | $T_A = 25°C$ | | | | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| Power Consumption | $T_A = 25°C$ | | | | | | | | | | |
| | $V_S = \pm 20V$ | | 80 | 150 | | | | | | | mW |
| | $V_S = \pm 15V$ | | | | | 50 | 85 | | 50 | 85 | mW |
| LM741A | $V_S = \pm 20V$ | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | 165 | | | | | | | mW |
| | $T_A = T_{AMAX}$ | | | 135 | | | | | | | mW |
| LM741E | $V_S = \pm 20V$ | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | 150 | | | | | | | mW |
| | $T_A = T_{AMAX}$ | | | 150 | | | | | | | mW |
| LM741 | $V_S = \pm 15V$ | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | | | 60 | 100 | | | | mW |
| | $T_A = T_{AMAX}$ | | | | | 45 | 75 | | | | mW |

**Note 1:** For operation at elevated temperatures, these devices must be derated based on thermal resistance, and $T_j$ max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

| Thermal Resistance | Cerdip (J) | DIP (N) | TO-5 (H) | SO-8 (M) |
|---|---|---|---|---|
| $\theta_{jA}$ (Junction to Ambient) | 100°C/W | 100°C/W | 150°C/W | 195°C/W |
| $\theta_{jC}$ (Junction to Case) | N/A | N/A | 80°C/W | N/A |

**Note 2:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

**Note 4:** Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

**Note 5:** For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

**National Semiconductor Corporation**

**PRELIMINARY**

# LM833 Dual Audio Operational Amplifier

## General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

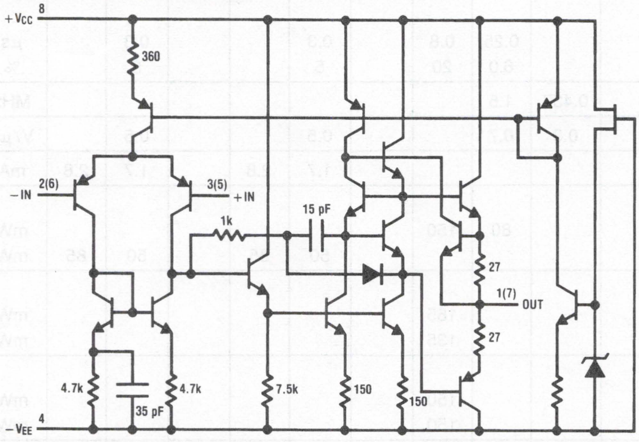
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

## Features

| | |
|---|---|
| ■ Wide dynamic range | >140 dB |
| ■ Low input noise voltage | 4.5 nV/$\sqrt{\text{Hz}}$ |
| ■ High slew rate | 7 V/$\mu$s (typ)<br>5 V/$\mu$s (min) |
| ■ High gain bandwidth product | 15 MHz (typ)<br>10 MHz (min) |
| ■ Wide power bandwidth | 120 kHz |
| ■ Low distortion | 0.002% |
| ■ Low offset voltage | 0.3 mV |
| ■ Large phase margin | 60° |

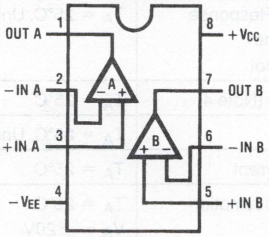
## Schematic Diagram (1/2 LM833)



+VCC
8
360
−IN
2(6)
3(5)
+IN
1k
15 pF
27
1(7)
OUT
27
4.7k
35 pF
4.7k
7.5k
150
150
−VEE
4

TL/H/5218-1

## Connection Diagram

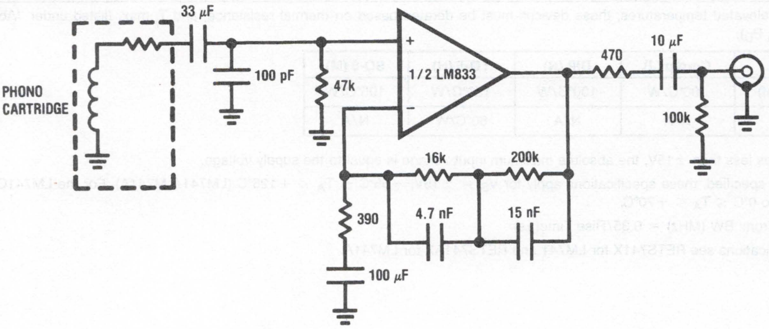


OUT A
1
8
+VCC
−IN A
2
A
7
OUT B
+IN A
3
B
6
−IN B
−VEE
4
5
+IN B

TL/H/5218-2

**Order Number LM833M or LM833N**
**See NS Package Number**
**M08A or N08E**

## Typical Application RIAA Preamp



33 μF
PHONO CARTRIDGE
100 pF
47k
1/2 LM833
470
10 μF
100k
16k
200k
390
4.7 nF
15 nF
100 μF

TL/H/5218-3

$A_V = 35$ dB f = 1 kHz
$E_n = 0.33\ \mu V$ A Weighted
S/N = 90 dB A Weighted, $V_{IN} = 10$ mV
@ f = 1 kHz

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | | |
|---|---|---|
| Supply Voltage | $V_{CC}$–$V_{EE}$ | 36V |
| Differential Input Voltage (Note 1) | $V_{ID}$ | ±30V |
| Input Voltage Range (Note 1) | $V_{IC}$ | ±15V |
| Power Dissipation (Note 2) | $P_D$ | 500 mW |
| Operating Temperature Range | $T_{OPR}$ | −40 ~ 85°C |
| Storage Temperature Range | $T_{STG}$ | −60 ~ 150°C |

Soldering Information

| | |
|---|---|
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## DC Electrical Characteristics ($T_A = 25°C, V_S = \pm 15V$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\Omega$ | | 0.3 | 5 | mV |
| $I_{OS}$ | Input Offset Current | | | 10 | 200 | nA |
| $I_B$ | Input Bias Current | | | 500 | 1000 | nA |
| $A_V$ | Voltage Gain | $R_L = 2\ k\Omega, V_O = \pm 10V$ | 90 | 110 | | dB |
| $V_{OM}$ | Output Voltage Swing | $R_L = 10\ k\Omega$<br>$R_L = 2\ k\Omega$ | ±12<br>±10 | ±13.5<br>±13.4 | | V<br>V |
| $V_{CM}$ | Input Common-Mode Range | | ±12 | ±14.0 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{IN} = \pm 12V$ | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = 15 \sim 5V, -15 \sim -5V$ | 80 | 100 | | dB |
| $I_Q$ | Supply Current | $V_O = 0V$, Both Amps | | 5 | 8 | mA |

## AC Electrical Characteristics ($T_A = 25°C, V_S = \pm 15V, R_L = 2\ k\Omega$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | $R_L = 2\ k\Omega$ | 5 | 7 | | V/µs |
| GBW | Gain Bandwidth Product | f = 100 kHz | 10 | 15 | | MHz |

## Design Electrical Characteristics ($T_A = 25°C, V_S = \pm 15V$)

The following parameters are not tested or guaranteed.

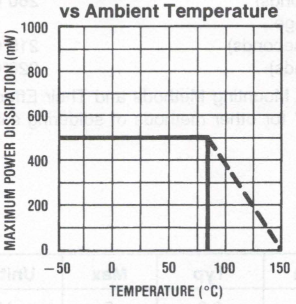
| Symbol | Parameter | Conditions | Typ | Units |
|---|---|---|---|---|
| $\Delta V_{OS}/\Delta T$ | Average Temperature Coefficient of Input Offset Voltage | | 2 | µV/°C |
| THD | Distortion | $R_L = 2\ k\Omega$, f = 20 ~ 20 kHz<br>$V_{OUT} = 3$ Vrms, $A_V = 1$ | 0.002 | % |
| $e_n$ | Input Referred Noise Voltage | $R_S = 100\Omega$, f = 1 kHz | 4.5 | nV/√Hz |
| $i_n$ | Input Referred Noise Current | f = 1 kHz | 0.7 | pA/√Hz |
| PBW | Power Bandwidth | $V_O = 27\ V_{pp}, R_L = 2\ k\Omega$, THD ≤ 1% | 120 | kHz |
| $f_U$ | Unity Gain Frequency | Open Loop | 9 | MHz |
| $\phi_M$ | Phase Margin | Open Loop | 60 | deg |
| | Input Referred Cross Talk | f = 20 ~ 20 kHz | −120 | dB |

**Note 1:** If supply voltage is less than ±15V, it is equal to supply voltage.

**Note 2:** This is the permissible value at $T_A \le 85°C$.

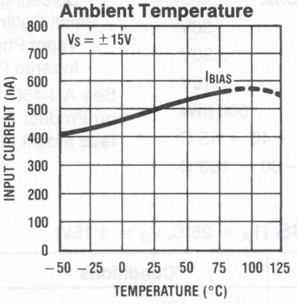
# Typical Performance Characteristics

**Maximum Power Dissipation vs Ambient Temperature**



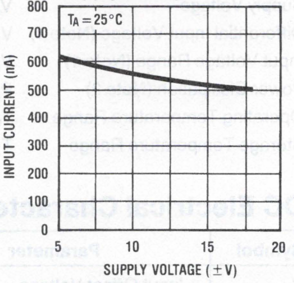
TL/H/5218–4

**Input Bias Current vs Ambient Temperature**



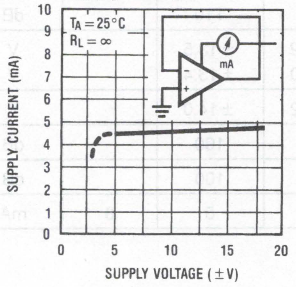
TL/H/5218–5

**Input Bias Current vs Supply Voltage**



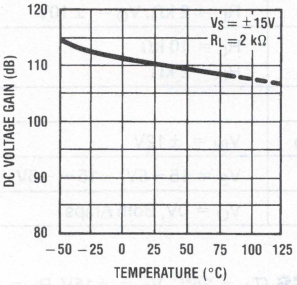
TL/H/5218–6

**Supply Current vs Supply Voltage**



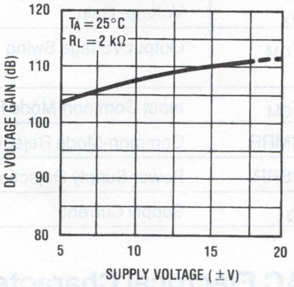
TL/H/5218–7

**DC Voltage Gain vs Ambient Temperature**



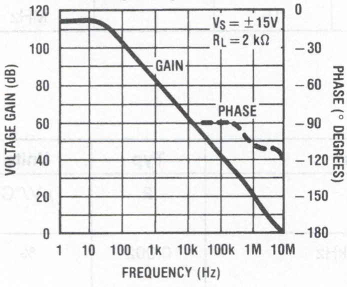
TL/H/5218–8

**DC Voltage Gain vs Supply Voltage**



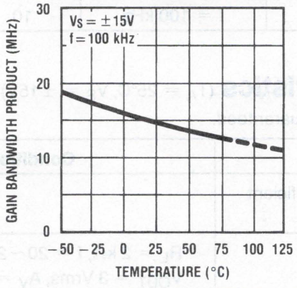
TL/H/5218–9

**Voltage Gain & Phase vs Frequency**



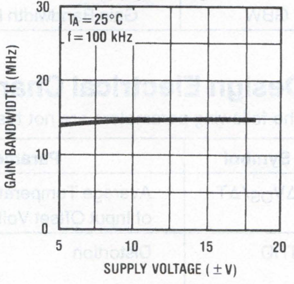
TL/H/5218–10

**Gain Bandwidth Product vs Ambient Temperature**



TL/H/5218–11

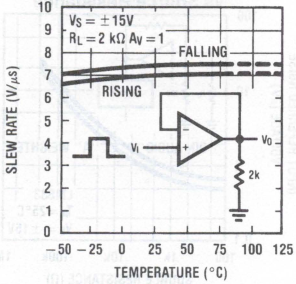
**Gain Bandwidth vs Supply Voltage**



TL/H/5218–12

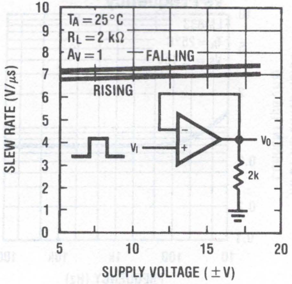
## Typical Performance Characteristics (Continued)

**Slew Rate vs Ambient Temperature**



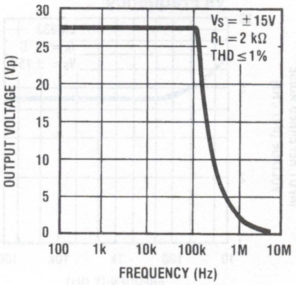
TL/H/5218–13

**Slew Rate vs Supply Voltage**



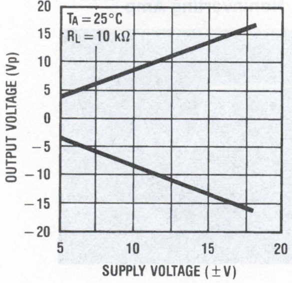
TL/H/5218–14

**Power Bandwidth**



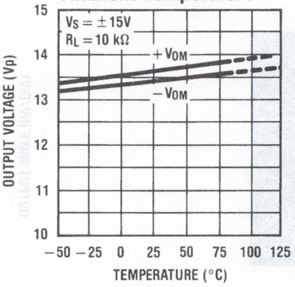
TL/H/5218–15

**Maximum Output Voltage vs Supply Voltage**



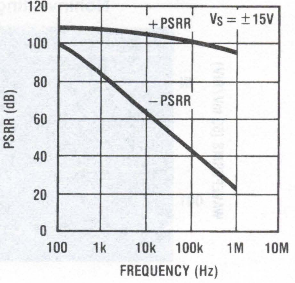
TL/H/5218–16

**Maximum Output Voltage vs Ambient Temperature**



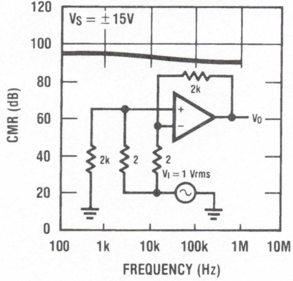
TL/H/5218–17

**PSRR vs Frequency**



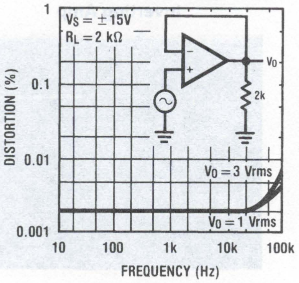
TL/H/5218–18

**CMR vs Frequency**



TL/H/5218–19

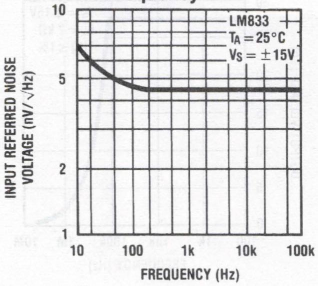
**Distortion vs Frequency**



TL/H/5218–20

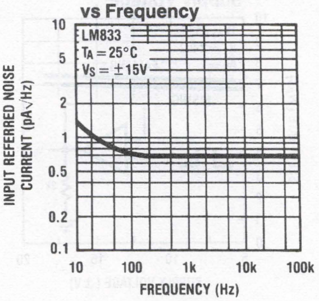
## Typical Performance Characteristics (Continued)

**Spot Noise Voltage vs Frequency**



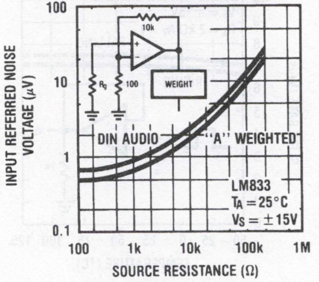
TL/H/5218–21

**Spot Noise Current vs Frequency**



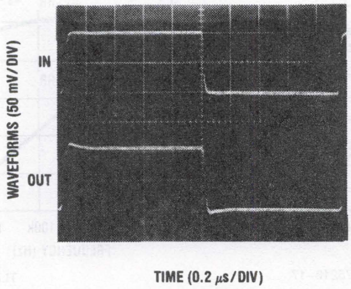
TL/H/5218–22

**Input Referred Noise Voltage vs Source Resistance**



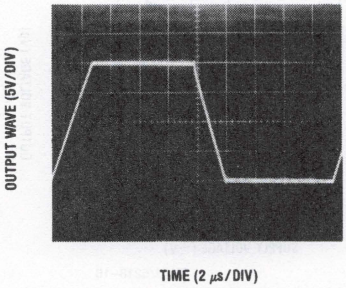
TL/H/5218–23

**Noninverting Amp**



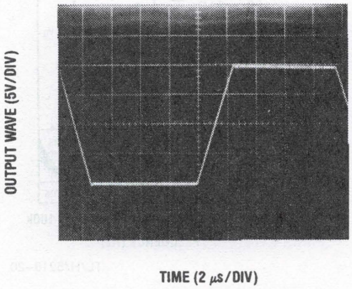
TL/H/5218–24

**Noninverting Amp**



TL/H/5218–25

**Inverting Amp**



TL/H/5218–26

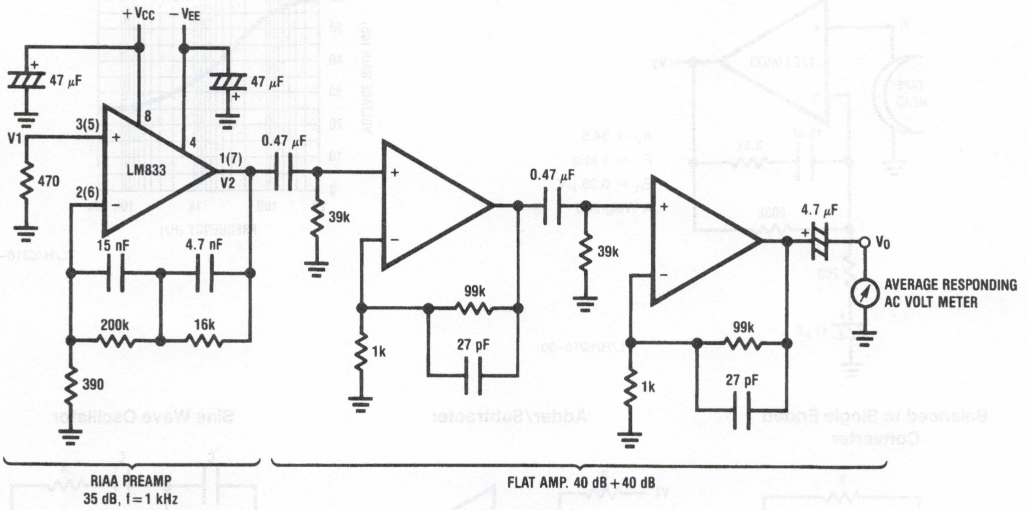
## Application Hints

The LM833 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

# Noise Measurement Circuit

Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.

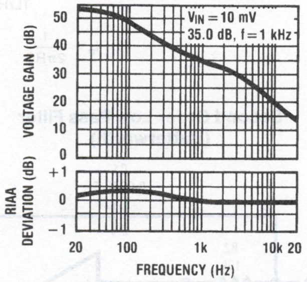

+VCC
−VEE
+
47 µF
47 µF
+
3(5)
V1
8
4
+
LM833
−
470
2(6)
1(7)
V2
0.47 µF
39k
+
−
0.47 µF
39k
+
−
4.7 µF
+
Vo
AVERAGE RESPONDING
AC VOLT METER
15 nF
4.7 nF
200k
16k
390
99k
1k
27 pF
99k
1k
27 pF
RIAA PREAMP
35 dB, f = 1 kHz
FLAT AMP. 40 dB + 40 dB

TL/H/5218-27

**Total Gain: 115 dB @f = 1 kHz**

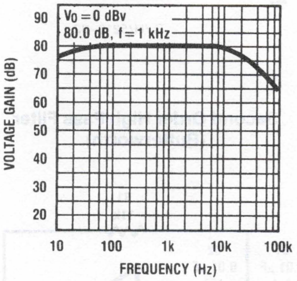
**Input Referred Noise Voltage: $e_n$ = V0/560,000 (V)**

**RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency**



TL/H/5218-28

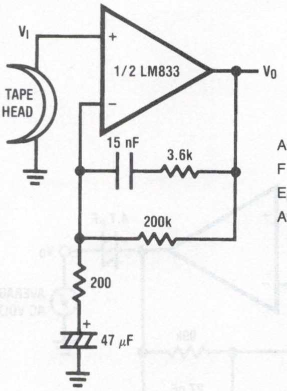
**Flat Amp Voltage Gain vs Frequency**



TL/H/5218-29

# Typical Applications

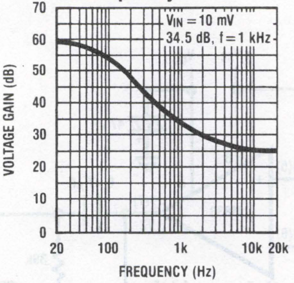
### NAB Preamp


V$_I$
TAPE HEAD
+
−
1/2 LM833
V$_O$
15 nF
3.6k
200k
200
+
47 μF

$A_V = 34.5$
$F = 1$ kHz
$E_n = 0.38\ \mu V$
A Weighted

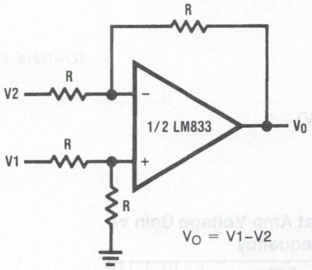
TL/H/5218-30

### NAB Preamp Voltage Gain vs Frequency



TL/H/5218-31

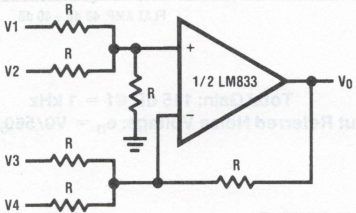
### Balanced to Single Ended Converter


R
V2
R
−
1/2 LM833
V$_O$
V1
R
+
R

$V_O = V1 - V2$

TL/H/5218-32

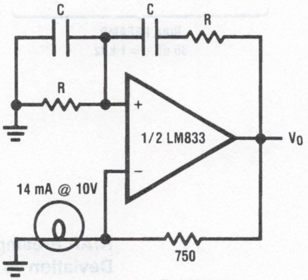
### Adder/Subtracter


V1
R
V2
R
R
+
1/2 LM833
V$_O$
V3
R
V4
R
R

$V_O = V1 + V2 - V3 - V4$

TL/H/5218-33

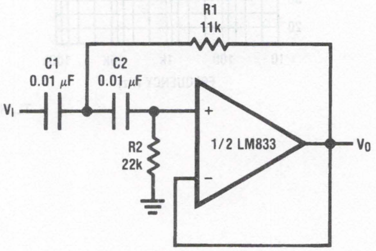
### Sine Wave Oscillator


C
C
R
R
+
1/2 LM833
V$_O$
−
14 mA @ 10V
750

TL/H/5218-34

$$f_O = \frac{1}{2\pi RC}$$

### Second Order High Pass Filter (Butterworth)


R1
11k
C1
0.01 μF
C2
0.01 μF
V$_I$
+
R2
22k
1/2 LM833
V$_O$
−

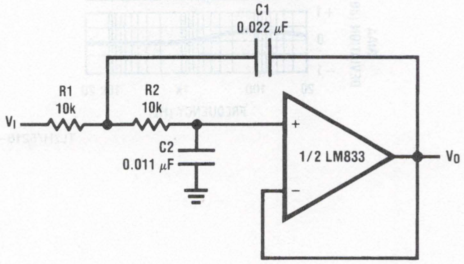
TL/H/5218-35

if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1
Illustration is $f_O = 1$ kHz

### Second Order Low Pass Filter (Butterworth)


C1
0.022 μF
R1
10k
R2
10k
V$_I$
+
C2
0.011 μF
1/2 LM833
V$_O$
−

TL/H/5218-36

if R1 = R2 = R

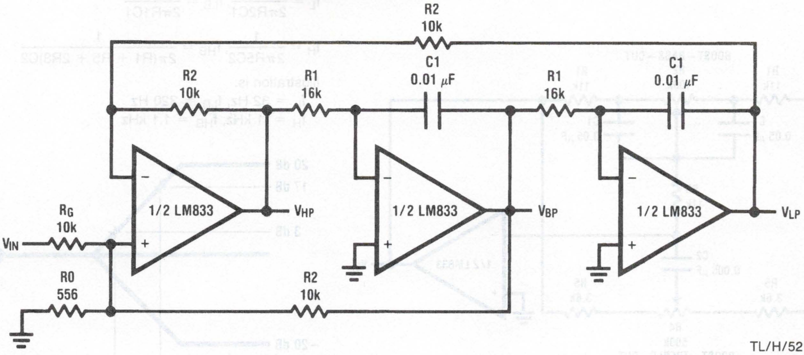
$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is $f_O = 1$ kHz

## Typical Applications (Continued)

### State Variable Filter

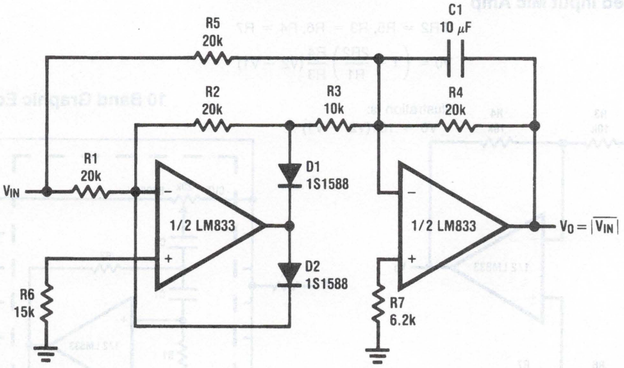

R2
10k
R2
10k
R1
16k
C1
0.01 μF
R1
16k
C1
0.01 μF
RG
10k
VIN
1/2 LM833
VHP
1/2 LM833
VBP
1/2 LM833
VLP
R0
556
R2
10k

TL/H/5218-37

$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

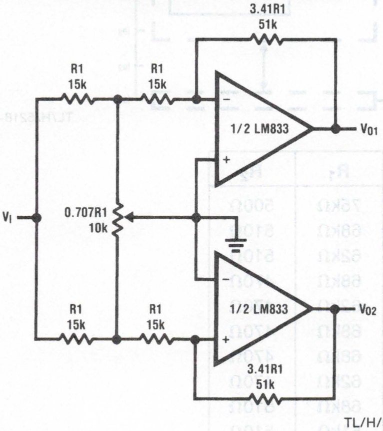
Illustration is $f_0 = 1$ kHz, $Q = 10$, $A_{BP} = 1$

### AC/DC Converter


R5
20k
C1
10 μF
R2
20k
R3
10k
R4
20k
R1
20k
VIN
D1
1S1588
D2
1S1588
1/2 LM833
1/2 LM833
V0 = |VIN|
R6
15k
R7
6.2k

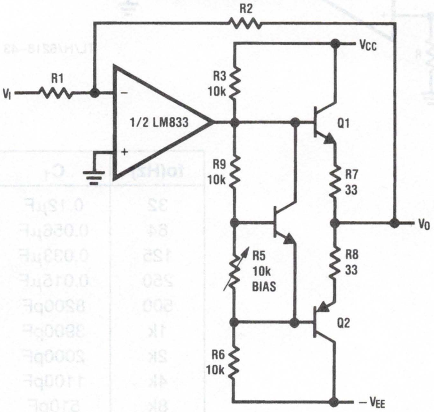
TL/H/5218-38

### 2 Channel Panning Circuit (Pan Pot)


3.41R1
51k
R1
15k
R1
15k
1/2 LM833
VO1
VI
0.707R1
10k
R1
15k
R1
15k
1/2 LM833
VO2
3.41R1
51k

TL/H/5218-39

### Line Driver


R2
VCC
R1
VI
R3
10k
1/2 LM833
Q1
R9
10k
R7
33
VO
R5
10k
BIAS
R8
33
Q2
R6
10k
−VEE

TL/H/5218-40

## Typical Application (Continued)

### Tone Control

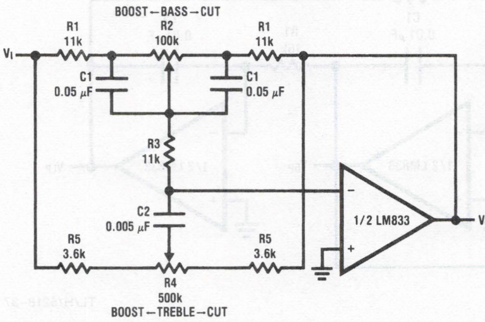
$$f_L = \frac{1}{2\pi R2C1}, \; f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2}, \; f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

Illustration is:

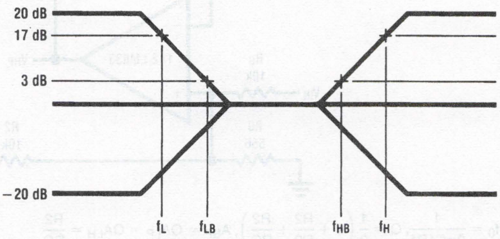
$f_L = 32$ Hz, $f_{LB} = 320$ Hz

$f_H = 11$ kHz, $f_{HB} = 1.1$ kHz



Vi
BOOST←BASS→CUT
R1 11k
R2 100k
R1 11k
C1 0.05 μF
C1 0.05 μF
R3 11k
C2 0.005 μF
R5 3.6k
R5 3.6k
R4 500k
BOOST←TREBLE→CUT
1/2 LM833
Vo

TL/H/5218-41



TL/H/5218-42

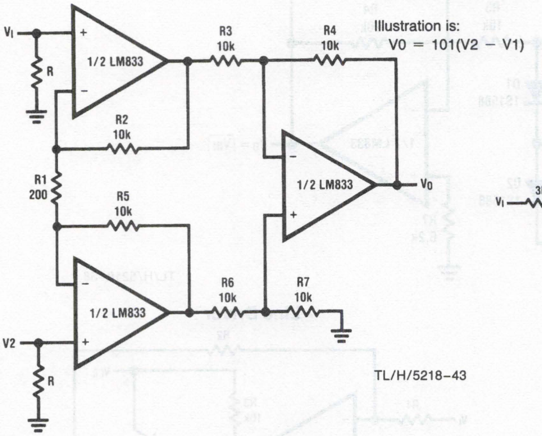
### Balanced Input Mic Amp

If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

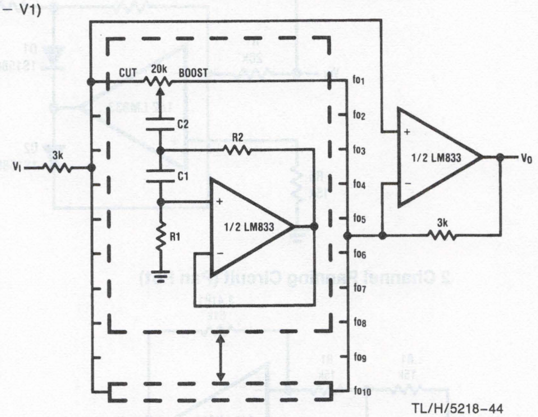
V0 = 101(V2 − V1)



VI
R
1/2 LM833
R3 10k
R4 10k
R2 10k
R1 200
R5 10k
1/2 LM833
Vo
1/2 LM833
R6 10k
R7 10k
V2
R

TL/H/5218-43

### 10 Band Graphic Equalizer



CUT
20k
BOOST
C2
C1
R2
R1
3k
Vi
1/2 LM833
fo1
fo2
fo3
fo4
fo5
fo6
fo7
fo8
fo9
fo10
1/2 LM833
Vo
3k

TL/H/5218-44

| fo(Hz) | $C_1$ | $C_2$ | $R_1$ | $R_2$ |
|---|---|---|---|---|
| 32 | 0.12μF | 4.7μF | 75kΩ | 500Ω |
| 64 | 0.056μF | 3.3μF | 68kΩ | 510Ω |
| 125 | 0.033μF | 1.5μF | 62kΩ | 510Ω |
| 250 | 0.015μF | 0.82μF | 68kΩ | 470Ω |
| 500 | 8200pF | 0.39μF | 62kΩ | 470Ω |
| 1k | 3900pF | 0.22μF | 68kΩ | 470Ω |
| 2k | 2000pF | 0.1μF | 68kΩ | 470Ω |
| 4k | 1100pF | 0.056μF | 62kΩ | 470Ω |
| 8k | 510pF | 0.022μF | 68kΩ | 510Ω |
| 16k | 330pF | 0.012μF | 51kΩ | 510Ω |

At volume of change = ±12 dB

Q = 1.7

Reference: "AUDIO/RADIO HANDBOOK", National Semiconductor, 1980, Page 2-61

**National Semiconductor Corporation**

**PRELIMINARY**

# LM837 Low Noise Quad Operational Amplifier

## General Description

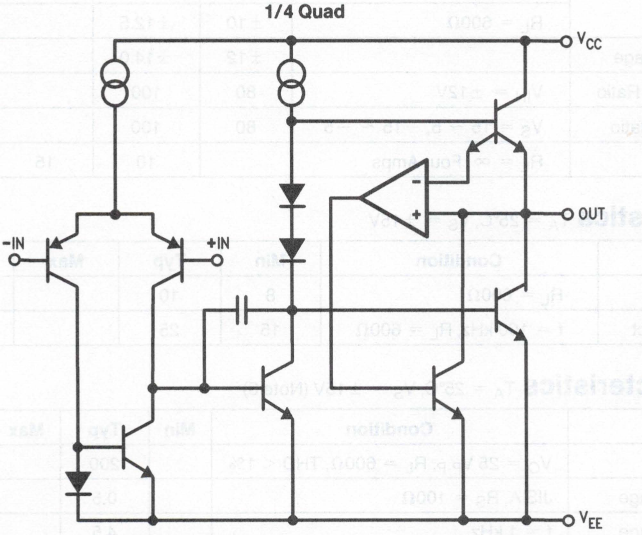
The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and therefore can be used to upgrade existing systems with little or no change.

## Features

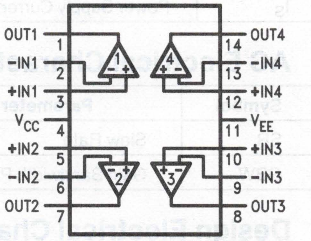
| | |
|---|---|
| ■ High slew rate | 10 V/µs (typ)<br>8 V/µs (min) |
| ■ Wide gain bandwidth product | 25 MHz (typ)<br>15 MHz (min) |
| ■ Power bandwidth | 200 kHz (typ) |
| ■ High output current | ±40 mA |
| ■ Excellent output drive performance | >600Ω |
| ■ Low input noise voltage | 4.5 nV/$\sqrt{\text{Hz}}$ |
| ■ Low total harmonic distortion | 0.0015% |
| ■ Low offset voltage | 0.3 mV |

## Schematic and Connection Diagrams



TL/H/9047-1

**Dual-In-Line Package**



TL/H/9047-2

**Top View**

**Order Number LM837M or LM837N**
**See NS Package Number M14A or N14A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | | |
|---|---|---|
| Supply Voltage | $V_{CC}/V_{EE}$ | ±18V |
| Differential Input Voltage (Note 1) | $V_{ID}$ | ±30V |
| Common Mode Input Voltage (Note 1) | $V_{IC}$ | ±15V |
| Power Dissipation (Note 2) | $P_D$ | 1.2W (N)<br>830 mW (M) |
| Operating Temperature Range | $T_{OPR}$ | −40°C to +85°C |
| Storage Temperature Range | $T_{STG}$ | −60°C to +150°C |

Soldering Information

| | |
|---|---|
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## DC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $R_S = 50\Omega$ | | 0.3 | 5 | mV |
| $I_{OS}$ | Input Offset Current | | | 10 | 200 | nA |
| $I_B$ | Input Bias Current | | | 500 | 1000 | nA |
| $A_V$ | Large Signal Voltage Gain | $R_L = 2 k\Omega, V_{OUT} = \pm 10V$ | 90 | 110 | | dB |
| $V_{OM}$ | Output Voltage Swing | $R_L = 2 k\Omega$ | ±12 | ±13.5 | | V |
| | | $R_L = 600\Omega$ | ±10 | ±12.5 | | V |
| $V_{CM}$ | Common Mode Input Voltage | | ±12 | ±14.0 | | V |
| CMRR | Common Mode Rejection Ratio | $V_{IN} = \pm 12V$ | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = 15 \sim 5, -15 \sim -5$ | 80 | 100 | | dB |
| $I_S$ | Power Supply Current | $R_L = \infty$, Four Amps | | 10 | 15 | mA |

## AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate | $R_L = 600\Omega$ | 8 | 10 | | V/μs |
| GBW | Gain Bandwidth Product | $f = 100$ kHz, $R_L = 600\Omega$ | 15 | 25 | | MHz |

## Design Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$ (Note 3)

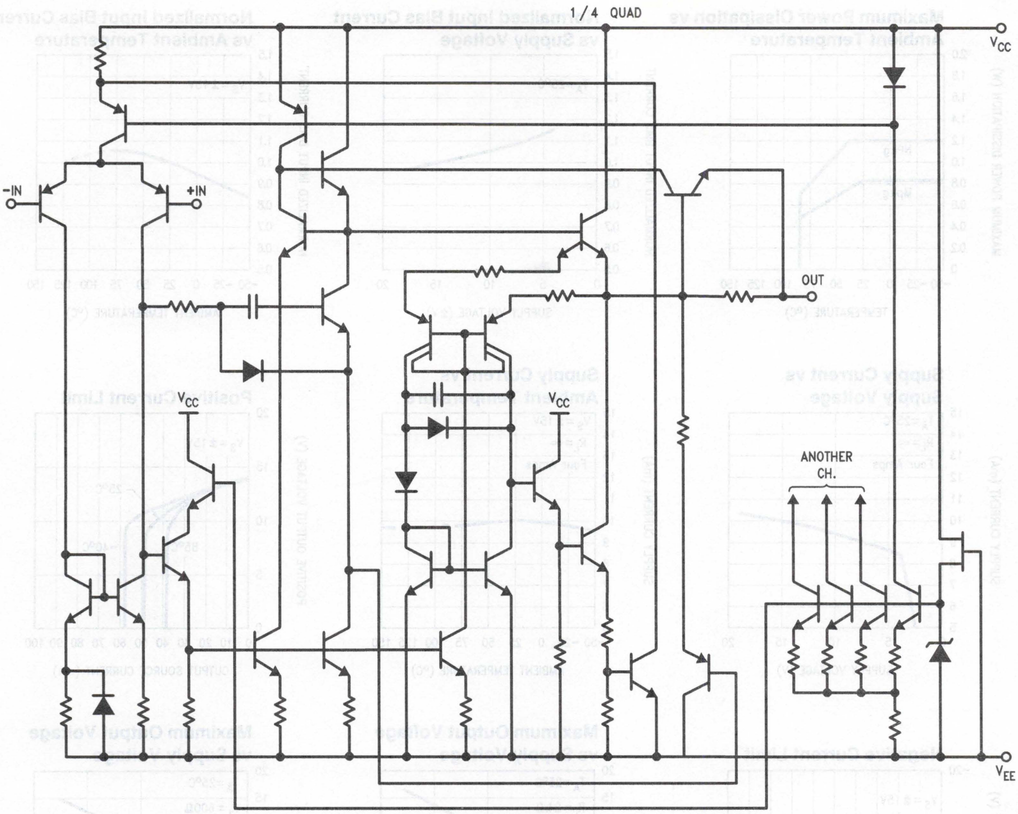
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PBW | Power Bandwidth | $V_O = 25\ V_{P\text{-}P}, R_L = 600\Omega$, THD < 1% | | 200 | | kHz |
| $e_{n1}$ | Equivalent Input Noise Voltage | JIS A, $R_S = 100\Omega$ | | 0.5 | | μV |
| $e_{n2}$ | Equivalent Input Noise Voltage | f = 1 kHz | | 4.5 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | f = 1 kHz | | 0.7 | | $pA/\sqrt{Hz}$ |
| THD | Total Harmonic Distortion | $A_V = 1, V_{OUT} = 3$ Vrms,<br>$f = 20 \sim 20$ kHz, $R_L = 600\Omega$ | | 0.0015 | | % |
| $f_U$ | Zero Cross Frequency | Open Loop | | 12 | | MHz |
| $\phi_m$ | Phase Margin | Open Loop | | 45 | | deg |
| | Input-Referred Crosstalk | $f = 20 \sim 20$ kHz | | −120 | | dB |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | | | 2 | | μV/°C |

**Note 1:** Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.

**Note 2:** For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90°C/W; LM837M, 150°C/W.

**Note 3:** The following parameters are not tested or guaranteed.

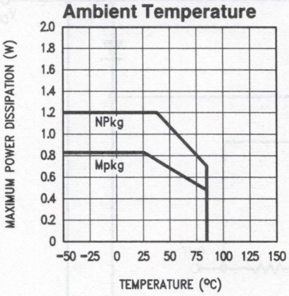
## Detailed Schematic


1/4 QUAD
$V_{CC}$
-IN
+IN
OUT
$V_{CC}$
$V_{CC}$
ANOTHER
CH.
$V_{EE}$

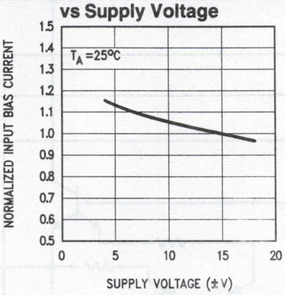
TL/H/9047-3

# Typical Performance Characteristics

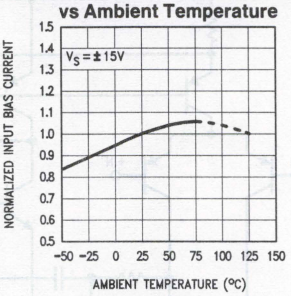
**Maximum Power Dissipation vs Ambient Temperature**



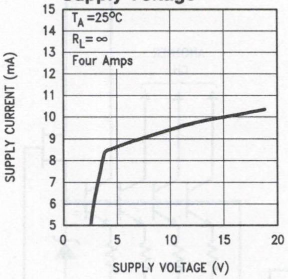
**Normalized Input Bias Current vs Supply Voltage**



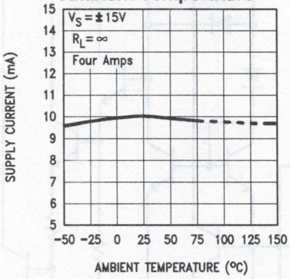
**Normalized Input Bias Current vs Ambient Temperature**



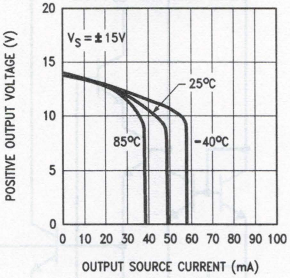
**Supply Current vs Supply Voltage**



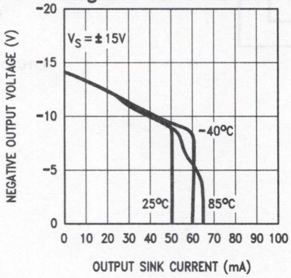
**Supply Current vs Ambient Temperature**



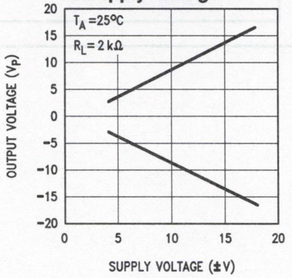
**Positive Current Limit**



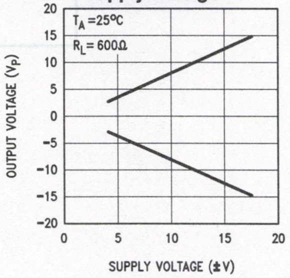
**Negative Current Limit**



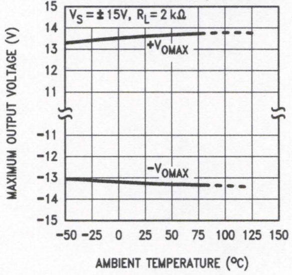
**Maximum Output Voltage vs Supply Voltage**



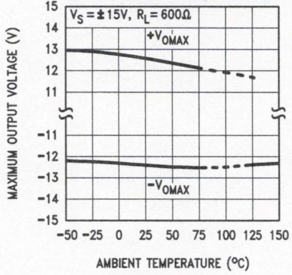
**Maximum Output Voltage vs Supply Voltage**



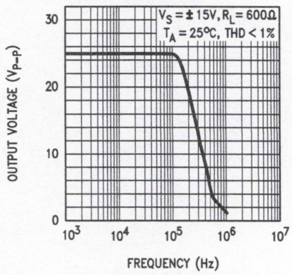
**Maximum Output Voltage vs Ambient Temperature**



**Maximum Output Voltage vs Ambient Temperature**



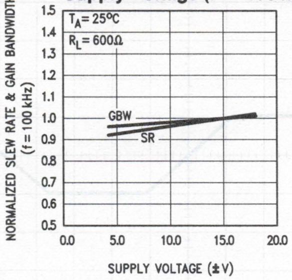
**Power Bandwidth**



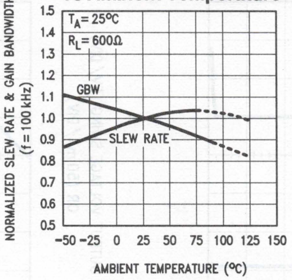
TL/H/9047–4

# Typical Performance Characteristics (Continued)

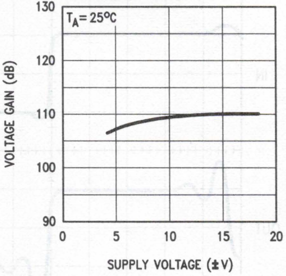
### Normalized Slew Rate & Gain Bandwidth vs Supply Voltage (f = 100 kHz)



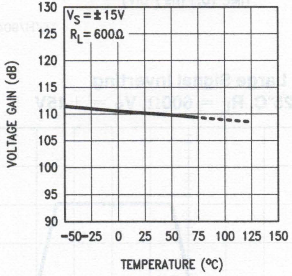
### Normalized Slew Rate & Gain Bandwidth (f = 100 kHz) vs Ambient Temperature



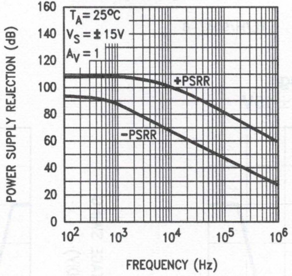
### Voltage Gain vs Supply Voltage



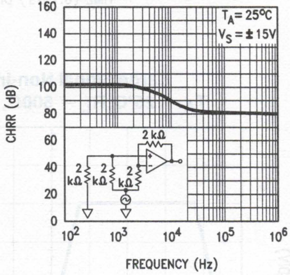
### Voltage Gain vs Ambient Temperature



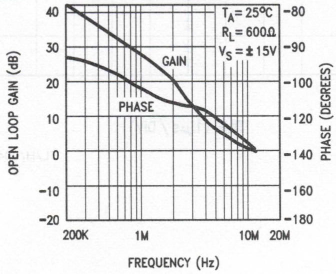
### Power Supply Rejection vs Frequency



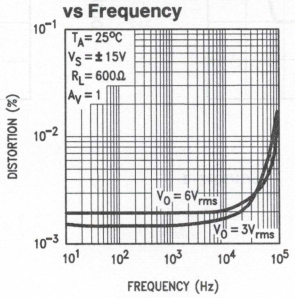
### CMRR vs Frequency



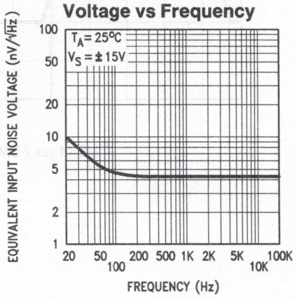
### Open Loop Gain & Phase vs Frequency



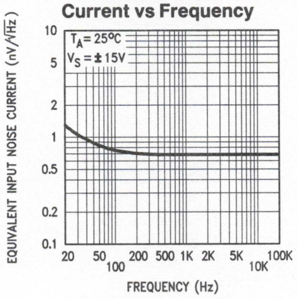
### Total Harmonic Distortion vs Frequency



### Equivalent Input Noise Voltage vs Frequency



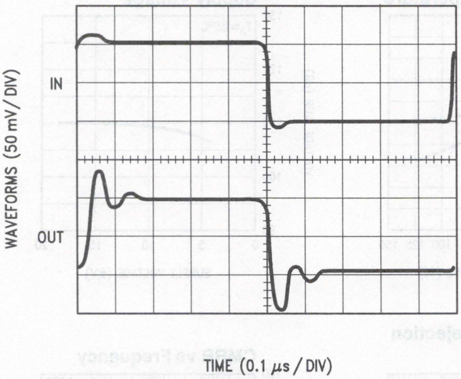
### Equivalent Input Noise Current vs Frequency



TL/H/9047–5

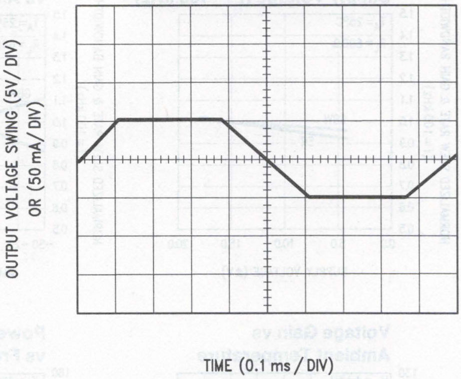
## Typical Performance Characteristics (Continued)

**Small Signal, Non-Inverting**
**$T_A = 25°C, A_V = 1, R_L = 600\Omega, V_S = \pm 15V$**



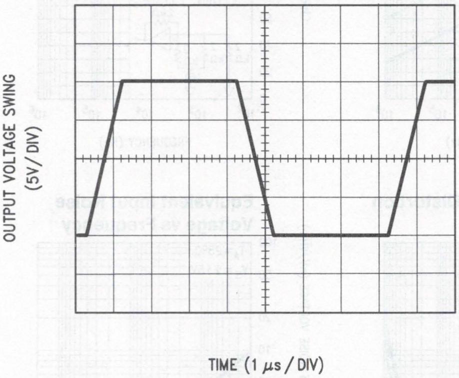
TL/H/9047-6

**Current Limit**
**$T_A = 25°C, V_S = \pm 15V, R_L = 100\Omega, A_V = 1$**



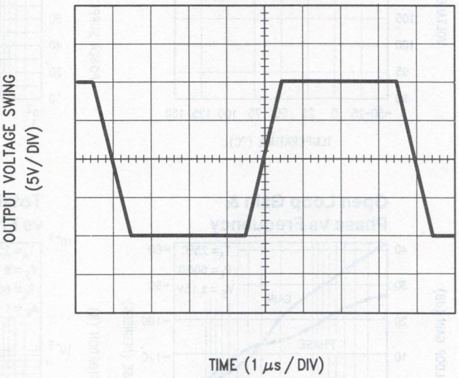
TL/H/9047-7

**Large Signal Non-Inverting**
**$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$**



TL/H/9047-8

**Large Signal Inverting**
**$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$**



TL/H/9047-9

**National Semiconductor Corporation**

# LM1558/LM1458 Dual Operational Amplifier

## General Description

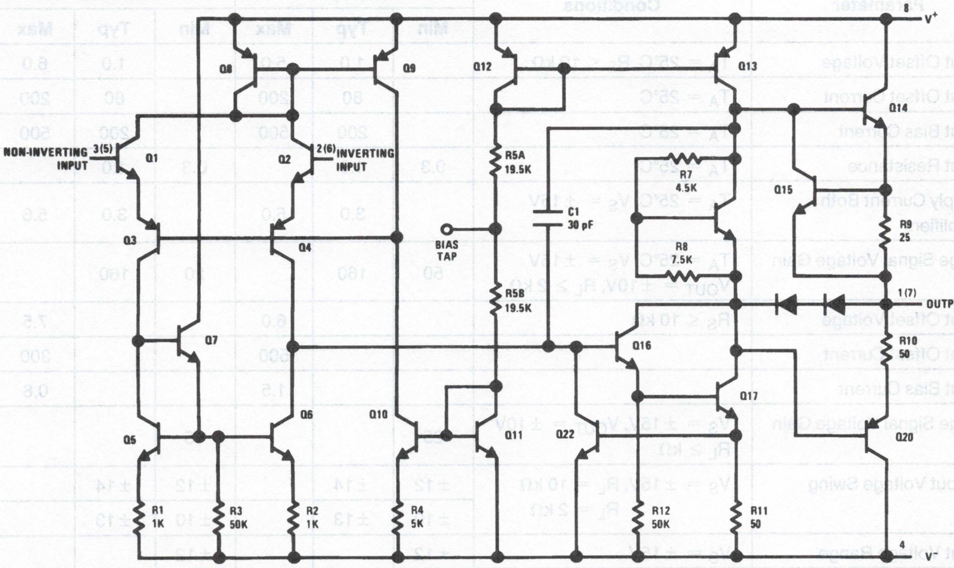
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

## Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

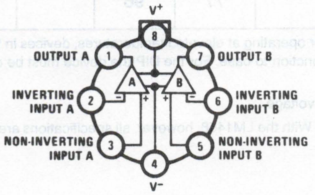
## Schematic and Connection Diagrams


8 V+
Q8
Q9
Q12
Q13
Q14
NON-INVERTING INPUT 3(5)
Q1
Q2
2(6) INVERTING INPUT
R5A 19.5K
R7 4.5K
Q15
C1 30 pF
R9 25
Q3
Q4
BIAS TAP
R8 7.5K
R5B 19.5K
1(7) OUTPUT
Q7
Q16
R10 50
Q17
Q6
Q10
Q11
Q22
Q20
Q5
R1 1K
R3 50K
R2 1K
R4 5K
R12 50K
R11 50
4 V-

TL/H/7886–1

**Note:** Numbers in parentheses are pin numbers for amplifier B.

**Metal Can Package**

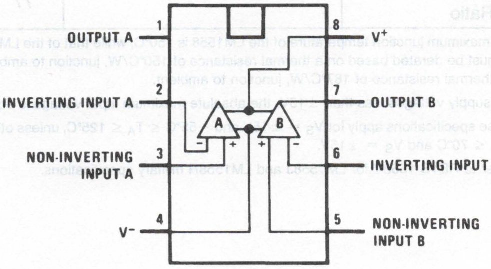

V+
8
OUTPUT A 1
7 OUTPUT B
A
B
INVERTING INPUT A 2
6 INVERTING INPUT B
NON-INVERTING INPUT A 3
5 NON-INVERTING INPUT B
4
V−

TL/H/7886–2

**Top View**

**Order Number LM1558H or LM1458H**
**See NS Package Number H08C**

**Dual-In-Line Package**


OUTPUT A 1
8 V+
INVERTING INPUT A 2
7 OUTPUT B
A
B
NON-INVERTING INPUT A 3
6 INVERTING INPUT B
V− 4
5 NON-INVERTING INPUT B

TL/H/7886–3

**Top View**

**Order Number LM1558J, LM1458J, LM1458M or LM1458N**
**See NS Package Number J08A, M08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Supply Voltage | |
| LM1558 | ±22V |
| LM1458 | ±18V |
| Power Dissipation (Note 1) | |
| LM1558H/LM1458H | 500 mW |
| LM1458N | 400 mW |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 2) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | |
| LM1558 | −55°C to +125°C |
| LM1458 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM1558 | | | LM1458 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A$ = 25°C, $R_S$ ≤ 10 kΩ | | 1.0 | 5.0 | | 1.0 | 6.0 | mV |
| Input Offset Current | $T_A$ = 25°C | | 80 | 200 | | 80 | 200 | nA |
| Input Bias Current | $T_A$ = 25°C | | 200 | 500 | | 200 | 500 | nA |
| Input Resistance | $T_A$ = 25°C | 0.3 | 1.0 | | 0.3 | 1.0 | | MΩ |
| Supply Current Both Amplifiers | $T_A$ = 25°C, $V_S$ = ±15V | | 3.0 | 5.0 | | 3.0 | 5.6 | mA |
| Large Signal Voltage Gain | $T_A$ = 25°C, $V_S$ = ±15V<br>$V_{OUT}$ = ±10V, $R_L$ ≥ 2 kΩ | 50 | 160 | | 20 | 160 | | V/mV |
| Input Offset Voltage | $R_S$ ≤ 10 kΩ | | | 6.0 | | | 7.5 | mV |
| Input Offset Current | | | | 500 | | | 300 | nA |
| Input Bias Current | | | | 1.5 | | | 0.8 | μA |
| Large Signal Voltage Gain | $V_S$ = ±15V, $V_{OUT}$ = ±10V<br>$R_L$ ≥ kΩ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 10 kΩ | ±12 | ±14 | | ±12 | ±14 | | V |
| | $R_L$ = 2 kΩ | ±10 | ±13 | | ±10 | ±13 | | V |
| Input Voltage Range | $V_S$ = ±15V | ±12 | | | ±12 | | | V |
| Common Mode Rejection Ratio | $R_S$ ≤ 10 kΩ | 70 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S$ ≤ 10 kΩ | 77 | 96 | | 77 | 96 | | dB |

**Note 1:** The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

**Note 2:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** These specifications apply for $V_S$ = ±15V and −55°C ≤ $T_A$ ≤ 125°C, unless otherwise specified. With the LM1458, however, all specifications are limited to 0°C ≤ $T_A$ ≤ 70°C and $V_S$ = ±15V.

**Note 4:** Refer to RETS 1558V for LM1558J and LM1558H military specifications.

**National Semiconductor Corporation**

# LM2900/LM3900, LM3301, LM3401 Quad Amplifiers

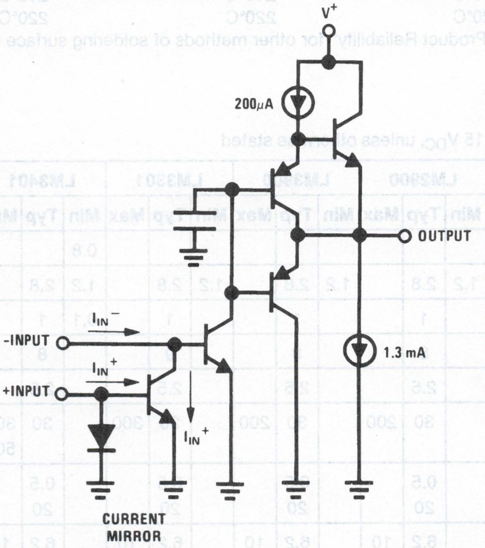
## General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

## Features

| | |
|---|---|
| ■ Wide single supply voltage | 4 $V_{DC}$ to 32 $V_{DC}$ |
| Range or dual supplies | ±2 $V_{DC}$ to ±16 $V_{DC}$ |
| ■ Supply current drain independent of supply voltage | |
| ■ Low input biasing current | 30 nA |
| ■ High open-loop gain | 70 dB |
| ■ Wide bandwidth | 2.5 MHz (unity gain) |
| ■ Large output voltage swing | $(V^+ - 1)$ Vp-p |
| ■ Internally frequency compensated for unity gain | |
| ■ Output short-circuit protection | |

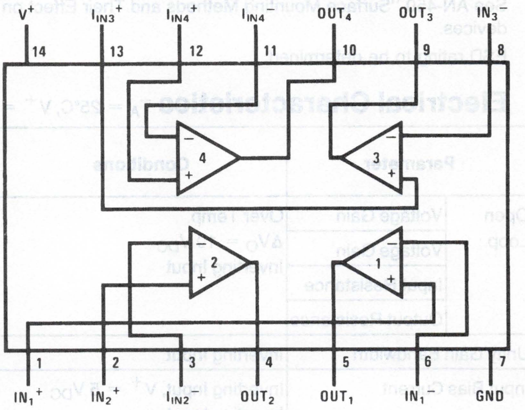
## Schematic and Connection Diagrams


V+
200μA
OUTPUT
$I_{IN}^-$
-INPUT
$I_{IN}^+$
+INPUT
1.3 mA
$I_{IN}^+$
CURRENT MIRROR

TL/H/7936-1

**Order Number LM3900M**
**See NS Package Number M14A**

**Dual-In-Line and Flat Package**


V+
$I_{IN3}^+$
$I_{IN4}^+$
$I_{IN4}^-$
$OUT_4$
$OUT_3$
$IN_3^-$
14
13
12
11
10
9
8
4
3
2
1
1
2
3
4
5
6
7
$IN_1^+$
$IN_2^+$
$I_{IN2}^-$
$OUT_2$
$OUT_1$
$IN_1^-$
GND

TL/H/7936-2

**Top View**

**Order Number LM2900N, LM3900N, LM3301N or LM3401N**
**See NS Package Number N14A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | LM2900/LM3900 | LM3301 | LM3401 |
|---|---|---|---|
| Supply Voltage | 32 $V_{DC}$<br>$\pm 16$ $V_{DC}$ | 28 $V_{DC}$<br>$\pm 14$ $V_{DC}$ | 18 $V_{DC}$<br>$\pm 9$ $V_{DC}$ |
| Power Dissipation ($T_A = 25°C$) (Note 1) | 1220 mW | | |
| Molded DIP | 1080 mW | 1080 mW | 1080 mW |
| Input Currents, $I_{IN}^+$ or $I_{IN}^-$ | 20 $mA_{DC}$ | 20 $mA_{DC}$ | 20 $mA_{DC}$ |
| Output Short-Circuit Duration—One Amplifier $T_A = 25°C$ (See Application Hints) | Continuous | Continuous | Continuous |
| Operating Temperature Range | | −40°C to +85°C | 0°C to +75°C |
| LM2900 | −40°C to +85°C | | |
| LM3900 | 0°C to +70°C | | |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C | 260°C | 260°C |
| Soldering Information | | | |
| Dual-In-Line Package | | | |
| Soldering (10 sec.) | 260°C | 260°C | 260°C |
| Small Outline Package | | | |
| Vapor Phase (60 sec.) | 215°C | 215°C | 215°C |
| Infrared (15 sec.) | 220°C | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics $T_A = 25°C$, $V^+ = 15$ $V_{DC}$, unless otherwise stated

| Parameter | | Conditions | | LM2900 | | | LM3900 | | | LM3301 | | | LM3401 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Open Loop | Voltage Gain | Over Temp. | | | | | | | | | | | 0.8 | | | V/mV |
| | Voltage Gain | $\Delta V_O = 10$ $V_{DC}$<br>Inverting Input | | 1.2 | 2.8 | | 1.2 | 2.8 | | 1.2 | 2.8 | | 1.2 | 2.8 | | |
| | Input Resistance | | | | 1 | | | 1 | | | 1 | | 0.1 | 1 | | MΩ |
| | Output Resistance | | | | 8 | | | 8 | | | 9 | | | 8 | | kΩ |
| Unity Gain Bandwidth | | Inverting Input | | | 2.5 | | | 2.5 | | | 2.5 | | | 2.5 | | MHz |
| Input Bias Current | | Inverting Input, $V^+ = 5$ $V_{DC}$<br>Inverting Input | | | 30 | 200 | | 30 | 200 | | 30 | 300 | | 30 | 300<br>500 | nA |
| Slew Rate | | Positive Output Swing<br>Negative Output Swing | | | 0.5<br>20 | | | 0.5<br>20 | | | 0.5<br>20 | | | 0.5<br>20 | | V/µs |
| Supply Current | | $R_L = \infty$ On All Amplifiers | | | 6.2 | 10 | | 6.2 | 10 | | 6.2 | 10 | | 6.2 | 10 | $mA_{DC}$ |
| Output Voltage Swing | $V_{OUT}$ High | $R_L = 2k$,<br>$V^+ = 15.0$ $V_{DC}$ | $I_{IN}^- = 0$,<br>$I_{IN}^+ = 0$ | 13.5 | | | 13.5 | | | 13.5 | | | 13.5 | | | $V_{DC}$ |
| | $V_{OUT}$ Low | | $I_{IN}^- = 10$ µA,<br>$I_{IN}^+ = 0$ | | 0.09 | 0.2 | | 0.09 | 0.2 | | 0.09 | 0.2 | | 0.09 | 0.2 | |
| | $V_{OUT}$ High | $V^+$ = Absolute Maximum Ratings | $I_{IN}^- = 0$,<br>$I_{IN}^+ = 0$<br>$R_L = \infty$, | 29.5 | | | 29.5 | | | 26.0 | | | 16.0 | | | |
| Output Current Capability | Source | | | 6 | 18 | | 6 | 10 | | 5 | 18 | | 5 | 10 | | $mA_{DC}$ |
| | Sink | (Note 2) | | 0.5 | 1.3 | | 0.5 | 1.3 | | 0.5 | 1.3 | | 0.5 | 1.3 | | |
| | $I_{SINK}$ | $V_{OL} = 1V$, $I_{IN}^- = 5$ µA | | | 5 | | | 5 | | | 5 | | | 5 | | |

## Electrical Characteristics (Note 6), $V^+ = 15\ V_{DC}$, unless otherwise stated (Continued)

| Parameter | Conditions | LM2900 | | | LM3900 | | | LM3301 | | | LM3401 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Power Supply Rejection | $T_A = 25°C$, f = 100 Hz | | 70 | | | 70 | | | 70 | | | 70 | | dB |
| Mirror Gain | @ 20 μA (Note 3)<br>@ 200 μA (Note 3) | 0.90<br>0.90 | 1.0<br>1.0 | 1.1<br>1.1 | 0.90<br>0.90 | 1.0<br>1.0 | 1.1<br>1.1 | 0.90<br>0.90 | 1<br>1 | 1.10<br>1.10 | 0.90<br>0.90 | 1<br>1 | 1.10<br>1.10 | μA/μA |
| ΔMirror Gain | @ 20 μA to 200 μA (Note 3) | | 2 | 5 | | 2 | 5 | | 2 | 5 | | 2 | 5 | % |
| Mirror Current | (Note 4) | | 10 | 500 | | 10 | 500 | | 10 | 500 | | 10 | 500 | $\mu A_{DC}$ |
| Negative Input Current | $T_A = 25°C$ (Note 5) | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | $mA_{DC}$ |
| Input Bias Current | Inverting Input | | 300 | | | 300 | | | | | | | | nA |

**Note 1:** For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 92°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

**Note 2:** The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

**Note 3:** This spec indicates the current gain of the current mirror which is used as the non-inverting input.

**Note 4:** Input $V_{BE}$ match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10 μA. This is therefore a typical design center for many of the application circuits.

**Note 5:** Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately $-0.3\ V_{DC}$. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

**Note 6:** These specs apply for $-40°C \leq T_A \leq +85°C$, unless otherwise stated.

## Application Hints

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated $+5\ V_{DC}$ power supply at $T_A = 25°C$ with a 100 kΩ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above $T_J$ max. Larger feedback resistors will reduce the current, 11 MΩ provides approximately 30 mA, an open circuit provides 1.3 mA, and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to $V^+$ as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at $T_A = 25°C$.

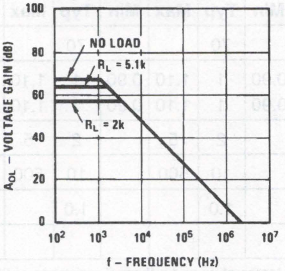
Unintentional signal coupling from the output to the non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional AC signal pickup.

Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{BE}$. Internal clamp transistors (see note 5) catch-negative input voltages at approximately $-0.3\ V_{DC}$ but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately 100 μA.

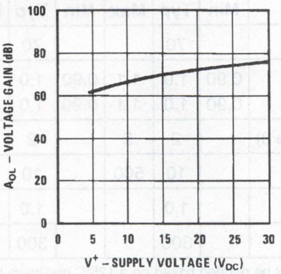
This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a DC amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the AC gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output DC voltage.

# Typical Performance Characteristics

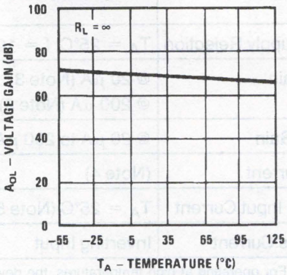
### Open Loop Gain



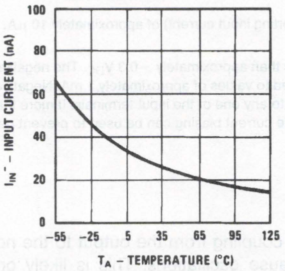
### Voltage Gain



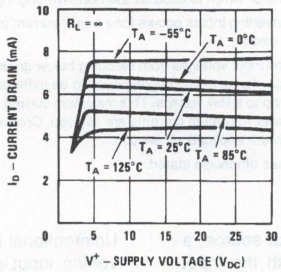
### Voltage Gain



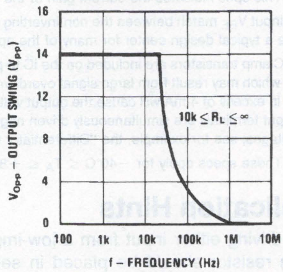
### Input Current



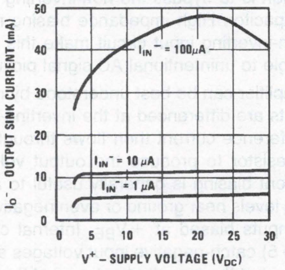
### Supply Current



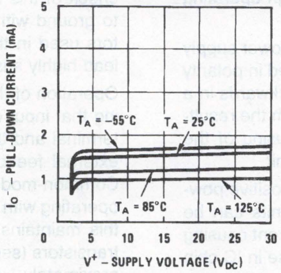
### Large Signal Frequency Response



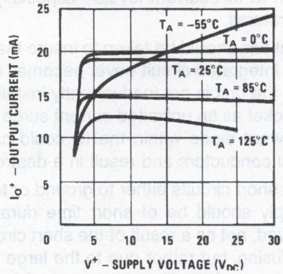
### Output Sink Current



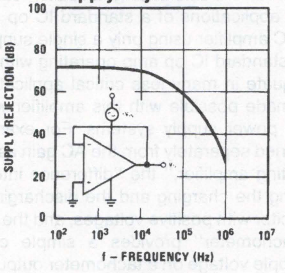
### Output Class-A Bias Current



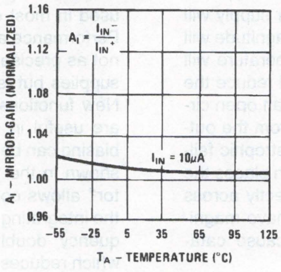
### Output Source Current



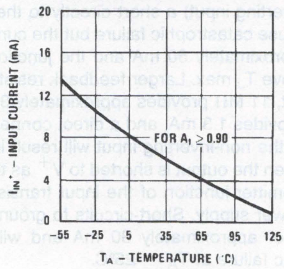
### Supply Rejection



### Mirror Gain



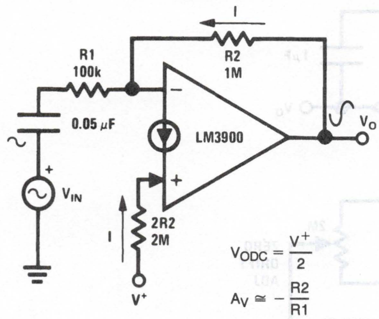
### Maximum Mirror Current



TL/H/7936-9

# Typical Applications ($V^+ = 15\ V_{DC}$)

## Inverting Amplifier

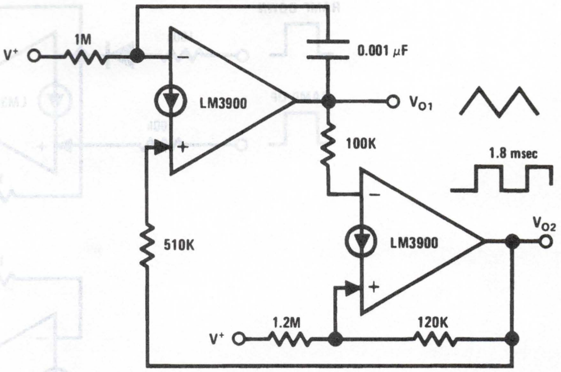

I
R1
100k
R2
1M
0.05 μF
LM3900
VO
VIN
2R2
2M
I
V+

$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong -\frac{R2}{R1}$$

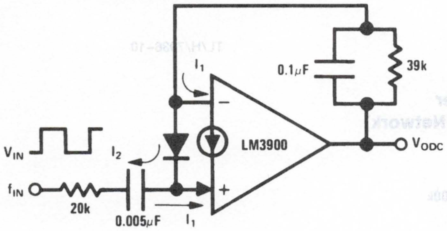
TL/H/7936-3

## Triangle/Square Generator


1M
V+
0.001 μF
LM3900
VO1
100K
1.8 msec
510K
LM3900
VO2
1.2M
120K
V+

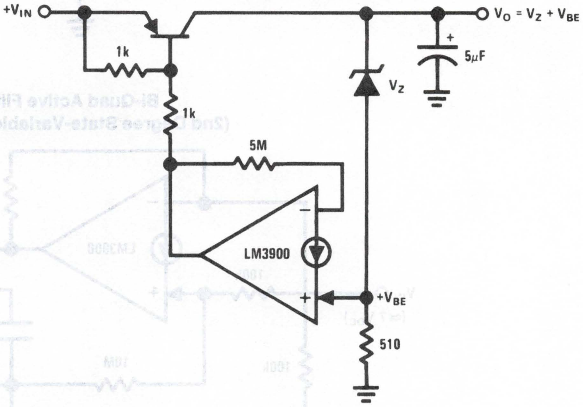
TL/H/7936-4

## Frequency-Doubling Tachometer


I1
0.1μF
39k
LM3900
VODC
VIN
I2
fIN
20k
0.005μF
I1

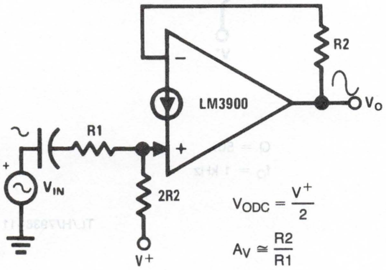
TL/H/7936-5

## Low $V_{IN} - V_{OUT}$ Voltage Regulator


+VIN
1k
VO = VZ + VBE
5μF
VZ
1k
5M
LM3900
+VBE
510

TL/H/7936-6

## Non-Inverting Amplifier

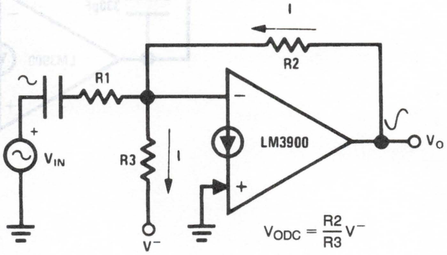

R2
LM3900
VO
R1
VIN
2R2
V+

$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-7

## Negative Supply Biasing


I
R2
R1
VIN
LM3900
VO
R3
I
V−

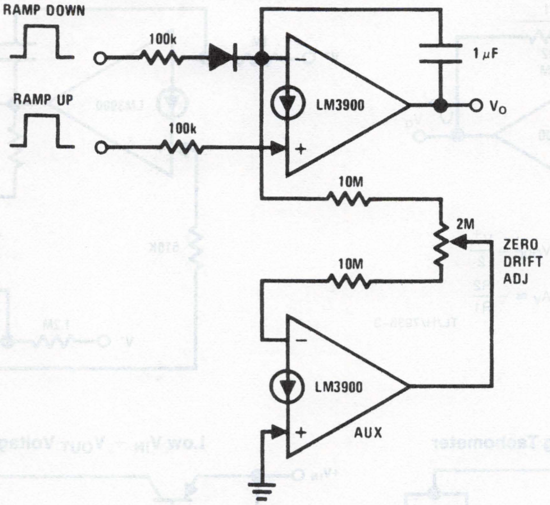
$$V_{ODC} = \frac{R2}{R3} V^-$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-8

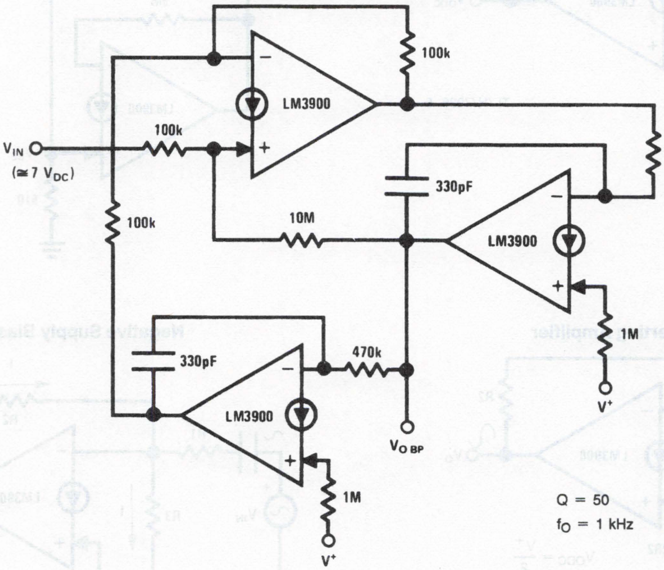
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Low-Drift Ramp and Hold Circuit


RAMP DOWN
100k
1 μF
LM3900
$V_O$
RAMP UP
100k
10M
2M
ZERO DRIFT ADJ
10M
LM3900
AUX

TL/H/7936-10

### Bi-Quad Active Filter (2nd Degree State-Variable Network)


100k
LM3900
$V_{IN}$
(≅ 7 $V_{DC}$)
100k
470k
330pF
100k
10M
LM3900
1M
$V^+$
330pF
470k
LM3900
1M
$V^+$
$V_{O\ BP}$

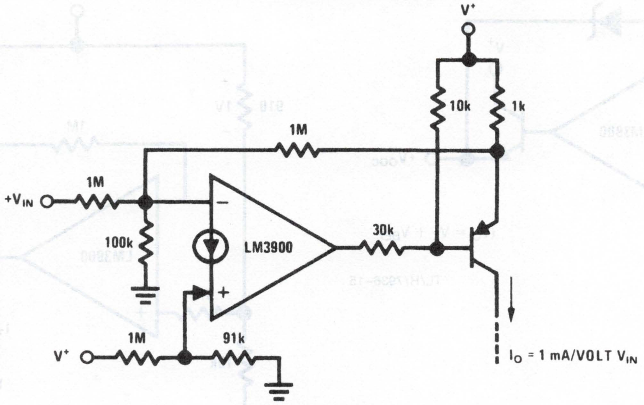
$Q = 50$

$f_O = 1$ kHz

TL/H/7936-11

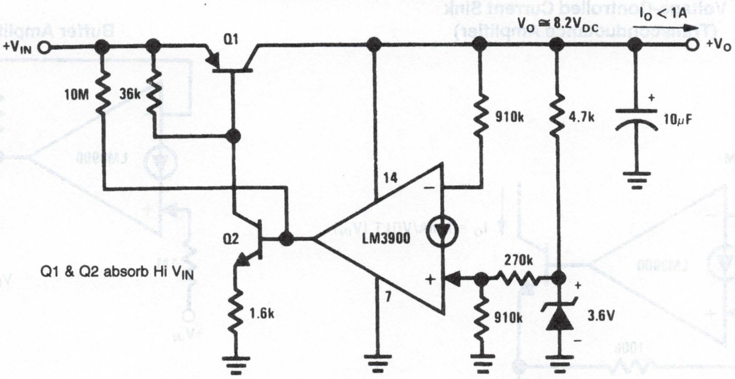
## Typical Applications $(V^+ = 15\ V_{DC})$ (Continued)

### Voltage-Controlled Current Source (Transconductance Amplifier)


V⁺
10k
1k
1M
1M
+V_IN
100k
LM3900
30k
1M
91k
V⁺
I_O = 1 mA/VOLT V_IN

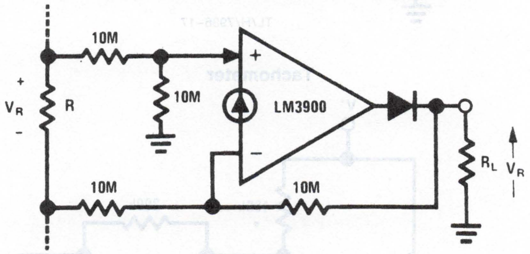
TL/H/7936-12

### Hi $V_{IN}$, Lo $(V_{IN} - V_O)$ Self-Regulator


I_O < 1A
V_O ≅ 8.2V_DC
+V_IN
Q1
+V_O
10M
36k
910k
4.7k
10μF
14
Q2
LM3900
Q1 & Q2 absorb Hi V_IN
270k
1.6k
7
910k
3.6V

TL/H/7936-13

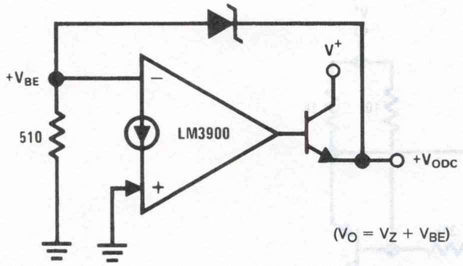
### Ground-Referencing a Differential Input Signal


10M
+
V_R
R
-
10M
LM3900
10M
10M
R_L
V_R

TL/H/7936-14

## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

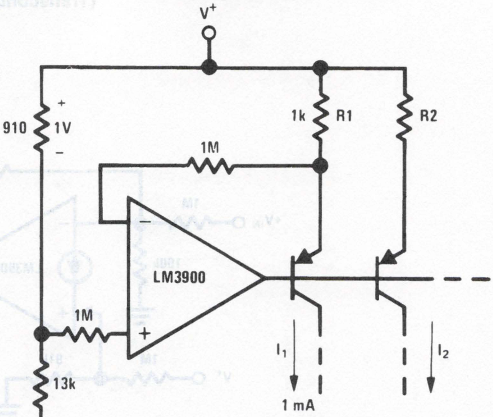
### Voltage Regulator


V_Z
V+
+V_BE
510
LM3900
+V_ODC

($V_O = V_Z + V_{BE}$)

TL/H/7936-15

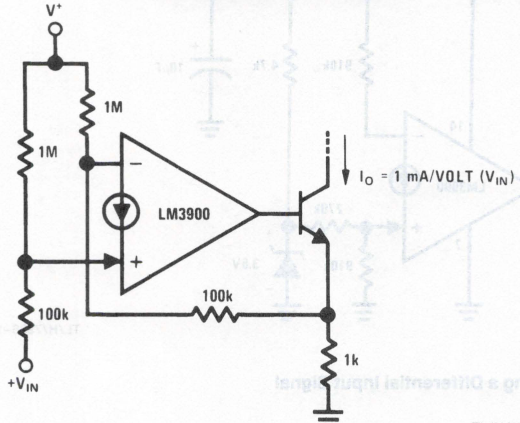
### Fixed Current Sources


V+
910
+
1V
−
1k
R1
R2
1M
LM3900
1M
13k
I1
1 mA
I2

$I_2 = \frac{R1}{R2} I_1$

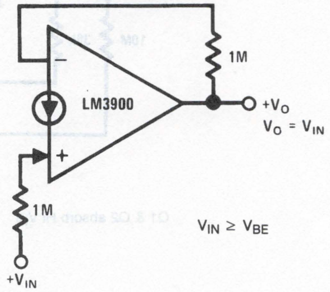
TL/H/7936-16

### Voltage-Controlled Current Sink (Transconductance Amplifier)


V+
1M
1M
LM3900
I_O = 1 mA/VOLT (V_IN)
100k
100k
1k
+V_IN

TL/H/7936-17

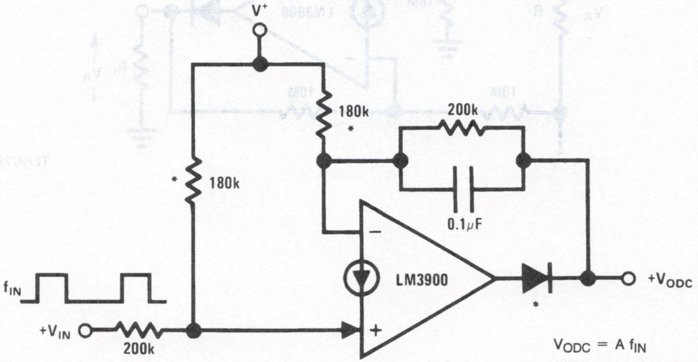
### Buffer Amplifier


1M
LM3900
+V_O
V_O = V_IN
1M
+V_IN

$V_{IN} \geq V_{BE}$

TL/H/7936-18

### Tachometer


V+
180k
*
200k
*
180k
0.1μF
LM3900
f_IN
+V_IN
200k
*
+V_ODC

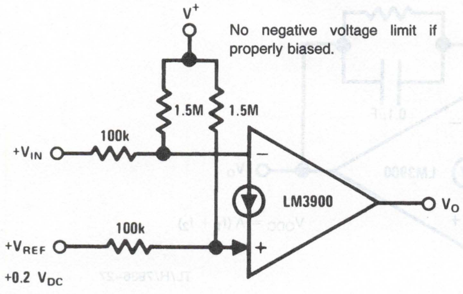
TL/H/7936-19

$V_{ODC} = A\ f_{IN}$

*Allows $V_O$ to go to zero.

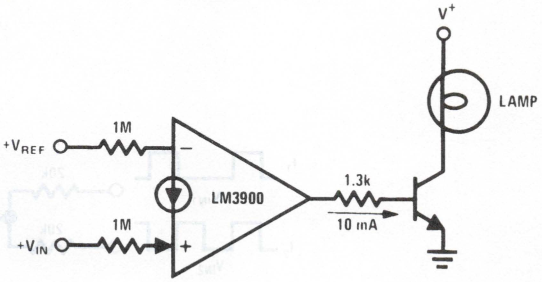
# Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Low-Voltage Comparator


V+
No negative voltage limit if properly biased.
1.5M
1.5M
100k
+VIN
LM3900
VO
100k
+VREF
+0.2 VDC

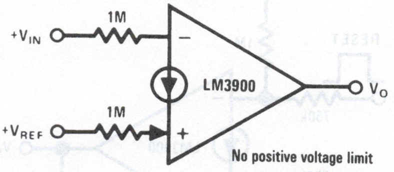
TL/H/7936-20

### Power Comparator


V+
LAMP
1M
+VREF
LM3900
1.3k
10 mA
1M
+VIN

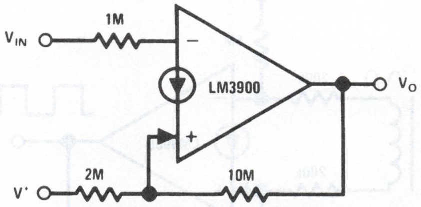
TL/H/7936-21

### Comparator


1M
+VIN
LM3900
VO
1M
+VREF
No positive voltage limit

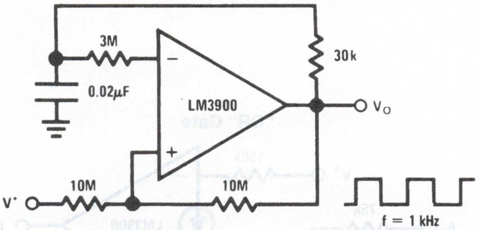
TL/H/7936-22

### Schmitt-Trigger


1M
VIN
LM3900
VO
2M
10M
V+

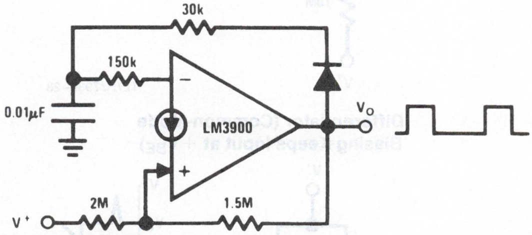
TL/H/7936-23

### Square-Wave Oscillator


3M
30k
0.02µF
LM3900
VO
10M
10M
V+
f = 1 kHz

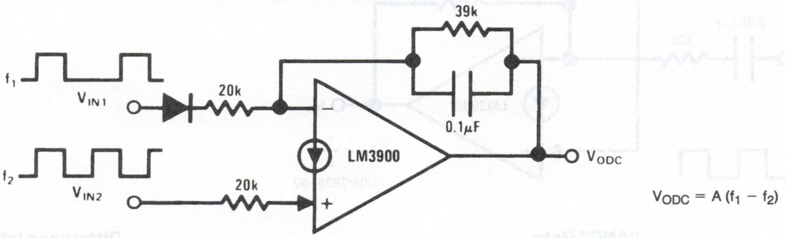
TL/H/7936-24

### Pulse Generator


30k
150k
0.01µF
LM3900
VO
2M
1.5M
V+

TL/H/7936-25

### Frequency Differencing Tachometer

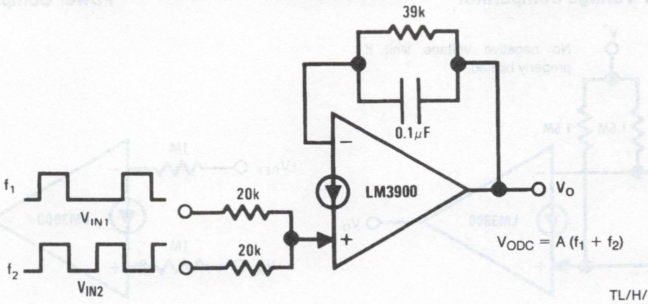

39k
f1
VIN1
20k
0.1µF
LM3900
VODC
f2
VIN2
20k

$V_{ODC} = A\,(f_1 - f_2)$

TL/H/7936-26

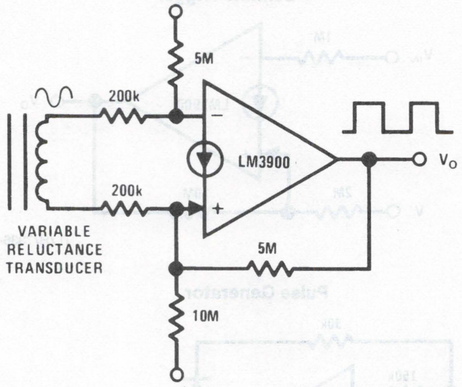
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Frequency Averaging Tachometer


39k
0.1 μF
LM3900
f1
f2
VIN1
VIN2
20k
20k
VO
VODC = A (f1 + f2)

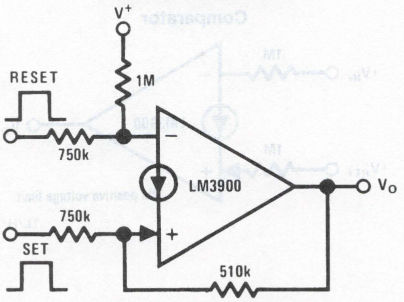
TL/H/7936-27

### Squaring Amplifier (W/Hysteresis)


V+
5M
200k
200k
LM3900
VO
5M
10M
V+
VARIABLE RELUCTANCE TRANSDUCER

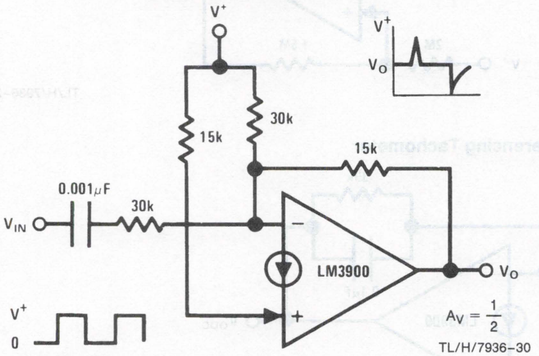
TL/H/7936-28

### Bi-Stable Multivibrator


V+
1M
RESET
750k
750k
SET
LM3900
VO
510k

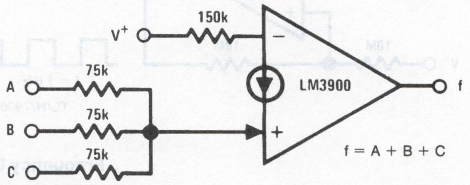
TL/H/7936-29

### Differentiator (Common-Mode Biasing Keeps Input at $+V_{BE}$)


V+
V+
VO
15k
30k
15k
0.001 μF
30k
VIN
LM3900
VO
V+
0
AV = 1/2

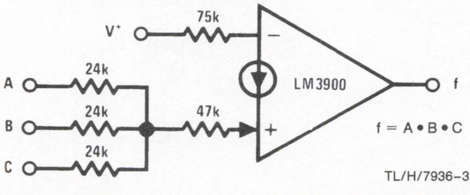
TL/H/7936-30

### "OR" Gate


V+
150k
75k
75k
75k
A
B
C
LM3900
f
f = A + B + C

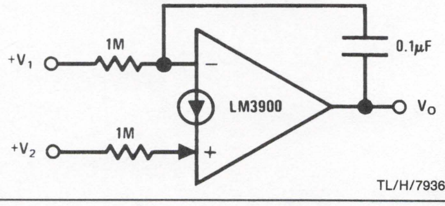
TL/H/7936-31

### "AND" Gate


V+
75k
24k
24k
24k
A
B
C
47k
LM3900
f
f = A • B • C

TL/H/7936-32

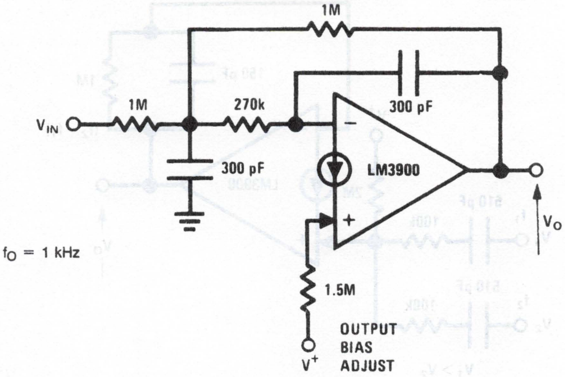
### Difference Integrator


+V1
1M
+V2
1M
0.1 μF
LM3900
VO

TL/H/7936-33

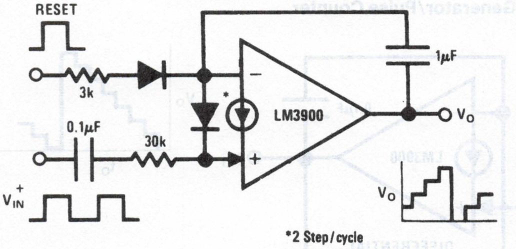
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Low Pass Active Filter


1M
1M
270k
300 pF
$V_{IN}$
300 pF
LM3900
$V_O$
1.5M
OUTPUT
BIAS
ADJUST
$V^+$
$f_O = 1\ kHz$

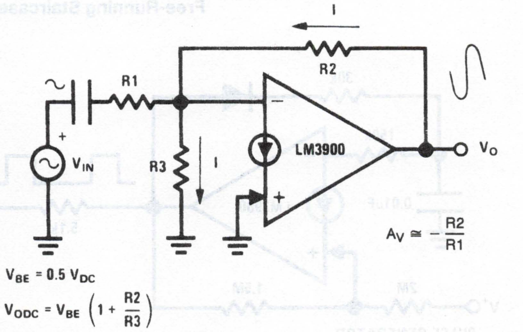
TL/H/7936-34

### Staircase Generator


RESET
3k
0.1μF
30k
$V_{IN}^+$
*
LM3900
1μF
$V_O$
$V_O$
*2 Step/cycle

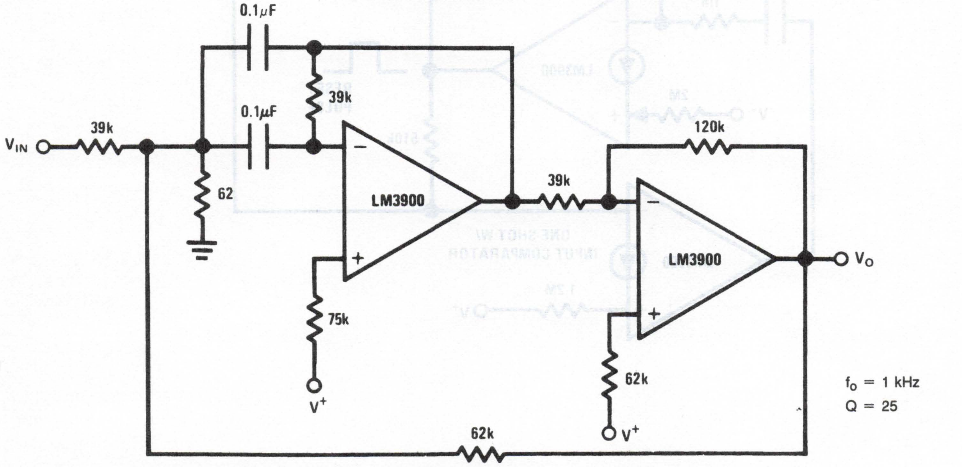
TL/H/7936-35

### $V_{BE}$ Biasing


I
R2
R1
+
$V_{IN}$
R3
I
LM3900
$V_O$
$A_V \cong -\frac{R2}{R1}$
$V_{BE} = 0.5\ V_{DC}$
$V_{ODC} = V_{BE}\left(1 + \frac{R2}{R3}\right)$

TL/H/7936-36

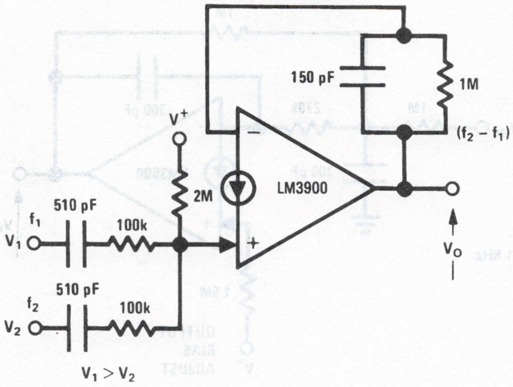
### Bandpass Active Filter


0.1μF
39k
0.1μF
$V_{IN}$
39k
62
LM3900
75k
$V^+$
39k
120k
LM3900
$V_O$
62k
$V^+$
62k
$f_O = 1\ kHz$
Q = 25

TL/H/7936-37

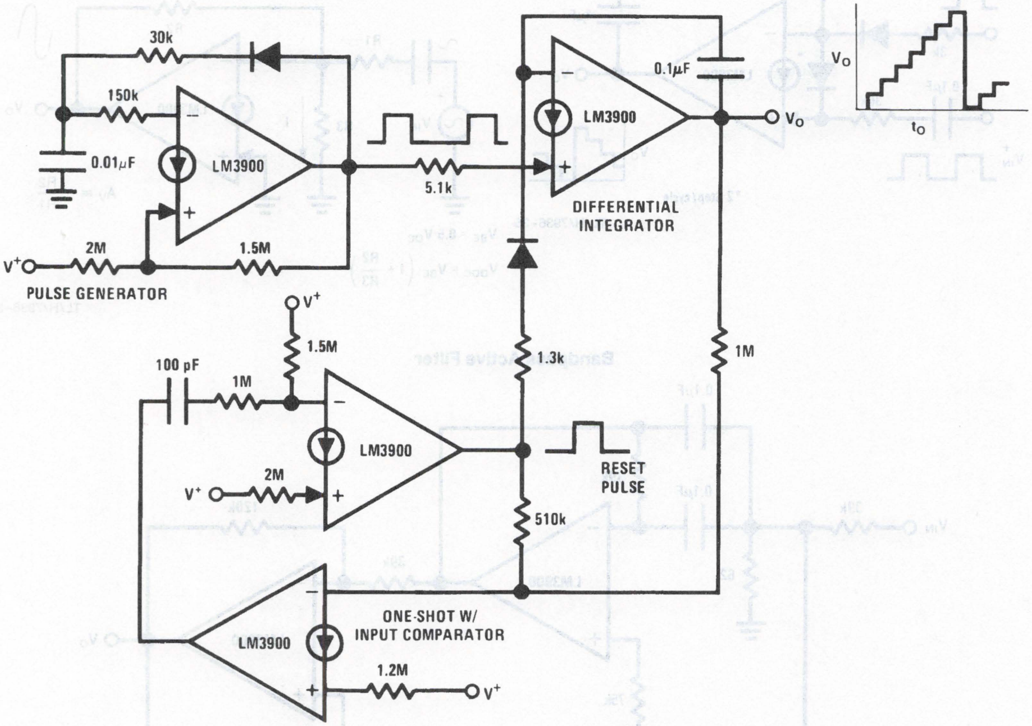
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Low-Frequency Mixer


150 pF
1M
$(f_2 - f_1)$
$V^+$
2M
LM3900
510 pF
$f_1$
$V_1$
100k
510 pF
$f_2$
$V_2$
100k
$V_1 > V_2$
$V_O$

TL/H/7936–38

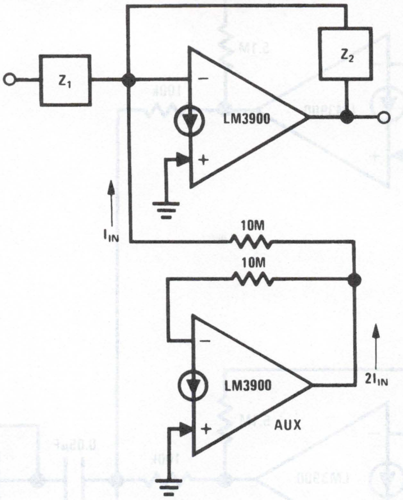
### Free-Running Staircase Generator/Pulse Counter


30k
150k
0.01µF
LM3900
2M
1.5M
$V^+$
PULSE GENERATOR
5.1k
0.1µF
LM3900
$V_O$
DIFFERENTIAL INTEGRATOR
$V_O$
$t_O$
$V^+$
1.5M
100 pF
1M
LM3900
2M
$V^+$
1.3k
1M
RESET PULSE
510k
LM3900
ONE-SHOT W/ INPUT COMPARATOR
1.2M
$V^+$

TL/H/7936–39

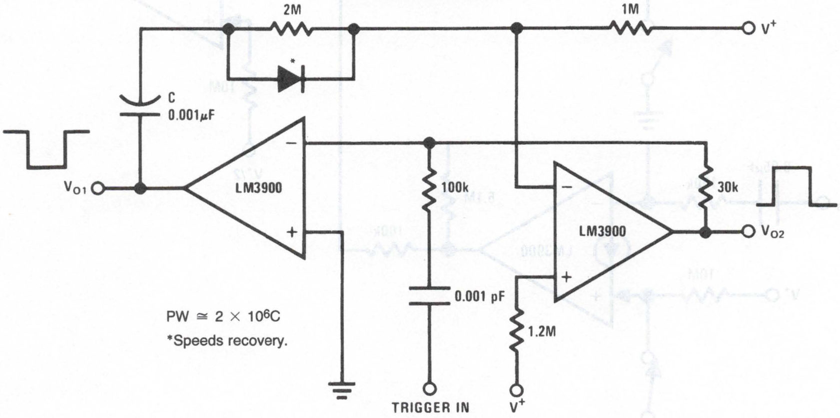
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Supplying $I_{IN}$ with Aux. Amp (to Allow Hi-Z Feedback Networks)


Z1
Z2
LM3900
I_IN
10M
10M
LM3900
2I_IN
AUX

TL/H/7936-40

### One-Shot Multivibrator

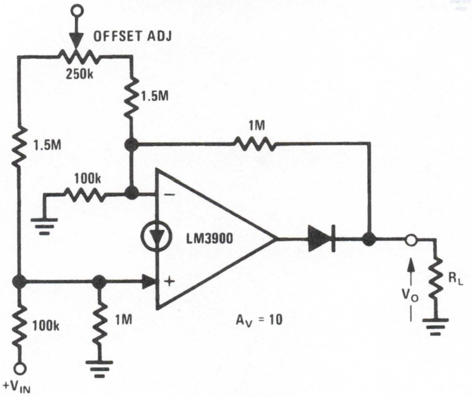

2M
*
1M
V+
C
0.001μF
V_O1
LM3900
100k
LM3900
30k
V_O2
0.001 pF
1.2M
TRIGGER IN
V+

PW ≅ 2 × 10⁶C

*Speeds recovery.

TL/H/7936-41

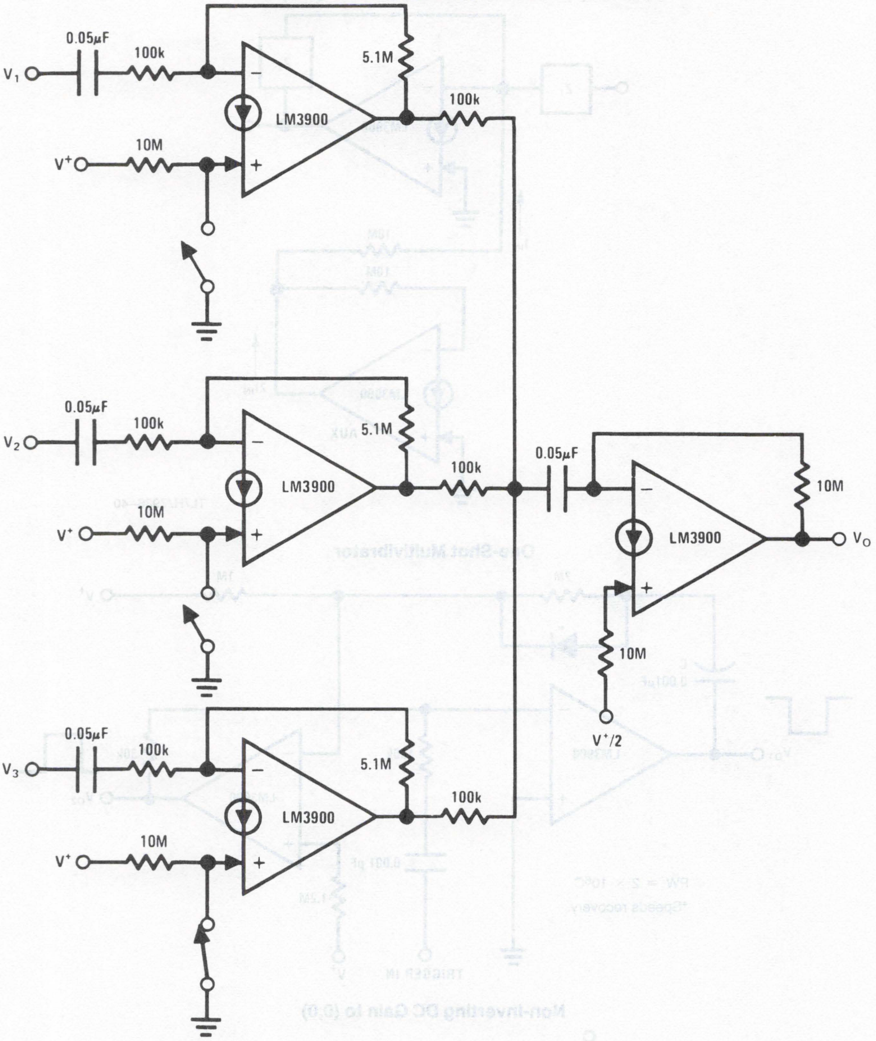
### Non-Inverting DC Gain to (0,0)


OFFSET ADJ
250k
1.5M
1.5M
1M
100k
LM3900
R_L
V_O
100k
1M
+V_IN
A_V = 10

TL/H/7936-42

## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

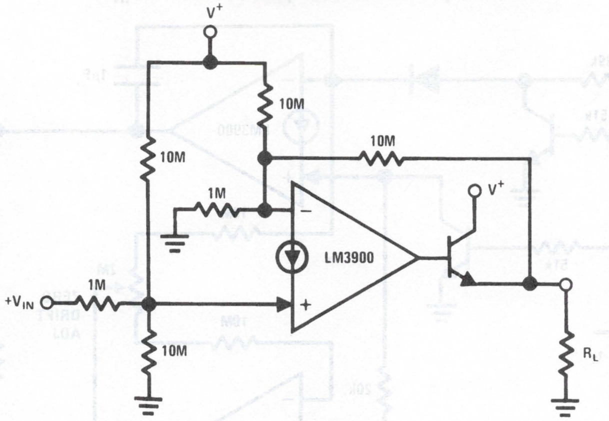
### Channel Selection by DC Control (or Audio Mixer)


0.05μF
100k
5.1M
V1
LM3900
100k
10M
V+
0.05μF
100k
5.1M
V2
LM3900
100k
10M
V+
0.05μF
10M
LM3900
VO
10M
V+/2
0.05μF
100k
5.1M
V3
LM3900
100k
10M
V+

TL/H/7936–43

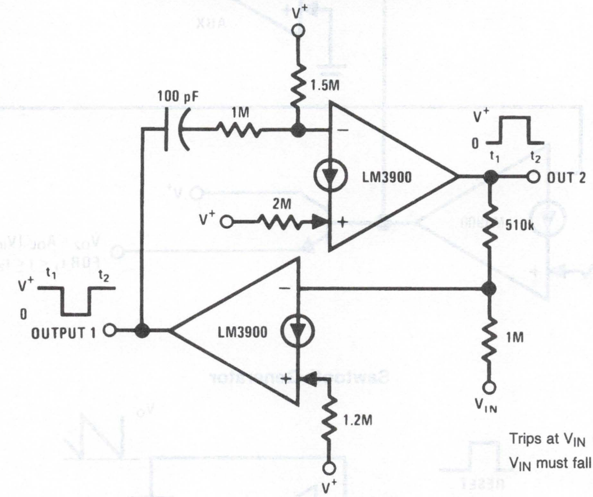
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Power Amplifier


V+
10M
10M
10M
1M
V+
LM3900
+VIN
1M
10M
RL

TL/H/7936–44

### One-Shot with DC Input Comparator

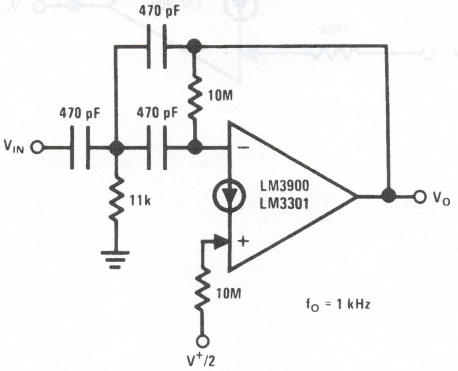

V+
1.5M
100 pF
1M
V+
0
t1
t2
LM3900
OUT 2
2M
V+
510k
V+
t1
t2
0
OUTPUT 1
LM3900
1M
VIN
1.2M
V+

Trips at $V_{IN} \cong 0.8\ V^+$

$V_{IN}$ must fall $0.8\ V^+$ prior to $t_2$

TL/H/7936–45

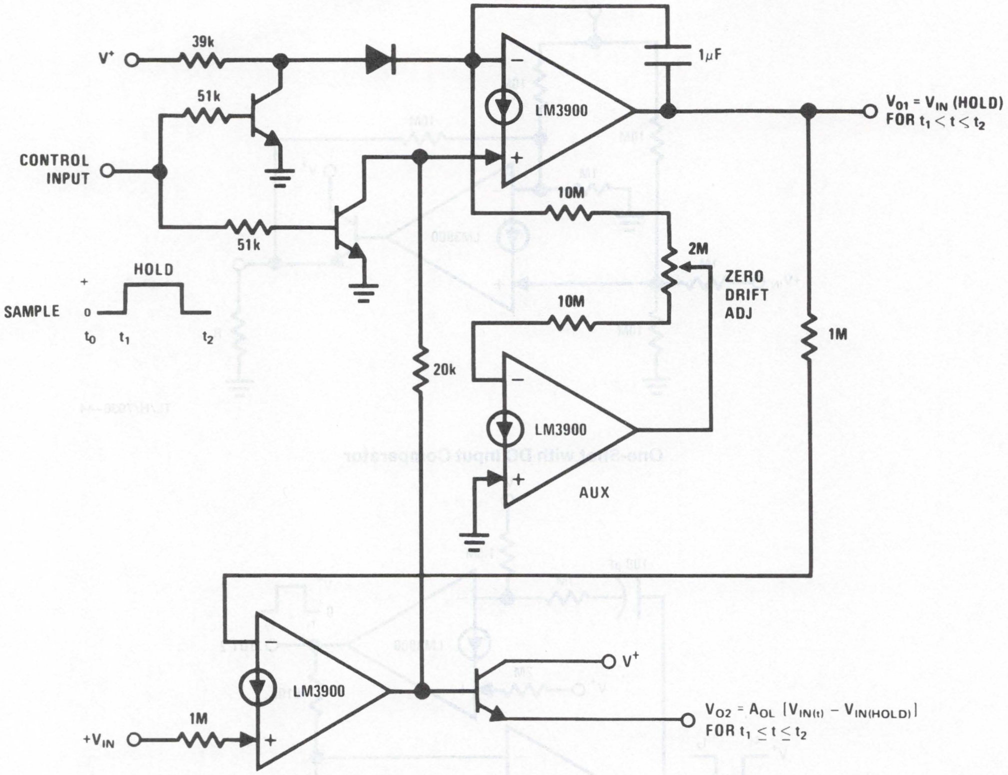
### High Pass Active Filter


470 pF
10M
470 pF
470 pF
VIN
LM3900
LM3301
VO
11k
10M
V+/2
fO = 1 kHz

TL/H/7936–46

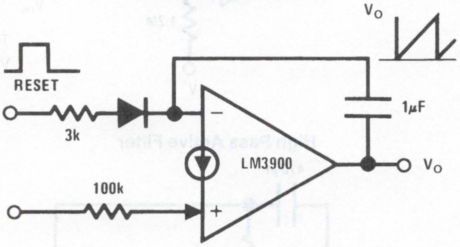
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Sample-Hold and Compare with New $+V_{IN}$


V⁺
39k
51k
CONTROL INPUT
51k
HOLD
+
SAMPLE
0
t₀
t₁
t₂
LM3900
1μF
V₀₁ = V_IN (HOLD) FOR t₁ < t < t₂
10M
2M
ZERO DRIFT ADJ
10M
20k
LM3900
AUX
1M
LM3900
V⁺
+V_IN
1M
V₀₂ = A_OL [V_IN(t) − V_IN(HOLD)] FOR t₁ ≤ t ≤ t₂

TL/H/7936-47

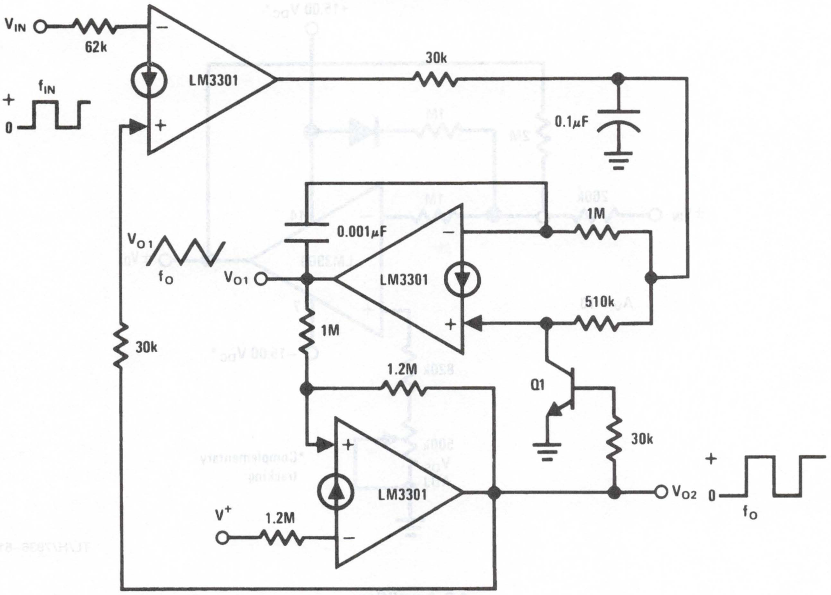
### Sawtooth Generator


V₀
RESET
3k
1μF
LM3900
V₀
100k
V⁺

TL/H/7936-48

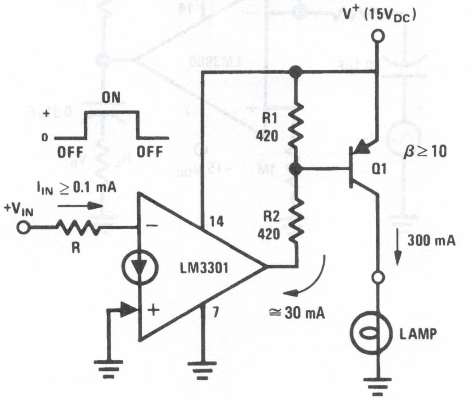
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Phase-Locked Loop


V<sub>IN</sub>
62k
f<sub>IN</sub>
+
0
LM3301
30k
0.1µF
0.001µF
1M
V<sub>O1</sub>
f<sub>O</sub>
V<sub>O1</sub>
LM3301
510k
1M
30k
1.2M
Q1
30k
+
LM3301
V<sub>O2</sub>
+
0
f<sub>O</sub>
V<sup>+</sup>
1.2M

TL/H/7936–49

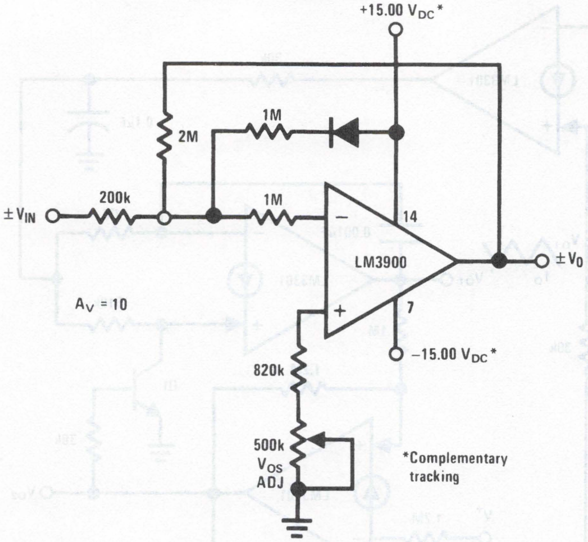
### Boosting to 300 mA Loads


V<sup>+</sup> (15V<sub>DC</sub>)
ON
+
0
OFF
OFF
R1
420
β ≥ 10
Q1
I<sub>IN</sub> ≥ 0.1 mA
+V<sub>IN</sub>
R
14
R2
420
300 mA
LM3301
≅ 30 mA
7
LAMP

TL/H/7936–50

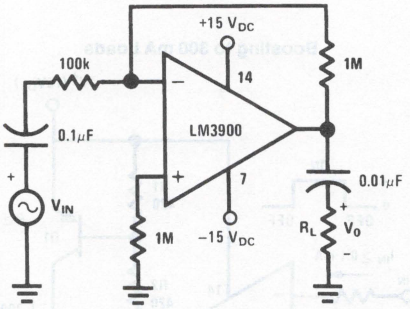
## Split-Supply Applications ($V^+ = +15\ V_{DC}$ & $V^- = -15\ V_{DC}$)

### Non-Inverting DC Gain


+15.00 V_DC*
2M
1M
200k
1M
±V_IN
14
LM3900
±V_O
A_V = 10
7
−15.00 V_DC*
820k
500k
V_OS
ADJ
*Complementary tracking

TL/H/7936–51

### AC Amplifier


+15 V_DC
100k
14
1M
0.1μF
LM3900
+
V_IN
7
0.01μF
1M
−15 V_DC
R_L
V_O
+
−

TL/H/7936–52

**National Semiconductor Corporation**

# LM3080/LM3080A Operational Transconductance Amplifier

## General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance ($g_m$) is directly proportional to the amplifier bias current ($I_{ABC}$).

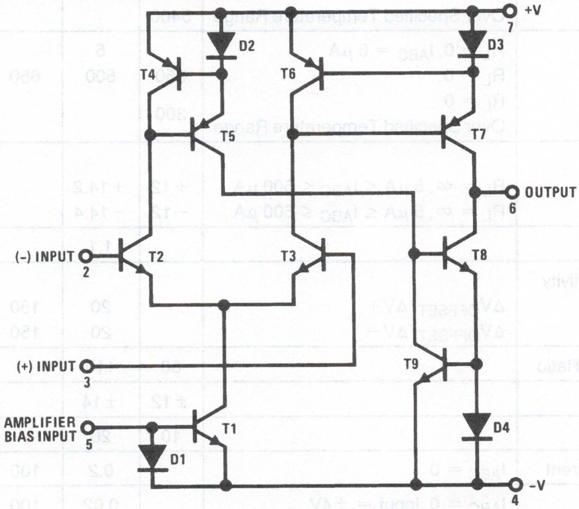
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080N and LM3080AN are guaranteed from 0°C to +70°C.

## Features

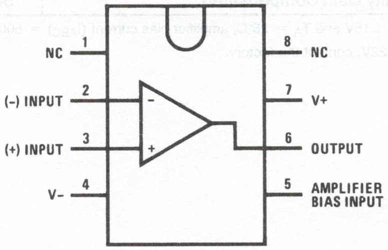
- Slew rate (unity gain compensated): 50 V/μs
- Fully adjustable gain: 0 to $g_m \bullet R_L$ limit
- Extended $g_m$ linearity: 3 decades
- Flexible supply voltage range: ±2V to ±18V
- Adjustable power consumption

## Schematic and Connection Diagrams


+V
7
D2
D3
T4
T6
T5
T7
OUTPUT
6
(−) INPUT
2
T2
T3
T8
(+) INPUT
3
T9
AMPLIFIER
BIAS INPUT
5
T1
D1
D4
−V
4

TL/H/7148–1

**Dual-In-Line Package**


NC
1
(−) INPUT
2
(+) INPUT
3
V−
4
8
NC
7
V+
6
OUTPUT
5
AMPLIFIER
BIAS INPUT
−
+

TL/H/7148–2

**Top View**

**Order Number LM3080AN or LM3080N**
**See NS Package Number N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (Note 2) | |
| LM3080 | ±18V |
| LM3080A | ±22V |
| Power Dissipation | 250 mW |
| Differential Input Voltage | ±5V |
| Amplifier Bias Current ($I_{ABC}$) | 2 mA |
| DC Input Voltage | $+V_S$ to $-V_S$ |
| Output Short Circuit Duration | Indefinite |
| Operating Temperature Range | |
| LM3080N or LM3080AN | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## Electrical Characteristics (Note 1)

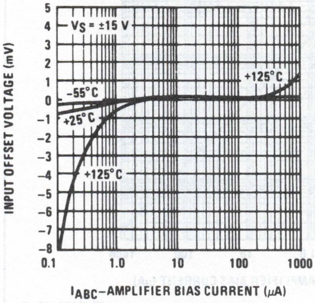
| Parameter | Conditions | LM3080 | | | LM3080A | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | | | 0.4 | 5 | | 0.4 | 2 | mV |
| | Over Specified Temperature Range | | | 6 | | | 5 | mV |
| | $I_{ABC} = 5\ \mu A$ | | 0.3 | | | 0.3 | 2 | mV |
| Input Offset Voltage Change | $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | | 0.1 | | | 0.1 | 3 | mV |
| Input Offset Current | | | 0.1 | 0.6 | | 0.1 | 0.6 | µA |
| Input Bias Current | | | 0.4 | 5 | | 0.4 | 5 | µA |
| | Over Specified Temperature Range | | 1 | 7 | | 1 | 8 | µA |
| Forward Transconductance ($g_m$) | | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | µmho |
| | Over Specified Temperature Range | 5400 | | | 4000 | | | µmho |
| Peak Output Current | $R_L = 0$, $I_{ABC} = 5\ \mu A$ | | 5 | | 3 | 5 | 7 | µA |
| | $R_L = 0$ | 350 | 500 | 650 | 350 | 500 | 650 | µA |
| | $R_L = 0$<br>Over Specified Temperature Range | 300 | | | 300 | | | µA |
| Peak Output Voltage | | | | | | | | |
| Positive | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | +12 | +14.2 | | +12 | +14.2 | | V |
| Negative | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | −12 | −14.4 | | −12 | −14.4 | | V |
| Amplifier Supply Current | | | 1.1 | | | 1.1 | | mA |
| Input Offset Voltage Sensitivity | | | | | | | | |
| Positive | $\Delta V_{OFFSET}/\Delta V+$ | | 20 | 150 | | 20 | 150 | µV/V |
| Negative | $\Delta V_{OFFSET}/\Delta V-$ | | 20 | 150 | | 20 | 150 | µV/V |
| Common Mode Rejection Ratio | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ±12 | ±14 | | ±12 | ±14 | | V |
| Input Resistance | | 10 | 26 | | 10 | 26 | | kΩ |
| Magnitude of Leakage Current | $I_{ABC} = 0$ | | 0.2 | 100 | | 0.2 | 5 | nA |
| Differential Input Current | $I_{ABC} = 0$, Input $= \pm 4V$ | | 0.02 | 100 | | 0.02 | 5 | nA |
| Open Loop Bandwidth | | | 2 | | | 2 | | MHz |
| Slew Rate | Unity Gain Compensated | | 50 | | | 50 | | V/µs |

**Note 1:** These specifications apply for $V_S = \pm 15V$ and $T_A = 25°C$, amplifier bias current ($I_{ABC}$) $= 500\ \mu A$, unless otherwise specified.

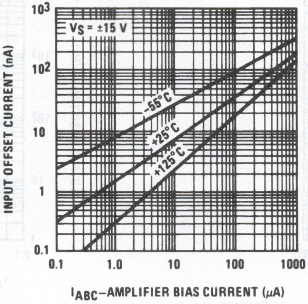
**Note 2:** Selection to supply voltage above ±22V, contact the factory.

# Typical Performance Characteristics

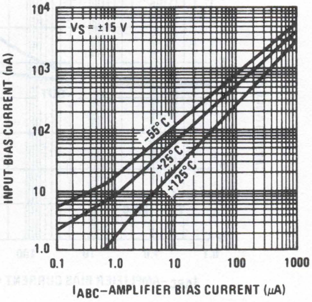
**Input Offset Voltage**



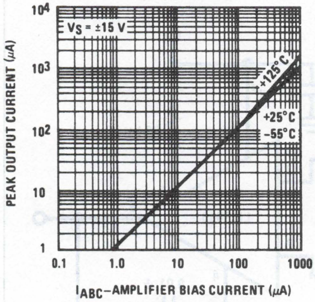
**Input Offset Current**



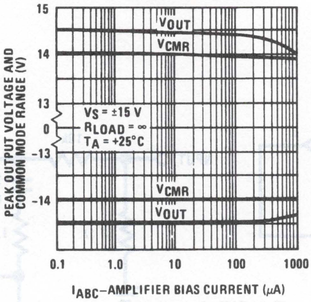
**Input Bias Current**



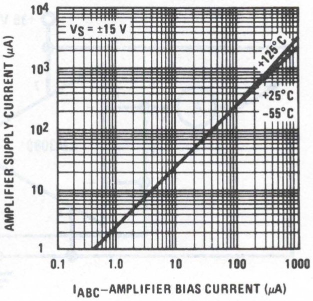
**Peak Output Current**



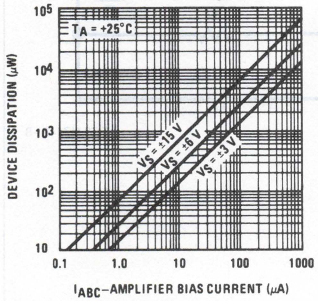
**Peak Output Voltage and Common Mode Range**



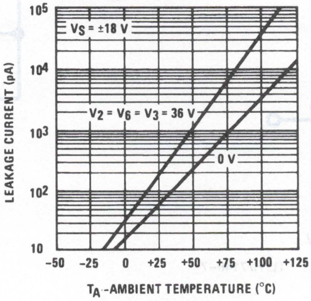
**Amplifier Supply Current**



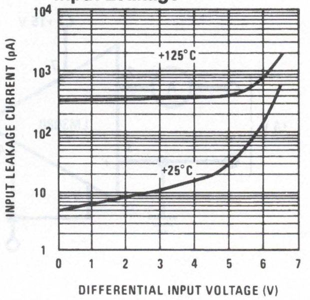
**Total Power Dissipation**



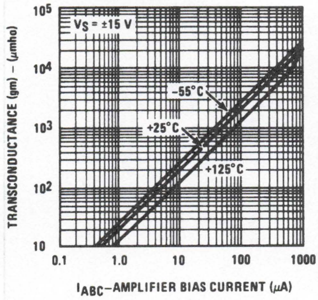
**Leakage Current**



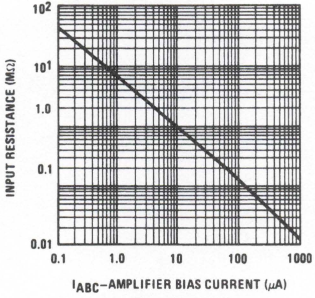
**Input Leakage**



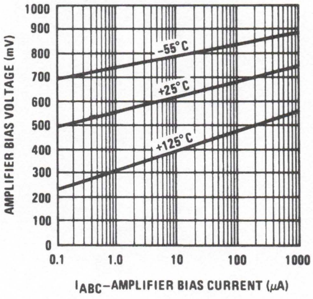
**Transconductance**



**Input Resistance**



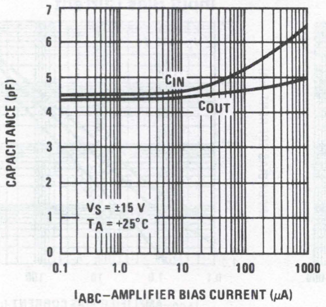
**Amplifier Bias Voltage vs Amplifier Bias Current**



TL/H/7148–3

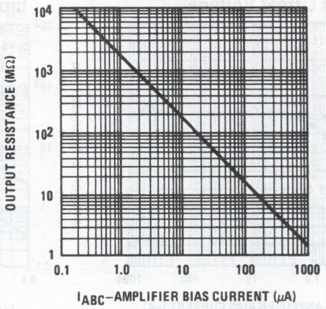
## Typical Performance Characteristics (Continued)

### Input and Output Capacitance



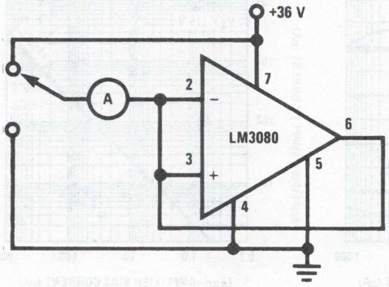
TL/H/7148-4

### Output Resistance



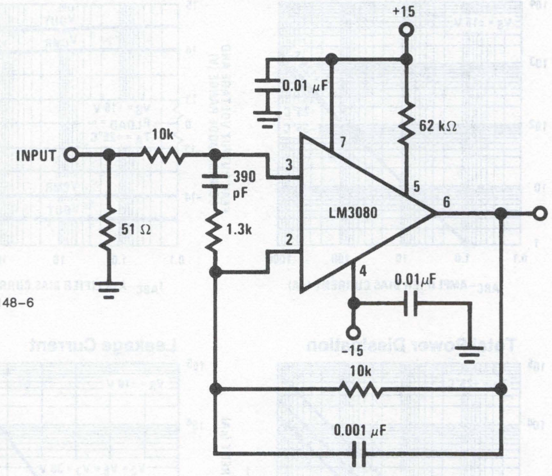
TL/H/7148-5

### Leakage Current Test Circuit


+36 V
A
2
7
–
LM3080
6
3
+
5
4

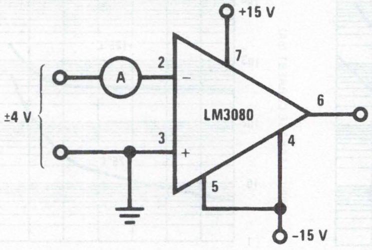
TL/H/7148-6

### Unity Gain Follower


+15
0.01 μF
62 kΩ
7
INPUT
10k
3
390 pF
5
6
LM3080
51 Ω
1.3k
2
4
0.01μF
–15
10k
0.001 μF

TL/H/7148-8

### Differential Input Current Test Circuit


+15 V
7
2
A
–
±4 V
LM3080
6
3
+
4
5
–15 V

TL/H/7148-7

**National Semiconductor Corporation**

# LM4250/LM4250C Programmable Operational Amplifier

## General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

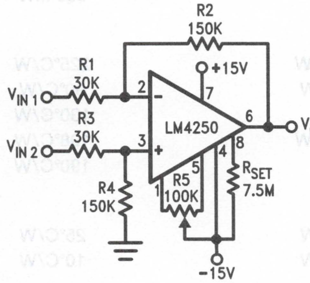
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

## Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

## Typical Applications

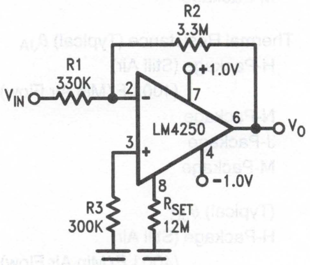
**X5 Difference Amplifier**


R2
150K
+15V
R1
30K
$V_{IN}$ 1
2
7
R3
30K
LM4250
6
$V_O$
$V_{IN}$ 2
3
8
4
5
R5
100K
1
$R_{SET}$
7.5M
R4
150K
−15V

Quiescent $P_D$ = 0.6 mW

TL/H/9300–3

**500 Nano-Watt X10 Amplifier**

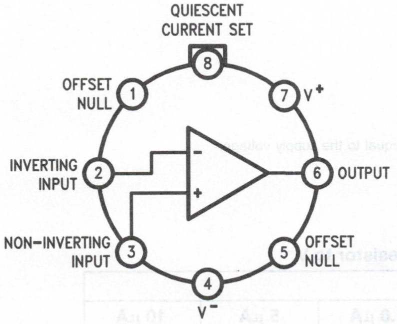

R2
3.3M
R1
330K
+1.0V
$V_{IN}$
2
7
6
$V_O$
LM4250
3
4
−1.0V
8
R3
300K
$R_{SET}$
12M

TL/H/9300–4

Quiescent $P_P$ = 500 mW

## Connection Diagrams

**Metal Can Package**

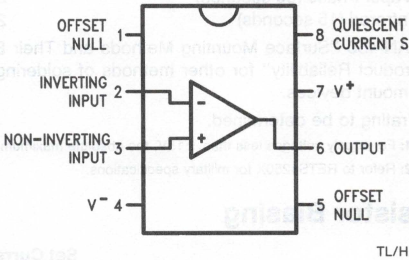

QUIESCENT CURRENT SET
8
OFFSET NULL
1
7
$V^+$
INVERTING INPUT
2
6
OUTPUT
NON-INVERTING INPUT
3
5
OFFSET NULL
4
$V^-$

TL/H/9300–2

**Top View**

**Order Number LM4250H or LM4250CH**
**See NS Package Number H08C**

**Dual-In-Line Package**


OFFSET NULL
1
8
QUIESCENT CURRENT SET
INVERTING INPUT
2
7
$V^+$
NON-INVERTING INPUT
3
6
OUTPUT
$V^-$
4
5
OFFSET NULL

TL/H/9300–5

**Top View**

**Order Number LM4250J, LM4250CJ, LM4250CN or LM4250M**
**See NS Package Number J08A, M08A or N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 2)**

| | LM4250 | LM4250C |
|---|---|---|
| Supply Voltage | ±18V | ±18V |
| Operating Temp. Range | $-55°C \leq T_A \leq +125°C$ | $0°C \leq T_A \leq +70°C$ |
| Differential Input Voltage | ±30V | ±30V |
| Input Voltage (Note 1) | ±15V | ±15V |
| $I_{SET}$ Current | 150 nA | 150 nA |
| Output Short Circuit Duration | Indefinite | Indefinite |
| $T_{JMAX}$ | | |
| H-Package | 150°C | 100°C |
| N-Package | | 100°C |
| J-Package | 150°C | 100°C |
| M-Package | | 100°C |
| Power Dissipation at $T_A$ = 25°C | | |
| H-Package (Still Air) | 500 mW | 300 mW |
| (400 LF/Min Air Flow) | 1200 mW | 1200 mW |
| N-Package | | 500 mW |
| J-Package | 1000 mW | 600 mW |
| M-Package | | 350 mW |
| Thermal Resistance (Typical) $\theta_{JA}$ | | |
| H-Package (Still Air) | 225°C/W | 225°C/W |
| (400 LF/Min Air Flow) | 90°C/W | 90°C/W |
| N-Package | | 130°C/W |
| J-Package | 108°C/W | 108°C/W |
| M-Package | | 190°C/W |
| (Typical) $\theta_{JC}$ | | |
| H-Package (Still Air) | 25°C/W | 25°C/W |
| (400 LF/Min Air Flow) | 10°C/W | 10°C/W |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |

| Soldering Information | |
|---|---|
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

**Note 1:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** Refer to RETS4250X for military specifications.

## Resistor Biasing

**Set Current Setting Resistor to V−**

| | $I_{SET}$ | | | | |
|---|---|---|---|---|---|
| $V_S$ | 0.1 μA | 0.5 μA | 1.0 μA | 5 μA | 10 μA |
| ±1.5V | 25.6 MΩ | 5.04 MΩ | 2.5 MΩ | 492 kΩ | 244 kΩ |
| ±3.0V | 55.6 MΩ | 11.0 MΩ | 5.5 MΩ | 1.09 MΩ | 544 kΩ |
| ±6.0V | 116 MΩ | 23.0 MΩ | 11.5 MΩ | 2.29 MΩ | 1.14 MΩ |
| ±9.0V | 176 MΩ | 35.0 MΩ | 17.5 MΩ | 3.49 MΩ | 1.74 MΩ |
| ±12.0V | 236 MΩ | 47.0 MΩ | 23.5 MΩ | 4.69 MΩ | 2.34 MΩ |
| ±15.0V | 296 MΩ | 59.0 MΩ | 29.5 MΩ | 5.89 MΩ | 2.94 MΩ |

## Electrical Characteristics LM4250 (−55°C ≤ $T_A$ ≤ +125°C unless otherwise specified.) $T_A = T_J$

| Parameter | Conditions | $V_S$ = ±1.5V | | | |
|---|---|---|---|---|---|
| | | $I_{SET}$ = 1 µA | | $I_{SET}$ = 10 µA | |
| | | Min | Max | Min | Max |
| $V_{OS}$ | $R_S \le 100$ kΩ, $T_A = 25°C$ | | 3 mV | | 5 mV |
| $I_{OS}$ | $T_A = 25°C$ | | 3 nA | | 10 nA |
| $I_{bias}$ | $T_A = 25°C$ | | 7.5 nA | | 50 nA |
| Large Signal Voltage Gain | $R_L = 100$ kΩ, $T_A = 25°C$<br>$V_O = \pm 0.6V$, $R_L = 10$ kΩ | 40k | | 50k | |
| Supply Current | $T_A = 25°C$ | | 7.5 µA | | 80 µA |
| Power Consumption | $T_A = 25°C$ | | 23 µW | | 240 µW |
| $V_{OS}$ | $R_S \le 100$ kΩ | | 4 mV | | 6 mV |
| $I_{OS}$ | $T_A = +125°C$<br>$T_A = -55°C$ | | 5 nA<br>3 nA | | 10 nA<br>10 nA |
| $I_{bias}$ | | | 7.5 nA | | 50 nA |
| Input Voltage Range | | ±0.6V | | ±0.6V | |
| Large Signal Voltage Gain | $V_O = \pm 0.5V$, $R_L = 100$ kΩ<br>$R_L = 10$ kΩ | 30k | | 30k | |
| Output Voltage Swing | $R_L = 100$ kΩ<br>$R_L = 10$ kΩ | ±0.6V | | ±0.6V | |
| Common Mode Rejection Ratio | $R_S \le 10$ kΩ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \le 10$ kΩ | 76 dB | | 76 dB | |
| Supply Current | | | 8 µA | | 90 µA |
| Power Consumption | | | 24 µW | | 270 µW |

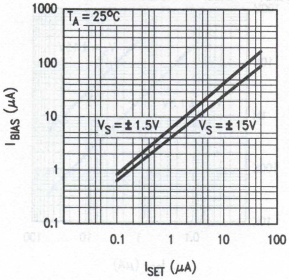
| Parameter | Conditions | $V_S$ = ±15V | | | |
|---|---|---|---|---|---|
| | | $I_{SET}$ = 1 µA | | $I_{SET}$ = 10 µA | |
| | | Min | Max | Min | Max |
| $V_{OS}$ | $R_S \le 100$ kΩ, $T_A = 25°C$ | | 3 mV | | 5 mV |
| $I_{OS}$ | $T_A = 25°C$ | | 3 nA | | 10 nA |
| $I_{bias}$ | $T_A = 25°C$ | | 7.5 nA | | 50 nA |
| Large Signal Voltage Gain | $R_L = 100$ kΩ, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 10$ kΩ | 100k | | 100k | |
| Supply Current | $T_A = 25°C$ | | 10 µA | | 90 µA |
| Power Consumption | $T_A = 25°C$ | | 300 µW | | 2.7 mW |
| $V_{OS}$ | $R_S \le 100$ kΩ | | 4 mV | | 6 mV |
| $I_{OS}$ | $T_A = +125°C$<br>$T_A = -55°C$ | | 25 nA<br>3 nA | | 25 nA<br>10 nA |
| $I_{bias}$ | | | 7.5 nA | | 50 nA |
| Input Voltage Range | | ±13.5V | | ±13.5V | |
| Large Signal Voltage Gain | $V_O = \pm 10V$, $R_L = 100$ kΩ<br>$R_L = 10$ kΩ | 50k | | 50k | |
| Output Voltage Swing | $R_L = 100$ kΩ<br>$R_L = 10$ kΩ | ±12V | | ±12V | |
| Common Mode Rejection Ratio | $R_S \le 10$ kΩ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \le 10$ kΩ | 76 dB | | 76 dB | |
| Supply Current | | | 11 µA | | 100 µA |
| Power Consumption | | | 330 µW | | 3 mW |

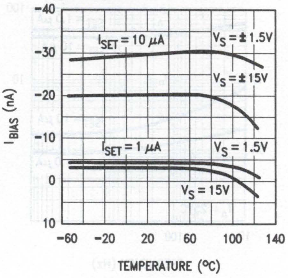
## Electrical Characteristics LM4250C ($-55^\circ C \le T_A \le +125^\circ C$ unless otherwise specified.) $T_A = T_J$

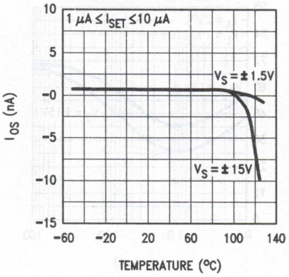
| Parameter | Conditions | $V_S = \pm 1.5V$ | | | |
|---|---|---|---|---|---|
| | | $I_{SET} = 1\ \mu A$ | | $I_{SET} = 10\ \mu A$ | |
| | | Min | Max | Min | Max |
| $V_{OS}$ | $R_S \le 100\ k\Omega$, $T_A = 25^\circ C$ | | 5 mV | | 6 mV |
| $I_{OS}$ | $T_A = 25^\circ C$ | | 6 nA | | 20 nA |
| $I_{bias}$ | $T_A = 25^\circ C$ | | 10 nA | | 75 nA |
| Large Signal Voltage Gain | $R_L = 100\ k\Omega$, $T_A = 25^\circ C$<br>$V_O = \pm 0.6V$, $R_L = 10\ k\Omega$ | 25k | | 25k | |
| Supply Current | $T_A = 25^\circ C$ | | 8 $\mu A$ | | 90 $\mu A$ |
| Power Consumption | $T_A = 25^\circ C$ | | 24 $\mu W$ | | 270 $\mu W$ |
| $V_{OS}$ | $R_S \le 10\ k\Omega$ | | 6.5 mV | | 7.5 mV |
| $I_{OS}$ | | | 8 nA | | 25 nA |
| $I_{bias}$ | | | 10 nA | | 80 nA |
| Input Voltage Range | | ±0.6V | | ±0.6V | |
| Large Signal Voltage Gain | $V_O = \pm 0.5V$, $R_L = 100\ k\Omega$<br>$R_L = 10\ k\Omega$ | 25k | | 25k | |
| Output Voltage Swing | $R_L = 100\ k\Omega$<br>$R_L = 10\ k\Omega$ | ±0.6V | | ±0.6V | |
| Common Mode Rejection Ratio | $R_S \le 10\ k\Omega$ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \le 10\ k\Omega$ | 74 dB | | 74 dB | |
| Supply Current | | | 8 $\mu A$ | | 90 $\mu A$ |
| Power Consumption | | | 24 $\mu W$ | | 270 $\mu W$ |

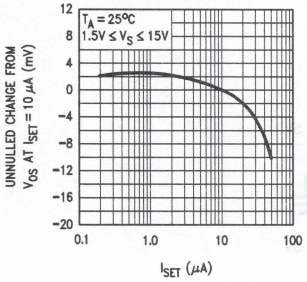
| Parameter | Conditions | $V_S = \pm 15V$ | | | |
|---|---|---|---|---|---|
| | | $I_{SET} = 1\ \mu A$ | | $I_{SET} = 10\ \mu A$ | |
| | | Min | Max | Min | Max |
| $V_{OS}$ | $R_S \le 100\ k\Omega$, $T_A = 25^\circ C$ | | 5 mV | | 6 mV |
| $I_{OS}$ | $T_A = 25^\circ C$ | | 6 nA | | 20 nA |
| $I_{bias}$ | $T_A = 25^\circ C$ | | 10 nA | | 75 nA |
| Large Signal Voltage Gain | $R_L = 100\ k\Omega$, $T_A = 25^\circ C$<br>$V_O = \pm 10V$, $R_L = 10\ k\Omega$ | 60k | | 60k | |
| Supply Current | $T_A = 25^\circ C$ | | 11 $\mu A$ | | 100 $\mu A$ |
| Power Consumption | $T_A = 25^\circ C$ | | 330 $\mu W$ | | 3 mW |
| $V_{OS}$ | $R_S \le 100\ k\Omega$ | | 6.5 mV | | 7.5 mV |
| $I_{OS}$ | | | 8 nA | | 25 nA |
| $I_{bias}$ | | | 10 nA | | 80 nA |
| Input Voltage Range | | ±13.5V | | ±13.5V | |
| Large Signal Voltage Gain | $V_O = \pm 10V$, $R_L = 100\ k\Omega$<br>$R_L = 10\ k\Omega$ | 50k | | 50k | |
| Output Voltage Swing | $R_L = 100\ k\Omega$<br>$R_L = 10\ k\Omega$ | ±12V | | ±12V | |
| Common Mode Rejection Ratio | $R_S \le 10\ k\Omega$ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \le 10\ k\Omega$ | 74 dB | | 74 dB | |
| Supply Current | | | 11 $\mu A$ | | 100 $\mu A$ |
| Power Consumption | | | 330 $\mu W$ | | 3 mW |

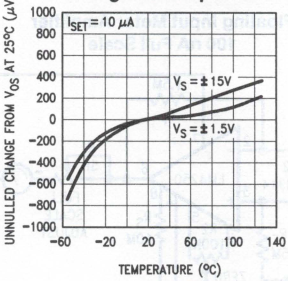
## Typical Performance Characteristics

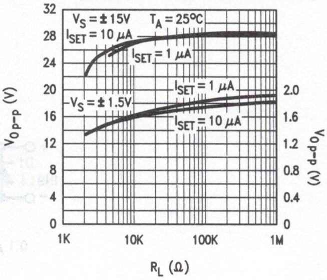

Input Bias Current vs $I_{SET}$

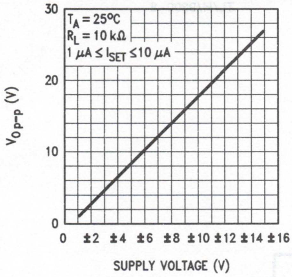

Input Bias Current vs Temperature

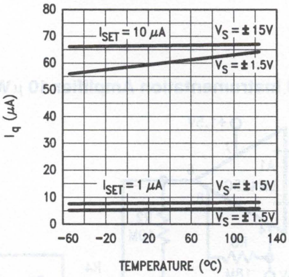

Input Offset Current vs Temperature

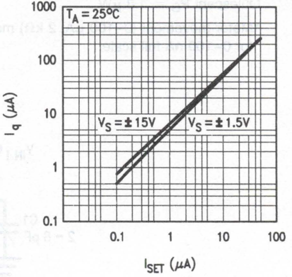

Unnulled Input Offset Voltage Change vs $I_{SET}$

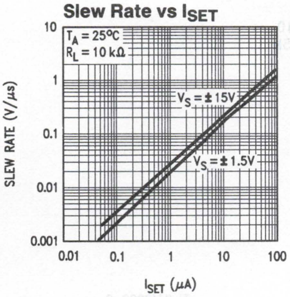

Unnulled Input Offset Voltage Change vs Temperature

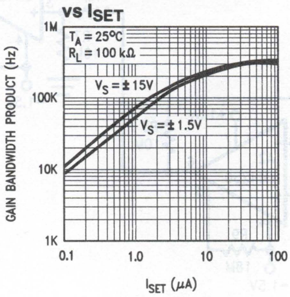

Peak to Peak Output Voltage Swing vs Load Resistance

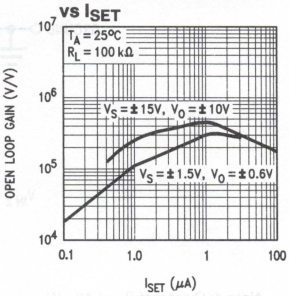

Peak to Peak Output Voltage Swing vs Supply Voltage


Quiescent Current ($I_q$) vs Temperature


Quiescent Current ($I_q$) vs $I_{SET}$


Slew Rate vs $I_{SET}$


Gain Bandwidth Product vs $I_{SET}$


Open Loop Voltage Gain vs $I_{SET}$

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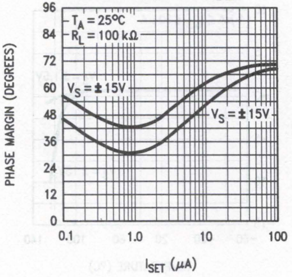
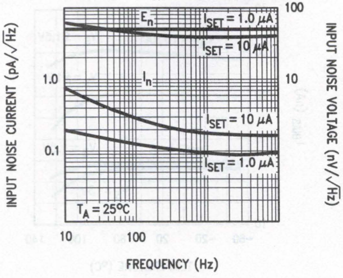
## Typical Performance Characteristics (Continued)

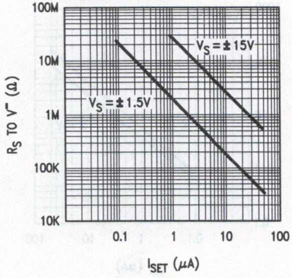
### Phase Margin vs $I_{SET}$



### Input Noise Current ($I_n$) and Voltage ($E_n$) vs Frequency



### $R_{SET}$ vs $I_{SET}$



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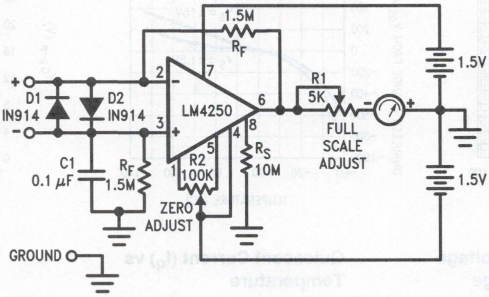
## Typical Applications (Continued)

### Floating Input Meter Amplifier 100 nA Full Scale

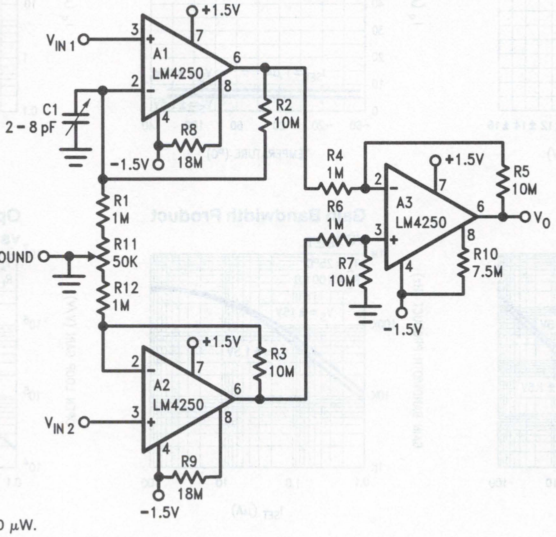

1.5M
$R_F$
+
−
D1
IN914
D2
IN914
C1
0.1 µF
$R_F$
1.5M
2
3
7
6
LM4250
5
1
4
8
R2
100K
ZERO ADJUST
$R_S$
10M
R1
5K
FULL SCALE ADJUST
1.5V
1.5V
GROUND

TL/H/9300-8

Quiescent $P_D$ = 1.8 µW

*Meter movement (0–100 µA, 2 kΩ) marked for 0–100 nA full scale.

### X100 Instrumentation Amplifier 10 µW


+1.5V
$V_{IN\ 1}$
3
2
7
6
8
4
A1
LM4250
C1
2 – 8 pF
R8
18M
−1.5V
R2
10M
R1
1M
R11
50K
GROUND
R12
1M
R4
1M
R6
1M
R7
10M
+1.5V
A3
LM4250
R5
10M
$V_O$
R10
7.5M
−1.5V
+1.5V
R3
10M
A2
LM4250
$V_{IN\ 2}$
R9
18M
−1.5V

TL/H/9300-9

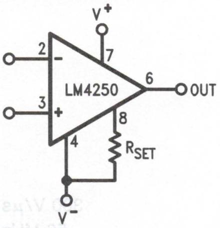
**Note 1:** Quiescent $P_D$ = 10 µW.

**Note 2:** R2, R3, R4, R5, R6 and R7 are 1% resistors.

**Note 3:** R11 and C1 are for DC and AC common mode rejection adjustments.

## Typical Applications (Continued)

**$R_{SET}$ Connected to V−**


V+
2
7
−
6
LM4250
OUT
3
+
8
4
RSET
V−

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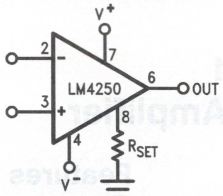
**$R_{SET}$ Connected to Ground**


V+
2
7
−
6
LM4250
OUT
3
+
8
4
RSET
V−

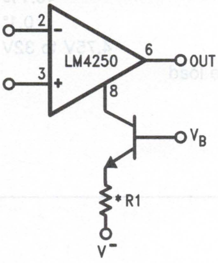
TL/H/9300–11

$I_{SET}$ Equations:

$$I_{SET} \approx \frac{V^{+} + |V^{-}| - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to } V^{-}.$$

$$I_{SET} \approx \frac{V^{+} - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to ground.}$$

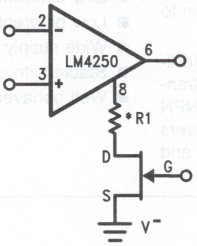
**Transistor Current Sourcing Biasing**


2
−
LM4250
6
OUT
3
+
8
VB
*R1
V−

*R1 limits $I_{SET}$ maximum

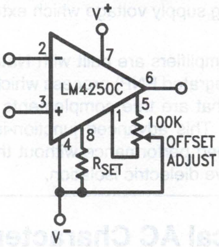
TL/H/9300–12

**FET Current Sourcing Biasing**


2
−
LM4250
6
3
+
8
*R1
D
G
VG
S
V−

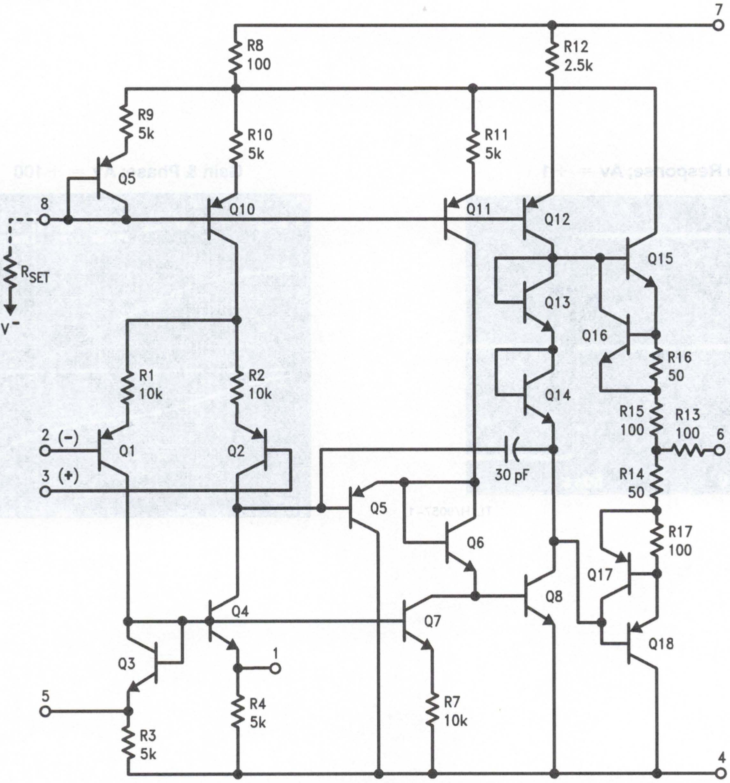
TL/H/9300–13

**Offset Null Circuit**


V+
2
7
−
6
LM4250C
3
+
5
1
100K
OFFSET ADJUST
4
8
RSET
V−

TL/H/9300–14

## Schematic Diagram


7
R8
100
R12
2.5k
R9
5k
R10
5k
R11
5k
Q5
8
Q10
Q11
Q12
R5
RSET
V−
Q15
Q13
Q16
R16
50
R1
10k
R2
10k
Q14
R15
100
R13
100
6
2 (−)
Q1
Q2
30 pF
3 (+)
R14
50
Q5
Q6
R17
100
Q17
Q8
Q4
Q7
Q18
Q3
1
5
R4
5k
R7
10k
R3
5k
4

TL/H/9300–1

**National Semiconductor Corporation**

**PRELIMINARY**

# LM6161/LM6261/LM6361 High Speed Operational Amplifier

## General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

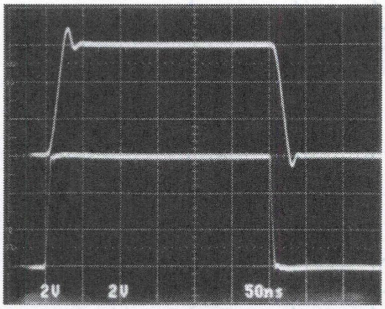
These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

## Features

| | |
|---|---|
| ■ High slew rate | 300 V/μs |
| ■ High unity gain freq | 50 MHz |
| ■ Low supply current | 5 mA |
| ■ Fast settling | 120 ns to 0.1% |
| ■ Low differential gain | <0.1% |
| ■ Low differential phase | 0.1° |
| ■ Wide supply range | 4.75V to 32V |
| ■ Stable with unlimited capacitive load | |
| ■ Well behaved; easy to apply | |

## Typical AC Characteristics

**Step Response; Av = +1**



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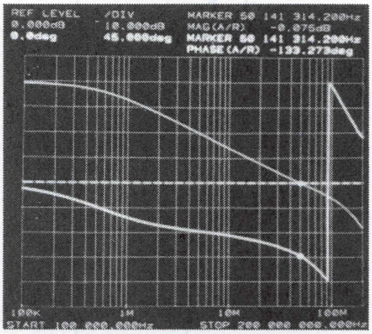
**Gain & Phase; Av = +100**



TL/H/9057-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (V+ − V−) | 36V |
| Differential Input Voltage (Note 8) | ±8V |
| CM Voltage | (V+ − 0.7V) to (V− − 7V) |
| Output Short Circuit to GND (Note 1) | Continuous |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

| | |
|---|---|
| Storage Temp Range | −65°C to +150°C |
| Operating Temperature Range (Note 2) | |
| LM6161 | −55°C to +125°C |
| LM6261 | −25°C to +85°C |
| LM6361 | 0°C to +70°C |
| Max Junction Temperature | 150°C |
| ESD Tolerance (Notes 8 and 9) | ±700V |
| Operating Supply Voltage Range | 4.75V to 32V |

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LM6161 Tested Limit (Note 4) | LM6161 Design Limit (Note 5) | LM6261 Tested Limit (Note 4) | LM6261 Design Limit (Note 5) | LM6361 Tested Limit (Note 4) | LM6361 Design Limit (Note 5) | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | 5 | 7<br>**10** | | 7 | **9** | 20 | **22** | mV max |
| Input Offset Voltage Average Drift | | 10 | | | | | | | μV/°C |
| Input Bias Current | | 2 | 3<br>**6** | | 3 | **5** | 5 | **6** | μA max |
| Input Offset Current | | 150 | 350<br>**800** | | 350 | **600** | 1500 | **1900** | nA max |
| Input Offset Current Average Drift | | 0.4 | | | | | | | nA/°C |
| Input Resistance | Differential | 325 | | | | | | | kΩ |
| Input Capacitance | Av = +1 @ 10 MHz | 1.5 | | | | | | | pF |
| Large Signal Voltage Gain | $V_{OUT}$ = ±10V, $R_L$ = 2 kΩ (Note 11) | 750 | 550<br>**300** | | 550 | **400** | 400 | **350** | V/V min |
| | $R_L$ = 10 kΩ | 2900 | | | | | | | V/V |
| Input Common-Mode Voltage Range | Supply = ±15V | +14.0 | +13.9<br>**+13.8** | | +13.9 | **+13.8** | +13.8 | **+13.7** | Volts min |
| | | −13.2 | −12.9<br>**−12.7** | | −12.9 | **−12.7** | −12.8 | **−12.7** | Volts min |
| | Supply = +5V (Note 6) | 4.0 | 3.9<br>**3.8** | | 3.9 | **3.8** | 3.8 | **3.7** | Volts min |
| | | 1.8 | 2.0<br>**2.2** | | 2.0 | **2.2** | 2.1 | **2.2** | Volts max |
| Common-Mode Rejection Ratio | −10V ≤ $V_{CM}$ ≤ +10V | 94 | 80<br>**74** | | 80 | **76** | 72 | **70** | dB min |
| Power Supply Rejection Ratio | ±10V ≤ V± ≤ ±16V | 90 | 80<br>**74** | | 80 | **76** | 72 | **70** | dB min |
| Output Voltage Swing | Supply = ±15V and $R_L$ = 2 kΩ | +14.2 | +13.5<br>**+13.3** | | +13.5 | **+13.3** | +13.4 | **+13.3** | Volts min |
| | | −13.4 | −13.0<br>**−12.7** | | −13.0 | **−12.8** | −12.9 | **−12.8** | Volts min |
| | Supply = +5V and $R_L$ = 2 kΩ (Note 6) | 4.2 | 3.5<br>**3.3** | | 3.5 | **3.3** | 3.4 | **3.3** | Volts min |
| | | 1.3 | 1.7<br>**2.0** | | 1.7 | **1.9** | 1.8 | **1.9** | Volts max |
| Output Short Circuit Current | Souce | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA min |
| | Sink | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA min |
| Supply Current | | 5.0 | 6.5<br>**6.8** | | 6.5 | **6.7** | 6.8 | **6.9** | mA max |

## AC Electrical Characteristics (Notes 3 & 7)

| Parameter | Conditions | Typ | LM6161 | | LM6261 | | LM6361 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Gain-Bandwidth Product | @ F = 20 MHz | 50 | 40<br>**32** | | 40 | **35** | 35 | **32** | MHZ min |
| | $V^+ = \pm 5V$ | 35 | | | | | | | MHz |
| Slew Rate | Av = +1 (Note 10) | 300 | 225<br>**200** | | 225 | **210** | 200 | **180** | V/$\mu$s min |
| | $V^+ = \pm 5V$ | 200 | | | | | | | V/$\mu$s |
| Power Bandwidth | $V_{OUT} = 20\ V_{pp}$ | 4.5 | | | | | | | MHz |
| Settling Time | 10V Step to 0.1%<br>Av = −1, $R_L = 2\ k\Omega$ | 120 | | | | | | | ns |
| Phase Margin | | 45 | | | | | | | Deg |
| Differential Gain | NTSC, Av = +4 | <0.1 | | | | | | | % |
| Differential Phase | NTSC, Av = +4 | 0.1 | | | | | | | Deg |
| Input Noise Voltage | f = 10 kHz | 15 | | | | | | | nV/√Hz |
| Input Noise Current | f = 10 kHz | 1.5 | | | | | | | pA/√Hz |

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, the cerdip (J) package is 125°C/W, and the TO-5 (H) package is 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Unless otherwise specified, all limits guaranteed for $T_A = T_j = 25°C$ with supply voltage = ±15V, $V_{CM} = 0V$, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_j$ in the "Absolute Maximum Ratings" section.

**Note 4:** Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

**Note 5:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

**Note 6:** For single supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 ($V^-$) to realize maximum output swing. This connection will degrade $V_{OS}$, $V_{OS}$ Drift, and Input Voltage Noise.

**Note 7:** $C_L \leq 5$ pF.

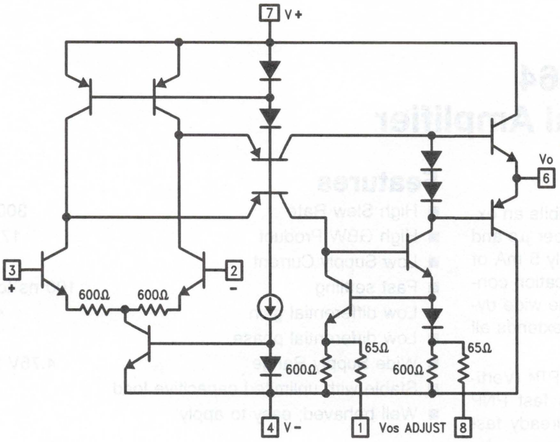
**Note 8:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

**Note 9:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

**Note 10:** $V_{IN} = 8V$ step. For $V^+ = \pm 5V$, $V_{IN} = 5V$ step.

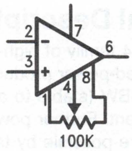
**Note 11:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

## Simplified Schematic and Pin Assignments


7 V+
Vo
6
3
+
2
-
600Ω
600Ω
65Ω
600Ω
600Ω
65Ω
4 V-
1 Vos ADJUST 8

TL/H/9057-3

**$V_{OS}$ Adjust Circuit**


2
3
-
+
7
6
8
4
1
100K

TL/H/9057-4

National
Semiconductor
Corporation

**PRELIMINARY**

# LM6164/LM6264/LM6364
# High Speed Operational Amplifier

## General Description

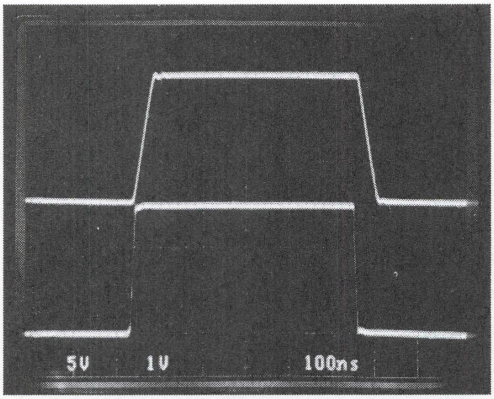
The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable to a gain of +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

## Features

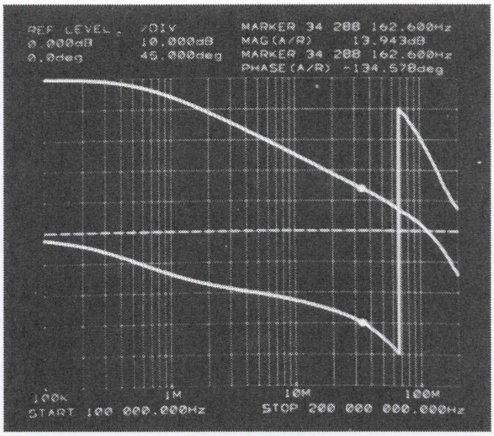
| | |
|---|---|
| ■ High Slew Rate | 300 V/μs |
| ■ High GBW Product | 175 MHz |
| ■ Low Supply Current | 5 mA |
| ■ Fast settling | 100 ns to 0.1% |
| ■ Low differential gain | <0.1% |
| ■ Low differential phase | <0.1° |
| ■ Wide Supply Range | 4.75V to 32V |
| ■ Stable with unlimited capacitive load | |
| ■ Well behaved; easy to apply | |

## Typical AC Characteristics



TL/H/9153-1

**Step Response; $A_V = +5$**



TL/H/9153-2

**Gain & Phase; $A_V = +300$**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 8) | ±8V |
| CM Input Voltage | ($V^+$ − 0.7V) to ($V^-$ − 7V) |
| Output Short Circuit to Gnd (Note 1) | Continuous |
| Lead Temp. (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range (Note 2) | |
| LM6164 | −55°C to +125°C |
| LM6264 | −25°C to +85°C |
| LM6364 | 0°C to +70°C |
| Max Junction Temperature (Note 2) | 150°C |
| ESD Tolerance (Notes 8 & 9) | ±700V |

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LM6164 | | LM6264 | | LM6364 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Input Offset Voltage | | 2 | 4<br>**6** | | 4 | **6** | 9 | **11** | mV<br>max |
| Input Offset Voltage Average Drift | | 6 | | | | | | | μV/°C |
| Input Bias Current | | 2.5 | 3<br>**6** | | 3 | **5** | 5 | **6** | μA<br>max |
| Input Offset Current | | 150 | 350<br>**800** | | 350 | **600** | 1500 | **1900** | nA<br>max |
| Input Offset Current Average Drift | | 0.3 | | | | | | | nA/°C |
| Input Resistance | Differential | 100 | | | | | | | kΩ |
| Input Capacitance | | 3.0 | | | | | | | pF |
| Large Signal Voltage Gain | $V_{OUT}$ = ±10V, $R_L$ = 2 kΩ (Note 11) | 2.5 | 1.8<br>**0.9** | | 1.8 | **1.2** | 1.3 | **1.1** | V/mV<br>min |
| | $R_L$ = 10 kΩ | 9 | | | | | | | |
| Input Common-Mode Voltage Range | Supply = ±15V | +14.0 | +13.9<br>+**13.8** | | +13.9 | +**13.8** | +13.8 | +**13.7** | V<br>min |
| | | −13.5 | −13.3<br>−**13.1** | | −13.3 | −**13.1** | −13.2 | −**13.1** | V<br>min |
| | Supply = +5V (Note 6) | 4.0 | 3.9<br>**3.8** | | 3.9 | **3.8** | 3.8 | **3.7** | V<br>min |
| | | 1.5 | 1.7<br>**1.9** | | 1.7 | **1.9** | 1.8 | **1.9** | V<br>max |
| Common-Mode Rejection Ratio | −10V ≤ $V_{CM}$ ≤ +10V | 105 | 86<br>**80** | | 86 | **82** | 80 | **78** | dB<br>min |
| Power Supply Rejection Ratio | ±10V ≤ V± ≤ ±16V | 96 | 86<br>**80** | | 86 | **82** | 80 | **78** | dB<br>min |
| Output Voltage Swing | Supply = ±15V and $R_L$ = 2 kΩ | +14.2 | +13.5<br>+**13.3** | | +13.5 | +**13.3** | +13.4 | +**13.3** | V<br>min |
| | | −13.4 | −13.0<br>−**12.7** | | −13.0 | −**12.8** | −12.9 | −**12.8** | V<br>min |
| | Supply = +5V and $R_L$ = 2 kΩ (Note 6) | 4.2 | 3.5<br>**3.3** | | 3.5 | **3.3** | 3.4 | **3.3** | V<br>min |
| | | 1.3 | 1.7<br>**2.0** | | 1.7 | **1.9** | 1.8 | **1.9** | V<br>max |

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LM6164 Tested Limit (Note 4) | LM6164 Design Limit (Note 5) | LM6264 Tested Limit (Note 4) | LM6264 Design Limit (Note 5) | LM6364 Tested Limit (Note 4) | LM6364 Design Limit (Note 5) | Units |
|---|---|---|---|---|---|---|---|---|---|
| Output Short Circuit Current | Source | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA<br>min |
| | Sink | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA<br>min |
| Supply Current | | 5.0 | 6.5<br>**6.8** | | 6.5 | **6.7** | 6.8 | **6.9** | mA<br>max |

## AC Electrical Characteristics (Notes 3 & 7)

| Parameter | Conditions | Typ | LM6164 Tested Limit (Note 4) | LM6164 Design Limit (Note 5) | LM6264 Tested Limit (Note 4) | LM6264 Design Limit (Note 5) | LM6364 Tested Limit (Note 4) | LM6364 Design Limit (Note 5) | Units |
|---|---|---|---|---|---|---|---|---|---|
| Gain-Bandwidth Product | @ F = 20 MHz | 175 | 140<br>**100** | | 140 | **120** | 120 | **100** | MHz<br>min |
| | V+ = ±5V | 120 | | | | | | | |
| Slew Rate | $A_V$ = +20 (Note 10) | 300 | 225<br>**200** | | 225 | **210** | 200 | **180** | V/µs<br>min |
| | V+ = ±5V | 200 | | | | | | | |
| Power Bandwidth | $V_{OUT}$ = 20 $V_{PP}$ | 4.5 | | | | | | | MHz |
| Setting Time | 10V Step to 0.1%<br>$A_V = -4$, $R_L = 2\ k\Omega$ | 100 | | | | | | | ns |
| Phase Margin | $A_V$ = +5 | 45 | | | | | | | Deg |
| Differential Gain | NTSC, $A_V$ = +10 | <0.1 | | | | | | | % |
| Differential Phase | NTSC, $A_V$ = +10 | <0.1 | | | | | | | Deg |
| Input Noise Voltage | F = 10 kHz | 8 | | | | | | | nV/√Hz |
| Input Noise Current | F = 10 kHz | 1.5 | | | | | | | pA/√Hz |

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, the cerdip (J) package is 125°C/Watt, and the TO-5 (H) package is 155°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Unless otherwise specified, all limits guranteed for $T_A = T_J = 25°C$ with supply voltage = ±15V, $V_{CM}$ = 0V, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range".

**Note 4:** Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

**Note 5:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

**Note 6:** For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, $V_{CM}$ = 2.5V, $V_{OUT}$ = 2.5V. Pin 1 & Pin 8 ($V_{OS}$ Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade $V_{OS}$.

**Note 7:** $C_L \leq 5$ pF.

**Note 8:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially $V_{OS}$, $I_{OS}$, and Noise).

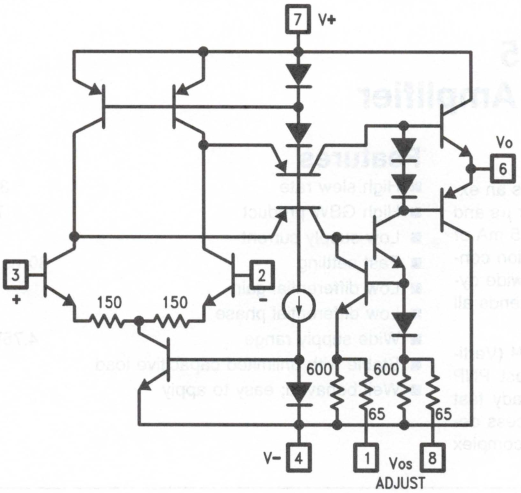
**Note 9:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

**Note 10:** $V_{IN}$ = 4V step. For V+ = ±5V, $V_{IN}$ = 1V step.

**Note 11:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

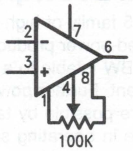
## Simplified Schematic & Pin Assignments

### Dual-In-Line Package


7
V+
Vo
6
3
+
2
-
150
150
600
600
65
65
V-
4
1
Vos
8
ADJUST

TL/H/9153–3

### $V_{OS}$ Adjust Circuit


2
-
7
6
3
+
4
8
1
100K

TL/H/9153–4

**Order Number LM6264J, LM6164J, LM6364N or LM6264N**
**See NS Package Number J08A or N08E**

**National Semiconductor Corporation**

**PRELIMINARY**

# LM6165/LM6265/LM6365
# High Speed Operational Amplifier

## General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V per μs and 725 MHz GBW (stable to a gain of +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

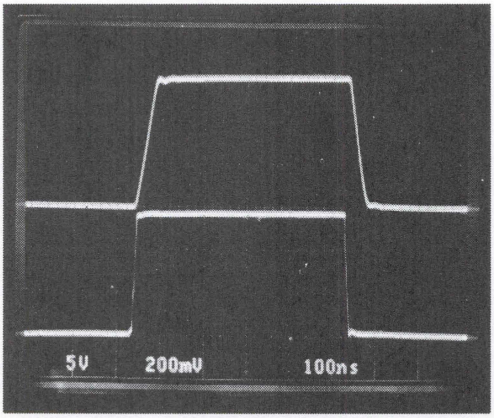
These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

## Features

| | |
|---|---|
| ■ High slew rate | 300 V/μs |
| ■ High GBW product | 725 MHz |
| ■ Low supply current | 5 mA |
| ■ Fast settling | 80 ns to 0.1% |
| ■ Low differential gain | <0.1% |
| ■ Low differential phase | <0.1° |
| ■ Wide supply range | 4.75V to 32V |
| ■ Stable with unlimited capacitive load | |
| ■ Well behaved; easy to apply | |

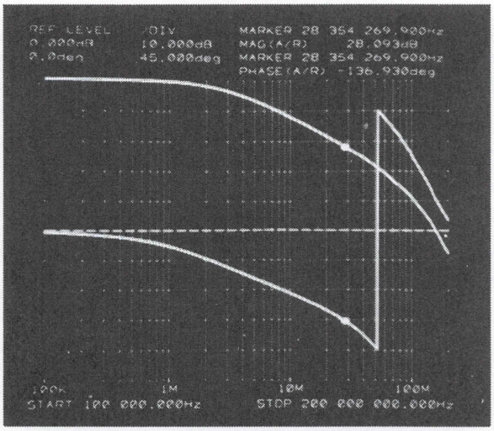
## Typical AC Characteristics

**Step Response; $A_V = +25$**



TL/H/9152-1

**Gain & Phase; $A_V = +300$**



TL/H/9152-2

## Absolute Maximum Rating

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 8) | ±8V |
| CM Input Voltage | ($V^+$ −0.7V) To ($V^-$ − 7V) |
| Output Short Circuit to Gnd (Note 1) | Continuous |
| Lead Temp (Soldering, 10 sec.) | 260°C |
| Storage Temp Range | −65°C to 150°C |
| Operating Temperature Range (Note 2) | |
| LM6165 | −55°C to +125°C |
| LM6265 | −25°C to +85°C |
| LM6365 | 0°C to 70°C |
| Max Junction Temperature (Note 2) | 150°C |
| ESD Tolerance (Notes 8 & 9) | ±700V |

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LM6165 Tested Limit (Note 4) | LM6165 Design Limit (Note 5) | LM6265 Tested Limit (Note 4) | LM6265 Design Limit (Note 5) | LM6365 Tested Limit (Note 4) | LM6365 Design Limit (Note 5) | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | 1 | 3<br>**4** | | 3 | **4** | 6 | **7** | mV<br>max |
| Input Offset Voltage Average Drift | | 3 | | | | | | | μV/°C |
| Input Bias Current | | 2.5 | 3<br>**6** | | 3 | **5** | 5 | **6** | μA<br>max |
| Input Offset Current | | 150 | 350<br>**800** | | 350 | **600** | 1500 | **1900** | na<br>max |
| Input Offset Current Average Drift | | 0.3 | | | | | | | nA/°C |
| Input Resistance | Differential | 20 | | | | | | | kΩ |
| Input Capacitance | | 6.0 | | | | | | | pF |
| Large Signal Voltage Gain | $V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 11) | 10.5 | 7.5<br>**5.0** | | 7.5 | **6.0** | 5.5 | **5.0** | V/mV<br>min |
| | $R_L = 10\ k\Omega$ | 38 | | | | | | | |
| Input Common-Mode Voltage Range | Supply = ±15V | +14.0 | +13.9<br>**+13.8** | | +13.9 | **+13.8** | +13.8 | **+13.7** | V<br>min |
| | | −13.6 | −13.4<br>**−13.2** | | −13.4 | **−13.2** | −13.3 | **−13.2** | V<br>min |
| | Supply = +5V (Note 6) | 4.0 | 3.9<br>**3.8** | | 3.9 | **3.8** | 3.8 | **3.7** | V<br>min |
| | | 1.4 | 1.6<br>**1.8** | | 1.6 | **1.8** | 1.7 | **1.8** | V<br>max |
| Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 102 | 88<br>**82** | | 88 | **84** | 80 | **78** | dB<br>min |
| Power Supply Rejection Ratio | $\pm 10V \leq V\pm \leq \pm 16V$ | 104 | 88<br>**82** | | 88 | **84** | 80 | **78** | dB<br>min |
| Output Voltage Swing | Supply = ±15V and $R_L = 2\ k\Omega$ | +14.2 | +13.5<br>**+13.3** | | +13.5 | **+13.3** | +13.4 | **+13.3** | V<br>min |
| | | −13.4 | −13.0<br>**−12.7** | | −13.0 | **−12.8** | −12.9 | **−12.8** | V<br>min |
| | Supply = +5V and $R_L = 2\ k\Omega$ (Note 6) | 4.2 | 3.5<br>**3.3** | | 3.5 | **3.3** | 3.4 | **3.3** | V<br>min |
| | | 1.3 | 1.7<br>**2.0** | | 1.7 | **1.9** | 1.8 | **1.9** | V<br>max |

## DC Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | Typ | LM6165 | | LM6265 | | LM6365 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit | Design Limit | Tested Limit | Design Limit | Tested Limit | Design Limit | |
| | | | (Note 4) | (Note 5) | (Note 4) | (Note 5) | (Note 4) | (Note 5) | |
| Output Short Circuit Current | Source | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA<br>min |
| | Sink | 65 | 30<br>**20** | | 30 | **25** | 30 | **25** | mA<br>min |
| Supply Current | | 5.0 | 6.5<br>**6.8** | | 6.5 | **6.7** | 6.8 | **6.9** | mA<br>max |

## AC Electrical Characteristics (Notes 3 & 7)

| Parameter | Conditions | Typ | LM6165 | | LM6265 | | LM6365 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit | Design Limit | Tested Limit | Design Limit | Tested Limit | Design Limit | |
| | | | (Note 4) | (Note 5) | (Note 4) | (Note 5) | (Note 4) | (Note 5) | |
| Gain-Bandwidth Product | @ F = 20 MHz | 725 | 575<br>**400** | | 575 | **475** | 500 | **400** | MHz<br>min |
| | $V+ = \pm 5V$ | 500 | | | | | | | |
| Slew Rate | $A_V = +25$ (Note 10) | 300 | 225<br>**200** | | 225 | **210** | 200 | **180** | V/µs<br>min |
| | $V+ = \pm 5V$ | 200 | | | | | | | |
| Power Bandwidth | $V_{OUT} = 20\ V_{PP}$ | 4.5 | | | | | | | MHz |
| Setting Time | 10V Step to 0.1%<br>$A_V = -25, R_L = 2\ k\Omega$ | 80 | | | | | | | ns |
| Phase Margin | $A_V = +25$ | 45 | | | | | | | Deg |
| Differential Gain | NTSC, $A_V = +25$ | <0.1 | | | | | | | % |
| Differential Phase | NTSC, $A_V = +25$ | <0.1 | | | | | | | Deg |
| Input Noise Voltage | F = 10 kHz | 5 | | | | | | | nV/√Hz |
| Input Noise Current | F = 10 kHz | 1.5 | | | | | | | pA/√Hz |

**Note 1:** Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 2:** The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, the cerdip (J) package is 125°C/Watt, and the TO-5 (H) package is 155°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

**Note 3:** Unless otherwise specified, all limits guaranteed for $T_a = T_j = 25°C$ with supply voltage = ±15V, $V_{CM} = 0V$, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range".

**Note 4:** Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

**Note 5:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

**Note 6:** For single supply operation, the following conditions apply: $V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5C$, $V_{OUT} = 2.5V$. Pin 1 & Pin 8 ($V_{OS}$ Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade $V_{OS}$.

**Note 7:** $C_L \leq 5$ pF.

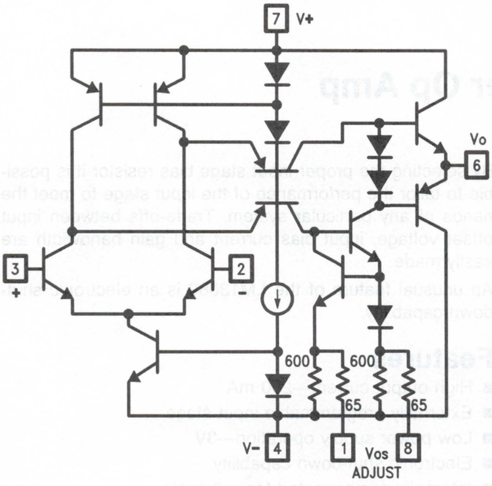
**Note 8:** In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exeeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially $V_{OS}$, $I_{OS}$, and Noise).

**Note 9:** The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

**Note 10:** $V_{IN} = 0.7V$ step. For $V+ = \pm 5V$, $V_{IN} = 0.2V$ step.

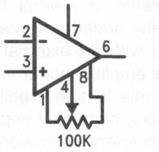
**Note 11:** Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

## Simplified Schematic & Pin Assignments


7
V+
Vo
6
3
+
2
600
600
65
65
V−
4
1
Vos
ADJUST
8

TL/H/9152–3

**V$_{OS}$ Adjust Circuit**


2
7
6
3
−
+
1
4
8
100K

TL/H/9152–4

**Order Number LM6165J, LM6265J, LM6265N or LM6365N**
**See NS Package Number J08A or N08E**

National Semiconductor Corporation

# LM13080 Programmable Power Op Amp

## General Description

The LM13080 is an internally compensated medium power operational amplifier designed for use in those applications requiring load currents of several hundred milliamperes. This amplifier has the added advantage of having an input stage programmed with an external resistor. The user is able to optimize the amplifier performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifiers, DC-to-DC converters, precision power comparators which can either sink or source current and motor speed controls.

The LM13080 may be powered from either single or dual power supplies, and will operate from as little as 3V.

As a power operational amplifier, the LM13080 is capable of delivering 0.25A to a load. This feature allows the system designer to fulfill his medium power circuit requirements without having to add external current boost transistors to the output of a standard operational amplifier.

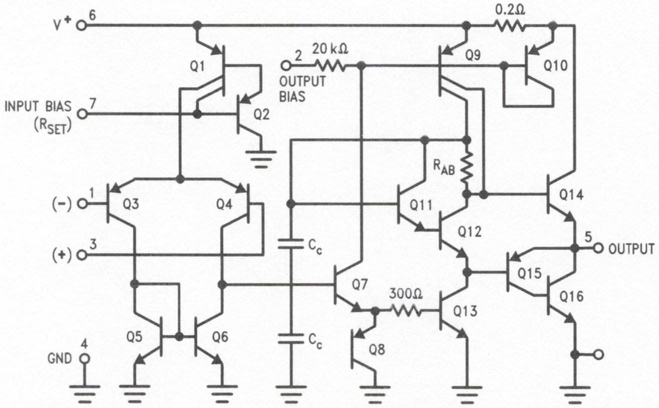
By selecting the proper input stage bias resistor it is possible to tailor the performance of the input stage to meet the needs of any particular system. Trade-offs between input offset voltage, input bias current and gain bandwidth are easily made.

An unusual feature of the LM13080 is an electronic shut-down capability.

## Features

- High output current—250 mA
- Externally programmable input stage
- Low power supply operation—3V
- Electronic shut-down capability
- Internally compensated for unity gain
- Low input bias current

## Schematic Diagram

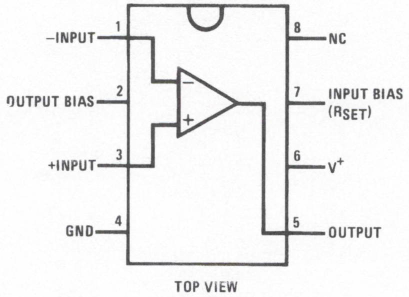


TL/H/7978-2

## Connection Diagram

**Order Number LM13080N**
**See NS Package Number N08E**

**Dual-In-Line Package**



TL/H/7978–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage Operation Range | 3V to 15V<br>±1.5V to ±7.5V |
| Power Dissipation (Note 1) | 1250 mW |
| Differential Input Voltage (Note 2) | 15V |
| Input Voltage Range (Note 3) | −0.3V to +15V |
| Input Current ($V_{IN} \le -0.3V$) (Note 4) | 20 mA |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## Electrical Characteristics

$V_S = 12V$, $R_{SET} = 680k$, $0°C \le T_A \le 70°C$, unless otherwise specified

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ (Note 5) | | ±3 | ±7 | mV |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$ | | 100 | 400 | nA |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$ | | ±30 | ±75 | nA |
| Supply Current | $R_L = \infty$, $T_A = 25°C$ (Note 6) | | 3 | 6 | mA |
| Output Voltage Swing | $V_S = \pm 6V$, $T_A = 25°C$ (Note 1) | | | | |
| $V_{OH}$ | $R_L = 50\Omega$ | 4.5 | 5 | | V |
| | $R_L = 8\Omega$ | 2 | | | V |
| $V_{OL}$ | $R_L = 50\Omega$ | | −5 | −4.5 | V |
| | $R_L = 8\Omega$ | | | −2 | V |
| Large Signal Voltage Gain | $V_S = \pm 6V$, $R_L = 50\Omega$,<br>f = 100 Hz, $T_A = 25°C$ | 3 | 10 | | V/mV |
| Input Common-Mode Voltage Range | $V_S \le 15V$, $T_A = 25°C$ (Note 3) | 1 | | $V_S - 1.5$ | V |
| Input Offset Voltage | (Note 5) | | | ±10 | mV |
| Input Offset Voltage Drift | | | 5 | | μV/°C |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ | | | 600 | nA |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$ | | | ±150 | nA |
| Input Offset Current Drift | | | 50 | | pA/°C |
| Supply Current | $R_L = \infty$ (Note 6) | | | 8 | mA |
| Output Voltage Swing | $V_S = \pm 6V$ (Note 1) | | | | |
| $V_{OH}$ | $R_L = 50\Omega$ | | | 4 | V |
| | $R_L = 8\Omega$ | | | 1.6 | V |
| $V_{OL}$ | $R_L = 50\Omega$ | −4 | | | V |
| | $R_L = 8\Omega$ | −1.6 | | | V |

## Electrical Characteristics $V_S = 12V$, $R_{SET} = 680k$, $0°C \le T_A \le 70°C$, unless otherwise specified (Continued)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Large Signal Voltage Gain | $V_S = \pm 6V$, $R_L = 50\Omega$, f = 100 Hz | 1 | | | V/mV |
| Input Common-Mode Voltage Range | $V_S \le 15V$ (Note 3) | 1.25 | | $V_S - 1.75$ | V |
| Common-Mode Rejection Ratio | $T_A = 25°C$ | 63 | 85 | | dB |
| Total Harmonic Distortion | $R_L = 8\Omega$, $V_O = 2$ Vrms, f = 1 kHz, $T_A = 25°C$ | | 0.5 | 5 | % |

**Note 1:** For operation at high temperatures, the LM13080 must be derated based upon a maximum junction temperature of 150°C and a thermal resistance of 100°C/W. The thermal resistance values given are for a still air ambient with the package soldered into a printed circuit board.

**Note 2:** Differential input voltages up to the magnitude of the power supply voltage will not damage the input circuitry. However, input voltages outside the input common-mode voltage range will not be able to properly control the output of the amplifier.

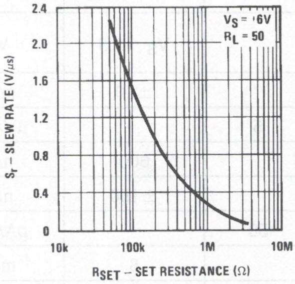
**Note 3:** The input voltage applied to either input should not be allowed to go more than 0.3V below the potential applied to pin 4; however, either input can be taken as high as 15V without causing damage to the circuit. Input voltages below the minimum common-mode voltage range may cause a phase reversal in the output.

**Note 4:** This input current will exist only when the voltage at either input lead is driven negative. It is due to the base-isolation junction of the PNP transistor tub becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also lateral NPN parasitic action on the IC chip. This transistor action can cause the output to take an undefined state for the time duration that an input is driven negative.

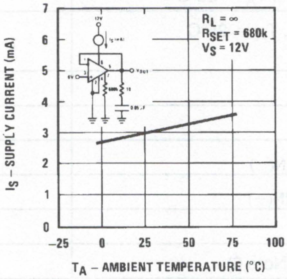
**Note 5:** $V_O = 6V$, $R_S = 0\Omega$, and over the full input common-mode voltage range.

**Note 6:** Supply current is measured with the amplifier connected in a unity gain follower configuration and the positive input set to one-half of the supply voltage.

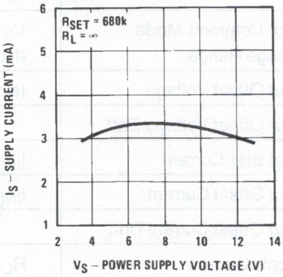
## Typical Performance Characteristics



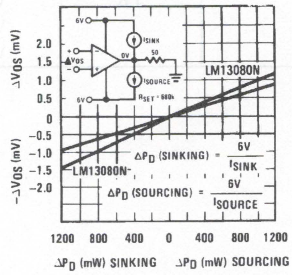
Slew Rate as Function of $R_{SET}$



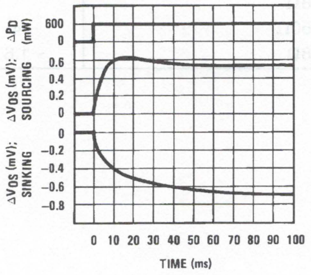
Supply Current



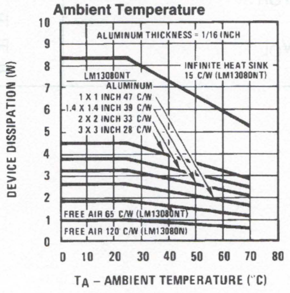
Supply Current



Offset Voltage Change vs Power Dissipation Due to Thermal Feedback



Thermal Feedback Time Constant



Device Dissipation vs Ambient Temperature

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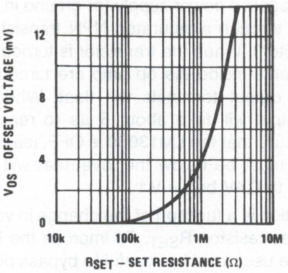
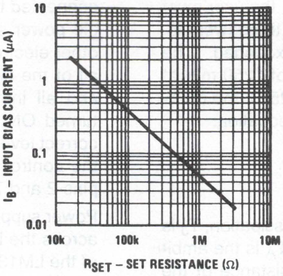
## Typical Performance Characteristics (Continued)

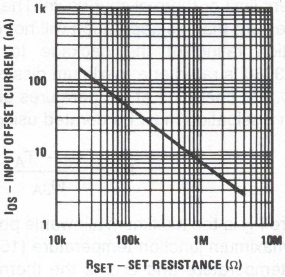
**Offset Voltage**



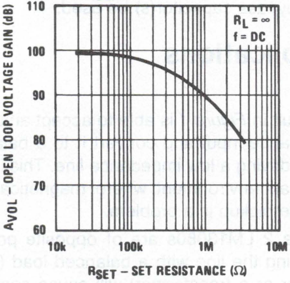
**Input Bias Current**



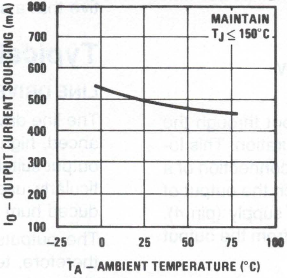
**Offset Current**



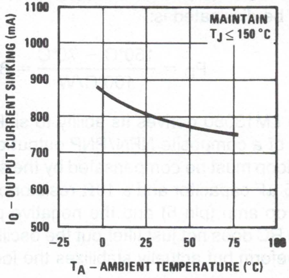
**Voltage Gain as a Function of $R_{SET}$**



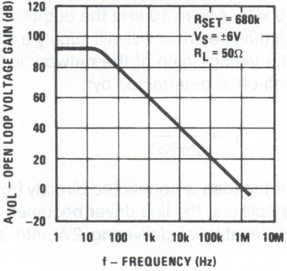
**Output Current Sourcing**



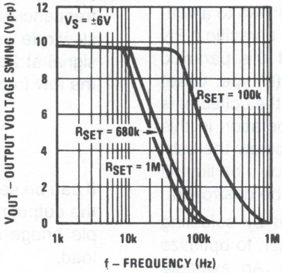
**Output Current Sinking**



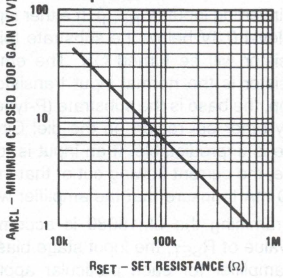
**Small Signal Open Loop Frequency Response**



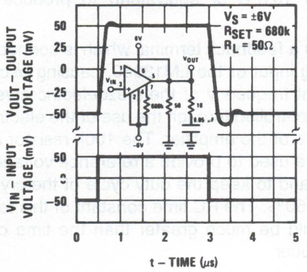
**Large Signal Frequency Response**



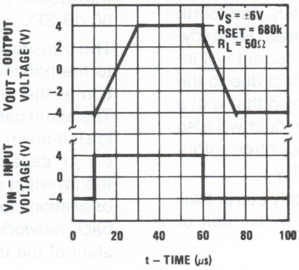
**Minimum Stable Closed Loop Gain**



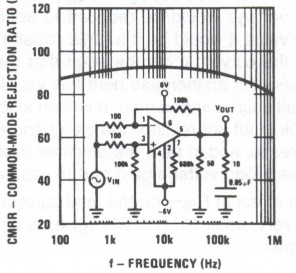
**Voltage Follower Pulse Response (Small Signal)**



**Voltage Follower Pulse Response (Large Signal)**



**Common-Mode Rejection Ratio**



TL/H/7978–3

## Application Hints

The LM13080 is a power op amp capable of sourcing or sinking more than 250 mA and does not include internal current limit or thermal shut-down. Therefore, the user must make sure that his application will not cause the power dissipation rating of the package to be exceeded. The LM13080 is rated at a maximum dissipation of 1250 mW at 25°C. For operation at temperatures above 25°C, the maximum dissipation must be derated using the equation:

$$P_D = \frac{T_J - T_A}{\Theta_{JA}}$$

where $P_D$ is the maximum allowable power dissipation, $T_J$ is the maximum junction temperature (150°C), $T_A$ is the ambient temperature and $\Theta_{JA}$ is the thermal resistance of the package operated in a still air environment. $\Theta_{JA}$ for the LM13080N is 100°C/W. For example, if the LM13080N is used in free air in a 70°C ambient, the maximum power that can be dissipated is:

$$P_D = \frac{150°C - 70°C}{100°C/W} = 800 \text{ mW}$$

The LM13080 derives its ability to sink current through the use of a composite NPN/PNP output configuration. This local loop must be compensated by the series connection of a 0.05 μF capacitor and a 10Ω resistor between the output of the op amp (pin 5) and the negative power supply (pin 4). The RC does not just filter out the oscillation from the output waveform but actually stabilizes the loop.

If the inputs of the LM13080 are driven below the input common-mode voltage range, it is possible that the output will experience a phase reversal. This is particularly true for the non-inverting input ($V_{IN(+)}$). If either input is driven to a voltage level 0.3V below the substrate (pin 4) a parasitic NPN transistor will be turned ON. The emitter of this parasitic transistor is the normal input transistor epi (N-type, base) region, the base is the substrate (P-type) and the collector is every other epi region on the die. Circuit operation in this mode is unpredictable. If an input is forced below the substrate, the current flowing out of that input should be limited to 20 mA to insure that the amplifier will not be destroyed.

Programming the LM13080 is accomplished by selecting the value of $R_{SET}$, the input stage bias resistor, to optimize the amplifier for each particular application. An example would be an application with low source resistance which requires a low offset voltage to make a precise DC measurement. By selecting an $R_{SET}$ of 100 kΩ, the normal offset voltage would be reduced to approximately one-fourth the value it would be if a 680k resistor was used. By studying the curves, it can be seen that the bias current will increase but an increase here has very little effect due to the small source impedance. It should also be noted that with a 100k input set resistor the gain bandwidth product will also increase, and in fact, the amplifier must be operated with a closed loop voltage gain of 6 to assure stability.

The effect of $R_{SET}$ on the total quiescent supply current will be very small ($\Delta I_S < 5\% \ I_S$) as long as $R_{SET}$ is 100k or greater.

To employ electronic shut-down the output bias pin, pin 2, and the negative end of the input bias resistor, $R_{SET}$, are connected to the negative power supply (or ground in a single power system) through a saturated NPN transistor (or other electronic switch). When the transistor is turned OFF, all of the bias currents inside the op amp are turned OFF and all input and output terminals will float. When first turned ON, the output will take about 5 μs to reach the correct level. To insure that the LM13080 is OFF, leakage in the control device must be below the level that will allow pins 2 and 7 to fall to 0.4V below $V^+$.

Power supply rejection is a function of the change in voltage across the input bias resistor, $R_{SET}$. To improve the PSRR of the LM13080, the user must be careful to bypass pin 7 to pin 6 or to establish a floating voltage referenced to the positive power supply to serve as a connection point for $R_{SET}$. In applications where PSRR is important, it is imperative that a supply bypass capacitor(s) be used.

## Typical Applications

### LINE DRIVER

The line driver circuit in *Figure 1* is able to accept an unbalanced, high impedance input and convert it to a balanced output suitable for driving a low impedance line. This is particularly useful in an environment where magnetically induced hum or noise pickup is a problem.

The outputs of the 2 LM13080s are of opposite polarity; therefore, terminating the line with a balanced load (i.e., a differential amplifier or a transformer) will cause common-mode interference pickup to be cancelled.

This circuit will drive a 20 Vp-p signal into a 50Ω load for frequencies up to 10 kHz. Above 10 kHz the output signal is slew rate limited, but the line driver will still supply a 13 Vp-p signal at 20 kHz. The voltage gain of the network is 2, and the low frequency roll-off is determined by:

$$f_L = \frac{1}{2\pi RC}$$

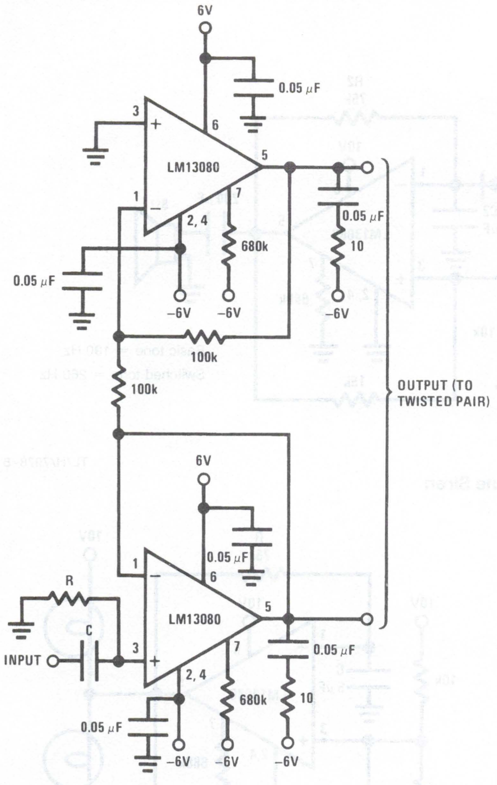
It can be seen that if the load is connected directly between the outputs of the amplifiers, the line driver becomes a simple bridge amplifier capable of delivering 2W into a 16Ω load.

### PIEZOELECTRIC ALARM

The piezoelectric alarm shown in *Figure 2* uses a 3-terminal transducer (Gulton 101FB or equivalent) to produce an 80 dB SPL alarm.

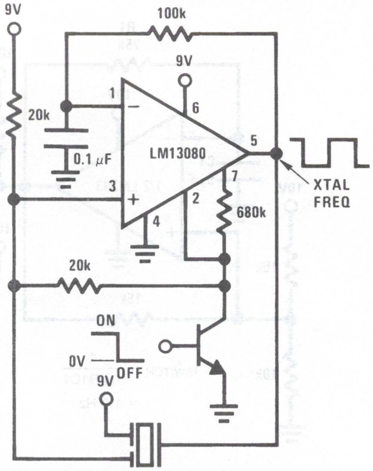
The transducer has a feedback terminal which is connected to the non-inverting input of the LM13080, causing oscillation at the resonant frequency of the piezoelectric crystal. The alarm can be controlled through the use of the electronic shut-down feature of the amplifier. The 100k resistor and 0.1 μF capacitor are used to provide a reference voltage at the inverting input and to keep the duty cycle of the crystal oscillation close to 50%. The RC time constant of this feedback network should be much greater than the time constant of the transducer.

## Typical Applications (Continued)


6V
0.05 μF
3
+
6
LM13080
5
1
−
7
2, 4
680k
0.05 μF
10
0.05 μF
−6V
−6V
−6V
100k
100k
OUTPUT (TO TWISTED PAIR)
6V
0.05 μF
1
−
6
R
LM13080
5
C
INPUT
3
+
7
0.05 μF
2, 4
680k
10
0.05 μF
−6V
−6V
−6V

TL/H/7978-5

**FIGURE 1. Line Driver—Unbalanced Input to Balanced Output**


9V
100k
9V
1
−
6
20k
0.1 μF
LM13080
5
3
+
7
2
XTAL FREQ
4
680k
20k
ON
0V
OFF
9V

TL/H/7978-6

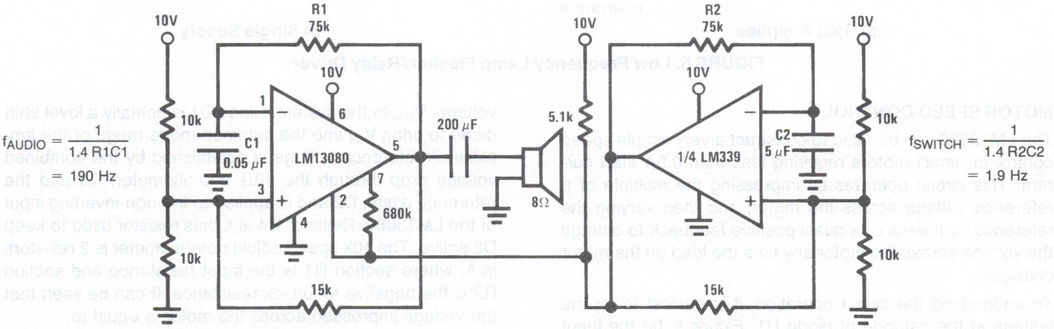
**FIGURE 2. Piezoelectric Alarm**

### SIRENS

Two separate circuits for sirens are shown. The first, *Figure 3*, is a 2-state or ON-OFF type siren where the LM13080 oscillates at an audio frequency and drives an 8Ω speaker and the LM339 acts as a switch which controls the audio burst rate. The second siren, *Figure 4*, provides a constant audio output but alternates between 2 separate tones. The LM13080 is set to oscillate at one basic frequency and this frequency is changed by adding a 200 kΩ charging resistor in parallel with the feedback resistor, R2.

### LAMP FLASHER—RELAY DRIVER

The LM13080 is easily adaptable to such applications as low frequency warning devices. The output of the oscillator is a squarewave that is used to drive lamps or small relays. As shown in *Figure 5*, the circuit alternately flashes 2 incandescent lamps.


10V
R1
75k
10V
1
6
10k
C1
0.05 μF
200 μF
LM13080
5
3
+
7
2
4
680k
10k
15k
8Ω
10V
5.1k
R2
75k
10V
10V
−
10k
C2
5 μF
1/4 LM339
+
10k
15k
$f_{AUDIO} = \frac{1}{1.4\ R1C1}$
$= 190$ Hz
$f_{SWITCH} = \frac{1}{1.4\ R2C2}$
$= 1.9$ Hz

TL/H/7978-7

**FIGURE 3. 2-State Siren**

## Typical Applications (Continued)

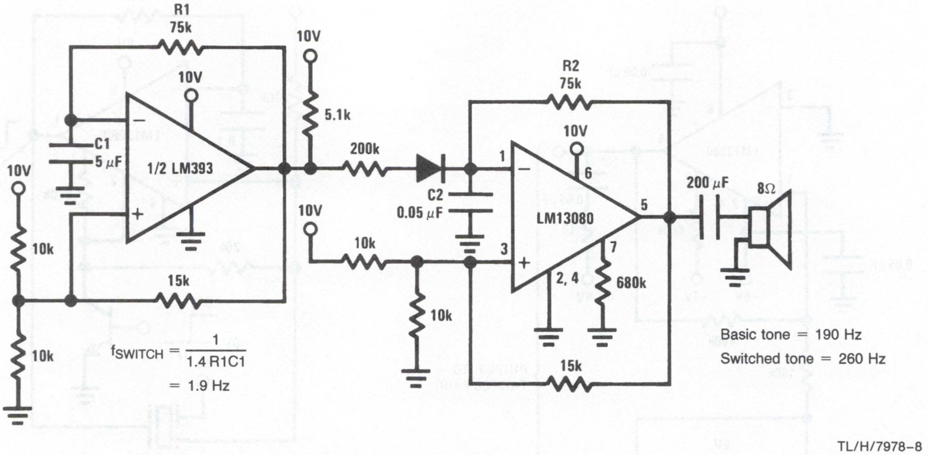
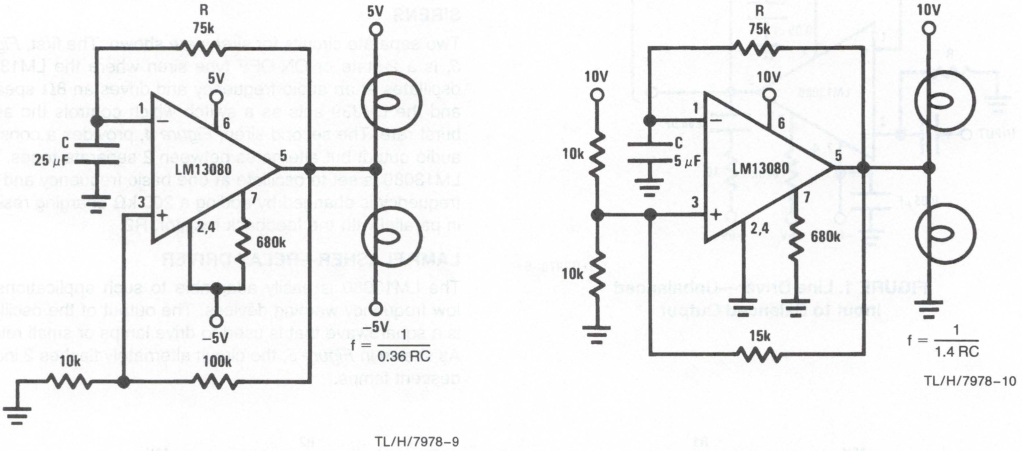

R1
75k
10V
10V
5.1k
C1
5 μF
1/2 LM393
10V
10k
15k
10k
$f_{SWITCH} = \frac{1}{1.4\,R1C1}$
= 1.9 Hz
200k
10V
10k
10k
C2
0.05 μF
R2
75k
10V
1
6
LM13080
5
3
7
2, 4
680k
15k
200 μF
8Ω
Basic tone = 190 Hz
Switched tone = 260 Hz
TL/H/7978-8

**FIGURE 4. 2-Tone Siren**


R
75k
5V
5V
1
6
C
25 μF
LM13080
5
3
2,4
7
680k
−5V
−5V
$f = \frac{1}{0.36\,RC}$
10k
100k
TL/H/7978-9
R
75k
10V
10V
10V
1
6
10k
C
5 μF
LM13080
5
3
7
2,4
680k
10k
15k
$f = \frac{1}{1.4\,RC}$
TL/H/7978-10

a) Split Supplies

b) Single Supply

**FIGURE 5. Low Frequency Lamp Flasher/Relay Driver**

**MOTOR SPEED CONTROL**

The LM13080 can be used to construct a very simple speed control for small motors requiring less than 0.5A start current. This circuit operates by impressing the multiple of a reference voltage across the motor, and then varying the reference by means of a quasi-positive feedback to change the voltage across the motor any time the load on the motor changes.

To understand the circuit operation, it is easiest to let the voltage at the cathode of diode D1, *Figure 6*, be the input voltage, $V_{IN}$, to the system. Diode D1 is actually a level shift diode to bring $V_{IN}$ into the common-mode range of the amplifier. A reference voltage is established by the combined voltage drop through the 10Ω potentiometer, R3 and the reference diode, D2 and is applied to the non-inverting input of the LM13080. Resistor R4 is a bias resistor used to keep D2 active. The 10k speed adjust potentiometer is 2 resistors in 1, where section R1 is the input resistance and section R2 is the negative feedback resistance. It can be seen that the voltage impressed across the motor is equal to:

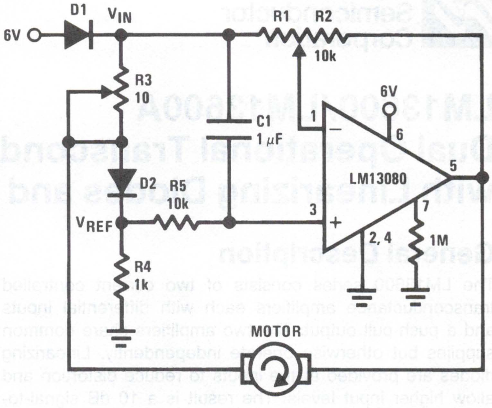
$$V_{MOTOR} = \frac{(V_{BE2} + I_3R3)\,R2}{R1} + V_{BE}$$

## Typical Applications (Continued)

The positive feedback is developed as a change in the voltage across R3 due to the change in the motor current caused by a variation in the motor's load. Resistor R3 is shown as a potentiometer so that the amount of positive feedback can be adjusted for smooth operation of the motor. Capacitor C1 and resistor R5 serve as a filter for the reference voltage at the non-inverting input of the amplifier.

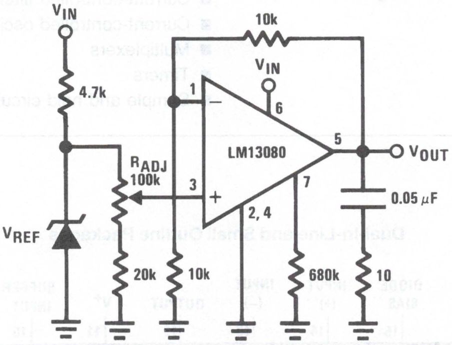
### VOLTAGE REGULATORS

In normal, positive or negative regulator application such as those shown in *Figure 7* and *Figure 8*, the LM13080 has 2 major advantages over standard operational amplifiers. The LM13080 has its own on-chip pass device and in addition can either sink or source 250 mA of load current.


D1
$V_{IN}$
6V
R1
R2
10k
R3
10
C1
1 μF
6V
1
6
5
LM13080
D2
R5
10k
3
7
$V_{REF}$
2, 4
1M
R4
1k
MOTOR

TL/H/7978-11

**FIGURE 6. Motor Speed Control**

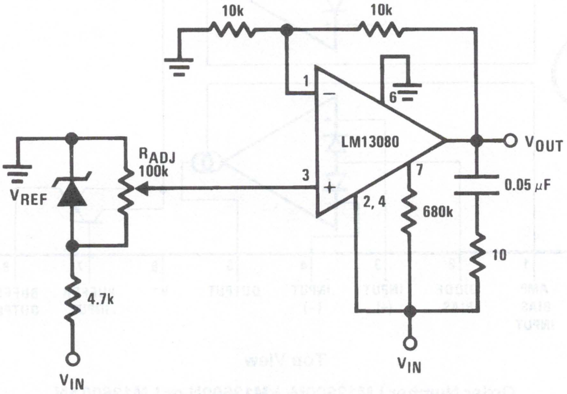

$V_{IN}$
10k
$V_{IN}$
4.7k
1
6
5
$V_{OUT}$
LM13080
$R_{ADJ}$
100k
3
7
0.05 μF
2, 4
$V_{REF}$
20k
10k
680k
10

TL/H/7978-12

$2V \leq V_{OUT} \leq (V_{IN} - 2V)$

**FIGURE 7. Positive Variable Voltage Regulator**

**Note:** Pin numbers apply to miniDIP.


10k
10k
1
6
LM13080
$V_{OUT}$
$R_{ADJ}$
100k
3
7
0.05 μF
$V_{REF}$
2, 4
680k
10
4.7k
$V_{IN}$
$V_{IN}$

TL/H/7978-13

$-15V \geq V_{OUT} \geq -(V_{IN} - 2V)$

**FIGURE 8. Negative Variable Voltage Regulator**

National
Semiconductor
Corporation

# LM13600/LM13600A
# Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

## General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

## Features

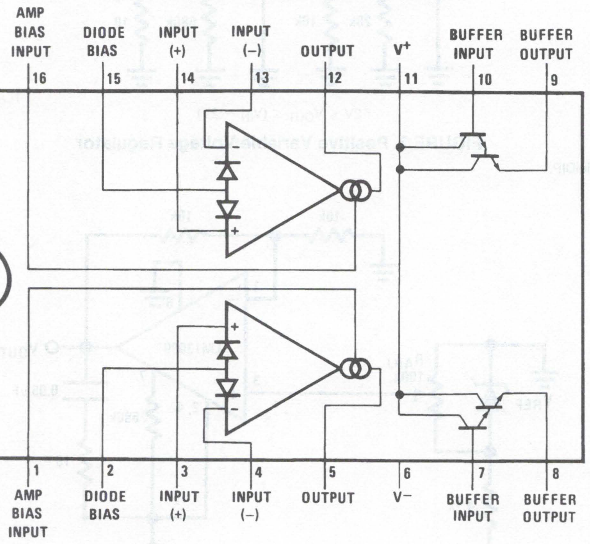
- $g_m$ adjustable over 6 decades
- Excellent $g_m$ linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio
- Wide supply range ±2V to ±22V

## Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

## Connection Diagram

**Dual-In-Line and Small Outline Packages**


AMP BIAS INPUT
16
DIODE BIAS
15
INPUT (+)
14
INPUT (−)
13
OUTPUT
12
V+
11
BUFFER INPUT
10
BUFFER OUTPUT
9
+
−
1
AMP BIAS INPUT
2
DIODE BIAS
3
INPUT (+)
4
INPUT (−)
5
OUTPUT
6
V−
7
BUFFER INPUT
8
BUFFER OUTPUT

TL/H/7980-2

**Top View**

**Order Number LM13600M, LM13600N or LM13600AN**
**See NS Package Number M16A or N16A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (Note 1) | |
| LM13600 | 36 $V_{DC}$ or ±18V |
| LM13600A | 44 $V_{DC}$ or ±22V |
| Power Dissipation (Note 2) $T_A = 25°C$ | 570 mW |
| Differential Input Voltage | ±5V |
| Diode Bias Current ($I_D$) | 2 mA |
| Amplifier Bias Current ($I_{ABC}$) | 2 mA |
| Output Short Circuit Duration | Indefinite |
| Buffer Output Current (Note 3) | 20 mA |
| Operating Temperature Range | 0°C to +70°C |
| DC Input Voltage | $+V_S$ to $-V_S$ |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM13600 | | | LM13600A | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($V_{OS}$) | | | 0.4 | 4 | | 0.4 | 1 | mV |
| | Over Specified Temperature Range | | | | | | 2 | mV |
| | $I_{ABC} = 5\ \mu A$ | | 0.3 | 4 | | 0.3 | 1 | mV |
| $V_{OS}$ Including Diodes | Diode Bias Current ($I_D$) = 500 µA | | 0.5 | 5 | | 0.5 | 2 | mV |
| Input Offset Change | $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | | 0.1 | 3 | | 0.1 | 1 | mV |
| Input Offset Current | | | 0.1 | 0.6 | | 0.1 | 0.6 | µA |
| Input Bias Current | | | 0.4 | 5 | | 0.4 | 5 | µA |
| | Over Specified Temperature Range | | 1 | 8 | | 1 | 7 | µA |
| Forward Transconductance ($g_m$) | | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | µmho |
| | Over Specified Temperature Range | 5400 | | | 4000 | | | µmho |
| $g_m$ Tracking | | | 0.3 | | | 0.3 | | dB |
| Peak Output Current | $R_L = 0$, $I_{ABC} = 5\ \mu A$ | | 5 | | 3 | 5 | 7 | µA |
| | $R_L = 0$, $I_{ABC} = 500\ \mu A$ | 350 | 500 | 650 | 350 | 500 | 650 | µA |
| | $R_L = 0$, Over Specified Temp Range | 300 | | | 300 | | | µA |
| Peak Output Voltage | | | | | | | | |
| Positive | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | +12 | +14.2 | | +12 | +14.2 | | V |
| Negative | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | −12 | −14.4 | | −12 | −14.4 | | V |
| Supply Current | $I_{ABC} = 500\ \mu A$, Both Channels | | 2.6 | | | 2.6 | | mA |
| $V_{OS}$ Sensitivity | | | | | | | | |
| Positive | $\Delta V_{OS}/\Delta V+$ | | 20 | 150 | | 20 | 150 | µV/V |
| Negative | $\Delta V_{OS}/\Delta V-$ | | 20 | 150 | | 20 | 150 | µV/V |
| CMRR | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| Crosstalk | Referred to Input (Note 5) $20\ Hz < f < 20\ kHz$ | | 100 | | | 100 | | dB |
| Differential Input Current | $I_{ABC} = 0$, Input = ±4V | | 0.02 | 100 | | 0.02 | 10 | nA |
| Leakage Current | $I_{ABC} = 0$ (Refer to Test Circuit) | | 0.2 | 100 | | 0.2 | 5 | nA |

## Electrical Characteristics (Note 4) (Continued)

| Parameter | Conditions | LM13600 |  |  | LM13600A |  |  | Units |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Resistance |  | 10 | 26 |  | 10 | 26 |  | kΩ |
| Open Loop Bandwidth |  |  | 2 |  |  | 2 |  | MHz |
| Slew Rate | Unity Gain Compensated |  | 50 |  |  | 50 |  | V/µs |
| Buffer Input Current | (Note 5), Except $I_{ABC} = 0\ \mu A$ |  | 0.2 | 0.4 |  | 0.2 | 0.4 | µA |
| Peak Buffer Output Voltage | (Note 5) | 10 |  |  | 10 |  |  | V |

**Note 1:** For selections to a supply voltage above ±22V, contact factory.

**Note 2:** For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

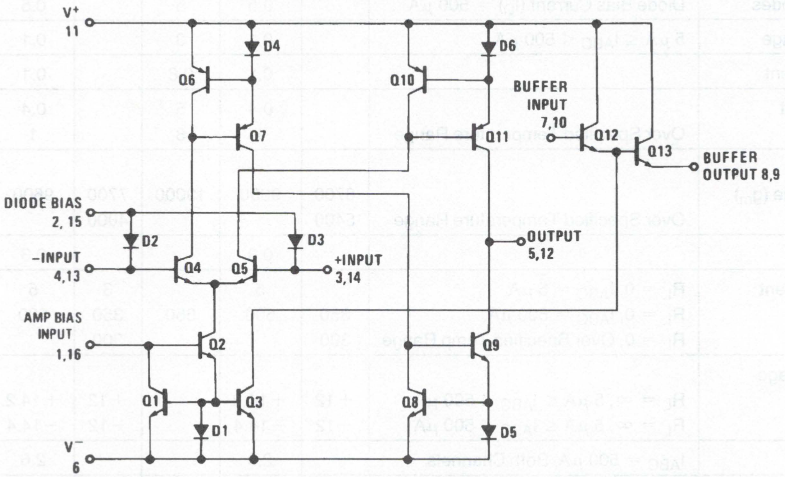
**Note 3:** Buffer output current should be limited so as to not exceed package dissipation.

**Note 4:** These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current ($I_{ABC}$) = 500 µA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

**Note 5:** These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\ \mu A$, $R_{OUT} = 5\ k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

## Schematic Diagram

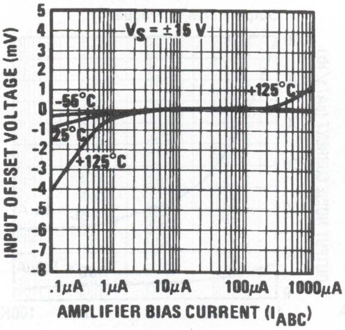
**One Operational Transconductance Amplifier**


V+
11
D4
Q6
Q7
Q10
D6
BUFFER
INPUT
7,10
Q11
Q12
Q13
BUFFER
OUTPUT 8,9
DIODE BIAS
2, 15
D2
D3
−INPUT
4,13
Q4
Q5
+INPUT
3,14
OUTPUT
5,12
AMP BIAS
INPUT
1,16
Q2
Q9
Q1
Q3
Q8
D1
D5
V−
6

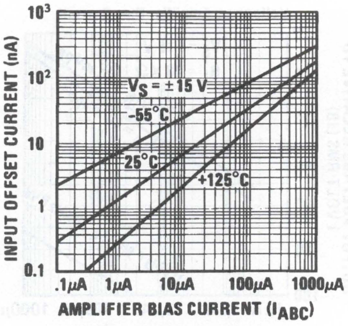
TL/H/7980–1

## Typical Performance Characteristics

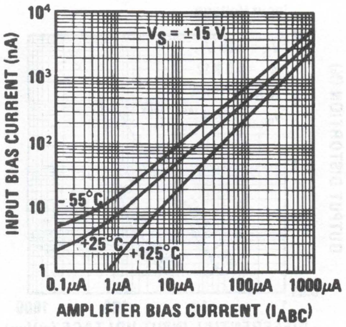
Input Offset Voltage



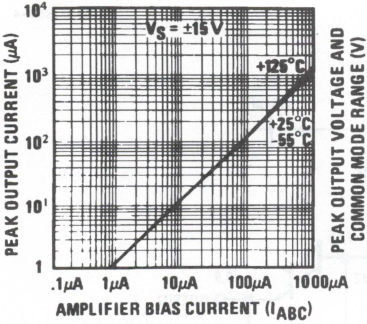
Input Offset Current



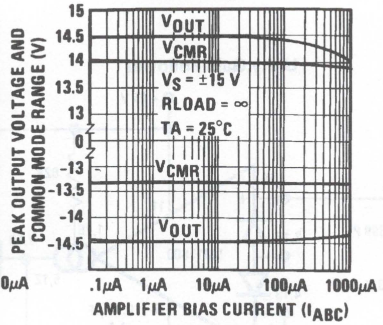
Input Bias Current



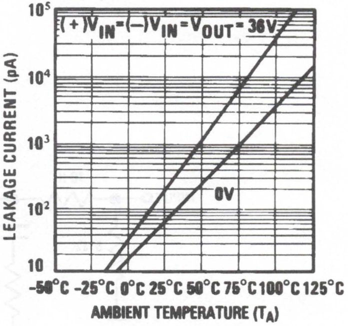
Peak Output Current



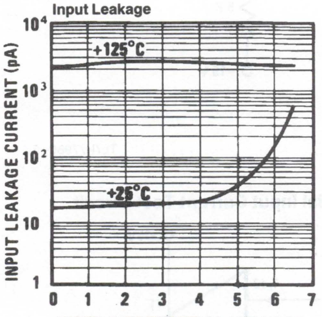
Peak Output Voltage and Common Mode Range



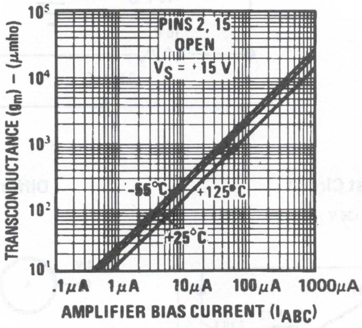
Leakage Current



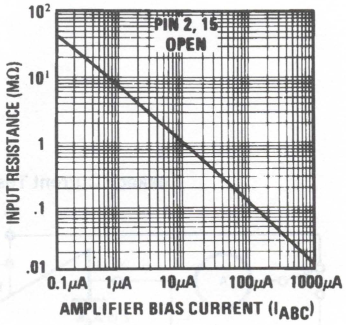
Input Leakage



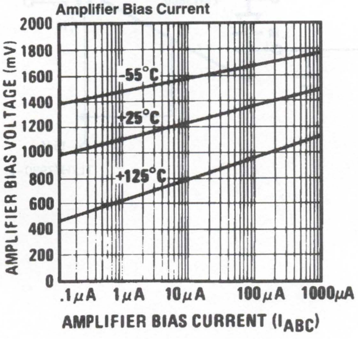
Transconductance



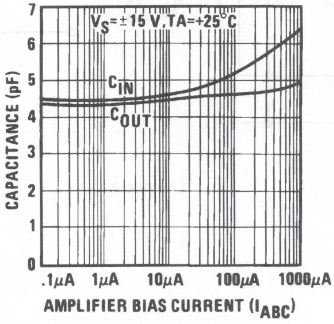
Input Resistance



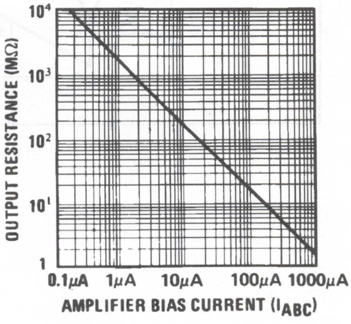
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance

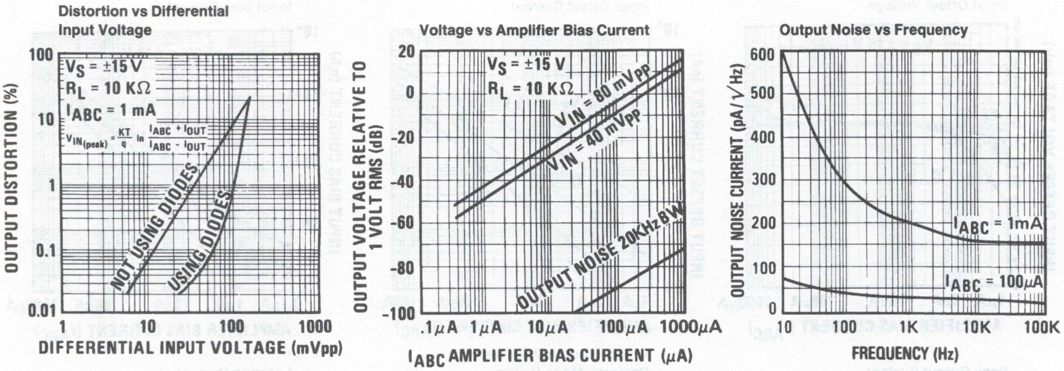


Output Resistance



TL/H/7980–3

## Typical Performance Characteristics (Continued)

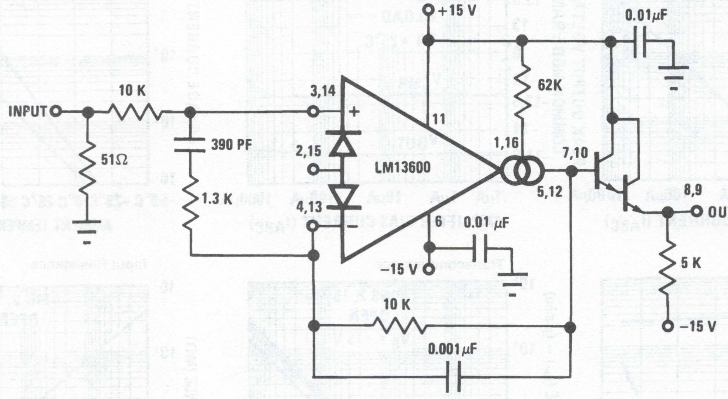

Distortion vs Differential Input Voltage

Voltage vs Amplifier Bias Current

Output Noise vs Frequency

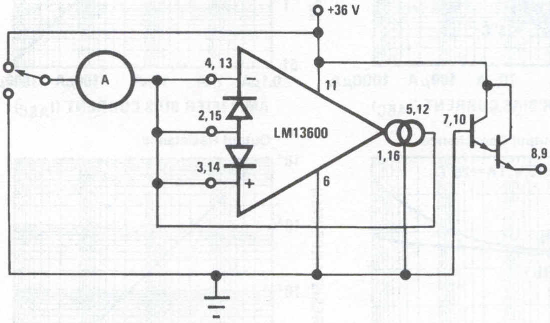
TL/H/7980–4

### Unity Gain Follower


+15 V
0.01μF
62K
INPUT
10 K
3,14
+
11
51Ω
390 PF
2,15
1,16
7,10
LM13600
5,12
8,9
OUTPUT
1.3 K
4,13
6
0.01 μF
−15 V
5 K
−15 V
10 K
0.001 μF

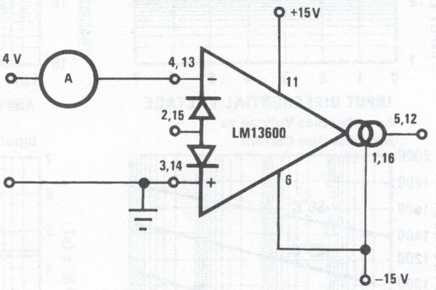
TL/H/7980–5

### Leakage Current Test Circuit


+36 V
A
4, 13
11
2,15
5,12
7,10
LM13600
1,16
8,9
3,14
+
6

TL/H/7980–6

### Differential Input Current Test Circuit


+15 V
±4 V
A
4, 13
11
2,15
5,12
LM13600
1,16
3,14
+
6
−15 V

TL/H/7980–7

## Circuit Description

The differential transistor pair $Q_4$ and $Q_5$ form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where $V_{IN}$ is the differential input voltage, kT/q is approximately 26 mV at 25°C and $I_5$ and $I_4$ are the collector currents of transistors $Q_5$ and $Q_4$ respectively. With the exception of $Q_3$ and $Q_{13}$, all transistors and diodes are identical in size. Transistors $Q_1$ and $Q_2$ with Diode $D_1$ form a current mirror which forces the sum of currents $I_4$ and $I_5$ to equal $I_{ABC}$;

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where $I_{ABC}$ is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of $I_4$ and $I_5$ approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[ \frac{I_{ABC}\, q}{2kT} \right] = I_5 - I_4 \quad (5)$$

Collector currents $I_4$ and $I_5$ are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to $I_5$ minus $I_4$ thus:

$$V_{IN} \left[ \frac{I_{ABC}\, q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to $I_{ABC}$.

## Linearizing Diodes

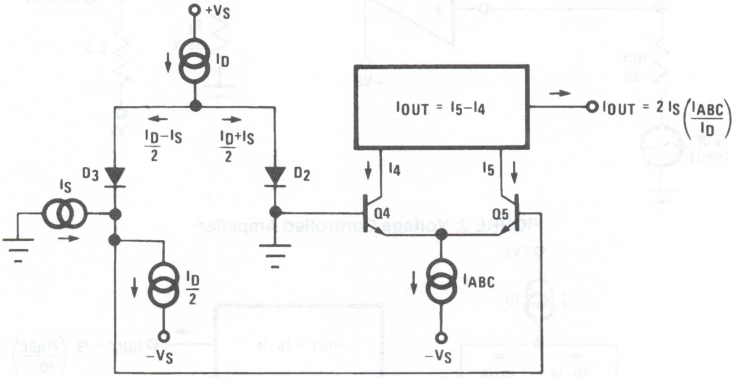
For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current $I_S$. Since the sum of $I_4$ and $I_5$ is $I_{ABC}$ and the difference is $I_{OUT}$, currents $I_4$ and $I_5$ can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \; I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left( \frac{2I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \quad (6)$$



TL/H/7980-8

FIGURE 1. Linearizing Diodes

## Linearizing Diodes (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

## Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of $I_{ABC}$ (2 mA). The lowest value of $I_{ABC}$ for which the amplifier will function therefore determines the overall dynamic range. At very low values of $I_{ABC}$, a buffer which has very low input bias current is desirable. An FET follower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of $I_{ABC}$, the buffer's input current is minimal. At higher levels of $I_{ABC}$, transistor $Q_3$ biases up $Q_{12}$ with a current proportional to $I_{ABC}$ for fast slew rate.

## Applications—Voltage Controlled Amplifiers

*Figure 2* shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, $I_{ABC}$ should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via $R_{IN}$ *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting $R_L$.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, $I_D$ should be as large as possible. This minimizes the dynamic junction resistance of the diodes ($r_e$) and maximizes their linearizing action when balanced against $R_{IN}$. A value of 1 mA is recommended for $I_D$ unless the specific application demands otherwise.

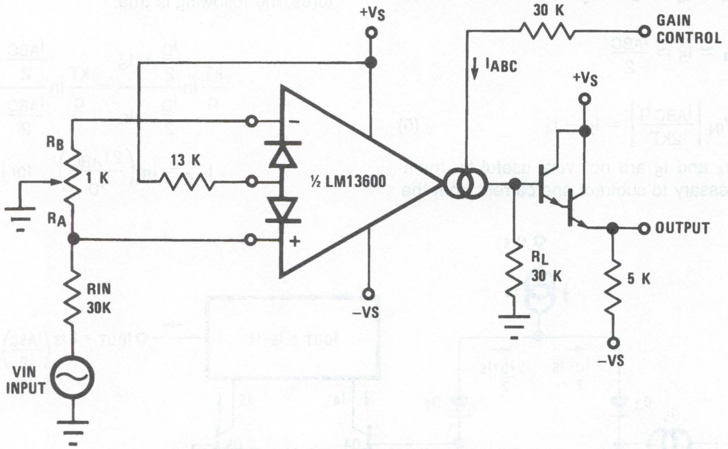


**FIGURE 2. Voltage Controlled Amplifier**

TL/H/7980–9

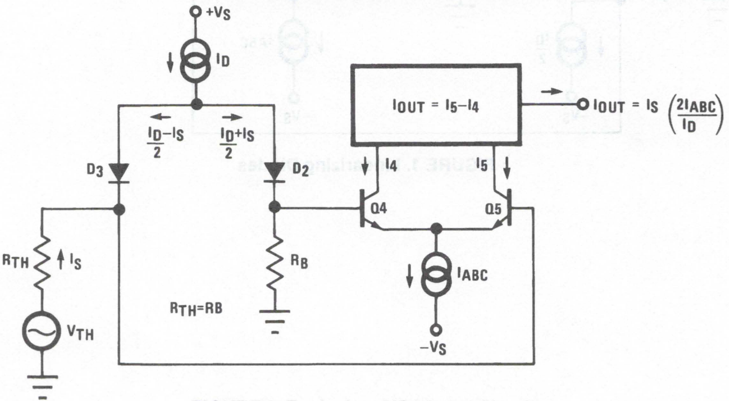


**FIGURE 3. Equivalent VCA Input Circuit**

TL/H/7980–10

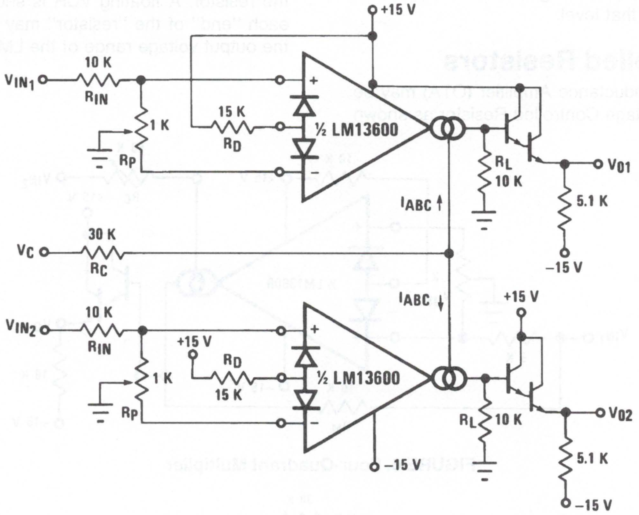
## Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. $R_P$ is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

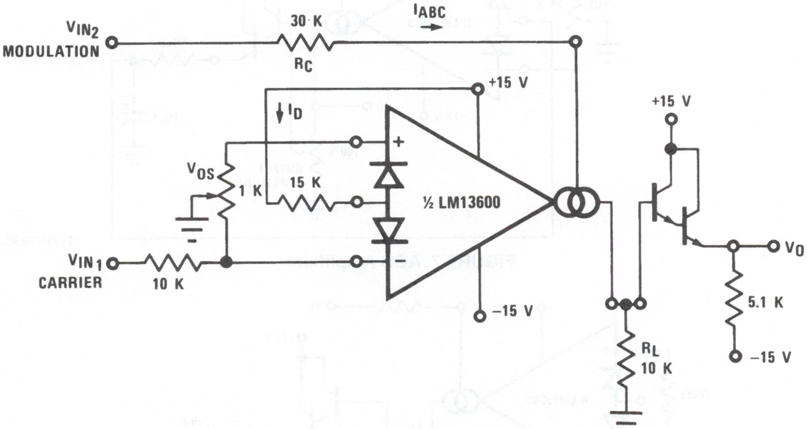
If $V_C$ is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$


+15 V
10 K
$V_{IN1}$
$R_{IN}$
1 K
$R_P$
15 K
$R_D$
½ LM13600
$R_L$
10 K
$V_{O1}$
$I_{ABC}$
5.1 K
30 K
$V_C$
$R_C$
−15 V
$I_{ABC}$
+15 V
10 K
$V_{IN2}$
$R_{IN}$
+15 V
$R_D$
1 K
15 K
½ LM13600
$R_P$
$R_L$
10 K
$V_{O2}$
5.1 K
−15 V
−15 V

TL/H/7980–11

FIGURE 4. Stereo Volume Control


$V_{IN2}$
MODULATION
30 K
$R_C$
$I_{ABC}$
+15 V
$I_D$
$V_{OS}$
1 K
15 K
½ LM13600
+15 V
$V_{IN1}$
CARRIER
10 K
−15 V
$V_O$
5.1 K
$R_L$
10 K
−15 V

TL/H/7980–12

FIGURE 5. Amplitude Modulator

## Stereo Volume Control (Continued)

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2\ (V^- + 1.4V)$ into $I_O$. The circuit of *Figure 6* adds $R_M$ to provide this current, resulting in a four-quadrant multiplier where $R_C$ is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. $R_M$ also serves as the load resistor for $I_O$.

Noting that the gain of the LM13600 amplifier of *Figure 3* may be controlled by varying the linearizing diode current $I_D$ as well as by varying $I_{ABC}$, *Figure 7* shows as AGC Amplifier using this approach. As $V_O$ reaches a high enough amplitude (3 $V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in $I_D$ reduces the amplifier gain so as to hold $V_O$ at that level.

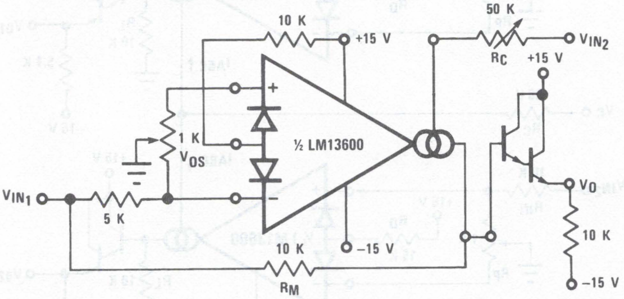
## Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at $R_X$ generates a $V_{IN}$ to the LM13600 which is then multiplied by the $g_m$ of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m\, R_A}$$

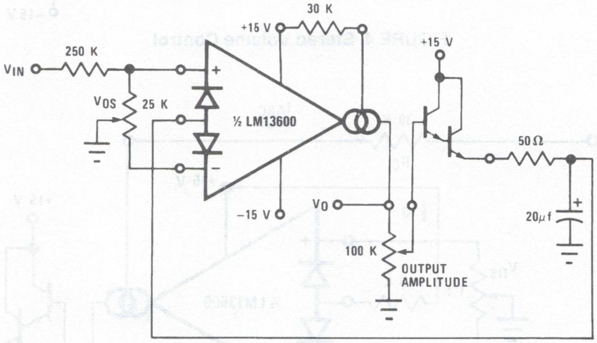
where $g_m \approx 19.2\ I_{ABC}$ at 25°C. Note that the attenuation of $V_O$ by R and $R_A$ is necessary to maintain $V_{IN}$ within the linear range of the LM13600 input.

*Figure 9* shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.


10 K
+15 V
50 K
$R_C$
$V_{IN_2}$
+15 V
+
1 K
$V_{OS}$
½ LM13600
$V_O$
$V_{IN_1}$
5 K
−
10 K
−15 V
10 K
$R_M$
10 K
−15 V

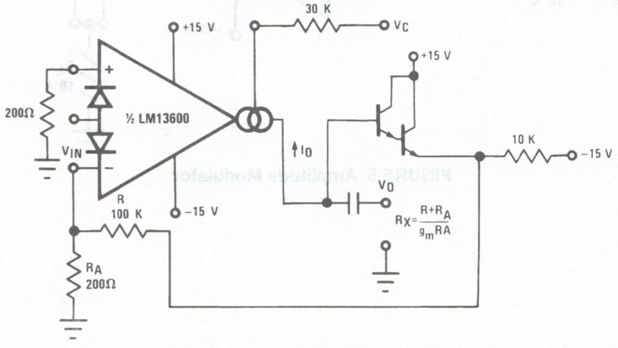
TL/H/7980-13

FIGURE 6. Four-Quadrant Multiplier


30 K
+15 V
+15 V
250 K
$V_{IN}$
$V_{OS}$
25 K
+
½ LM13600
−
−15 V
$V_O$
50 Ω
20µf
+
100 K
OUTPUT AMPLITUDE

TL/H/7980-14

FIGURE 7. AGC Amplifier


+15 V
30 K
$V_C$
+15 V
+
200Ω
½ LM13600
$I_O$
$V_{IN}$
−
10 K
−15 V
$V_O$
R
100 K
−15 V
$R_X = \frac{R+R_A}{g_m R_A}$
$R_A$
200Ω

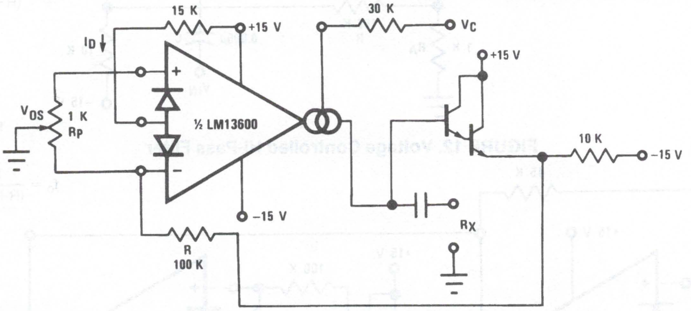
TL/H/7980-15

FIGURE 8. Voltage Controlled Resistor, Single-Ended

## Voltage Controlled Filters

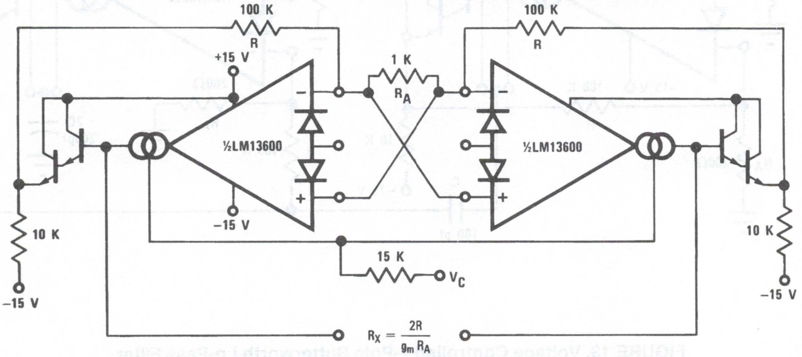
OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which $X_C/g_m$ equals the closed-loop gain of $(R/R_A)$. At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where $g_m$ is again $19.2 \times I_{ABC}$ at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent $g_m$ tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.


15 K
+15 V
30 K
$V_C$
$I_D$
+15 V
$V_{OS}$
1 K
$R_P$
½ LM13600
10 K
−15 V
−15 V
$R_X$
R
100 K

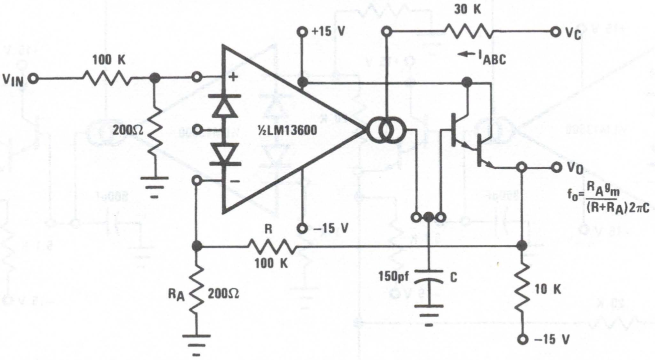
TL/H/7980-16

FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes


100 K
R
100 K
R
+15 V
1 K
$R_A$
½LM13600
½LM13600
−15 V
10 K
−15 V
15 K
$V_C$
10 K
−15 V
$R_X = \frac{2R}{g_m R_A}$

TL/H/7980-17

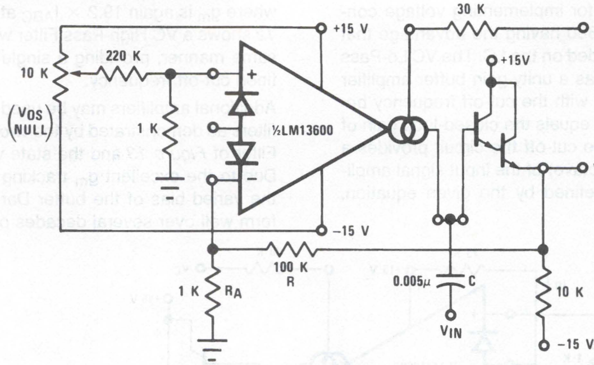
FIGURE 10. Floating Voltage Controlled Resistor


+15 V
30 K
$V_C$
$I_{ABC}$
$V_{IN}$
100 K
200Ω
½LM13600
$V_O$
$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$
R
−15 V
100 K
150pf
C
$R_A$
200Ω
10 K
−15 V

TL/H/7980-18

FIGURE 11. Voltage Controlled Low-Pass Filter

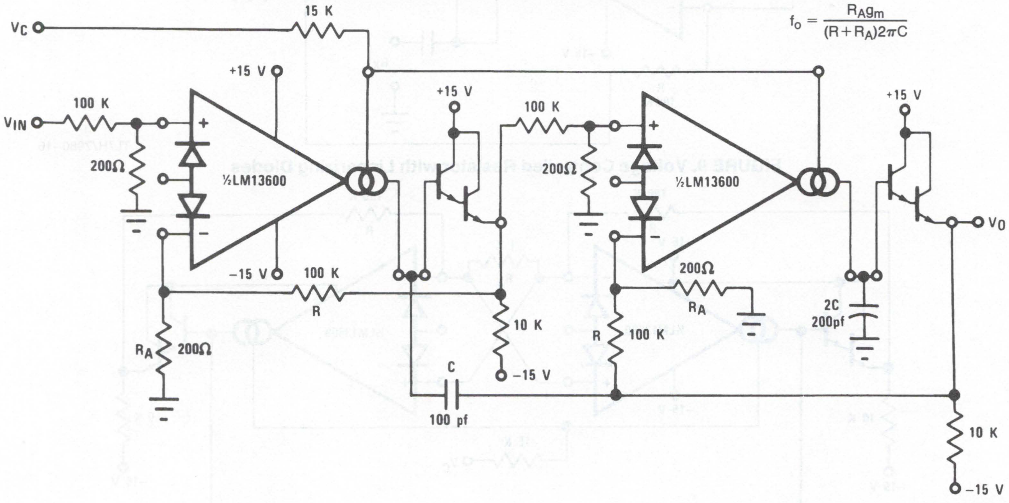
## Voltage Controlled Filters (Continued)


+15 V
30 K
+15V
220 K
10 K
VOS NULL
1 K
½LM13600
VO
−15 V
100 K
R
1 K
RA
0.005µ
C
VIN
10 K
−15 V

$$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$$

TL/H/7980-19

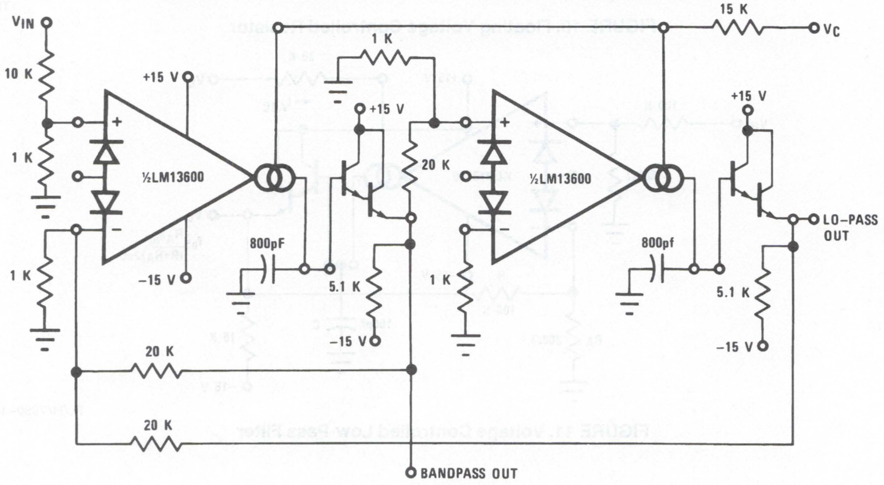
FIGURE 12. Voltage Controlled Hi-Pass Filter


VC
15 K
+15 V
100 K
VIN
200Ω
½LM13600
−15 V
100 K
R
RA
200Ω
+15 V
100 K
200Ω
10 K
−15 V
C
100 pf
½LM13600
200Ω
RA
R
100 K
2C
200pf
+15 V
VO
10 K
−15 V

$$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$$

TL/H/7980-20

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter


VIN
10 K
1 K
1 K
+15 V
½LM13600
−15 V
1 K
+15 V
800pF
20 K
5.1 K
−15 V
15 K
VC
½LM13600
1 K
800pf
+15 V
LO-PASS OUT
5.1 K
−15 V
20 K
20 K
BANDPASS OUT

TL/H/7980-21

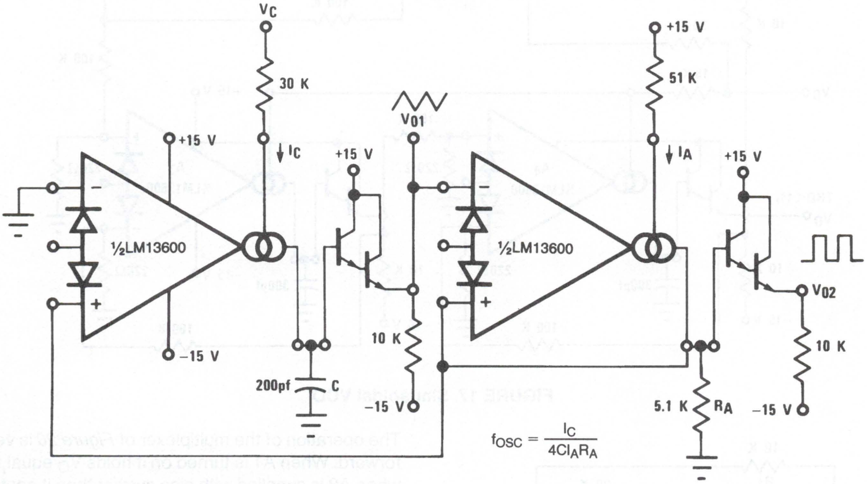
FIGURE 14. Voltage Controlled State Variable Filter

## Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as $I_C$ is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When $V_{O2}$ is high, $I_F$ is added to $I_C$ to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When $V_{O2}$ is low, $I_F$ goes to zero and the capacitor discharge current is set by $I_C$.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

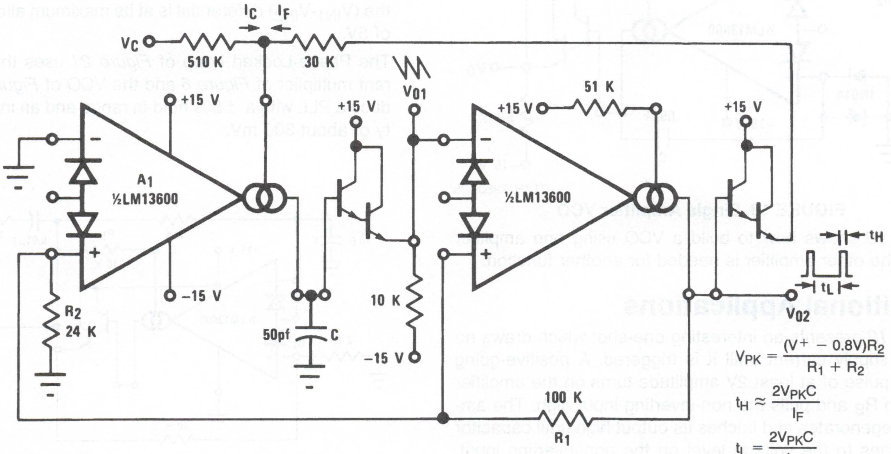


$V_C$
30 K
$I_C$
+15 V
+15 V
$V_{O1}$
−
+
½LM13600
−15 V
200pf
C
10 K
−15 V
+15 V
51 K
$I_A$
+15 V
½LM13600
$V_{O2}$
10 K
5.1 K
$R_A$
−15 V

$$f_{OSC} = \frac{I_C}{4CI_AR_A}$$

TL/H/7980–22

**FIGURE 15. Triangular/Square-Wave VCO**



$I_C$
$I_F$
$V_C$
510 K
30 K
$V_{O1}$
+15 V
+15 V
$A_1$
½LM13600
−
+
−15 V
$R_2$
24 K
50pf
C
10 K
−15 V
+15 V
51 K
+15 V
½LM13600
$t_H$
$t_L$
$V_{O2}$
100 K
$R_1$

$$V_{PK} = \frac{(V^+ - 0.8V)R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_F}$$

$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_O \approx \frac{I_C}{2V_{PK}C} \text{ for } I_C \ll I_F$$

TL/H/7980–23

**FIGURE 16. Ramp/Pulse VCO**

## Voltage Controlled Oscillators (Continued)

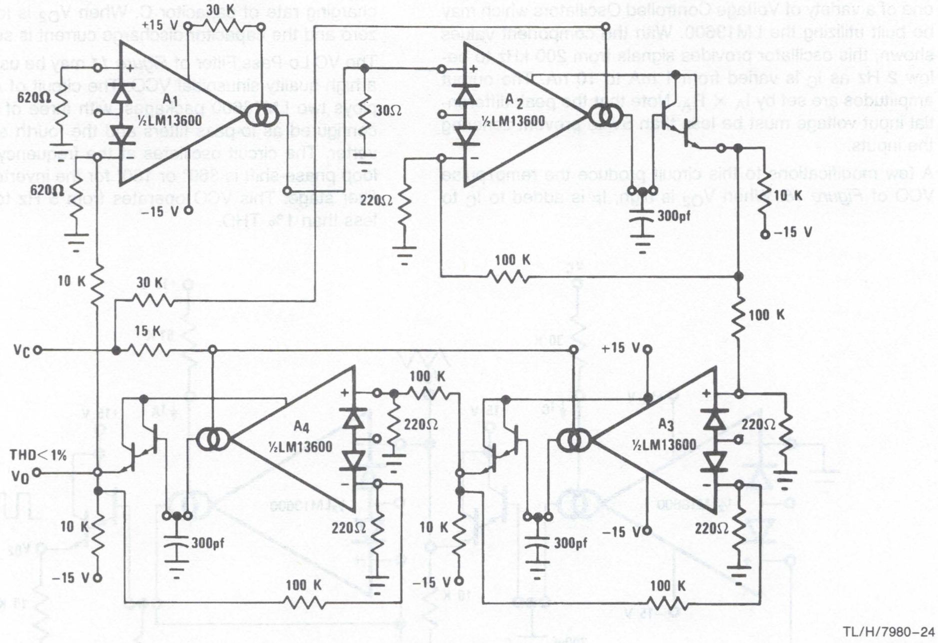

+15 V
30 K
620Ω
620Ω
A1
½LM13600
30Ω
220Ω
−15 V
A2
½LM13600
300pf
10 K
−15 V
100 K
10 K
30 K
15 K
VC
100 K
+15 V
THD<1%
VO
A4
½LM13600
100 K
220Ω
300pf
220Ω
10 K
−15 V
100 K
A3
½LM13600
220Ω
10 K
−15 V
300pf
−15 V
220Ω
100 K
−15 V
TL/H/7980–24

FIGURE 17. Sinusoidal VCO

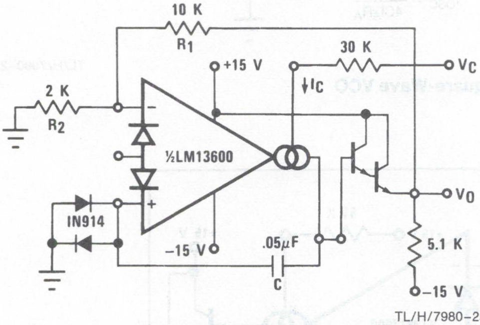

10 K
R1
+15 V
30 K
VC
IC
2 K
R2
½LM13600
VO
IN914
−15 V
.05μF
C
5.1 K
−15 V
TL/H/7980–25

FIGURE 18. Single Amplifier VCO

*Figure 18* shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

## Additional Applications

*Figure 19* presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through $R_B$ and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so than an additional discharge current flows through $D_I$ when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from $V_O$, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds $V_O$ equal to $V_{IN1}$ and when A2 is supplied with bias current then it controls $V_O$. $C_C$ and $R_C$ serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13600 slew rate into 150 pF when the ($V_{IN1}$-$V_{IN2}$) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

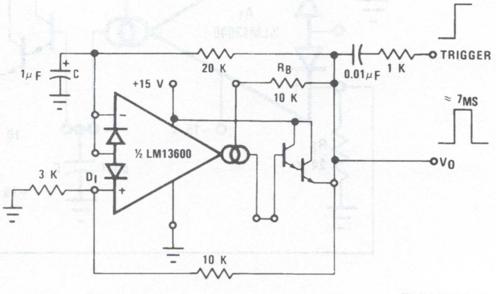

1μF
C
20 K
0.01μF
1 K
TRIGGER
+15 V
RB
10 K
≈ 7MS
½ LM13600
VO
3 K
DI
10 K
TL/H/7980–26

FIGURE 19. Zero Stand-By Power Timer

## Additional Applications (Continued)

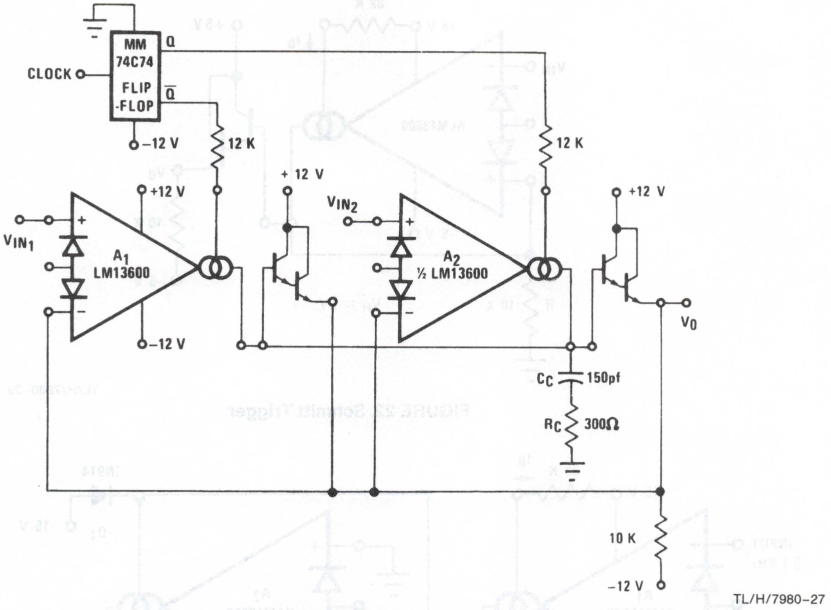

MM 74C74 FLIP-FLOP
Q
Q̄
CLOCK
−12 V
12 K
12 K
+12 V
+ 12 V
$V_{IN_1}$
$A_1$ LM13600
−12 V
$V_{IN_2}$
$A_2$ ½ LM13600
+12 V
$V_O$
$C_C$
150pf
$R_C$
300Ω
10 K
−12 V
TL/H/7980–27

FIGURE 20. Multiplexer

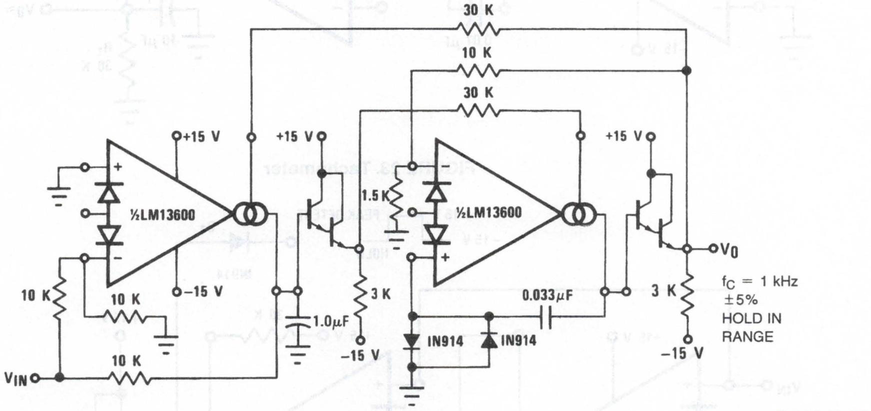

30 K
10 K
30 K
+15 V
+15 V
+15 V
½LM13600
½LM13600
1.5 K
−15 V
10 K
10 K
10 K
$V_{IN}$
1.0µF
3 K
−15 V
0.033µF
IN914
IN914
3 K
−15 V
$V_O$
$f_C$ = 1 kHz
±5%
HOLD IN
RANGE
TL/H/7980–28

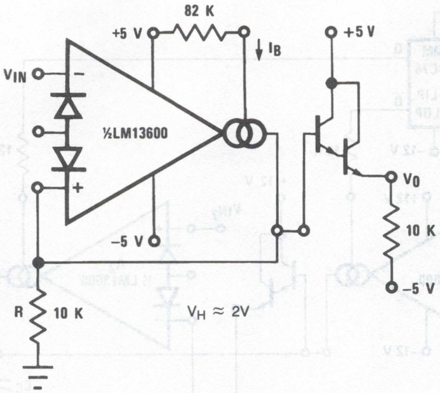
FIGURE 21. Phase Lock Loop

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying $I_B$ will produce a Schmitt Trigger with variable hysteresis.

*Figure 23* shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into $C_f$ and $R_t$. This once-per-cycle charge is then balanced by the current of $V_O/R_t$. The maximum $f_{IN}$ is limited by the amount of time required to charge $C_t$ from $V_L$ to $V_H$ with a current of $I_B$, where $V_L$ and $V_H$ represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for $C_t$ when A1 switches low.

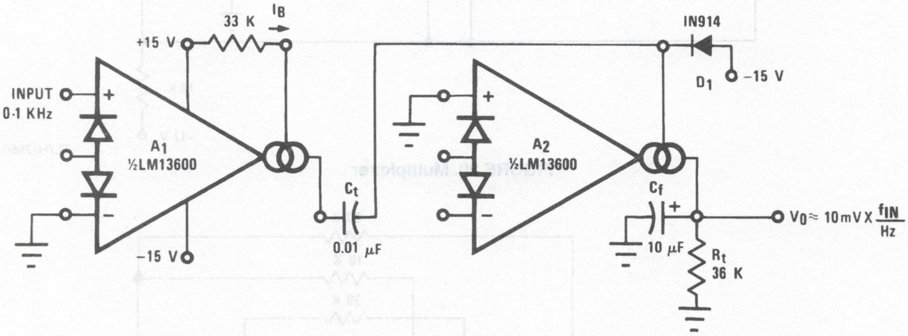
The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever $V_{IN}$ becomes more positive than $V_O$. A1 then charges storage capacitor C to hold $V_O$ equal to $V_{IN}PK$. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that $V_O$ remains constant.

## Additional Applications (Continued)


82 K
+5 V
I_B
V_IN
½LM13600
−5 V
+5 V
V_O
10 K
−5 V
R
10 K
V_H ≈ 2V

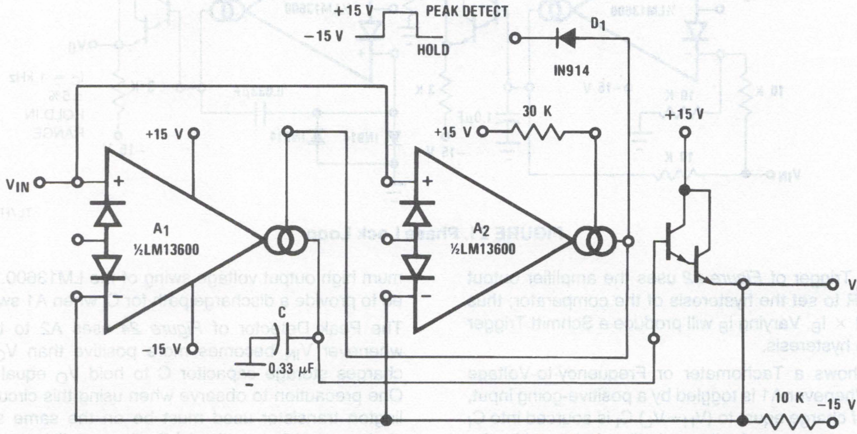
TL/H/7980-29

FIGURE 22. Schmitt Trigger


I_B
33 K
+15 V
INPUT
0-1 KHz
A1
½LM13600
−15 V
C_t
0.01 µF
IN914
D1
−15 V
A2
½LM13600
C_f
10 µF
R_t
36 K
V_O ≈ 10mV X f_IN/Hz

TL/H/7980-30

FIGURE 23. Tachometer


+15 V
−15 V
PEAK DETECT
HOLD
D1
IN914
30 K
+15 V
+15 V
+15 V
V_IN
A1
½LM13600
C
0.33 µF
−15 V
A2
½LM13600
V_O
10 K
−15 V

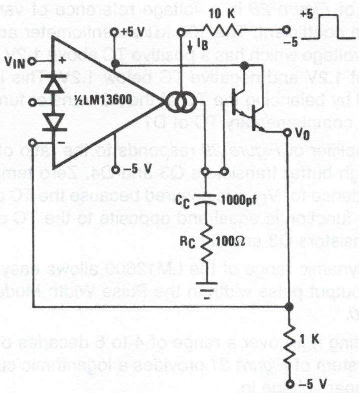
TL/H/7980-31

FIGURE 24. Peak Detector and Hold Circuit

## Additional Applications (Continued)

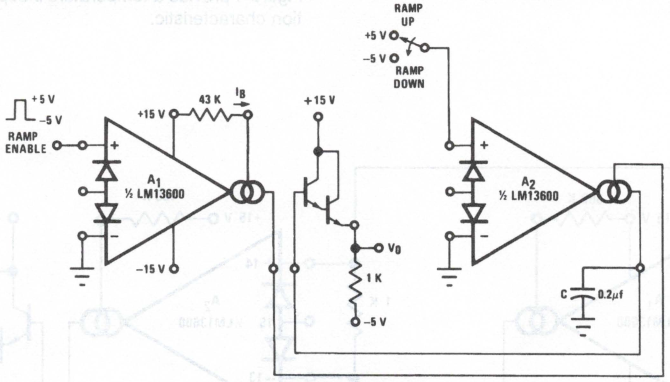
The Sample-Hold circuit of *Figure 25* also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of *Figure 26* sources $I_B$ into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that $V_O$ reads directly in RMS volts.


10 K
+5
-5
SAMPLE
HOLD
+5 V
I_B
V_IN
+
-
½LM13600
V_O
-5 V
C_C
1000pf
R_C
100Ω
1 K
-5 V

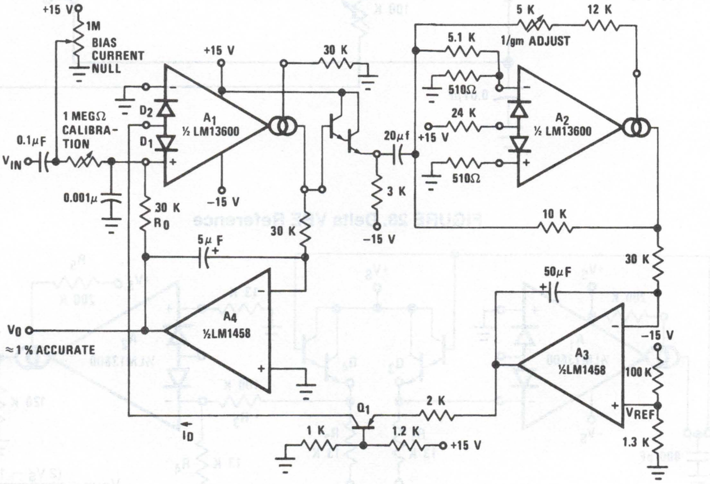
TL/H/7980-32

FIGURE 25. Sample-Hold Circuit


+5 V
-5 V
RAMP ENABLE
+15 V
43 K
I_B
+
-
A1
½ LM13600
-15 V
+15 V
V_O
1 K
-5 V
RAMP UP
+5 V
-5 V
RAMP DOWN
+
-
A2
½ LM13600
C
0.2µf

TL/H/7980-33

FIGURE 26. Ramp and Hold


+15 V
1M
BIAS CURRENT NULL
+15 V
30 K
5 K
12 K
5.1 K
1/gm ADJUST
510Ω
D2
1 MEGΩ CALIBRATION
0.1µF
V_IN
D1
A1
½ LM13600
24 K
A2
½ LM13600
20µf
+15 V
510Ω
3 K
-15 V
0.001µ
30 K
R_O
-15 V
5µF
30 K
10 K
30 K
50µF
V_O
≈1% ACCURATE
A4
½LM1458
A3
½LM1458
-15 V
100 K
V_REF
1.3 K
I_D
Q1
2 K
1 K
1.2 K
+15 V

TL/H/7980-34

FIGURE 27. True RMS Converter

## Additional Applications (Continued)

The circuit of *Figure 28* is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of *Figure 29* responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for $V_{OUT}$ is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 30*.

For generating $I_{ABC}$ over a range of 4 to 6 decades of current, the system of *Figure 31* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B}1 = \frac{(R_1+R_2)\,V_{IN}1}{R_1}$$

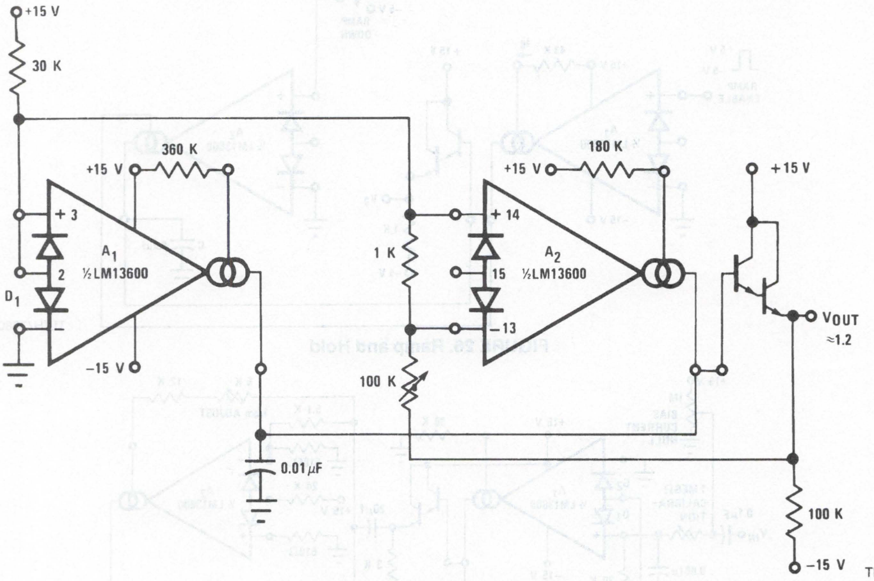
The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B}1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for $I_{ABC}$ yields:

$$I_{ABC} = I_1 \exp\left[\frac{2(R_1+R_2)\,V_C}{R_1I_2R_C}\right]$$

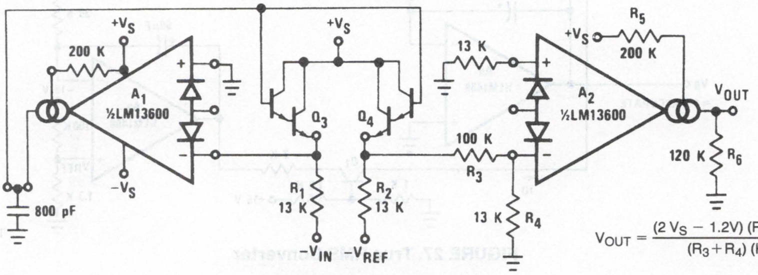
This logarithmic current can be used to bias the circuit of *Figure 4* provide a temperature independent stereo attenuation characteristic.



+15 V
30 K
360 K
+15 V
+ 3
2
A1
½LM13600
D1
−15 V
0.01 µF
1 K
100 K
180 K
+15 V
+ 14
15
13
A2
½LM13600
+15 V
VOUT
≈1.2
100 K
−15 V

TL/H/7980-35

FIGURE 28. Delta VBE Reference



+VS
200 K
A1
½LM13600
−VS
800 pF
+VS
Q3
Q4
R1
13 K
R2
13 K
−VIN
−VREF
13 K
100 K
R3
13 K
R4
A2
½LM13600
+VS
R5
200 K
VOUT
120 K
R6

$$V_{OUT} = \frac{(2\,V_S - 1.2V)\,(R_4)\,(R_6)}{(R_3+R_4)\,(R_5)}\ln\frac{V_{IN}\,R_2}{V_{REF}\,R_1}$$

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FIGURE 29. Log Amplifier

## Additional Applications (Continued)

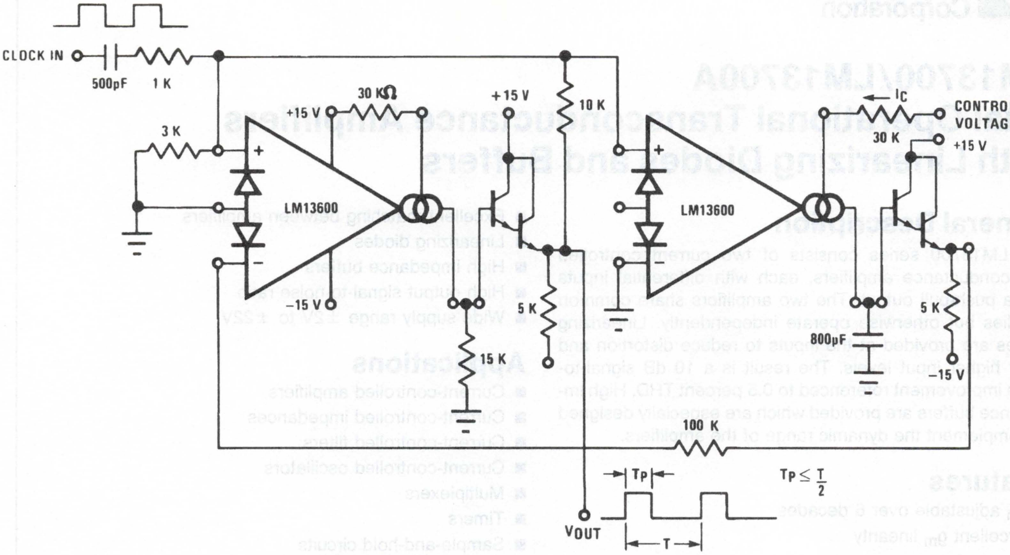
CLOCK IN
500pF
1 K
3 K
+15 V
30 KΩ
LM13600
−15 V
+15 V
10 K
5 K
15 K
100 K
VOUT
Tp
T
Tp ≤ T/2
IC
CONTROL VOLTAGE
30 K
+15 V
LM13600
800pF
5 K
−15 V

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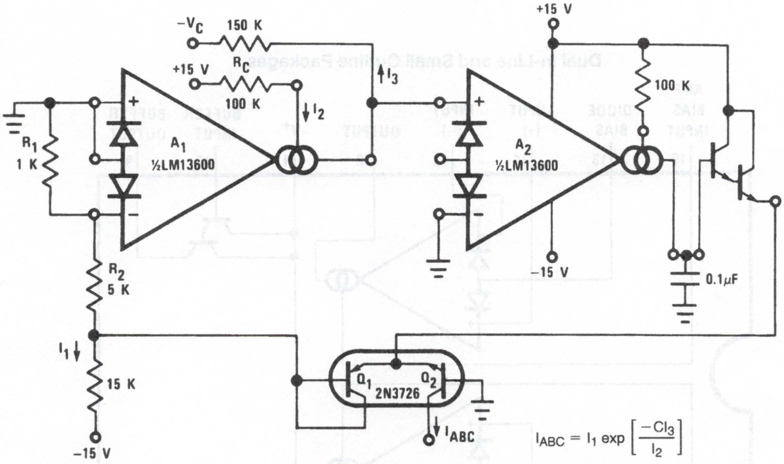
FIGURE 30. Pulse Width Modulator


−VC
150 K
+15 V
RC
100 K
I3
I2
A1
½LM13600
R1
1 K
R2
5 K
I1
15 K
−15 V
Q1
Q2
2N3726
IABC
+15 V
100 K
A2
½LM13600
−15 V
0.1μF

$$I_{ABC} = I_1 \exp\left[\frac{-CI_3}{I_2}\right]$$

TL/H/7980-38

FIGURE 31. Logarithmic Current Source

National Semiconductor Corporation

# LM13700/LM13700A
# Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

## General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

## Features

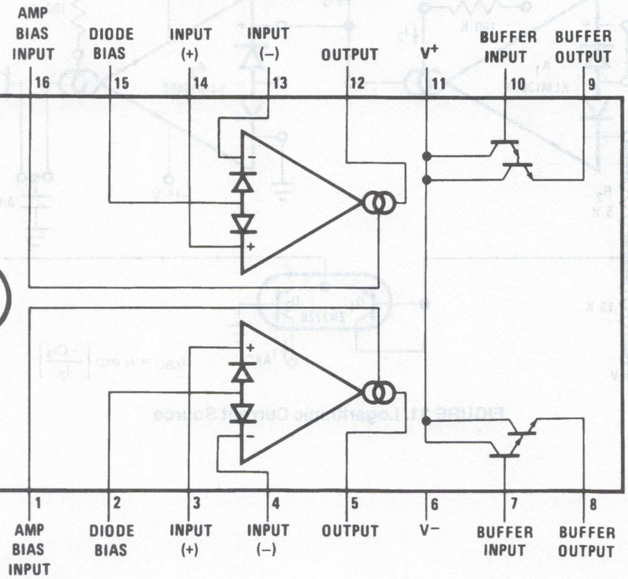
- $g_m$ adjustable over 6 decades
- Excellent $g_m$ linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio
- Wide supply range ±2V to ±22V

## Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

## Connection Diagram

**Dual In-Line and Small Outline Packages**


AMP BIAS INPUT
DIODE BIAS
INPUT (+)
INPUT (−)
OUTPUT
V+
BUFFER INPUT
BUFFER OUTPUT
16
15
14
13
12
11
10
9
−
+
+
−
1
2
3
4
5
6
7
8
AMP BIAS INPUT
DIODE BIAS
INPUT (+)
INPUT (−)
OUTPUT
V−
BUFFER INPUT
BUFFER OUTPUT

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**Top View**

**Order Number LM13700M, LM13700N or LM13700AN**
**See NS Package Number M16A or N16A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (Note 1) | |
| LM13700 | 36 $V_{DC}$ or ±18V |
| LM13700A | 44 $V_{DC}$ or ±22V |
| Power Dissipation (Note 2) $T_A = 25°C$ | |
| LM13700N, LM13700AN | 570 mW |
| Differential Input Voltage | ±5V |
| Diode Bias Current ($I_D$) | 2 mA |
| Amplifier Bias Current ($I_{ABC}$) | 2 mA |
| Output Short Circuit Duration | Indefinite |
| Buffer Output Current (Note 3) | 20 mA |
| Operating Temperature Range | |
| LM13700N, LM13700AN | 0°C to +70°C |
| DC Input Voltage | $+V_S$ to $-V_S$ |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM13700 Min | LM13700 Typ | LM13700 Max | LM13700A Min | LM13700A Typ | LM13700A Max | Units |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($V_{OS}$) | | | 0.4 | 4 | | 0.4 | 1 | mV |
| | Over Specified Temperature Range | | | | | | 2 | |
| | $I_{ABC} = 5\ \mu A$ | | 0.3 | 4 | | 0.3 | 1 | |
| $V_{OS}$ Including Diodes | Diode Bias Current ($I_D$) = 500 µA | | 0.5 | 5 | | 0.5 | 2 | mV |
| Input Offset Change | $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | | 0.1 | 3 | | 0.1 | 1 | mV |
| Input Offset Current | | | 0.1 | 0.6 | | 0.1 | 0.6 | µA |
| Input Bias Current | Over Specified Temperature Range | | 0.4 | 5 | | 0.4 | 5 | µA |
| | | | 1 | 8 | | 1 | 7 | |
| Forward Transconductance ($g_m$) | | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | µmho |
| | Over Specified Temperature Range | 5400 | | | 4000 | | | |
| $g_m$ Tracking | | | 0.3 | | | 0.3 | | dB |
| Peak Output Current | $R_L = 0$, $I_{ABC} = 5\ \mu A$ | | 5 | | 3 | 5 | 7 | µA |
| | $R_L = 0$, $I_{ABC} = 500\ \mu A$ | 350 | 500 | 650 | 350 | 500 | 650 | |
| | $R_L = 0$, Over Specified Temp Range | 300 | | | 300 | | | |
| Peak Output Voltage | | | | | | | | |
| Positive | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | +12 | +14.2 | | +12 | +14.2 | | V |
| Negative | $R_L = \infty$, $5\ \mu A \leq I_{ABC} \leq 500\ \mu A$ | −12 | −14.4 | | −12 | −14.4 | | V |
| Supply Current | $I_{ABC} = 500\ \mu A$, Both Channels | | 2.6 | | | 2.6 | | mA |
| $V_{OS}$ Sensitivity | | | | | | | | |
| Positive | $\Delta V_{OS}/\Delta V^+$ | | 20 | 150 | | 20 | 150 | µV/V |
| Negative | $\Delta V_{OS}/\Delta V^-$ | | 20 | 150 | | 20 | 150 | µV/V |
| CMRR | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| Crosstalk | Referred to Input (Note 5)<br>20 Hz < f < 20 kHz | | 100 | | | 100 | | dB |
| Differential Input Current | $I_{ABC} = 0$, Input = ±4V | | 0.02 | 100 | | 0.02 | 10 | nA |
| Leakage Current | $I_{ABC} = 0$ (Refer to Test Circuit) | | 0.2 | 100 | | 0.2 | 5 | nA |
| Input Resistance | | 10 | 26 | | 10 | 26 | | kΩ |

## Electrical Characteristics (Note 4) (Continued)

| Parameter | Conditions | LM13700 | | | LM13700A | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Bandwidth | | | 2 | | | 2 | | MHz |
| Slew Rate | Unity Gain Compensated | | 50 | | | 50 | | V/µs |
| Buffer Input Current | (Note 5) | | 0.5 | 2 | | 0.5 | 2 | µA |
| Peak Buffer Output Voltage | (Note 5) | 10 | | | 10 | | | V |

**Note 1:** For selections to a supply voltage above ±22V, contact factory.

**Note 2:** For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W; LM13700M, 110°C/W.

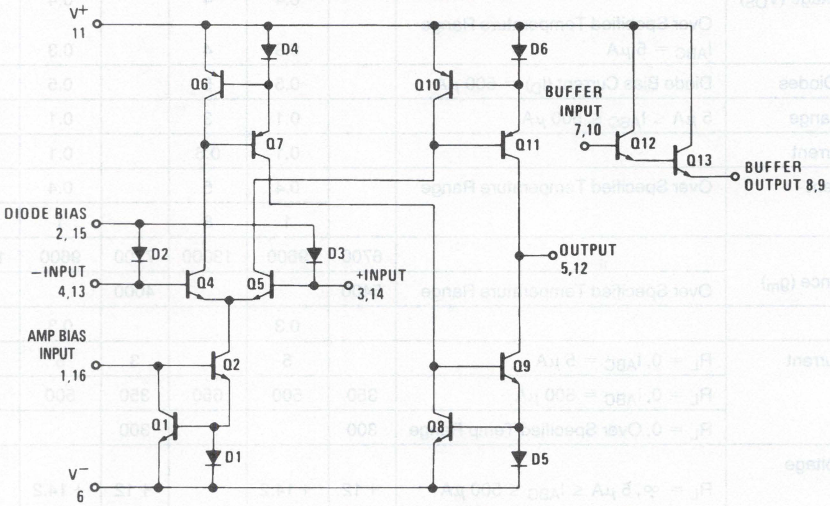
**Note 3:** Buffer output current should be limited so as to not exceed package dissipation.

**Note 4:** These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current ($I_{ABC}$) = 500 µA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

**Note 5:** These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\ \mu A$, $R_{OUT} = 5\ k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

## Schematic Diagram

**One Operational Transconductance Amplifier**


V+
11
D4
Q6
Q7
Q10
D6
BUFFER
INPUT
7,10
Q11
Q12
Q13
BUFFER
OUTPUT 8,9
DIODE BIAS
2, 15
D2
D3
−INPUT
4,13
Q4
Q5
+INPUT
3,14
OUTPUT
5,12
AMP BIAS
INPUT
1,16
Q2
Q9
Q1
Q8
D1
D5
V−
6

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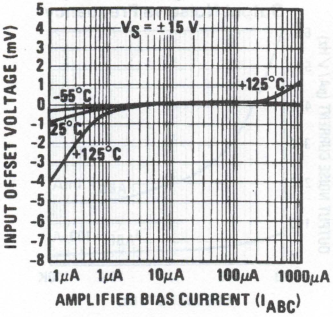
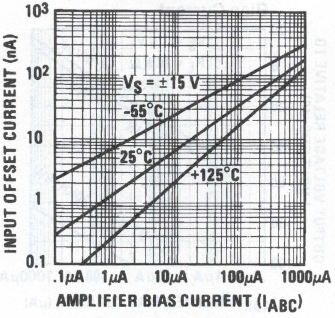
## Typical Performance Characteristics

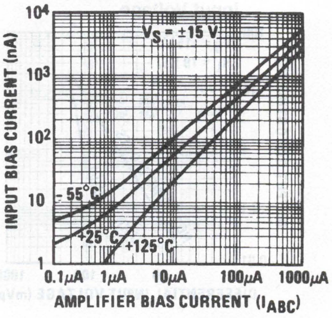
Input Offset Voltage



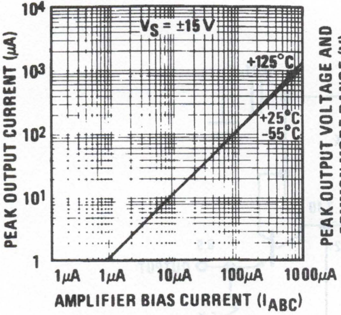
Input Offset Current



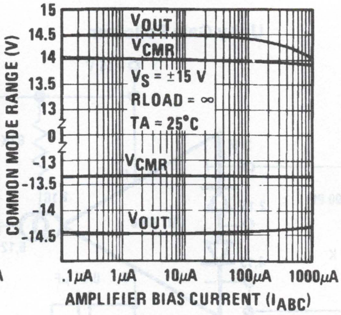
Input Bias Current



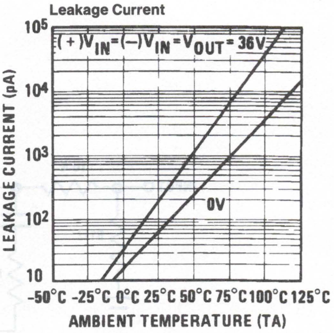
Peak Output Current



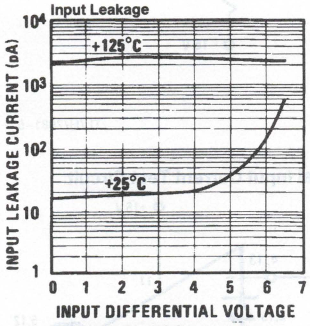
Peak Output Voltage and Common Mode Range



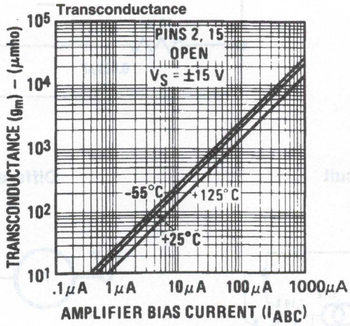
Leakage Current



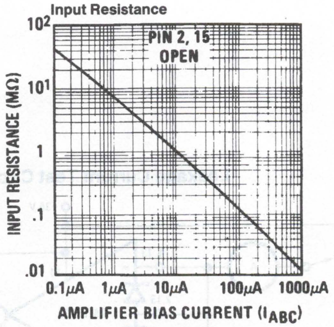
Input Leakage



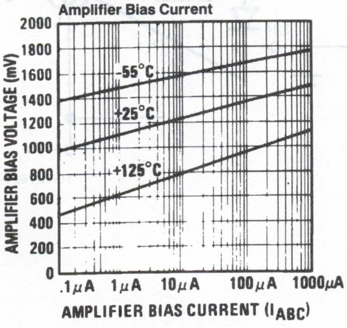
Transconductance



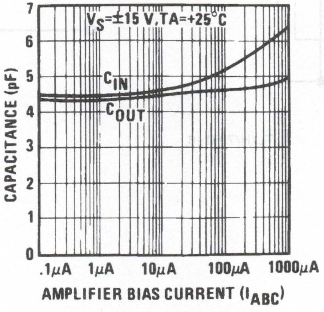
Input Resistance



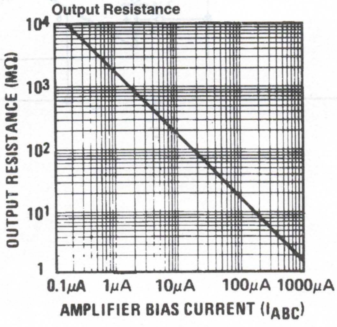
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance



Output Resistance



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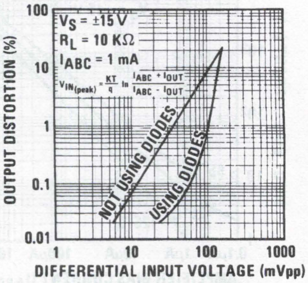
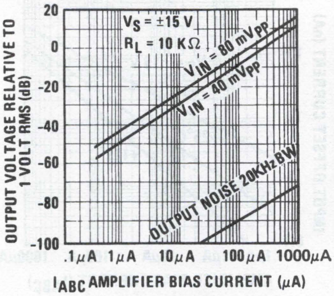
## Typical Performance Characteristics (Continued)

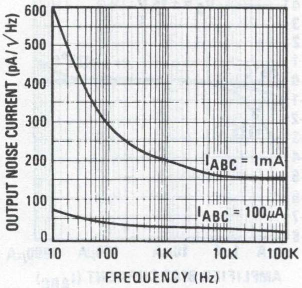
**Distortion vs Differential Input Voltage**



**Voltage vs Amplifier Bias Current**

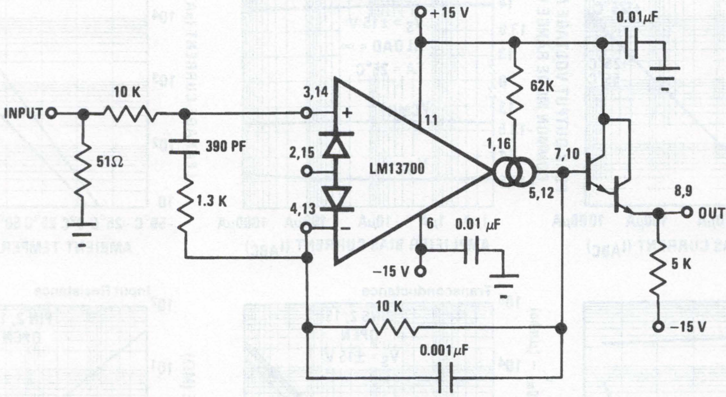


**Output Noise vs Frequency**



TL/H/7981-4

**Unity Gain Follower**


+15 V
0.01μF
62K
INPUT
10 K
3,14
+
11
51Ω
390 PF
2,15
LM13700
1,16
7,10
1.3 K
5,12
8,9
OUTPUT
4,13
−
6
0.01 μF
−15 V
5 K
−15 V
10 K
0.001μF

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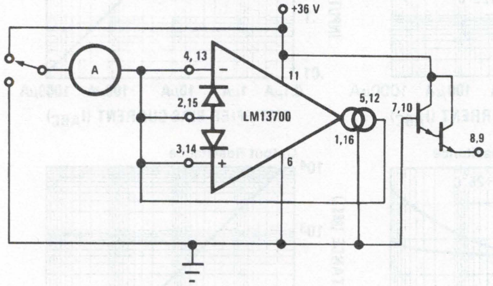
**Leakage Current Test Circuit**


+36 V
A
4, 13
−
11
2,15
LM13700
5,12
7,10
1,16
8,9
3,14
+
6

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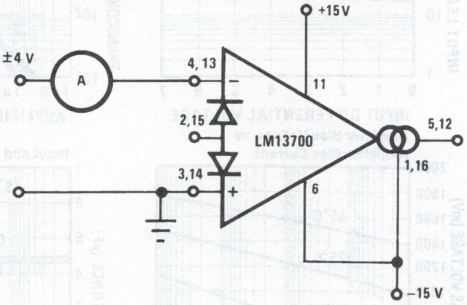
**Differential Input Current Test Circuit**


+15V
±4 V
A
4, 13
11
2,15
LM13700
5,12
1,16
3,14
+
6
−15 V

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## Circuit Description

The differential transistor pair $Q_4$ and $Q_5$ form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where $V_{IN}$ is the differential input voltage, $kT/q$ is approximately 26 mV at 25°C and $I_5$ and $I_4$ are the collector currents of transistors $Q_5$ and $Q_4$ respectively. With the exception of $Q_3$ and $Q_{13}$, all transistors and diodes are identical in size. Transistors $Q_1$ and $Q_2$ with Diode $D_1$ form a current mirror which forces the sum of currents $I_4$ and $I_5$ to equal $I_{ABC}$;

$$I_4 + I_5 = I_{ABC} \qquad (2)$$

where $I_{ABC}$ is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of $I_4$ and $I_5$ approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_5 - I_4 \qquad (4)$$

Collector currents $I_4$ and $I_5$ are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to $I_5$ minus $I_4$ thus:

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to $I_{ABC}$.

## Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current $I_S$. Since the sum of $I_4$ and $I_5$ is $I_{ABC}$ and the difference is $I_{OUT}$, currents $I_4$ and $I_5$ can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S \left(\frac{2I_{ABC}}{I_D}\right) \quad \text{for } |I_S| < \frac{I_D}{2} \qquad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

## Applications: Voltage Controlled Amplifiers

*Figure 2* shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.

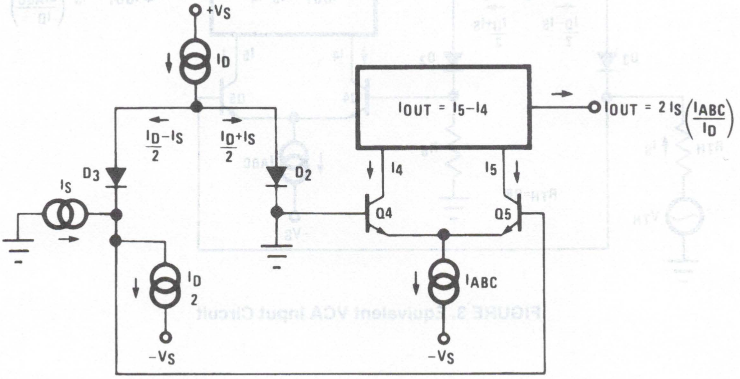

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**FIGURE 1. Linearizing Diodes**

## Applications: Voltage Controlled Amplifiers (Continued)

For optimum signal-to-noise performance, $I_{ABC}$ should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via $R_{IN}$ *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting $R_L$.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, $I_D$ should be as large as possible. This minimizes the dynamic junction resistance of the diodes ($r_e$) and maximizes their linearizing action when balanced against $R_{IN}$. A value of 1 mA is recommended for $I_D$ unless the specific application demands otherwise.

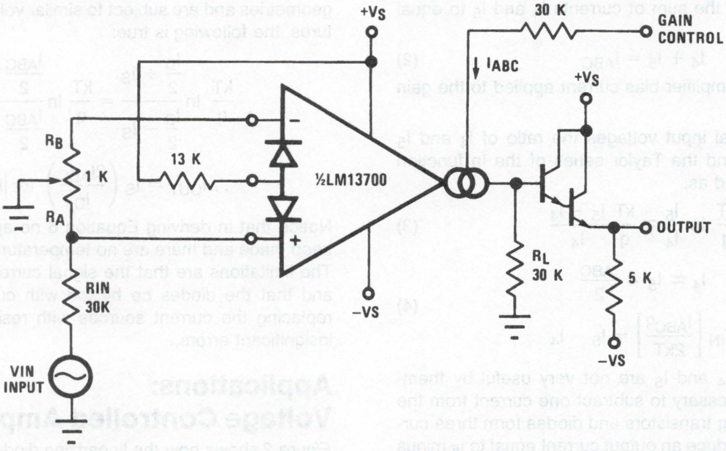
+VS
30 K
GAIN CONTROL
IABC
+VS
RB
1 K
RA
13 K
½LM13700
−
+
OUTPUT
RL
30 K
5 K
−VS
RIN
30K
VIN
INPUT
−VS
−VS

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FIGURE 2. Voltage Controlled Amplifier

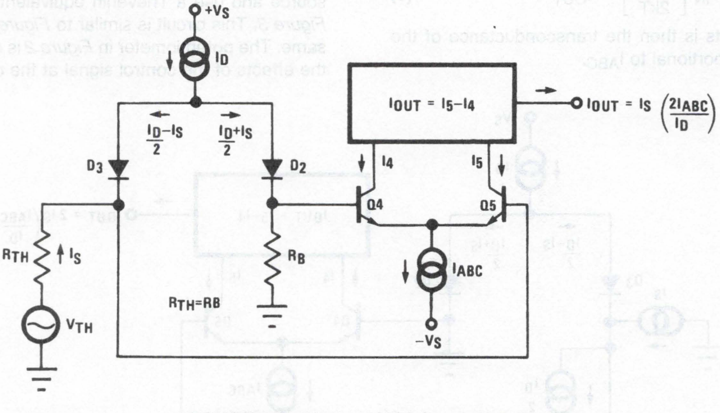
+VS
ID
ID−IS / 2
ID+IS / 2
D3
D2
IOUT = I5−I4
IOUT = IS (2IABC / ID)
I4
I5
Q4
Q5
RTH
IS
RB
RTH=RB
IABC
−VS
VTH

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FIGURE 3. Equivalent VCA Input Circuit

## Stereo Volume Control

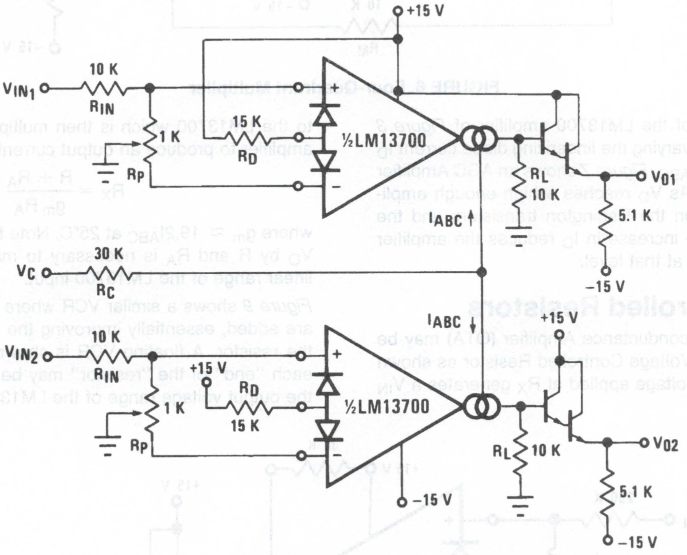
The circuit of *Figure 4* uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. $R_P$ is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If $V_C$ is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

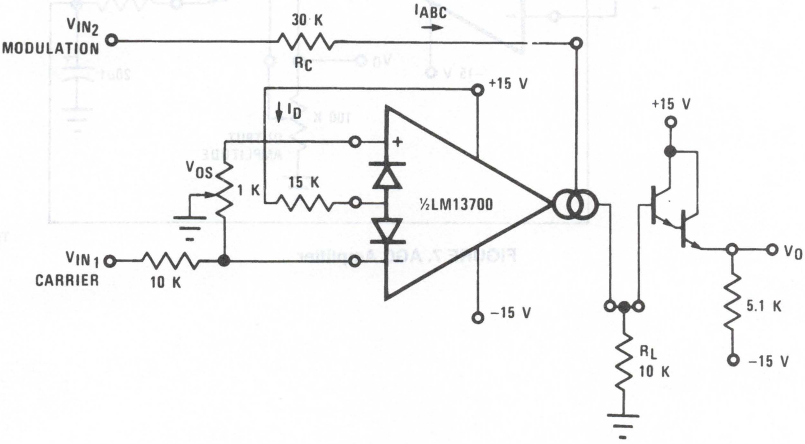
$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2(V^- + 1.4V)$ into $I_O$. The circuit of *Figure 6* adds $R_M$ to provide this current, resulting in a four-quadrant multiplier where $R_C$ is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. $R_M$ also serves as the load resistor for $I_O$.


+15 V
V_IN1
10 K
R_IN
1 K
R_P
15 K
R_D
½LM13700
R_L
10 K
V01
I_ABC
5.1 K
−15 V
V_C
30 K
R_C
+15 V
V_IN2
10 K
R_IN
+15 V
R_D
1 K
15 K
R_P
½LM13700
R_L
10 K
V02
5.1 K
−15 V
−15 V

TL/H/7981–11

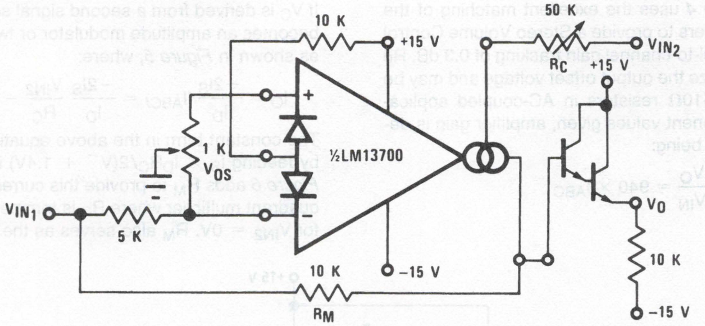
FIGURE 4. Stereo Volume Control


V_IN2
MODULATION
30 K
R_C
I_ABC
+15 V
I_D
V_OS
1 K
15 K
½LM13700
V_IN1
CARRIER
10 K
−15 V
+15 V
V_O
5.1 K
−15 V
R_L
10 K

TL/H/7981–12

FIGURE 5. Amplitude Modulator

## Stereo Volume Control (Continued)



TL/H/7981–13

**FIGURE 6. Four-Quadrant Multiplier**

Noting that the gain of the LM13700 amplifier of *Figure 3* may be controlled by varying the linearizing diode current $I_D$ as well as by varying $I_{ABC}$, *Figure 7* shows an AGC Amplifier using this approach. As $V_O$ reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in $I_D$ reduces the amplifier gain so as to hold $V_O$ at that level.

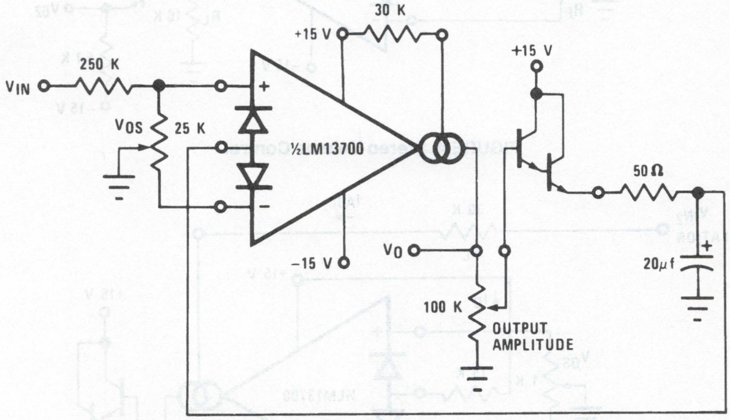
## Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at $R_X$ generates a $V_{IN}$ to the LM13700 which is then multiplied by the $g_m$ of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of $V_O$ by R and $R_A$ is necessary to maintain $V_{IN}$ within the linear range of the LM13700 input.

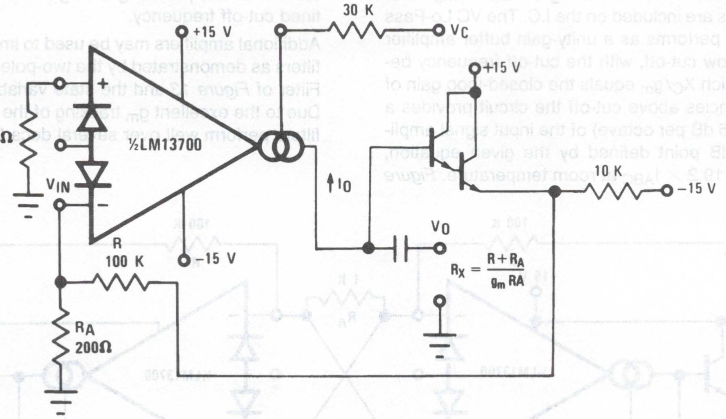
*Figure 9* shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each “end” of the “resistor” may be at any voltage within the output voltage range of the LM13700.



TL/H/7981–14

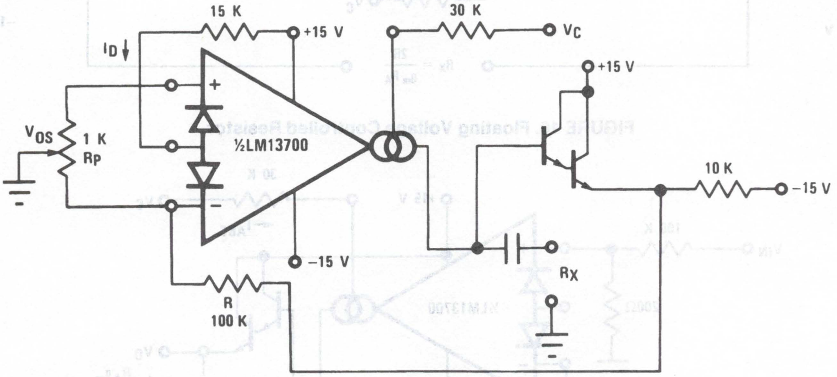
**FIGURE 7. AGC Amplifier**

## Voltage Controlled Resistors (Continued)


+15 V
30 K
$V_C$
+15 V
+
−
200Ω
½LM13700
$V_{IN}$
$I_O$
10 K
−15 V
R
100 K
−15 V
$V_O$
$R_X = \frac{R + R_A}{g_m R_A}$
$R_A$
200Ω

TL/H/7981–15

FIGURE 8. Voltage Controlled Resistor, Single-Ended


15 K
+15 V
30 K
$V_C$
$I_D$
+15 V
+
−
$V_{OS}$
1 K
$R_P$
½LM13700
10 K
−15 V
−15 V
$R_X$
R
100 K

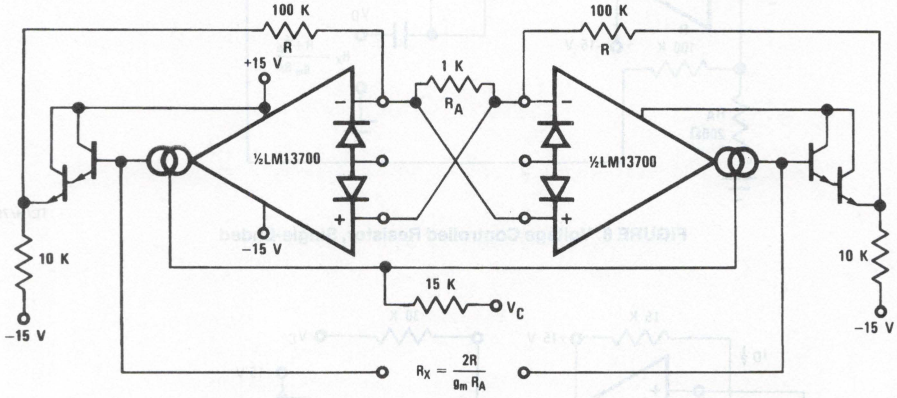
TL/H/7981–16

FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

## Voltage Controlled Filters

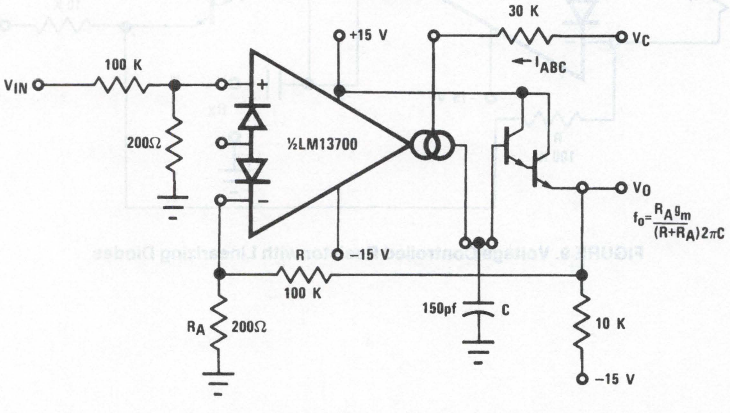
OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which $X_C/g_m$ equals the closed-loop gain of $(R/R_A)$. At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where $g_m$ is again $19.2 \times I_{ABC}$ at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent $g_m$ tracking of the two amplifiers, these filters perform well over several decades of frequency.


100 K
R
+15 V
1 K
$R_A$
100 K
R
½LM13700
½LM13700
−15 V
10 K
−15 V
10 K
−15 V
15 K
$V_C$
$R_X = \frac{2R}{g_m R_A}$

TL/H/7981–17

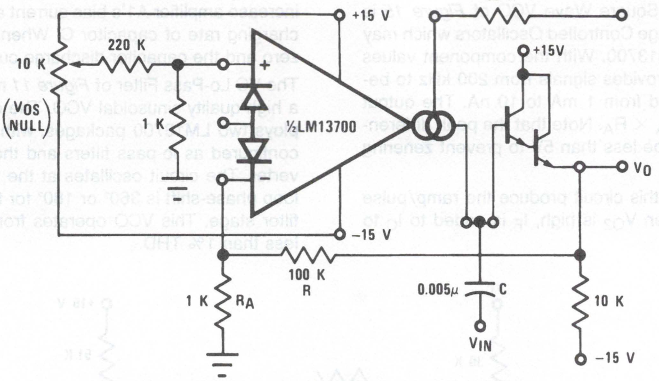
**FIGURE 10. Floating Voltage Controlled Resistor**


30 K
$V_C$
$I_{ABC}$
+15 V
$V_{IN}$
100 K
200Ω
½LM13700
$V_O$
$f_o = \frac{R_A g_m}{(R+R_A)2\pi C}$
R
−15 V
100 K
$R_A$
200Ω
150pf
C
10 K
−15 V

TL/H/7981–18

**FIGURE 11. Voltage Controlled Low-Pass Filter**

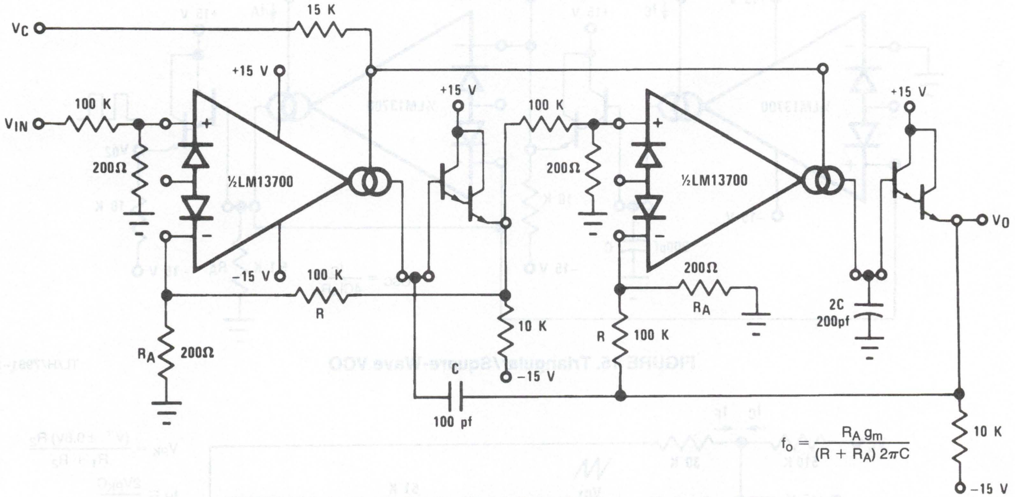
## Voltage Controlled Filters (Continued)


30 K
+15 V
220 K
10 K
+15V
(VOS NULL)
1 K
½LM13700
VO
-15 V
100 K
R
1 K
RA
0.005μ
C
VIN
10 K
-15 V

$$f_o = \frac{R_A\, g_m}{(R + R_A)\, 2\pi C}$$

**FIGURE 12. Voltage Controlled Hi-Pass Filter**

TL/H/7981-19


VC
15 K
+15 V
100 K
VIN
200Ω
½LM13700
-15 V
100 K
R
RA
200Ω
+15 V
100 K
200Ω
10 K
-15 V
C
100 pf
½LM13700
200Ω
RA
R
100 K
2C
200pf
+15 V
VO
10 K
-15 V

$$f_o = \frac{R_A\, g_m}{(R + R_A)\, 2\pi C}$$

**FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter**

TL/H/7981-20

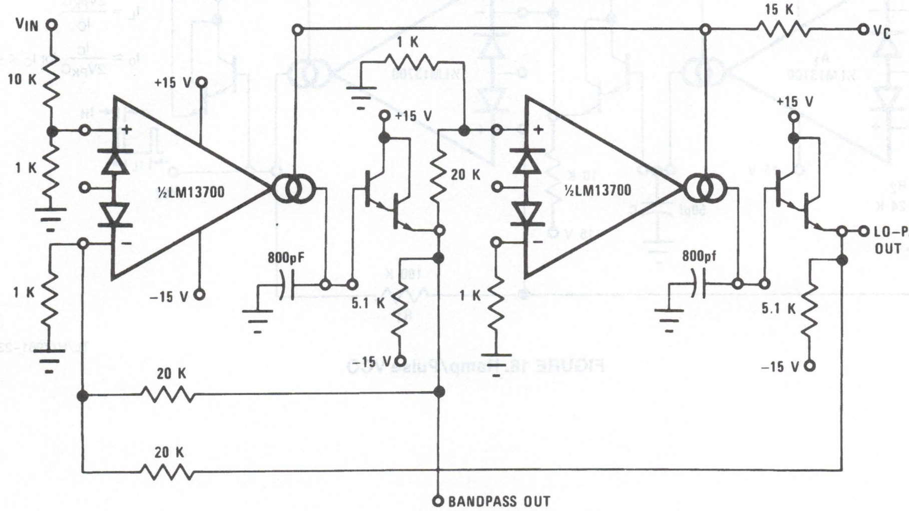

VIN
10 K
1 K
1 K
+15 V
½LM13700
-15 V
800pF
1 K
+15 V
20 K
5.1 K
-15 V
15 K
VC
½LM13700
1 K
800pf
+15 V
5.1 K
-15 V
LO-PASS OUT
20 K
20 K
BANDPASS OUT

**FIGURE 14. Voltage Controlled State Variable Filter**

TL/H/7981-21

## Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as $I_C$ is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When $V_{O2}$ is high, $I_F$ is added to $I_C$ to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When $V_{O2}$ is low, $I_F$ goes to zero and the capacitor discharge current is set by $I_C$.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

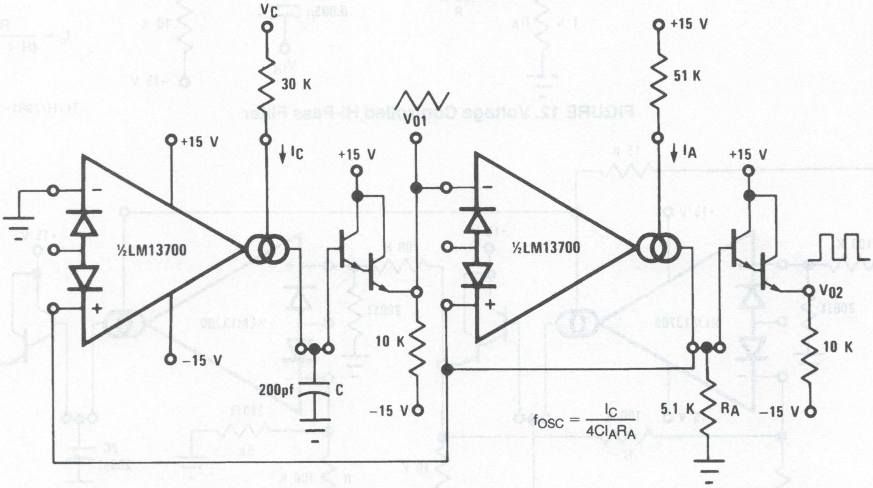
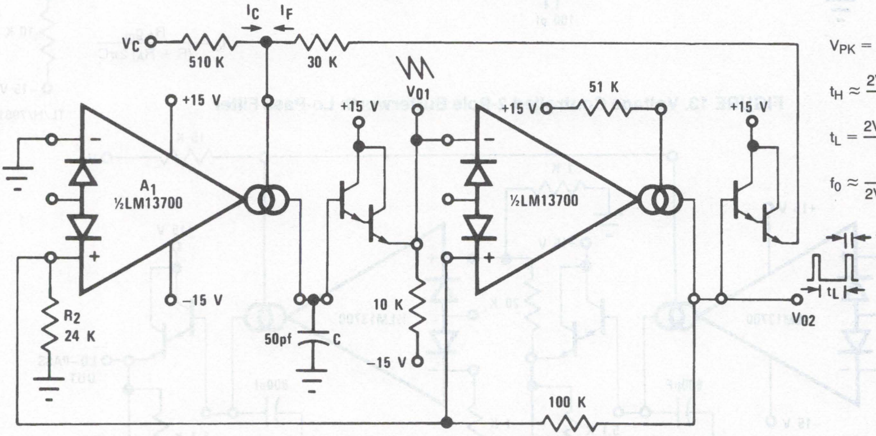

V_C
30 K
I_C
+15 V
+15 V
½LM13700
−15 V
200pf
C
V_O1
10 K
−15 V
+15 V
51 K
I_A
+15 V
½LM13700
V_O2
10 K
5.1 K
R_A
−15 V
f_OSC = I_C / 4CI_AR_A

**FIGURE 15. Triangular/Square-Wave VCO**

TL/H/7981-22


V_C
510 K
I_C
I_F
30 K
+15 V
A_1
½LM13700
−15 V
R_2
24 K
+15 V
V_O1
50pf
C
10 K
−15 V
51 K
+15 V
½LM13700
+15 V
100 K
R_1
t_H
t_L
V_O2

$$V_{PK} = \frac{(V^+ \pm 0.8V)\,R_2}{R_1 + R_2}$$

$$t_H \approx \frac{2V_{PK}C}{I_F}$$

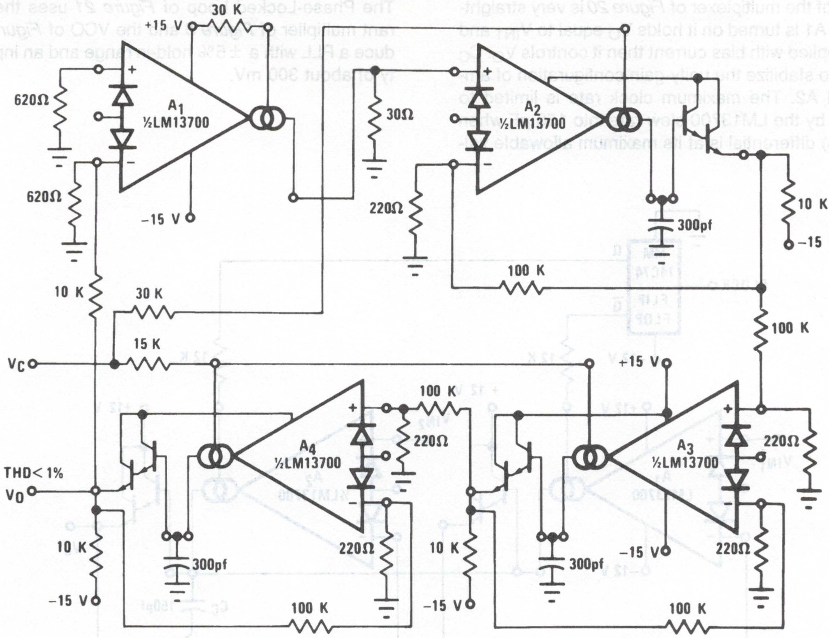
$$t_L = \frac{2V_{PK}C}{I_C}$$

$$f_0 \approx \frac{I_C}{2V_{PK}C} \text{ for } I_C << I_F$$

TL/H/7981-23

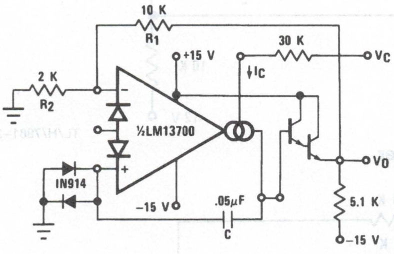
**FIGURE 16. Ramp/Pulse VCO**

## Voltage Controlled Oscillators (Continued)


30 K
+15 V
620Ω
A1
½LM13700
30Ω
620Ω
−15 V
A2
½LM13700
220Ω
300pf
10 K
−15 V
100 K
10 K
30 K
15 K
100 K
VC
+15 V
100 K
220Ω
A4
½LM13700
THD< 1%
VO
10 K
300pf
220Ω
−15 V
100 K
10 K
−15 V
300pf
A3
½LM13700
220Ω
−15 V
220Ω
100 K

TL/H/7981-24

FIGURE 17. Sinusoidal VCO


10 K
R1
2 K
R2
+15 V
30 K
VC
IC
½LM13700
VO
IN914
−15 V
.05μF
C
5.1 K
−15 V

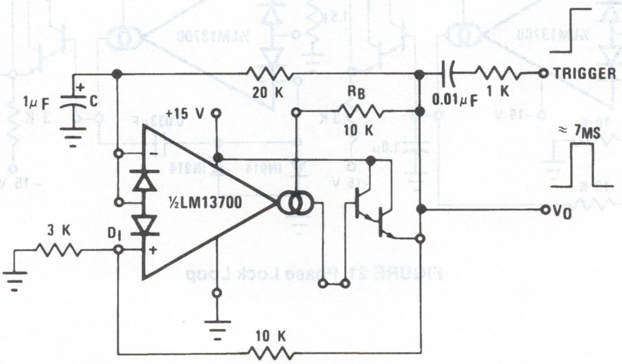
TL/H/7981-25

FIGURE 18. Single Amplifier VCO

*Figure 18* shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

## Additional Applications

*Figure 19* presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through $R_B$ and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through $D_I$ when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from $V_O$, can perform another function and draw zero stand-by power as well.


TRIGGER
20 K
RB
0.01μF
1 K
1μF
C
+15 V
10 K
≈ 7MS
½LM13700
VO
3 K
DI
10 K

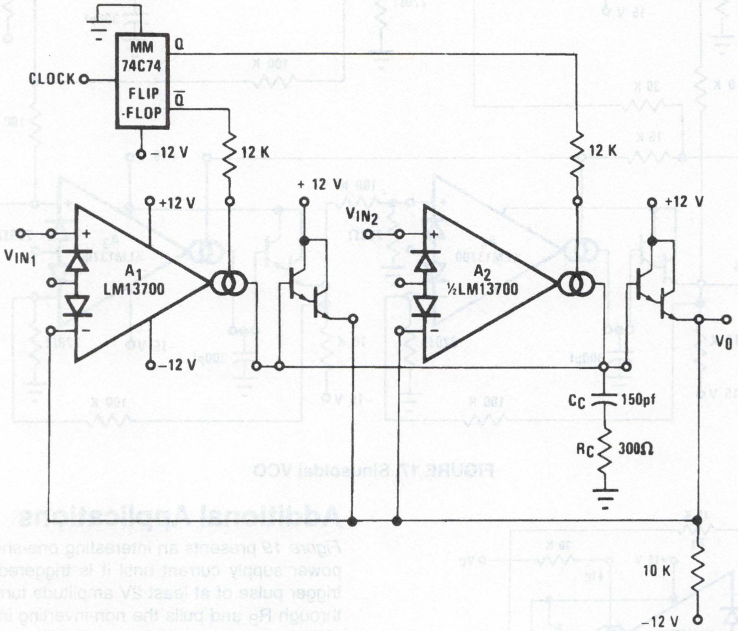
TL/H/7981-26

FIGURE 19. Zero Stand-By Power Timer

## Additional Applications (Continued)

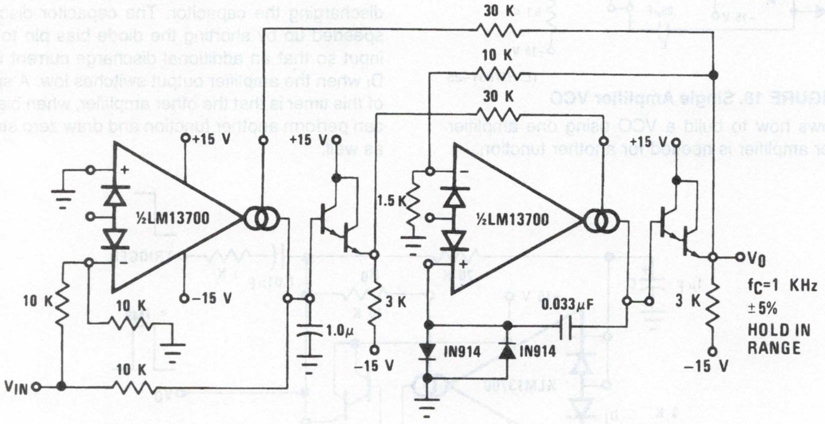
The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds $V_O$ equal to $V_{IN1}$ and when A2 is supplied with bias current then it controls $V_O$. $C_C$ and $R_C$ serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the ($V_{IN1}-V_{IN2}$) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.


MM
74C74
FLIP
FLOP
Q
Q̄
CLOCK
−12 V
12 K
12 K
+12 V
+ 12 V
+12 V
$V_{IN_1}$
$V_{IN_2}$
$A_1$
LM13700
$A_2$
½LM13700
−12 V
$V_O$
$C_C$
150pf
$R_C$
300Ω
10 K
−12 V

TL/H/7981–27

**FIGURE 20. Multiplexer**

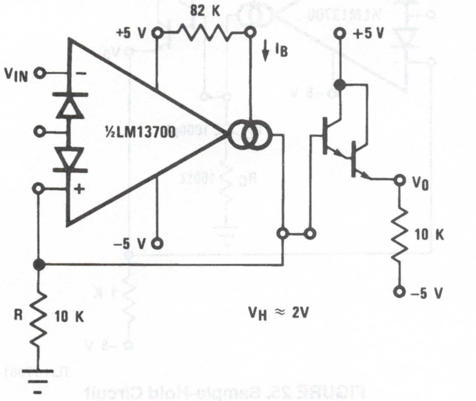

30 K
10 K
30 K
+15 V
+15 V
+15 V
½LM13700
½LM13700
1.5 K
10 K
10 K
−15 V
1.0µ
3 K
−15 V
10 K
$V_{IN}$
IN914
IN914
0.033µF
$V_O$
3 K
−15 V
$f_C$=1 KHz
±5%
HOLD IN
RANGE

TL/H/7981–28

**FIGURE 21. Phase Lock Loop**

## Additional Applications (Continued)

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying $I_B$ will produce a Schmitt Trigger with variable hysteresis.

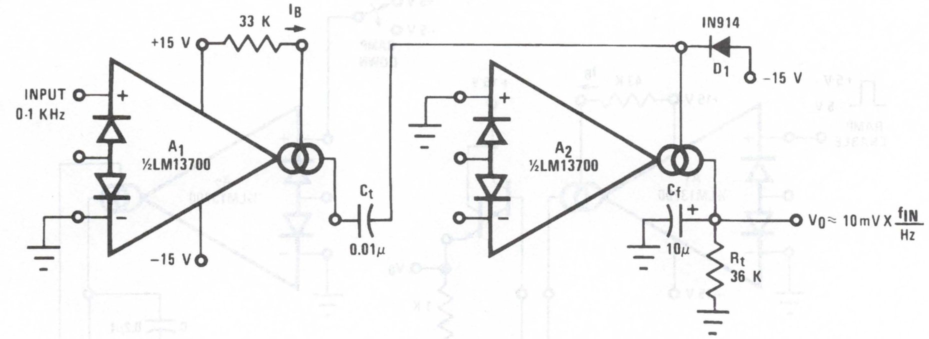

82 K
+5 V
$I_B$
+5 V
$V_{IN}$
−
½LM13700
+
$V_O$
−5 V
10 K
−5 V
R
10 K
$V_H \approx 2V$

TL/H/7981–29

**FIGURE 22. Schmitt Trigger**

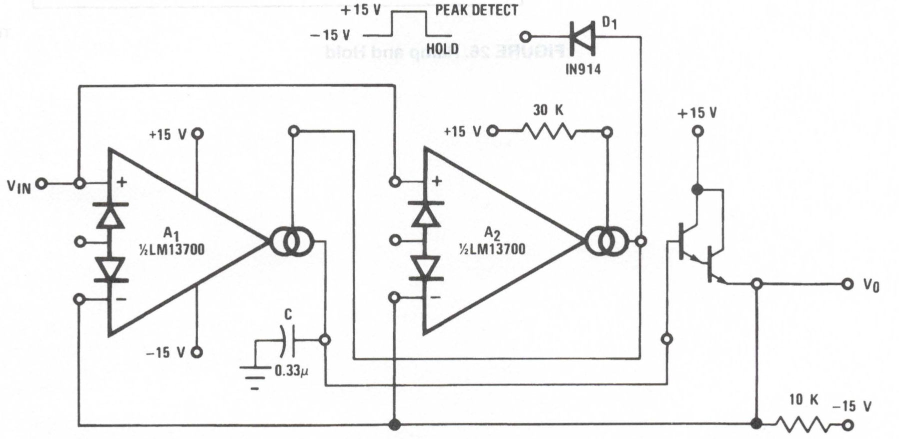
*Figure 23* shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\,C_t$ is sourced into $C_f$ and $R_t$. This once per cycle charge is then balanced by the current of $V_O/R_t$. The maximum $F_{IN}$ is limited by the amount of time required to charge $C_t$ from $V_L$ to $V_H$ with a current of $I_B$, where $V_L$ and $V_H$ represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for $C_t$ when A1 switches low.

The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever $V_{IN}$ becomes more positive than $V_O$. A1 then charges storage capacitor C to hold $V_O$ equal to $V_{IN}$ PK. Pulling the output of A2 low through D1 serves to turn off A1 so that $V_O$ remains constant.


$I_B$
33 K
+15 V
INPUT
0.1 KHz
+
$A_1$
½LM13700
−
−15 V
$C_t$
0.01μ
IN914
$D_1$
−15 V
+
$A_2$
½LM13700
−
$C_f$
+
10μ
$R_t$
36 K
$V_O \approx 10\,mV \times \frac{f_{IN}}{Hz}$

TL/H/7981–30

**FIGURE 23. Tachometer**


+15 V
PEAK DETECT
−15 V
HOLD
$D_1$
IN914
+15 V
$V_{IN}$
+
$A_1$
½LM13700
−
−15 V
C
0.33μ
30 K
+15 V
+
$A_2$
½LM13700
−
+15 V
$V_O$
10 K
−15 V

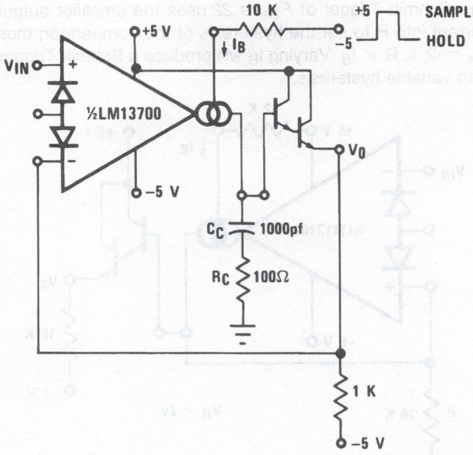
TL/H/7981–31

**FIGURE 24. Peak Detector and Hold Circuit**

## Additional Applications (Continued)

The Ramp-and-Hold of *Figure 26* sources $I_B$ into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

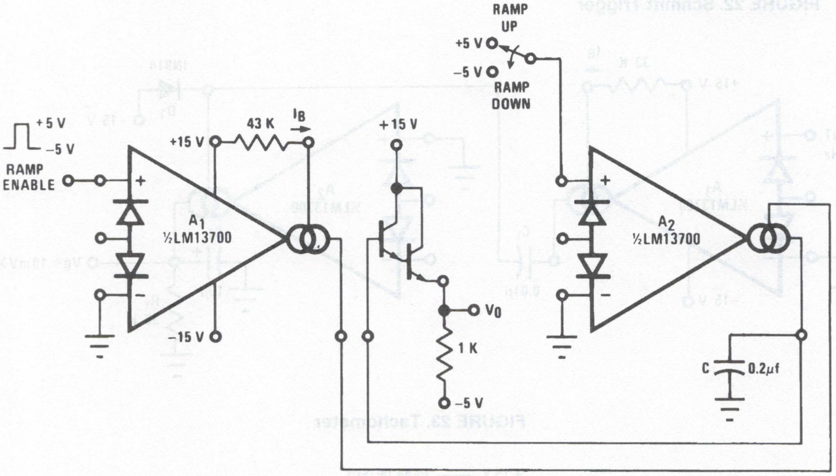
The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that $V_O$ reads directly in RMS volts.



+5 V
10 K
+5
−5
SAMPLE
HOLD
I_B
V_IN
+
−
½LM13700
V_O
−5 V
C_C
1000pf
R_C
100Ω
1 K
−5 V

TL/H/7981-32

FIGURE 25. Sample-Hold Circuit

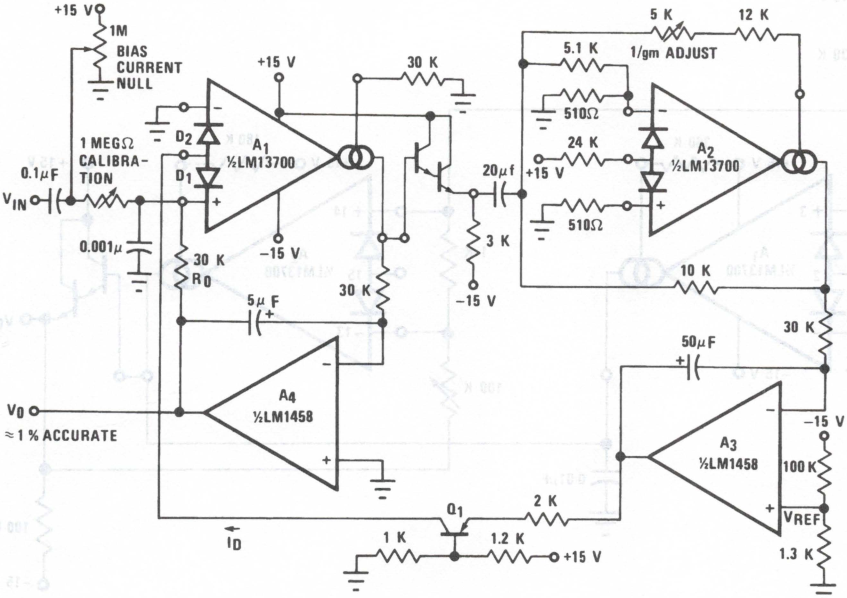


RAMP
UP
+5 V
−5 V
RAMP
DOWN
+5 V
−5 V
RAMP
ENABLE
+15 V
43 K
I_B
+15 V
A_1
½LM13700
+
−
−15 V
V_O
1 K
−5 V
A_2
½LM13700
C
0.2μf

TL/H/7981-33

FIGURE 26. Ramp and Hold

## Additional Applications (Continued)


+15 V
1M
BIAS
CURRENT
NULL
1 MEGΩ
CALIBRA-
TION
0.1μF
$V_{IN}$
0.001μ
$D_2$
$D_1$
30 K
$R_0$
+15 V
$A_1$
½LM13700
−15 V
30 K
5μ F
30 K
$A_4$
½LM1458
$V_0$
≈1% ACCURATE
$I_D$
$Q_1$
1 K
1.2 K
+15 V
2 K
20μf
+15 V
3 K
−15 V
5.1 K
5 K
1/gm ADJUST
12 K
510Ω
24 K
510Ω
$A_2$
½LM13700
10 K
30 K
50μF
$A_3$
½LM1458
−15 V
100 K
$V_{REF}$
1.3 K

TL/H/7981–34

**FIGURE 27. True RMS Converter**

The circuit of *Figure 28* is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 29*.

For generating $I_{ABC}$ over a range of 4 to 6 decades of current, the system of *Figure 30* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{-2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1 + R_2)\,V_{IN}1}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

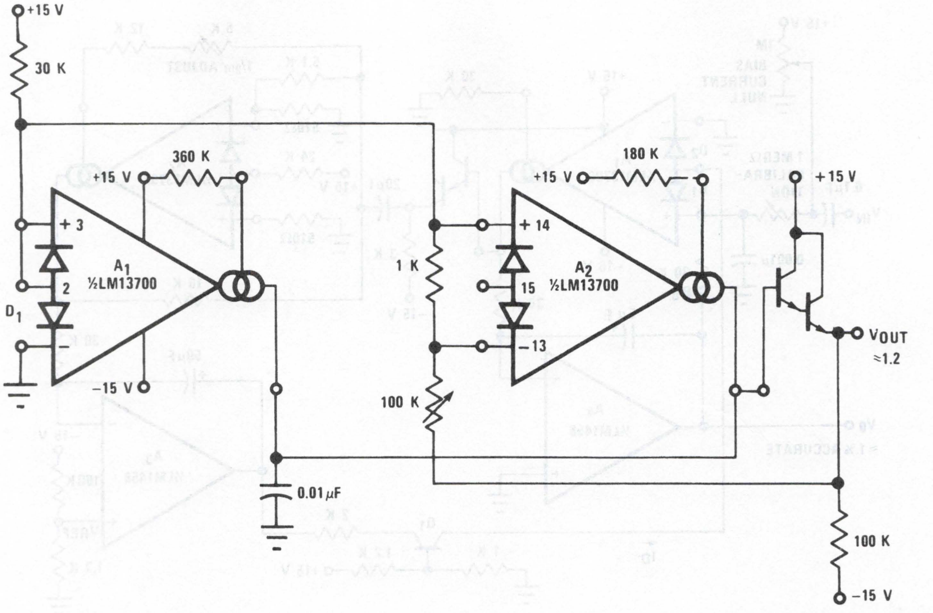
$$V_B1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for $I_{ABC}$ yields:

$$I_{ABC} = I_1 \exp\frac{2(R_1 + R_2)\,V_C}{R_1\,I_2\,R_C}$$

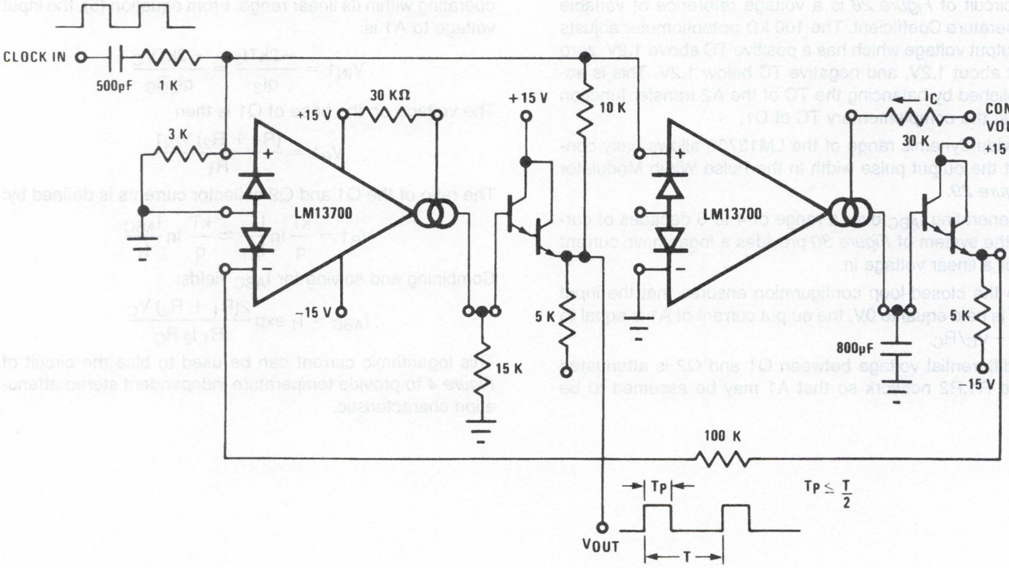
This logarithmic current can be used to bias the circuit of *Figure 4* to provide temperature independent stereo attenuation characteristic.

## Additional Applications (Continued)


+15 V
30 K
360 K
+15 V
+ 3
2
A1
½LM13700
D1
−15 V
1 K
100 K
0.01 μF
+ 14
15
−13
180 K
+15 V
A2
½LM13700
+15 V
VOUT
≈1.2
100 K
−15 V

TL/H/7981-35

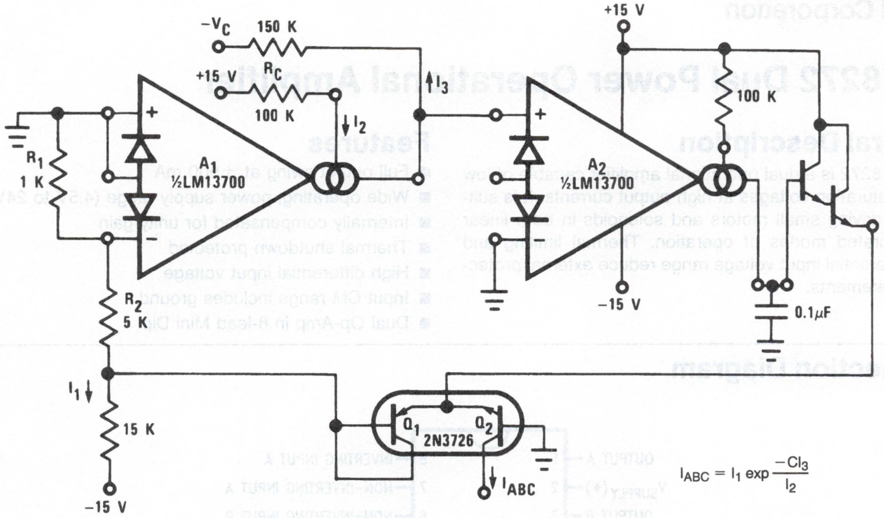
FIGURE 28. Delta VBE Reference


CLOCK IN
500pF
1 K
3 K
+15 V
30 KΩ
+
−
LM13700
−15 V
+15 V
10 K
5 K
15 K
IC
CONTROL VOLTAGE
30 K
+15 V
+
−
LM13700
5 K
800pF
−15 V
100 K
Tp
Tp ≤ T/2
VOUT
T

TL/H/7981-36

FIGURE 29. Pulse Width Modulator

## Additional Applications (Continued)


−V_C
150 K
+15 V
R_C
100 K
I_2
I_3
+
−
R_1
1 K
A_1
½LM13700
R_2
5 K
I_1
15 K
−15 V
Q_1
Q_2
2N3726
I_ABC
+15 V
100 K
+
A_2
½LM13700
−15 V
0.1μF

$$I_{ABC} = I_1 \exp \frac{-CI_3}{I_2}$$

TL/H/7981–37

FIGURE 30. Logarithmic Current Source

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**ADVANCED INFORMATION**

# LM18272 Dual Power Operational Amplifier

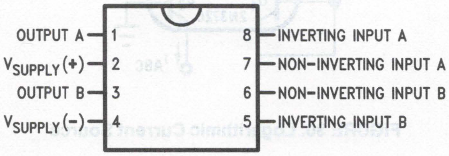
## General Description

The LM18272 is a dual operational amplifier capable of low output saturation voltages at high output currents. It is suitable for driving small motors and solenoids in both linear and saturated modes of operation. Thermal limiting and wide differential input voltage range reduce external protection requirements.

## Features

- Full output swing at ±500 mA
- Wide operating, power supply range (4.5V to 24V)
- Internally compensated for unity gain
- Thermal shutdown protected
- High differential input voltage
- Input CM range includes ground
- Dual Op-Amp in 8-lead Mini Dip

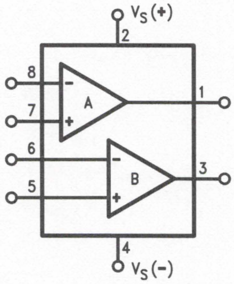
## Connection Diagram



OUTPUT A
1
$V_{SUPPLY}(+)$
2
OUTPUT B
3
$V_{SUPPLY}(-)$
4
8
INVERTING INPUT A
7
NON-INVERTING INPUT A
6
NON-INVERTING INPUT B
5
INVERTING INPUT B

TL/H/9310–1

**Order Number LM18272N**
**See NS Package Number N08E**



$V_S(+)$
2
8
7
6
5
A
B
1
3
4
$V_S(-)$

TL/H/9310–2

National Semiconductor Corporation

**PRELIMINARY**

# LMC660AM/LMC660AI/LMC660C CMOS Quad Operational Amplifier

## General Description

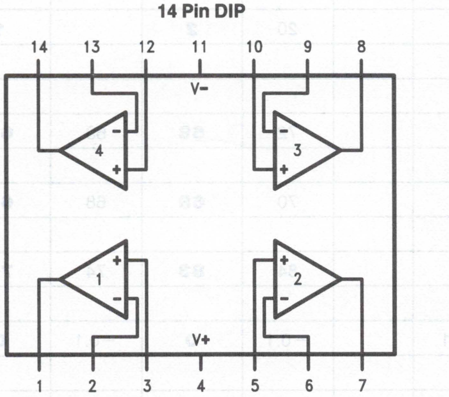
The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input $V_{OS}$, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

## Features

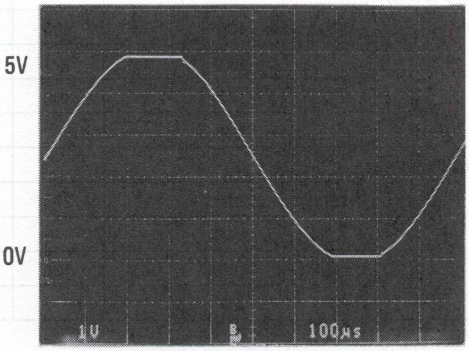
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV max
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- $I_{SS}$ = 375 μA/amplifier; independent of $V^+$
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Insensitive to latch-up

## Connection Diagram



**Order Number LMC660AMD or LMC660AID**
**Order Number LMC660AIN or LMC660CN**
**See NS Package Number D14E or N14A**

## Output Swing



$V^+$ = 5V $R_L$ = 2 kΩ

TL/H/8767-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Differential Input Voltage | ±Supply Voltage |
| Either Input beyond $V^+$ or $V^-$ | 0.7V |
| Supply Voltage | 16V |
| Output Short Circuit to GND (Note 1) | Continuous |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temp. Range | −65°C to +150°C |
| Operating Temperature Range | |
| LMC660AM | −55°C to +125°C |
| LMC660AI | −40°C to +85°C |
| LMC660C | 0°C to +70°C |
| Operating Supply Range | 4.75V to 15.5V |
| Junction Temperature (Note 2) | 150°C |

ESD rating is to be determined.

## DC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LMC660AM Tested Limit (Note 4) | LMC660AM Design Limit (Note 5) | LMC660AI Tested Limit (Note 4) | LMC660AI Design Limit (Note 5) | LMC660C Tested Limit (Note 4) | LMC660C Design Limit (Note 5) | Units |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | 1 | 3<br>**3.5** | | 3 | **3.3** | 6 | **6.3** | mV max |
| Input Offset Voltage Average Drift | | 1.3 | | | | | | | µV/°C |
| Input Bias Current | (Note 9) | 0.04 | 20<br>**30** | | 20 | **4** | | **2** | pA max |
| Input Offset Current | (Note 9) | 0.01 | 20<br>**30** | | 20 | **2** | | **1** | pA max |
| Input Resistance | | >1 | | | | | | | TerraΩ |
| Common Mode Rejection Ratio | $0V \le V_{CM} \le 12.0V$<br>$V^+ = 15V$ | 83 | 70<br>**68** | | 72 | **68** | 63 | **62** | dB min |
| Positive Power Supply Rejection Ratio | $5V \le V^+ \le 15V$<br>$V_O = 2.5V$ | 83 | 70<br>**68** | | 70 | **68** | 68 | **62** | dB min |
| Negative Power Supply Rejection Ratio | $0V \le V^- \le -10V$ | 94 | 84<br>**82** | | 84 | **83** | 74 | **73** | dB min |
| Input Common-Mode Voltage Range | $V^+ = 5V$ & 15V<br>For CMRR ≥ 50 dB | −0.4 | −0.1<br>**0** | | −0.1 | **0** | −0.1 | **0** | V max |
| | | $V^+ - 1.9$ | $V^+ - 2.3$<br>**$V^+ - 2.6$** | | $V^+ - 2.3$ | **$V^+ - 2.5$** | $V^+ - 2.3$ | **$V^+ - 2.4$** | V min |
| Large Signal Voltage Gain | $R_L = 2\ k\Omega$ (Note 6) | | | | | | | | |
| | Sourcing | 2000 | 400<br>**300** | | 400 | **440** | 200 | **300** | V/mV min |
| | Sinking | 500 | 180<br>**70** | | 180 | **120** | 90 | **80** | V/mV min |
| | $R_L = 600\Omega$ (Note 6) | | | | | | | | |
| | Sourcing | 1000 | 200<br>**150** | | 200 | **220** | 100 | **150** | V/mV min |
| | Sinking | 250 | 100<br>**35** | | 100 | **60** | 50 | **40** | V/mV min |

## DC Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | Typ | LMC660AM | | LMC660AI | | LMC660C | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Output Swing | $V^+ = 5V$<br>$R_L = 2\ k\Omega$ to $V^+/2$ | 4.87 | 4.82 | | 4.82 | **4.79** | 4.78 | **4.76** | V<br>min |
| | | | **4.77** | | | | | | |
| | | 0.10 | 0.15 | | 0.15 | **0.17** | 0.19 | **0.21** | V<br>max |
| | | | **0.19** | | | | | | |
| | $V^+ = 5V$<br>$R_L = 600\Omega$ to $V^+/2$ | 4.61 | 4.41 | | 4.41 | **4.31** | 4.27 | **4.21** | V<br>min |
| | | | **4.24** | | | | | | |
| | | 0.30 | 0.50 | | 0.50 | **0.56** | 0.63 | **0.69** | V<br>max |
| | | | **0.63** | | | | | | |
| | $V^+ = 15V$<br>$R_L = 2\ k\Omega$ to $V^+/2$ | 14.63 | 14.50 | | 14.50 | **14.44** | 14.37 | **14.32** | V<br>min |
| | | | **14.40** | | | | | | |
| | | 0.26 | 0.35 | | 0.35 | **0.40** | 0.44 | **0.48** | V<br>max |
| | | | **0.43** | | | | | | |
| | $V^+ = 15V$<br>$R_L = 600\Omega$ to $V^+/2$ | 13.90 | 13.35 | | 13.35 | **13.15** | 12.92 | **12.76** | V<br>min |
| | | | **13.02** | | | | | | |
| | | 0.79 | 1.16 | | 1.16 | **1.32** | 1.45 | **1.58** | V<br>max |
| | | | **1.42** | | | | | | |
| Output Current<br>$V^+ = 5V$ | Sourcing, $V_O = 0V$ | 22 | 16 | | 16 | **14** | 13 | **11** | mA<br>min |
| | | | **12** | | | | | | |
| | Sinking, $V_O = 5V$ | 21 | 16 | | 16 | **14** | 13 | **11** | mA<br>min |
| | | | **12** | | | | | | |
| Output Current<br>$V^+ = 15V$ | Sourcing, $V_O = 0V$ | 40 | 19 | | 28 | **25** | 23 | **21** | mA<br>min |
| | | | **19** | | | | | | |
| | Sinking, $V_O = 13V$ | 39 | 19 | | 28 | **24** | 23 | **20** | mA<br>min |
| | | | **19** | | | | | | |
| Supply Current | All Four Amplifiers | 1.5 | 2.2 | | 2.2 | **2.6** | 2.7 | **2.9** | mA<br>min |
| | | | **2.9** | | | | | | |

## AC Electrical Characteristics (Note 3)

| Parameter | Conditions | Typ | LMC660AM | | LMC660AI | | LMC660C | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Slew Rate | (Note 7) | 1.1 | 0.8 | | 0.8 | **0.6** | | **0.7** | V/$\mu$s |
| | | | **0.5** | | | | | | min |
| Gain-Bandwidth Product | | 1.4 | | | | | | | MHz min |
| Phase Margin | | 50 | | | | | | | Deg |
| Gain Margin | | 17 | | | | | | | dB |
| Amp-to-Amp Isolation | (Note 8) | 130 | | | | | | | dB |
| Input Referred Voltage Noise | F = 1 kHz | 22 | | | | | | | nV/$\sqrt{}$Hz |
| Input Referred Current Noise | F = 1 kHz | 0.0002 | | | | | | | pA/$\sqrt{}$Hz |
| Total Harmonic Distortion | F = 10 kHz, $A_V = -10$<br>$R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ | 0.01 | | | | | | | % |

**Note 1:** Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

**Note 2:** The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 75°C/W., the molded plastic SO (M) package is 105°C/W., and the cavity DIP (D) package is 92°C/W. All numbers apply for packages soldered directly into a PC board.

**Note 3:** Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1\ M\Omega$ unless otherwise specified.

**Note 4:** These limits are guaranteed and are used in calculating outgoing AQL.

**Note 5:** These limits are guaranteed, but are not used in calculating outgoing AQL.

**Note 6:** $V^+ = 15V$, $V_{CM} = 7.5V$ and $R_L$ connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

**Note 7:** $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

**Note 8:** Input referred. $V^+ = 15V$ and $R_L = 10\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

**Note 9:** The specifications in the Design Limit column reflect the true performance of the part, while those in the Tested Limit column are degraded to allow for the unavoidable inaccuracies involved in cost-effective high-speed automatic testing.

**National Semiconductor Corporation**

**PRELIMINARY**

# LMC668A/LMC668 Chopper Stabilized Operational Amplifier

## General Description

The LMC668 is a high performance versatile chopper-stabilized amplifier with low input offset voltage. This low offset is achieved through a nulling scheme that provides continuous error correction. A nulling amplifier alternately nulls itself and the main amplifier. Two external capacitors are used to store the correcting voltages on the amplifier nulling inputs. The LMC668 has exceptionally low offset drift over time and temperature. The nulling circuit also provides for very high open loop gain, CMRR, and PSRR at low frequencies.

The clock oscillator and all the other control circuitry are completely self contained. The 14-pin version has an Internal/External Clock select pin and an External Clock In pin for use in applications requiring synchronized or special chopping frequencies. The 8-pin version does not allow for an external clock or the output clamp. Both versions are pin compatible replacements for the ICL7650 series of parts.

## Features

- Low input offset voltage
- High gain, CMRR and PSRR
- Low offset voltage drift with time and temperature
- Low DC input bias current
- Low intermodulation effects

## Key Specifications

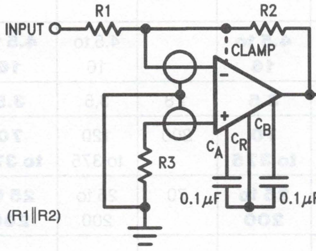
| | |
|---|---|
| ■ Input offset voltage | $< \pm 5\ \mu V$ |
| ■ DC input bias current | $<60$ pA |
| ■ Large signal voltage gain | $>10^6$ V/V |
| ■ Common mode rejection ratio | $>120$ dB |
| ■ Power supply rejection ratio | $>120$ dB |
| ■ Internal chopping frequency | Typ 200 Hz |

## Ordering Information

| Part | Temp Range | Package |
|---|---|---|
| LMC668ACJ | 0°C to 70°C | 14 pin CERDIP |
| LMC668CJ | 0°C to 70°C | 14 pin CERDIP |
| LMC668ACJ-8 | 0°C to 70°C | 8 pin CERDIP |
| LMC668CJ-8 | 0°C to 70°C | 8 pin CERDIP |
| LMC668ACN | 0°C to 70°C | 14 pin Plastic |
| LMC668CN | 0°C to 70°C | 14 pin Plastic |
| LMC668ACN-8 | 0°C to 70°C | 8 pin Plastic |
| LMC668CN-8 | 0°C to 70°C | 8 pin Plastic |

## Typical Applications

**Inverting Amplifier with Optional Clamp**



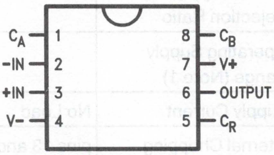
R3 = (R1||R2)

(R1||R2) ≥ 100 KΩ For Full Clamp Effect

TL/H/9128-1

## Connection Diagram

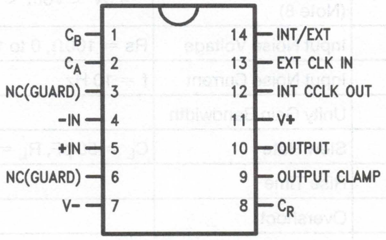
**LMC668-8**



TL/H/9128-2

**Top View**

**LMC668**



TL/H/9128-9

**Top View**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V^+$ to $V^-$) | 18V |
| Input Voltage | ($V^+$ + 0.3V) to ($V^-$ − 0.3V) |
| Voltage on Oscillator Control Pins | $V^+$ to $V^-$ |
| Except EXT CLOCK IN: | ($V^+$ + 0.3V) to ($V^+$ − 6.0V) |
| Duration of Output Short Circuit | Indefinite |
| Current into any pin | 10 mA |
| —while operating (Note 2) | 100 μA |

| | |
|---|---|
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| ESD Susceptibility (Note 4) | 1500V |
| Power Dissipation (Note 3) | |
| CERDIP J Package | 500 mW |
| Plastic N Package | 375 mW |
| Operating Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| LMC668ACJ/CJ | 0°C to 70°C |
| LMC668ACN/CN | 0°C to 70°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 125°C |

## Electrical Characteristics: Vsupply = ±5V unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all others limits $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LMC668A Typ (Note 5) | LMC668A Tested Limit (Note 6) | LMC668A Design Limit (Note 7) | LMC668 Typ (Note 5) | LMC668 Tested Limit (Note 6) | LMC668 Design Limit (Note 7) | Limit Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | 0V Common Mode | ±1 | ±5 | **±15** | ±1 | ±10 | **±20** | μV |
| $\Delta V_{OS}$/$\Delta T$ | Average Temperature Coefficient of Input Offset Voltage | CJ Suffix Parts<br>CN Suffix Parts | ±0.05<br>±0.05 | | | ±0.05<br>±0.05 | | | μV/°C<br>μV/°C |
| $I_{Bias}$ | Input Bias Current | 0V Common Mode | ±20 | ±60 | | ±20 | ±60 | | pA |
| $R_{IN}$ | Input Resistance | | $10^{12}$ | | | $10^{12}$ | | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 10 KΩ | $5x10^6$ | $1x10^6$ | **$0.5x10^6$** | $5x10^6$ | $1x10^6$ | **$0.5x10^6$** | V/V |
| $V_{OUT}$ | Output Voltage Swing | Clamp not Connected $R_L$ = 10 KΩ<br>$R_L$ = 100 KΩ | ±4.85<br>±4.95 | ±4.7 | **±4.7** | ±4.85<br>±4.95 | ±4.7 | **±4.7** | V<br>V |
| CMVR | Common Mode Voltage Range | | −5.2 to +2.0 | −5.0 to +1.6 | **−5.0 to +1.6** | −5.2 to +2.0 | −5.0 to +1.6 | **−5.0 to +1.6** | V<br>V |
| CMRR | Common Mode Rejection Ratio | CMVR = −5V to +1.6V | 125 | 120 | **107** | 125 | 110 | **107** | dB |
| PSRR | Power Supply Rejection Ratio | ±3V to ±8V | 130 | 120 | **108** | 130 | 120 | **108** | dB |
| $V^+$ to $V^-$ | Operating Supply Range (Note 1) | | | 4.5 to 16 | **4.5 to 16** | | 4.5 to 16 | **4.5 to 16** | V<br>V |
| $I_{SUPP}$ | Supply Current | No Load | 1.8 | 3.5 | **3.5** | 1.8 | 3.5 | **3.5** | mA |
| $f_{CLK}$ | Internal Chopping Frequency | pins 13 and 14 open (14 pin DIP) | 200 | 120 to 375 | **70 to 375** | 200 | 120 to 375 | **70 to 375** | Hz<br>Hz |
| | Clamp ON Current (Note 8) | $R_L$ = 100 KΩ | 70 | 25 to 200 | **25 to 200** | 70 | 25 to 200 | **25 to 200** | μA<br>μA |
| | Clamp Off Current (Note 8) | −4.0V < Vout < +4.0V | 1 | | | 1 | | | pA |
| $e_n$ | Input Noise Voltage | Rs = 100Ω, 0 to 10 Hz | 2 | | | 2 | | | μVp-p |
| $I_n$ | Input Noise Current | f = 10 Hz | 0.01 | | | 0.01 | | | pA/$\sqrt{HZ}$ |
| GBW | Unity Gain Bandwidth | | 1.0 | | | 1.0 | | | MHz |
| SR | Slew Rate | $C_L$ = 50 pF, $R_L$ = 10 KΩ | 2.5 | | | 2.5 | | | V/μs |
| $t_r$ | Rise Time | | 0.2 | | | 0.2 | | | μs |
| | Overshoot | | 20 | | | 20 | | | % |
| | Offset Voltage vs Time | | 100 | | | 100 | | | nV/mth |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

**Note 2:** To avoid possible destructive latchup, currents greater than 100 μA should not be forced into the input pins.

**Note 3:** The maximum allowable power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\Theta_{JA}$, and ambient temperature, $T_A$. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. $\Theta_{JA}$ is typically 120°C/W for the J package and 140°C/W for the N package.

**Note 4:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

**Note 5:** Specifications in the "Typical" column are at 25°C and represent the most likely parametric norm.

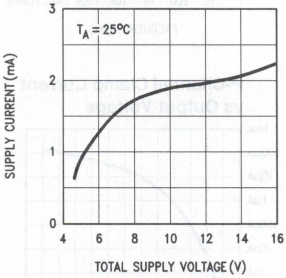
**Note 6:** Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 7:** Guaranteed and not 100% production tested. These limits are not used to calculate outgoing quality levels.

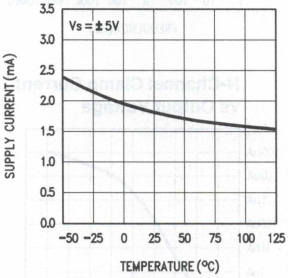
**Note 8:** See Output Clamp discussion in Application Hints.

## Typical Performance Characteristics

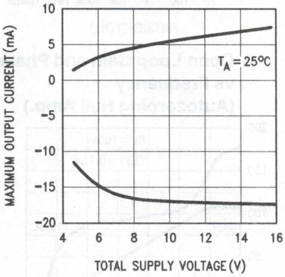
### Supply Current vs Supply Voltage



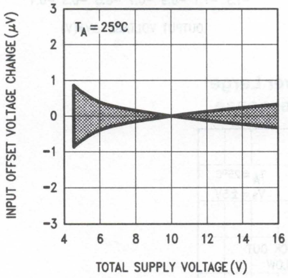
### Supply Current vs Ambient Temperature



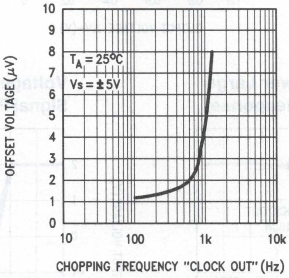
### Max Output Current vs Supply Voltage



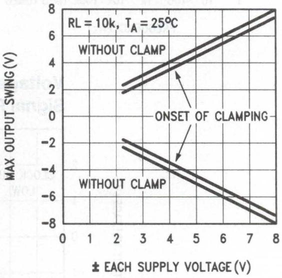
### Input Offset Voltage Change vs Supply Voltage



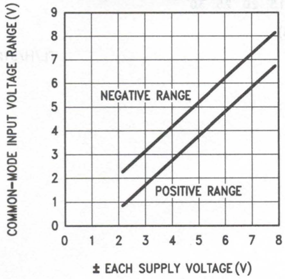
### Input Offset Voltage vs Chopping Frequency



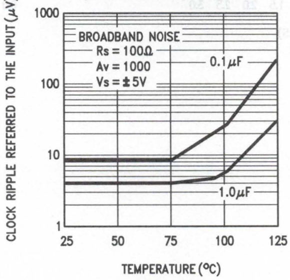
### Max Output Swing vs Supply Voltage



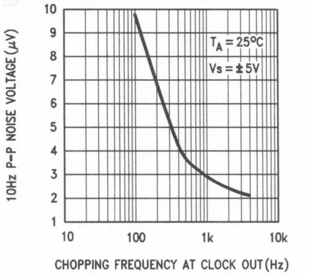
### Common-Mode Input Voltage Range vs Supply Voltage



### Clock Ripple Referred to the Input vs Temperature



### 10 Hz P-P Noise Voltage vs Chopping Frequency



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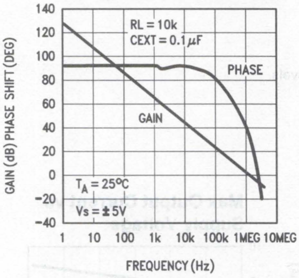
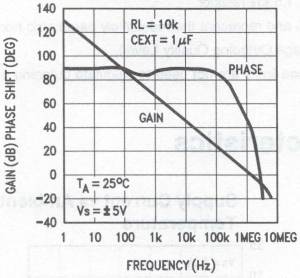
# Typical Performance Characteristics (Continued)

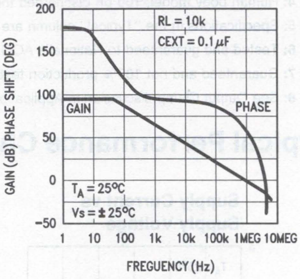
### Open Loop Gain and Phase Shift vs Frequency (Autozeroing Main Amp.)



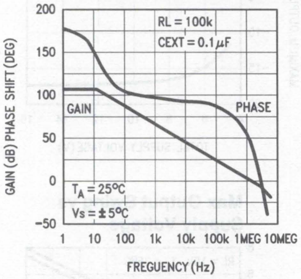
### Open Loop Gain and Phase Shift vs Frequency (Autozeroing Main Amp.)



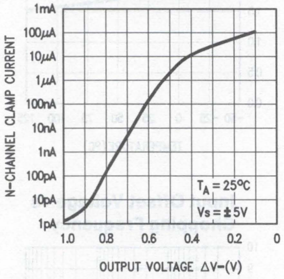
### Open Loop Gain and Phase Shift vs Frequency (Autozeroing Null Amp.)



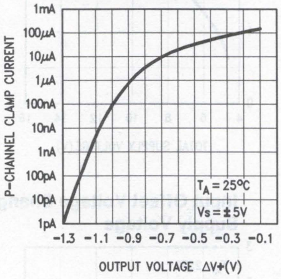
### Open Loop Gain and Phase Shift vs Frequency (Autozeroing Null Amp.)



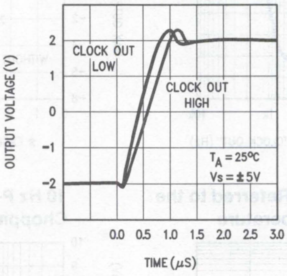
### N-Channel Clamp Current vs Output Voltage



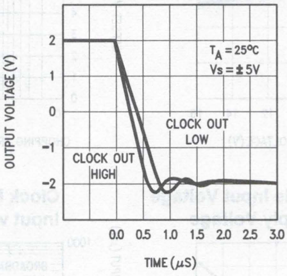
### P-Channel Clamp Current vs Output Voltage



### Voltage Follower Large Signal Pulse Response



### Voltage Follower Large Signal Pulse Response



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## Application Hints

### THEORY OF OPERATION

*Figure 1* shows a simplified block diagram of the LMC668's analog signal path. The circuit effectively consists of two amplifiers, some MOS switches, and a pair of external capacitors. The "main amplifier" is a conventional MOS operational amplifier and is connected to the external feedback components. This amplifier is always active. The "null amplifier" has its inverting input connected to the main amplifier's inverting input. The null amplifier's non-inverting input is switched between the main amplifier's two inputs. Each amplifier also has an additional input pin that can be use to adjust $V_{OS}$.

In operation, the null amplifier's inputs are first shorted together, and its output is connected to its $V_{OS}$ input. This creates a negative feedback loop that adjusts the input $V_{OS}$ to zero. When switches A' and B' are opened, the correction voltage at the $V_{OS}$ input is stored by capacitor $C_A$, holding the null amplifier offset voltage at zero. Switch B is then closed, shorting the main amplifier's non-inverting input to the null amplifier's non-inverting input. Since the main amplifier is enclosed in the external feedback loop, its two inputs should ideally be at the same voltage. Any voltage difference between the main amplifier's inputs will be amplified by the nulling amplifier and applied to the main amp's $V_{OS}$ adjust pin. The closed loop system reaches equilibrium when the main amplifier's input $V_{OS}$ equals zero. The correction voltage for the main amplifier is stored on $C_B$, and the entire process repeats at the chopping frequency (around 200 Hz).

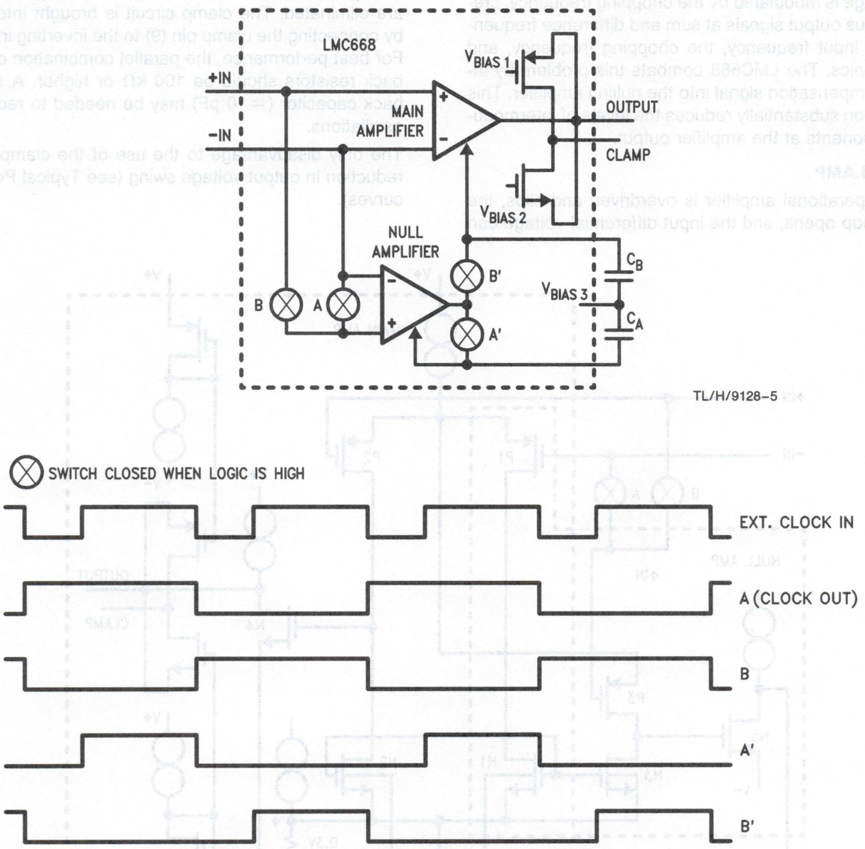

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**FIGURE 1. Block Diagram of LMC668 Analog Signal Path**

## Application Hints (Continued)

*Figure 2* shows a simplified schematic of the block diagram in *Figure 1*. Note that transistor P1 serves as the inverting input for both the main amplifier and the null amplifier. Note also that the "back gate" substrate connections on transistors N1 and N2 are the $V_{OS}$ adjust inputs. Increasing the back gate voltage on these transistors increases the channel conductivity, but to a lesser degree than would be caused by an equivalent voltage change at the "normal" gate.

### INTERMODULATION

An ideal operational amplifier has infinite gain at all frequencies, so that when feedback is applied, the voltage differential between the two inputs will be zero. A real amplifier has finite gain that decreases with increasing frequency, resulting in a small voltage across the inputs that increases with signal frequency. In a typical chopper-stabilized amplifier, the ac voltage is modulated by the chopping frequency, creating spurious output signals at sum and difference frequencies of the input frequency, the chopping frequency, and their harmonics. The LMC668 combats this problem by injecting a compensation signal into the nulling amplifier. This compensation substantially reduces the levels of intermodulation components at the amplifier output.

### OUTPUT CLAMP

When an operational amplifier is overdriven and clips, the feedback loop opens, and the input differential voltage can become quite large. This voltage is equivalent to a large input offset voltage, so the LMC668's offset correction circuitry attempts to compensate for it, and the external capacitors are eventually charged to rather high voltages before the correction circuit saturates. When the overdrive is removed the capacitors can't be immediately discharged so the circuit takes a long time to recover from the saturated condition.

The 14-pin version of the LMC668 includes a circuit whose purpose is to prevent excessive overdrive recovery time by introducing a current path from the amplifier output to the inverting input. This current path is inactive until the output voltage approaches the supply voltage. Just before the onset of clipping, the current path becomes active and clamps the output voltage before it saturates. Since the clamping action occurs within the feedback loop, the input differential voltage will remain near zero volts and long recovery times are eliminated. The clamp circuit is brought into operation by connecting the clamp pin (9) to the inverting input (pin 4). For best performance, the parallel combination of the feedback resistors should be 100 kΩ or higher. A small feedback capacitor (≈10 pF) may be needed to reduce clamp oscillations.

The only disadvantage to the use of the clamp is a slight reduction in output voltage swing (see Typical Performance curves).

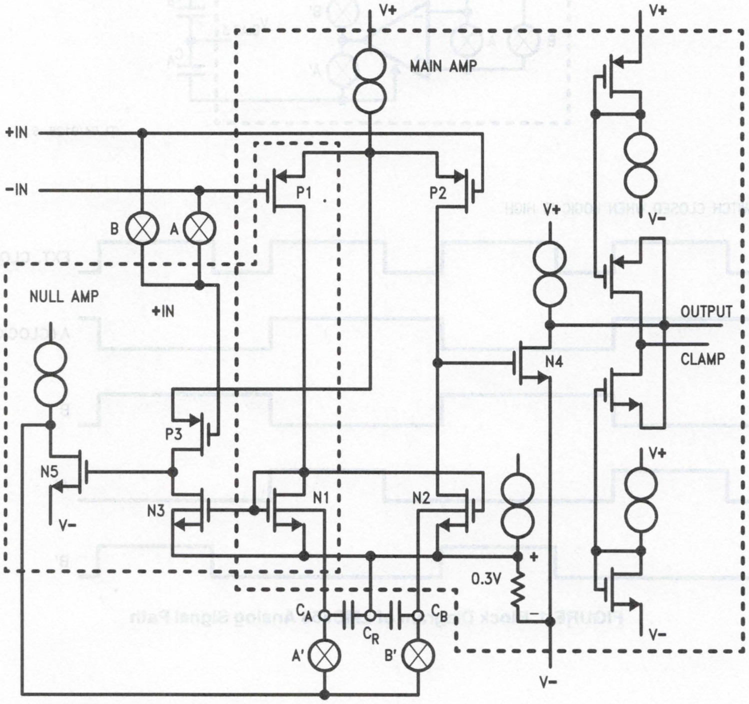

**FIGURE 2. Simplified Schematic of the LMC668 Analog Signal Path**

## Application Hints (Continued)

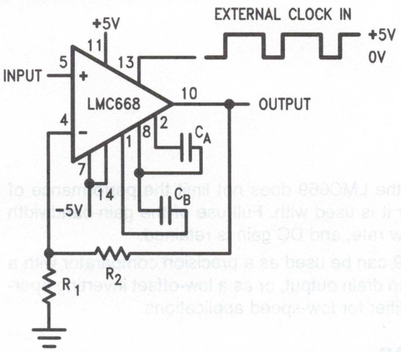

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**FIGURE 3. Using External Clock (14-pin LMC668 only). For operation with internal clock, leave pins 13 and 14 open.**

### THERMOELECTRIC EFFECTS

When dissimilar metals come into contact with one another, thermocouples are created that generate dc error voltages. To reduce the effects of thermocouples, temperatures throughout the sensitive parts of the system should be as similar as possible. Circuitry should be enclosed to limit air movement, junctions with high thermoelectric coefficients should be avoided, and power dissipation should be minimized as much as possible to avoid thermal gradients.

### CLOCK CONSIDERATIONS

The internal clock in the LMC668 is set to oscillate around 400 Hz. This signal is available at pin 12 of the 14-pin LMC668. The actual chopping rate is half of the clock frequency. The 14-pin version of the device provides the option of using a different clock frequency from an external source. To do this the INT/EXT pin must be tied to $V^-$ to disable the internal clock *(Figure 3)*. This pin has an internal pull-up, so it may be left open when the internal clock is used. At frequencies below 500 Hz, the external clock's duty cycle is not critical, but above this frequency, a 60% to 80% positive duty cycle will give better results since the null storage capacitors ($C_A$ and $C_B$) are charged only on the positive half of the clock waveform. A positive duty cycle ensures that the capacitors will be fully charged and any transients will have settled before they are disconnected from the charging circuitry. The maximum recommended clock frequency is approximately 1 kHz. Higher frequencies should be avoided because the offset voltage is degraded at fast chopping rates. The external clock signal should swing between ground and $V^+$ for supply voltages up to ±6V, and between $V^+$ and $V^+ -6V$ for higher supplies. Voltages outside of this range may cause damage to the IC.

### EXTERNAL CAPACITORS

$C_A$ and $C_B$ should be connected from the $C_A$ and $C_B$ pins to the $C_R$ pin. Where possible, the outside foil leads should be connected to $C_R$. If the internal 200 Hz clock is used, the capacitors should be 0.1 $\mu$F. The optimum capacitance varies inversely with chopping frequency. Good quality film capacitors (mylar, polypropylene, polystyrene, polycarbonate, etc.) will give best results. Capacitors with low dielectric absorption (polypropylene and polystyrene) yield the fastest initial settling and turn-on performance. Ceramic capacitors may be adequate in some applications, but these may require several seconds to settle to very low offset values.

### LOAD IMPEDANCE

The LMC668 output stage has a relatively high (18 kΩ) output impedance, so the load impedance will have a strong influence on amplifier performance. This is illustrated in the Typical Performance Curves showing open-loop gain for two different load resistors. It is recommended that the load impedance be kept above 10 kΩ to avoid drastic loss of gain, especially at high frequencies. This load resistance will result in a smooth first-order rolloff in the open-loop gain from 0.1 Hz to 2 MHz, with phase errors under 10° in the transition region where the main amplifier takes over from the null amplifier.

### LEAKAGE CURRENTS AND INPUT GUARDING

When the low input bias currents of the LMC668 are essential to an application, it is important to take special steps to reduce external sources of leakage currents. Circuit boards must be thoroughly cleaned with appropriate solvents and blown dry with compressed air, and the cleaned traces should be coated with epoxy or silicone rubber to prevent contamination.

Leakage currents due to circuit board traces at supply potentials near the input pins can be excessive for some applications, and these can be minimized by using a guard ring around the input pins. This ring should be tied to a voltage that is near the voltage on the input pins. It will absorb most of the leakage currents from high potential pins and traces.

### OUTPUT GLITCHES

The CMOS switches in the LMC668, like all analog switches, produce transients when they are turned on or off. These transients are minimized by careful balancing of the internal switches, but they will still couple to the amplifier output. The transients can be minimized by keeping source impedances low. Input referred glitches on the order of 100 $\mu$V are typical with a source impedance of 10 kΩ and $Av = 1000$. Glitch amplitude increases with higher source resistance and decreases when the clamp circuit is used. At low gains ($Av < 10$), output glitch amplitude is not as strongly dependent on gain. Typical output glitch amplitudes for $R_1 = R_2 = 100$ kΩ *(Figure 3)*, are 100 mV to 150 mVp-p.

**National Semiconductor Corporation**

**PRELIMINARY**

# LMC669 Auto-Zero

## General Description

The LMC669 uses sampled-data techniques to reduce the input offset voltage ($V_{OS}$) of an amplifier or system to approximately 5 $\mu$V. A four-stage comparator samples the summing node of an inverting-amplifier and generates a correction voltage that is applied to the amplifier's non-inverting input. The offset correction is independent of time, temperature, and supply voltage, and requires no initial or periodic user offset adjustments.

The user may also adjust clock frequency, sample rate, and the correction voltage's step size and magnitude.

The Auto-Zero operates on supply voltages of ±8V to ±20V with a quiescent current of 3 mA.

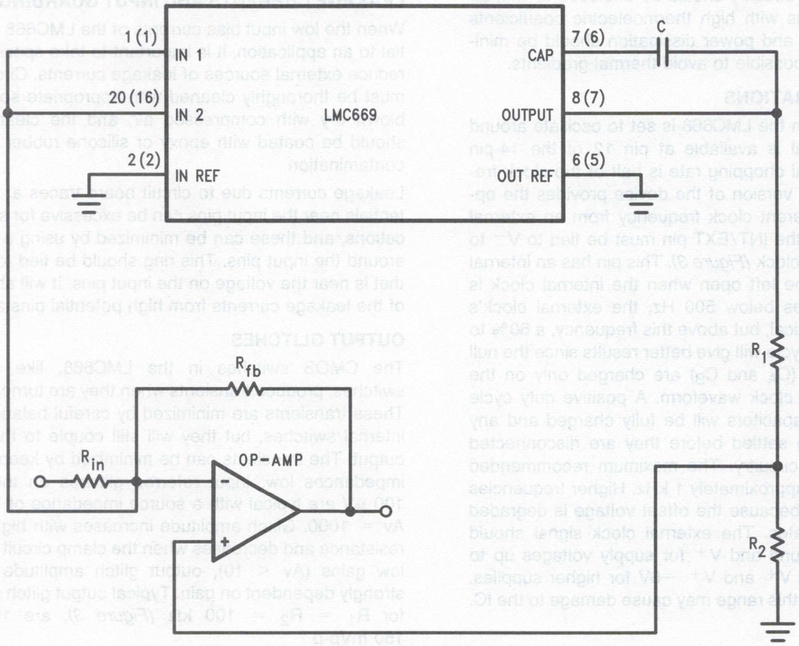
The use of the LMC669 does not limit the performance of the amplifier it is used with. Full use of the gain-bandwidth product, slew rate, and DC gain is retained.

The LMC669 can be used as a precision comparator with a latched, open drain output, or as a low-offset inverting operational amplifier for low-speed applications.

## Features

- 5 microvolts typical offset voltage
- Temperature independent offset correction
- Internal or external clocking
- Automatic and continuous offset voltage correction
- High voltage CMOS—up to ±20V supplies

## Typical Application



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**Numbers in ( ) are for 16-pin packages**

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Positive Supply Voltage ($V^+$) | $+22V$ |
| Negative Supply Voltage ($V^-$) | $-22V$ |
| Voltage of Logic Pins<br>T1, T2, $\overline{\text{RESET}}$, CLK | $-0.2V$ to $(V^+ + 0.2V)$ |
| Voltage at Inputs | $-0.2V$ to $(V^+ + 0.2V)$ |
| Input Current (Note 3)<br>INREF, IN1 and IN2 | 20 mA |
| Power Dissipation (Note 4) | 500 mW |
| Storage Temperature | $-65°C$ to $+150°C$ |
| Lead Temp. (soldering, 10 seconds) | 300°C |

## Operating Ranges (Notes 1 & 2)

| | |
|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| LMC669D | $-40°C \le T_A \le +85°C$ |
| Positive Supply Voltage | $+8V$ to $+20V$ |
| Negative Supply Voltage | $-8V$ to $-20V$ |
| INREF, IN1 and IN2 Voltage (Note 5) | $-200$ mV to $+2V$ |

ESD rating to be determined.

## Electrical Characteristics

The following specifications apply for $V^+ = +15V$, and $V^- = 15V$ unless otherwise specified. **Boldface limits apply for $T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J = 25°C$.

| Symbol | Parameter | | Conditions | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Maximum Input Offset Voltage (Note 9) | LMC669BIN, BIM | Signal applied to both IN1 & IN2, $T_{CLK}$ = 50 µs, $V_{INREF}$ = 0V, 0.5V | ±5 | **±25** | | µV |
| | | LMC669BCN, BCM | | | ±25 | | |
| | | LMC669CIN, CIM | | ±10 | **±50** | | |
| | | LMC669CCN, CCM | | | ±50 | | |
| | | LMC669CD | | ±5 | **±25** | | |
| $V_{OS}$ | Maximum Input Offset Voltage (Note 9) | LMC669BIN, BIM | Signal applied only to IN1 or IN2, $T_{CLK}$ = 50 µs, $V_{INREF}$ = 0V | ±10 | **±50** | | µV |
| | | LMC669BCN, BCM | | | ±50 | | |
| | | LMC669CIN, CIM | | ±20 | **±100** | | |
| | | LMC669CCN, CCM | | | ±100 | | |
| | | LMC669CD | | ±10 | **±50** | | |
| $I_b$ | Maximum Input Bias Current | IN2 | Clock Off | 1 | 100 | | pA |
| | | | | **400** | | | pA |
| | | IN1 or IN1 & IN2 | | 5 | 100 | | pA |
| | | | | **40** | | **75** | nA |
| $\frac{\Delta V_{OS}}{\Delta T}$ | Average Input Offset Drift | | | 0.1 | | | µV/°C |
| $V_{IN1}$, $V_{IN2}$ | IN1 & IN2 Input Voltage Range (Note 5) | min | | $-200$ | 0 | | mV |
| | | max | | $+2.0$ | $+0.5$ | | V |
| $V_{IN\,REF}$ | IN REF Input Voltage Range (Note 5) | min | | $-200$ | 0 | | mV |
| | | max | | $+2.0$ | $+0.5$ | | V |
| $V_{OUT\,REF}$ | OUT REF Input Voltage Range | min | | $-100$ | | | mV |
| | | max | | $+100$ | | | mV |
| PSRR | Power Supply Rejection Ratio | | | 120 | | | dB |
| $V_{OUT}$ | Integrator Output Voltage Range | | | ±14 | ±12 | **±11** | V |
| $V_{CO}$ | Comparator Open-Drain Output Voltage Range | Low (max) | Sink Current = 1.0 mA | 0.25 | **0.4** | | V |
| | | High (min) | | 25 | 20 | **19** | |
| $I_S^+$ | Maximum Positive Supply Current | | $\overline{\text{RESET}}$ Low, $T_{CLK}$ = 50 µs | 3.2 | 6.0 | | mA |
| | | | | | **10.0** | | |

## Electrical Characteristics

The following specifications apply for $V^+ = +15V$, and $V^- = -15V$ unless otherwise specified. **Boldface limits apply for $T_{MIN}$ to $T_{MAX}$;** all other limits $T_A = T_J = 25°C$. (Continued)

| Symbol | Parameter | | Conditions | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | Units |
|---|---|---|---|---|---|---|---|
| $I_S-$ | Maximum Negative Supply Current | | $\overline{\text{RESET}}$ Low, $T_{CLK} = 50\ \mu s$ | 2.0 | 5.0 | | mA |
| | | | | | **7.0** | | |
| $f_S$ | Maximum Sample Rate | | $\overline{\text{RESET}}$ Low, Internal Clock | 100 | 66.6 | **56** | kHz |
| $f_{CLK}$ | Clock Frequency Range | | min | 100 | | **100** | Hz |
| | | | max | 100 | | **100** | kHz |
| $T_R$ | Minimum $\overline{\text{RESET}}$ Pulse Width | | | 80 | 150 | **175** | ns |
| $V_{TH}$ | Digital Input Threshold Voltage | T1, T2, $\overline{\text{RESET}}$ | High (min) | 2.9 | 3.5 | | V |
| | | | Low (max) | 2.9 | 1.5 | | V |
| | | CLK | High (min) | 3.5 | 4.0 | | V |
| | | | Low (max) | 1.5 | 1.0 | | V |
| $I_{D\ IN}$ | T1, T2, $\overline{\text{RESET}}$, & CLK Maximum Digital Input Current | | High | 1.0 | | | pA |
| | | | | | **1.0** | | $\mu A$ |
| | | | Low | 1.0 | | | pA |
| | | | | | **1.0** | | $\mu A$ |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are with respect to AGND.

**Note 3:** This input current will exist only when an input is driven to a voltage greater than $(V^+ + 0.2V)$ or less than $-0.2V$. It is due to internal diode clamps at the inputs turning on. If the current is limited to 20 mA, the overdrive will not be harmful to the LMC669.

**Note 4:** The typical junction-to-ambient thermal resistance ($\theta_{JA}$) of the 16 pin J package is 80°C/W.

**Note 5:** If input currents are limited, input voltages may be driven beyond these limits and the device will still be functional. The comparator output will be correct as long as the voltage on either the INREF pin or the two input IN1 & IN2 pins is between −200 mV and +2V.

**Note 6:** Typicals are at 25°C and represent most likely parametric norm.

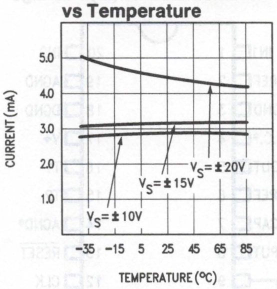
**Note 7:** Guaranteed and 100% tested.

**Note 8:** Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

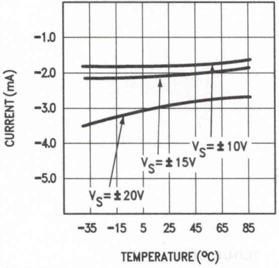
**Note 9:** The LMC669CD exhibits a warm-up drift of approximately 3 $\mu$V to 5 $\mu$V in the negative direction. There are two factors that work together to cause this. Firstly, as the die becomes warm, a temperature gradient forms between pin 2 and pins 1 and 16. Secondly, a thermocouple is created between the metal of the leadframe and the metal of the wire (usually copper) used to connect the IC to a circuit. It takes about 6 minutes for the drift to stabilize. The N and M packages do not exhibit this drift because their leadframes are 90% copper.

## Typical Performance Characteristics

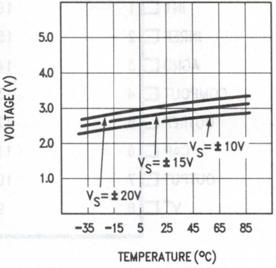
**Positive Supply Current vs Temperature**



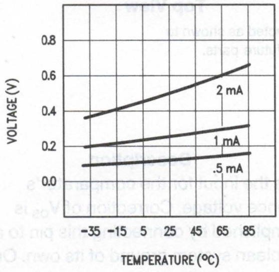
**Negative Supply Current vs Temperature**



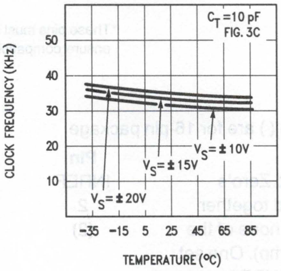
**T1, T2 & $\overline{RESET}$ thresholds vs Temperature**



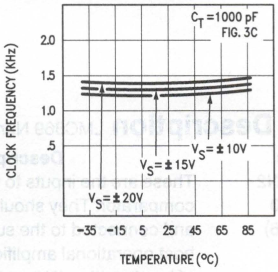
**$V_{COMP\ OUT}$ vs Temperature**



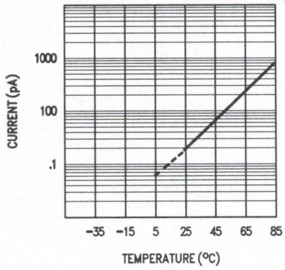
**Clock Frequency vs Temperature**



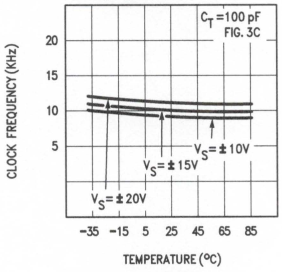
**Clock Frequency vs Temperature**



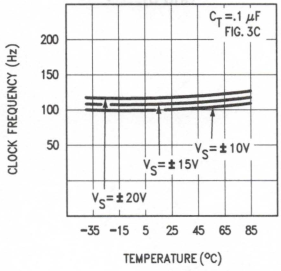
**Integrator Summing Node Leakage Current**



**Clock Frequency vs Temperature**

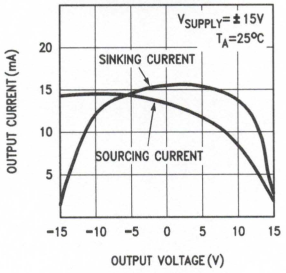


**Clock Frequency vs Temperature**



TL/H/8561–2

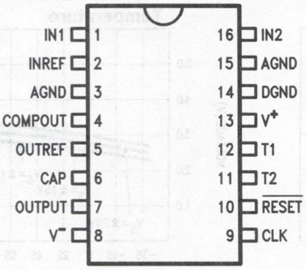
**Output Current Limit vs Output Voltage**



TL/H/8561–3

## Connection Diagram

**16-Pin Dual-In-Line Package**

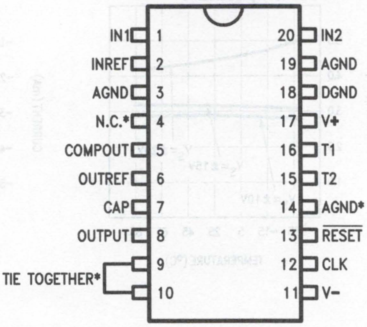

IN1 1
INREF 2
AGND 3
COMPOUT 4
OUTREF 5
CAP 6
OUTPUT 7
V⁻ 8
16 IN2
15 AGND
14 DGND
13 V⁺
12 T1
11 T2
10 RESET
9 CLK

TL/H/8561-4

**Top View**

**Order Number LMC669D**
**See NS Package Number D16C**

**20-Pin Dual-In-Line (N) Package**
**20-Pin Small-Outline (M) Package**


IN1 1
INREF 2
AGND 3
N.C.* 4
COMPOUT 5
OUTREF 6
CAP 7
OUTPUT 8
9
TIE TOGETHER*
10
20 IN2
19 AGND
18 DGND
17 V+
16 T1
15 T2
14 AGND*
13 RESET
12 CLK
11 V−

TL/H/8561-17

**Top View**

*These pins must be connected as shown to ensure compatibility with future parts.

## Pin Description

LMC669 Numbers in ( ) are for 16-pin package

| Pin | Description |
|---|---|
| IN1, IN2<br>1, 20<br>(1, 16) | These are the inputs to the Auto Zero's comparator. They should be tied together and connected to the summing node of the host operational amplifier (op amp). One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V+ (also refer to notes 3 and 5). |
| INREF<br>2<br>(2) | This is the input for the comparator's reference voltage. Correction of $V_{OS}$ is accomplished by connecting this pin to a good clean system ground of its own. One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V+ (also refer to notes 3 and 5). |

## Pin Description 16-pin LMC669 (Continued)

| Pin | Description |
|---|---|
| AGND<br>3,19<br>(3,15) | These act to shield the IN1, IN2, and INREF connections from stray capacitance and leakage which could degrade the part's performance. They should be connected to a high quality ground. |
| DGND<br>18<br>(14) | Provides a separate ground for the internal digital circuitry to prevent noise from corrupting the comparator inputs. It should have its own ground connection. |
| COMPOUT<br>5<br>(4) | This is the latched output from the internal comparator. It is an open drain which can be left unconnected if not needed. Its response time is equal to the sample rate's period. The rise time, from 10% to 90%, is nominally 500 ns with a 10 kΩ pull-up resistor. The output is typically capable of swinging from +0.25 (at 1 mA) to +25 volts. |
| OUTREF<br>6<br>(5) | Output reference; for proper integrator operation this input should be connected to a good system ground, such as the ground to which INREF is connected. |
| OUTPUT<br>8<br>(7) | This is the LMC669's integrator output. It can swing from −12 to +12 volts in 0.2 volt steps with a ≥10 KΩ load and no external integrating capacitor. |
| CAP<br>7<br>(6) | When a capacitor is used to decrease the correction voltage's step size, it is connected between CAP and OUTPUT. It parallels an internal 10 pF capacitor. |
| CLK<br>12<br>(9) | External clock input/internal adjust. The frequency of the internal clock (nominally 100 kHz) may be reduced with an external capacitor or an external clock connected to the CLK input. The logic thresholds for this input are 4 volts for a logic high and 1 volt for logic low. The internal clock can be stopped by applying a logic high, through a diode, to the CLK input. When a logic low is applied to the diode, the internal clock runs freely. (See Figure 3) |
| RESET<br>13<br>(10) | Comparator reset. At power-up, or when $\overline{\text{RESET}}$ is pulled low during normal operation, the Auto Zero will run at its fastest sample rate. This allows for the quickest $V_{OS}$ nulling. |
| 4 | Leave this pin unconnected. |
| 9, 10 | Connect these pins together. |
| 14 | Connect to analog ground. |
| T1, T2<br>16, 15<br>(12, 11) | These pins select one of five clock divider ratios. The ratio, hence the sample rate can be changed by applying V+ or ground to T1 and T2. The ratio chosen by these inputs is valid after the comparator's output changes state; i.e., a zero-crossing between the offset and correction voltage has taken place. These inputs can also be changed at any time to modify the LMC669's sample rate. Use the table below to determine the reduction in the clock's frequency for each combination of T1 and T2. |
| V+, V−<br>17, 11<br>(13, 8) | Positive and negative power supply inputs. Typical supply voltages are ±15 volts, but operation will take place from ±8 to ±20 volts. Power supply current is typically 3 mA. Bypass capacitors (0.01 ~ 0.1 μF) should be connected to the power supply pins. |

| T1 | T2 | $\overline{\text{RESET}}$ | ÷ |
|---|---|---|---|
| X | X | 0 | 1 |
| 1 | 1 | 1 | 4 |
| 1 | 0 | 1 | 16 |
| 0 | 1 | 1 | 128 |
| 0 | 0 | 1 | 1024 |

## Application Hints

### 1.0 INTRODUCTION

In its standard application shown in *Figure 1*, the LMC669 continuously samples the summing node of an inverting amplifier and generates a correction voltage for the amplifier's non-inverting input, nulling the amplifier's input offset voltage ($V_{OS}$) to 5 μV. The offset correction is independent of time, temperature, and supply voltage. The LMC669 eliminates the need for initial or periodic offset adjustments, compensates for $V_{OS}$ drift due to temperature changes, allows the use of greater DC gain, and increases immunity to changes in power supply voltages.

At the input of the LMC669 is a sampled-data differential comparator with very low offset voltage. When the comparator samples the summing node voltage and determines that it is not at ground, the LMC669's output generates a small voltage step in the opposite direction of the error. The size of the step and the sample rate are user-selectable. The correction voltage continues to step up or down until the summing node is within the $V_{OS}$ of the LMC669—typically 5 μV. At this point the Auto Zero continues to monitor the summing node and perform any needed corrections. An internal divider generates five different sampling rates for any given clock frequency.

The only external parts needed for $V_{OS}$ correction of most amplifiers are two resistors and one capacitor. Since the capacitor is in the feedback loop of an integrator, it should be a low leakage type (polycarbonate, polypropylene, polystyrene, mylar, etc.). The tolerance of the resistors and capacitor is not critical (10% components are satisfactory).

## Application Hints (Continued)

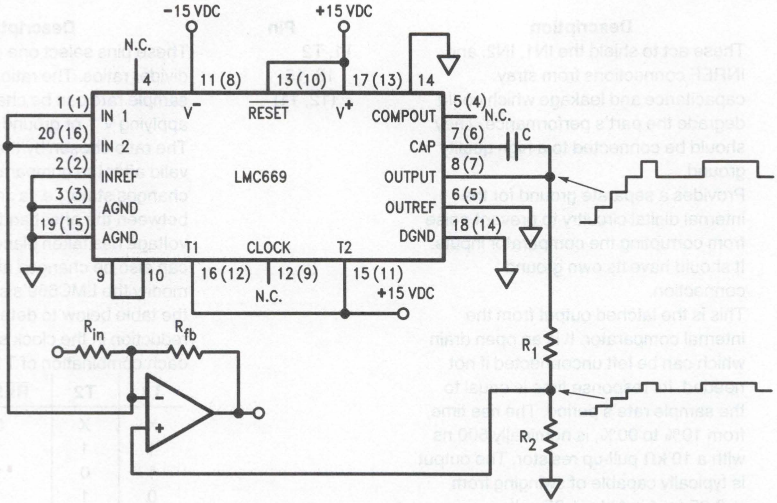


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**FIGURE 1. Typical Application**

### 1.1 CIRCUIT OPERATION

At the heart of the LMC669 is a four-stage precision sampled-data comparator, shown in *Figure 2.* The circuit operates by successively zeroing the offset of each stage, resulting in a very high gain amplifier with extremely low input offset voltage.

After a comparator decision is made, the latch is enabled and holds the comparator's output state. At the same time this state appears at COMPOUT. The latch also generates a ±1V signal that charges capacitor $C_1$ to ± 1V. $C_1$'s charge is then transferred to the integrator's feedback capacitor $C_2$. Since $C_2$ is five times larger than $C_1$, a 200 mV step will appear at the integrator's output. Further reduction of the step size is possible with an external capacitor connected in parallel with $C_2$ (between OUTPUT and CAP). The integrator output is then attenuated by a resistive divider network before being applied to the external op amp's non-inverting input, completing the offset correction loop.

### 1.2 CLOCKS

In order to control the events that take place in the LMC669, an internal Schmitt trigger oscillator generates a 100 kHz clock. This oscillator's frequency can be lowered by connecting a capacitor between the CLK input and ground as in *Figure 3c.* It can also be overridden by applying an external clock source (≤ 100 kHz) to the CLK input (*Figure 3a*). Further, the clock can be halted with a diode connected as shown in *Figure 3(b).*

The clock signal drives the input of the divider (See *Figure 2*). Depending on the logic levels at inputs T1, T2, and $\overline{\text{RESET}}$, the clock can be divided by five different ratios (1, 4, 16, 128, and 1024). The output of the divider triggers the sequencer which controls the auto-zero function.

When the LMC669 is powered-up or reset the internal divider automatically divides by one. This allows the Auto-Zero to operate at maximum sampling rate so that large initial offsets can be rapidly corrected. When the comparator toggles for the first time, this indicates that input null has been achieved and that maximum sample rate is no longer required. The latch then switches the divider from ÷ 1 to the ratio programmed via T1 and T2. By employing this "two speed" approach the device can move quickly to handle turn-on transients and then shift to the optimum "gear" for long term offset correction. It is also possible to return to the maximum sample rate via the $\overline{\text{RESET}}$ input so that non-power-up transients can be dealt with as well.

### 1.3 INPUT RANGE

The IN1, IN2, and INREF inputs can accept signal levels between 0 and +2 V. However, as long as both IN1 and IN2, or INREF, is kept between 0 and 2V the other input (or inputs) can be taken to V+ and, if input current limiting (≤20 mA) is provided, to V−. In most auto-zero applications IN1 and IN2 will be able to go to these extended limits since INREF will normally be grounded.

## Application Hints (Continued)

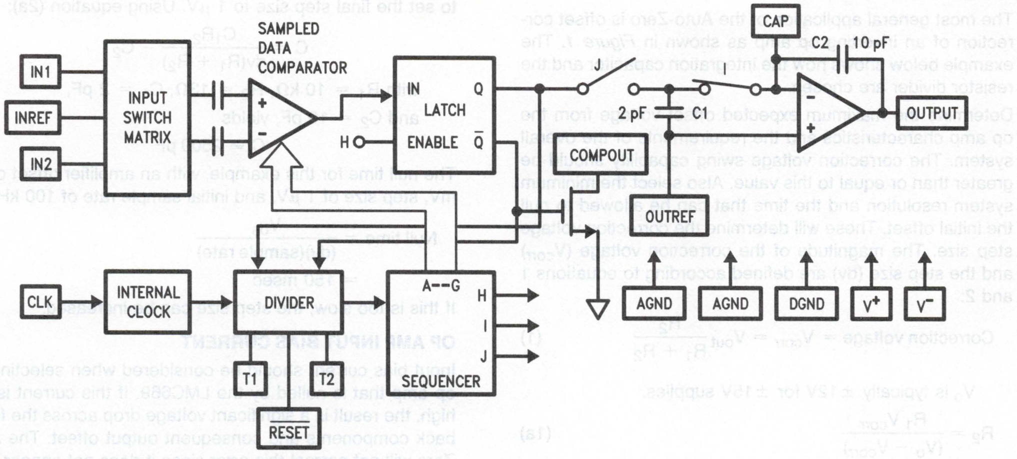

IN1
INREF
IN2
INPUT SWITCH MATRIX
SAMPLED DATA COMPARATOR
+
−
IN
Q
LATCH
H
ENABLE
$\overline{Q}$
CAP
C2
10 pF
2 pF
C1
COMPOUT
OUTPUT
OUTREF
AGND
AGND
DGND
$V^+$
$V^-$
CLK
INTERNAL CLOCK
DIVIDER
A--G
H
I
J
SEQUENCER
T1
T2
RESET
TL/H/8561-6

**FIGURE 2. Block Diagram**

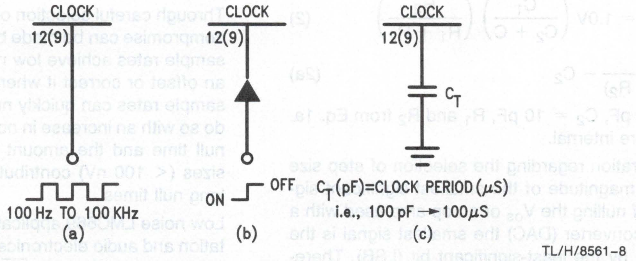

CLOCK
12(9)
100 Hz TO 100 KHz
(a)
CLOCK
12(9)
OFF
ON
(b)
CLOCK
12(9)
$C_T$
$C_T$(pF)=CLOCK PERIOD ($\mu$S)
i.e., 100 pF → 100$\mu$S
(c)
TL/H/8561-8

**FIGURE 3. Clock Input. External clock (a), controlling internal clock (b), reducing internal clock frequency (c).**

## Application Hints (Continued)

### 2.0 APPLICATION CIRCUITS

The most general application of the Auto-Zero is offset correction of an inverting op amp as shown in *Figure 1*. The example below shows how the integration capacitor and the resistor divider are chosen.

Determine the maximum expected offset voltage from the op amp characteristics and the requirements of the overall system. The correction voltage swing capability should be greater than or equal to this value. Also select the minimum system resolution and the time that can be allowed to null the initial offset. These will determine the correction voltage step size. The magnitude of the correction voltage ($V_{corr}$) and the step size (dv) are defined according to equations 1 and 2:

$$\text{Correction voltage} = V_{corr} = V_{out}\frac{R_2}{R_1 + R_2} \qquad (1)$$

$V_o$ is typically ±12V for ±15V supplies.

$$R_2 = \frac{R_1\,V_{corr}}{(V_o - V_{corr})} \qquad (1a)$$

$$= \frac{10\text{K}\,V_{corr}}{(12 - V_{corr})}$$

for $R_1 = 10\ \text{k}\Omega$ (For proper operation $R_1 + R_2$ should be greater than $10\ \text{k}\Omega$.)

$$\text{step size} = dv = 1.0\text{V}\left(\frac{C_1}{C_2 + C}\right)\left(\frac{R_2}{R_1 + R_2}\right) \qquad (2)$$

$$C = \frac{C_1R_2}{dv\,(R_1 + R_2)} - C_2 \qquad (2a)$$

with $C_1 = 2$ pF, $C_2 = 10$ pF, $R_1$ and $R_2$ from Eq. 1a. $C_1$ and $C_2$ are internal.

A further consideration regarding the selection of step size is resolution: the magnitude of the smallest significant signal. In the case of nulling the $V_{os}$ of an op amp used with a digital-to-analog converter (DAC) the smallest signal is the voltage produced by the least-significant bit (LSB). Therefore, the correction voltage's step size would need to be much smaller than the magnitude of the DAC's LSB in order to retain the DAC's desired resolution.

Finally, for proper operation, the sampling period should be longer than the amplifier's settling time. 10 μs or more should be adequate for most contemporary amplifiers.

### DESIGN EXAMPLE

As an example, assume that the offset of the op amp in *Figure 1* is expected to be no more than 15 mV and the system can tolerate a 1 μV square wave at a rate equal to the internal clock. Begin by using $R_1$ and $R_2$ to set the maximum correction voltage to 15 mV. The LMC669's output can swing to ±12 volts with a 10 KΩ load and a ±15 volt power supply. $R_1$ and $R_2$ should be chosen to reduce this to 15 mV:

$$R_2 = \frac{R_1\,V_{corr}}{V_o - V_{corr}}$$

$$= \frac{(10\text{K})\,(0.015)}{(12 - 0.015)}$$

$$= 12.5\Omega \approx 13\Omega$$

for ±15V supplies and $R_1 = 10$K.

Now choose C, the integrator's external feedback capacitor, to set the final step size to 1 μV. Using equation (2a):

$$C = \frac{C_1R_2}{dv(R_1 + R_2)} - C_2$$

with $R_1 = 10\ \text{k}\Omega$, $R_2 = 13\Omega$, $C_1 = 2$ pF, and $C_2 = 10$ pF, yields

$$C \cong 2500\ \text{pF}$$

The null time for this example, with an amplifier offset of 15 mV, step size of 1 μV, and initial sample rate of 100 kHz, is

$$\text{Null time} = \frac{V_{os}}{(dv)(\text{sample rate})} \qquad (3)$$

$$= 150\ \text{msec}$$

If this is too slow, the step size can be increased.

### OP AMP INPUT BIAS CURRENT

Input bias current should be considered when selecting an op amp that is nulled by the LMC669. If this current is too high, the result is a significant voltage drop across the feedback components and consequent output offset. The Auto Zero will not correct this error since it does not appear as a voltage at the summing node. Therefore, use low resistance feedback networks, or op amps with low input bias current such as the LF156, LF400, and LF411.

### NOISE

Through careful selection of the sample rate and step size a compromise can be made between noise and null time. Low sample rates achieve low noise but take a long time to null an offset or correct it when a sudden change occurs. High sample rates can quickly null or correct changes in $V_{os}$ but do so with an increase in noise. Step size directly affects the null time and the amount of noise introduced: small step sizes (< 100 nV) contribute almost no noise, but result in long null times.

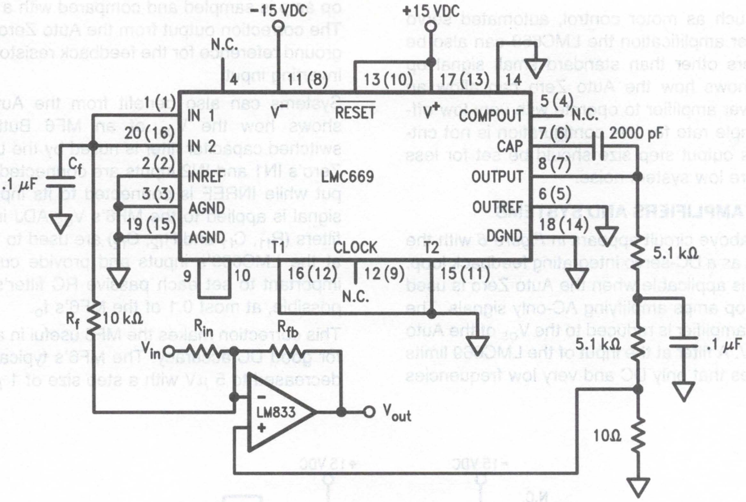
Low noise LMC669 applications are beneficial to instrumentation and audio electronics. An LM833 low noise operational amplifier ($4.5\ \text{nV}/\sqrt{\text{Hz}}$) with the LMC669 is shown in *Figure 4*. In this circuit the Auto Zero adds only $1\ \text{nV}/\sqrt{\text{Hz}}$ referred to the amplifier's input. To achieve this the step size is set to 100 nV. The sample rate, with the internal clock free-running, is set to 98 Hz (clock frequency ÷ 1024), and input and output filters are added to the LMC669. The input filter prevents switching transients from reaching the amplifier input and the output filter attenuates AC components of the steps at the Auto Zero's output. The filter at the op amp's input also introduces a pole at

$$F_p = \frac{1}{2\pi(R_{in} + R_f)\,C_f}$$

and a zero at

$$F_z = \frac{1}{2\pi R_f C_f}$$

The maximum $V_{os}$ that can be corrected by the circuit in *Figure 4* is 12 mV. More offset correction can be obtained while retaining good noise performance by increasing the size of $R_2$ and C the same percentage. Increasing C compensates for the reduced attenuation caused by increasing $R_2$. This allows the step size to remain the same but increases the amount of correction voltage applied to the op amp.



-15 VDC
+15 VDC
N.C.
4
11 (8)
13 (10)
17 (13)
14
1 (1)
IN 1
V⁻
RESET
V⁺
COMPOUT
5 (4)
N.C.
20 (16)
IN 2
CAP
7 (6)
2000 pF
C_f
2 (2)
INREF
LMC669
8 (7)
OUTPUT
.1 µF
3 (3)
AGND
6 (5)
OUTREF
19 (15)
AGND
18 (14)
DGND
T1
CLOCK
T2
5.1 kΩ
9
10
16 (12)
12 (9)
15 (11)
N.C.
R_f
10 kΩ
R_in
R_fb
V_in
5.1 kΩ
.1 µF
LM833
V_out
10Ω

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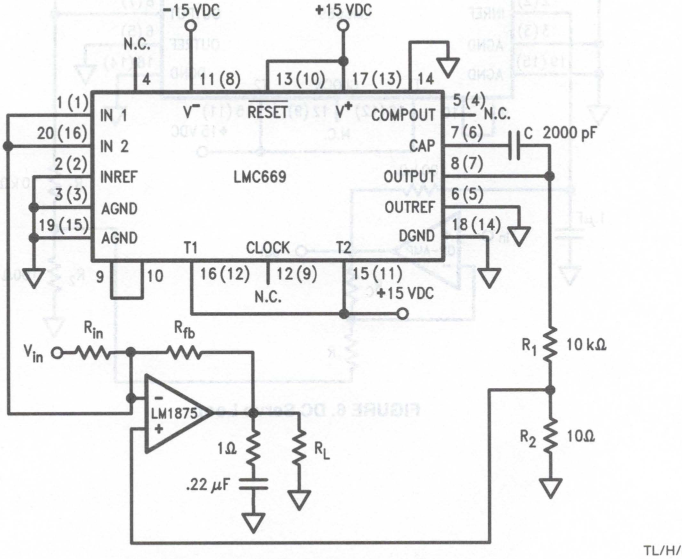
**FIGURE 4. Low Noise Application**



-15 VDC
+15 VDC
N.C.
4
11 (8)
13 (10)
17 (13)
14
1 (1)
IN 1
V⁻
RESET
V⁺
COMPOUT
5 (4)
N.C.
20 (16)
IN 2
CAP
7 (6)
C 2000 pF
2 (2)
INREF
LMC669
8 (7)
OUTPUT
3 (3)
AGND
6 (5)
OUTREF
19 (15)
AGND
18 (14)
DGND
T1
CLOCK
T2
9
10
16 (12)
12 (9)
15 (11)
+15 VDC
N.C.
R_in
R_fb
V_in
LM1875
1Ω
.22 µF
R_L
R_1 10 kΩ
R_2 10Ω

TL/H/8561–10

**FIGURE 5. Zeroing LM1875 Power Op-Amp**

## Application Hints (Continued)

### POWER AMPLIFIERS

For applications such as motor control, automated servo systems, and power amplification the LMC669 can also be used with amplifiers other than standard small signal op amps. *Figure 5* shows how the Auto Zero can allow an LM1875 audio power amplifier to operate with very low offset. While the sample rate for this configuration is not critical, the LMC669's output step size should be set for less than 1 $\mu$V to ensure low system noise.

### NON-INVERTING AMPLIFIERS AND SYSTEMS

A variation of the above circuit appears in *Figure 6* with the LMC669 operating as a DC-servo integrating feedback loop. This configuration is applicable when the Auto Zero is used with non-inverting op amps amplifying AC-only signals. The output error of the amplifier is reduced to the $V_{OS}$ of the Auto Zero, typically 5 $\mu$V. A filter at the input of the LMC669 limits current and ensures that only DC and very low frequencies (< 0.6 Hz) are sampled. In this application the output of the op amp is sampled and compared with a reference ground. The correction output from the Auto Zero now replaces the ground reference for the feedback resistor connected to the inverting input.

Systems can also benefit from the Auto Zero. *Figure 7* shows how the $V_{OS}$ of an MF6 Butterworth low-pass switched capacitor filter is nulled by the LMC669. The Auto Zero's IN1 and IN2 inputs are connected to the MF6's output while INREF is connected to its input. The correction signal is applied to the MF6's $V_{OS}$ ADJ input. RC low-pass filters ($R_{f1}$, $C_{f1}$ and $R_{f2}$, $C_{f2}$) are used to reduce AC signals at the LMC669's inputs and provide current limiting. It is important to set each passive RC filter's cutoff as low as possible, at most 0.1 of the MF6's $f_O$.

This correction makes the MF6 useful in applications calling for good DC accuracy. The MF6's typical 250 mV offset is decreased to 5 $\mu$V with a step size of 1 $\mu$V.

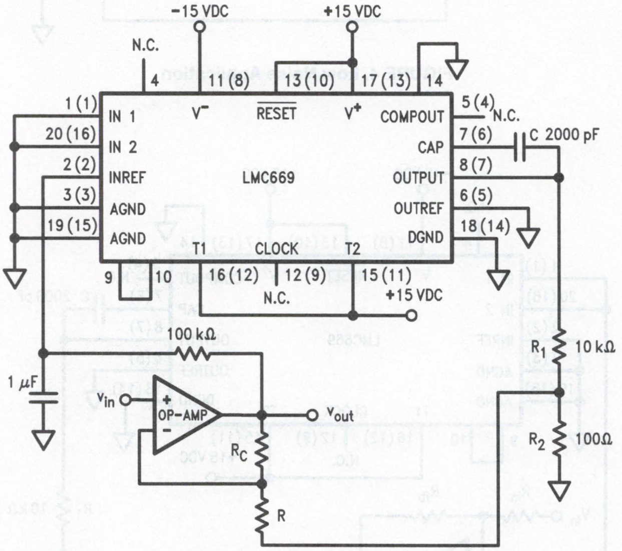

−15 VDC
+15 VDC
N.C.
4
11 (8)
13 (10)
17 (13)
14
1 (1)
IN 1
V⁻
RESET
V⁺
COMPOUT
5 (4)
N.C.
20 (16)
IN 2
CAP
7 (6)
C 2000 pF
2 (2)
INREF
LMC669
OUTPUT
8 (7)
3 (3)
AGND
OUTREF
6 (5)
19 (15)
AGND
DGND
18 (14)
T1
CLOCK
T2
9
10
16 (12)
12 (9)
15 (11)
N.C.
+15 VDC
100 kΩ
1 μF
V_in
+
OP-AMP
−
V_out
R_C
R
R_1
10 kΩ
R_2
100Ω

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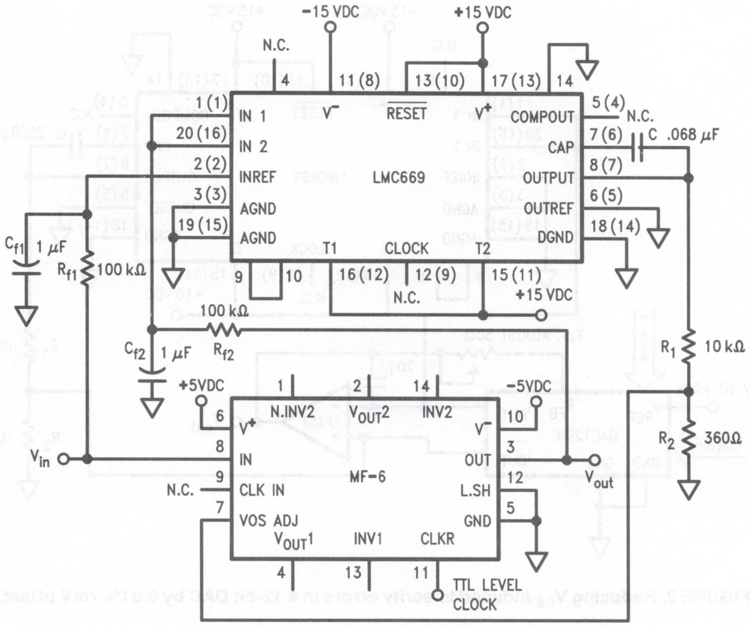
FIGURE 6. DC Servo Loop

## Application Hints (Continued)


−15 VDC
+15 VDC
N.C.
4
11 (8)
13 (10)
17 (13)
14
1 (1)
IN 1
V−
RESET
V+
COMPOUT
5 (4)
N.C.
20 (16)
IN 2
CAP
7 (6)
C .068 µF
2 (2)
INREF
LMC669
OUTPUT
8 (7)
3 (3)
AGND
OUTREF
6 (5)
19 (15)
AGND
DGND
18 (14)
T1
CLOCK
T2
Cf1 1 µF
Rf1 100 kΩ
9
10
16 (12)
12 (9)
15 (11)
N.C.
+15 VDC
100 kΩ
Cf2 1 µF
Rf2
R1 10 kΩ
+5VDC
1
2
14
−5VDC
N.INV2
VOUT2
INV2
6
V+
V−
10
8
IN
OUT
3
Vin
R2 360Ω
Vout
N.C.
9
CLK IN
MF-6
L.SH
12
7
VOS ADJ
GND
5
VOUT1
INV1
CLKR
4
13
11
TTL LEVEL CLOCK

TL/H/8561-12

**FIGURE 7. Auto zeroing a system. In this case the 250 mV offset of a switched-capacitor low-pass filter is corrected by the LMC669.**

### MAINTAINING DAC LINEARITY

The LMC669 is particularly useful for zeroing the offset of an op amp used with a CMOS digital-to-analog converter (DAC). For good linearity the DAC's two outputs ($I_{out}$ and $\overline{I_{out}}$) must be connected to identical ground potentials. The presence of op amp $V_{OS}$ (and its drift due to temperature) will degrade the DAC's linearity. Even though the effects of $V_{OS}$ can be corrected by trimming, a static trim will not be very helpful if the $V_{OS}$ changes with respect to temperature.

*Figure 8* shows the DAC1208 with a 10V reference driving an LF357. The linearity of this DAC will degrade by 0.01% for each millivolt of op amp $V_{OS}$. Therefore, the LF357's typical offset of 5 mV will turn the 12-bit DAC1208's 0.012% linearity error into 0.062%. What was a 12 bit linear device now has only 9 bits linearity. The original linearity specification can be retained by connecting an LMC669 to the inputs of the LF357, rendering the non-linearity due to $V_{OS}$ and temperature drift negligible. The DAC is now able to operate at its published linearity specifications independent of $V_{OS}$ and temperature.

*Figure 9* shows the schematic of a unipolar power DAC. One use of the power DAC is as a digitally controlled power supply having the ability to sink current, in the case of inductive loads, as well as source current. The linearity of the DAC is preserved by the nulling action of the LMC669 connected to the inputs of the LM1875 power amplifier. The amplifier can generate an output voltage from 0 to 25 volts and a maximum current of 3 amperes. The actual output is determined by

$$V_{out} = \frac{-V_{ref}\,(D)}{4096}$$

("D" is the value of the digital code, base 10). The magnitude of each step is

$$1\ \text{LSB} = \frac{|V_{ref}|}{4096}$$

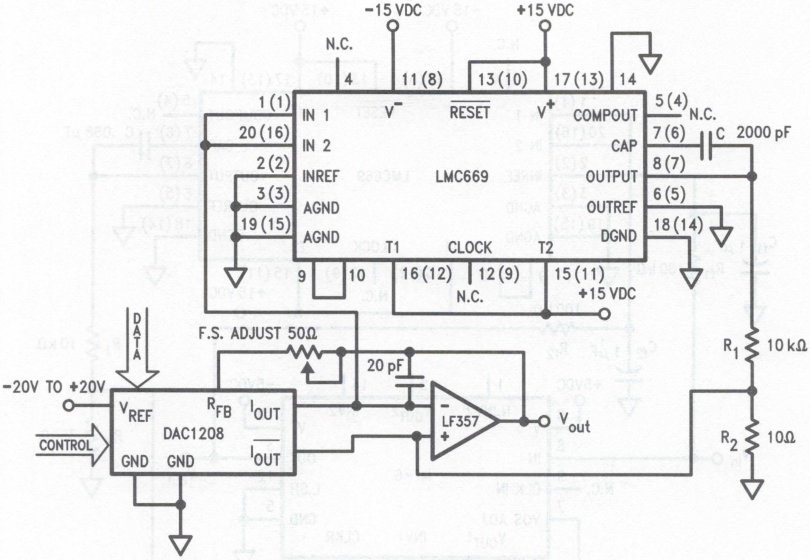
Stable operation of the LM1875 is ensured by the RC combination connected to the inverting input.

### LMC669 AS A COMPARATOR

The LMC669's operation as a comparator is shown in *Figure 10*. Its input impedance is 5 kΩ with 160 pF to ground. For proper operation as a comparator IN1 and IN2, or INREF, should be kept between 0 and 2V while the other input (or inputs) can be taken to $V^+$. If input current limiting ($\leq$20 mA) is provided, the inputs can also go to $V^-$. (In addition, please refer to notes 3 and 5 under "Electrical Characteristics".)

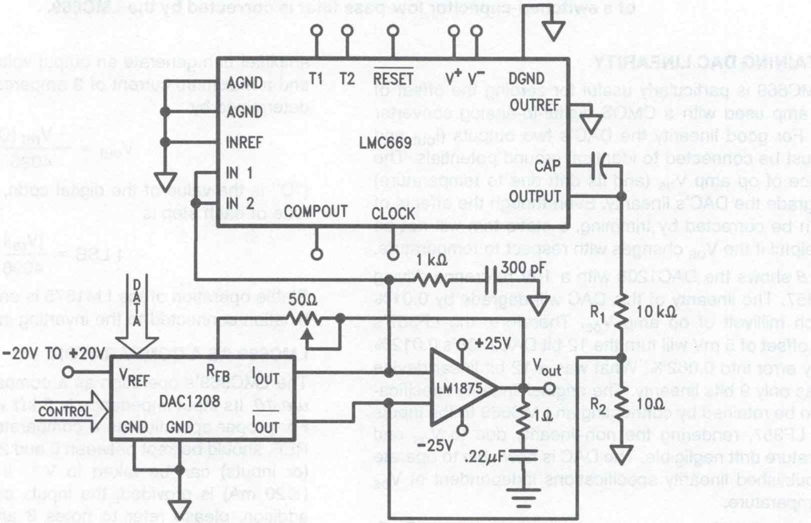
The open collector output can be pulled-up to typically 25 volts. When the sink current is 1 mA the output can pull-down to 0.25V. Outputs closer to ground are possible with a larger pullup resistor.

## Application Hints (Continued)


-15 VDC
+15 VDC
N.C.
4
11 (8)
13 (10)
17 (13)
14
1 (1)
IN 1
$V^-$
RESET
$V^+$
COMPOUT
5 (4)
N.C.
20 (16)
IN 2
CAP
7 (6)
C 2000 pF
2 (2)
INREF
LMC669
OUTPUT
8 (7)
3 (3)
AGND
OUTREF
6 (5)
19 (15)
AGND
DGND
18 (14)
T1
CLOCK
T2
9
10
16 (12)
12 (9)
15 (11)
N.C.
+15 VDC
DATA
F.S. ADJUST 50Ω
20 pF
-20V TO +20V
$V_{REF}$
$R_{FB}$
$I_{OUT}$
DAC1208
CONTROL
$\overline{I_{OUT}}$
GND
GND
LF357
$V_{out}$
$R_1$
10 kΩ
$R_2$
10Ω

TL/H/8561–13

FIGURE 8. Reducing $V_{OS}$-induced linearity errors in a 12-bit DAC by 0.01% /mV offset.


AGND
AGND
INREF
IN 1
IN 2
T1
T2
RESET
$V^+$
$V^-$
DGND
OUTREF
LMC669
CAP
OUTPUT
COMPOUT
CLOCK
1 kΩ
300 pF
DATA
50Ω
$R_1$
10 kΩ
+25V
-20V TO +20V
$V_{REF}$
$R_{FB}$
$I_{OUT}$
$V_{out}$
DAC1208
LM1875
CONTROL
GND
GND
$\overline{I_{OUT}}$
1Ω
$R_2$
10Ω
-25V
22μF

TL/H/8561–14

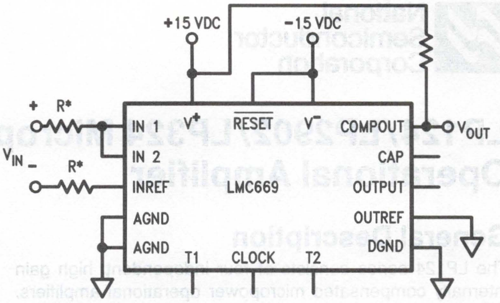
FIGURE 9. Power DAC with ±20$V_{p-p}$ and 3A output capabilities.

## Application Hints (Continued)

### LOW-FREQUENCY, HIGH-GAIN AMPLIFIER

For applications that require precision high-gain DC and low-frequency performance, the LMC669 can be connected as an amplifier as shown in *Figure 11*. For a closed-loop gain of −1000 the useful frequency range is typically

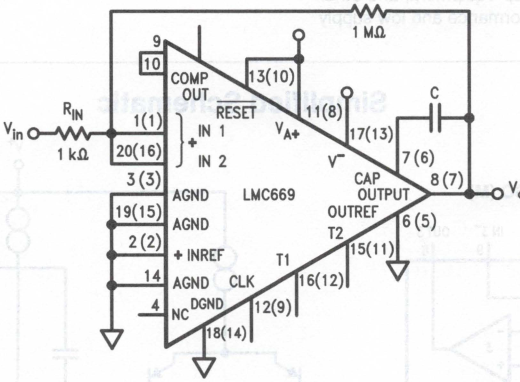
$$F_{max} = 20 \frac{\text{Hz}}{\text{mV of step size}}$$


+15 VDC
−15 VDC
+
R*
V_IN
−
R*
IN 1
IN 2
INREF
AGND
AGND
V+
RESET
V−
COMPOUT
CAP
OUTPUT
OUTREF
DGND
LMC669
T1
CLOCK
T2
V_OUT

TL/H/8561–16

*R = 10K. For inputs greater than 2 volts.

**FIGURE 10. Low-Speed Precision Comparator**


R_f
1 MΩ
C
V_in
R_IN
1 kΩ
9
10
COMP OUT
RESET
13(10)
11(8)
V_A+
1(1)
20(16)
IN 1
IN 2
+
17(13)
V−
7(6)
3(3)
CAP
OUTPUT
8(7)
V_out
19(15)
AGND
LMC669
AGND
OUTREF
6(5)
2(2)
+ INREF
T2
15(11)
T1
14
AGND
CLK
16(12)
4
NC
DGND
12(9)
18(14)

TL/H/8561–15

**FIGURE 11. Low Offset, High Gain, Low Frequency Op Amp.**

$$\text{Bandwidth} \cong 20 \frac{\text{Hz}}{\text{mV of step size}}, \text{ sample rate} = 100 \text{ kHz.}$$

**National Semiconductor Corporation**

**PRELIMINARY**

# LP124/LP2902/LP324 Micropower Quad Operational Amplifier

## General Description

The LP124 series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP124 has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

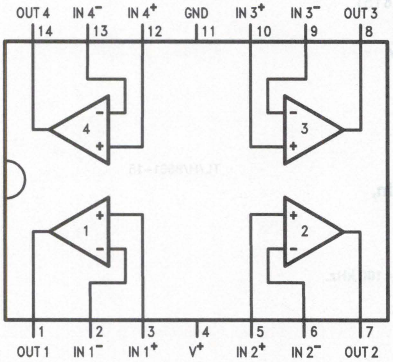
These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

## Features

| | |
|---|---|
| ■ Low supply current | 125 μA (max) |
| ■ Low offset voltage | 2 mV (max) |
| ■ Low input bias current | 4 nA (max) |
| ■ Input common mode to GND | |
| ■ Interfaces to CMOS logic | |
| ■ Wide supply range | $3V < V^{+} < 32V$ |
| ■ Small Outline Package available | |
| ■ Pin-for-pin compatible with LM124 | |

## Connection Diagram

**Dual-in-Line (J, N) and SO (M)**



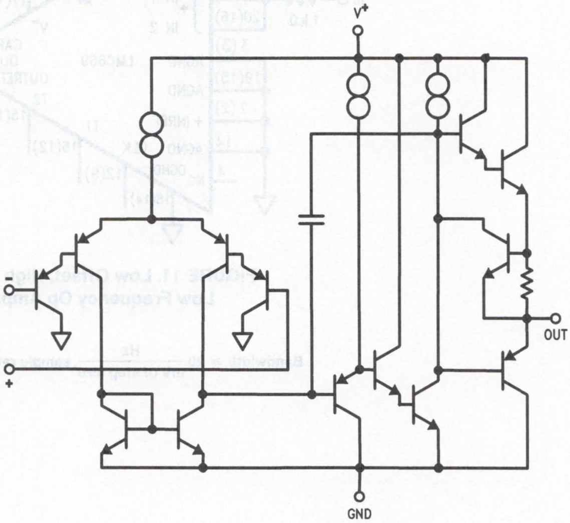
TL/H/8562-1

**Order Number LP124J or LP324J**
**See NS Package Number J14A**

**Order Number LP324M or LP2902M**
**See NS Package Number M14A**

**Order Number LP324N or LP2902N**
**See NS Package Number N14A**

## Simplified Schematic



TL/H/8562-2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 32V or ± 16V |
| LP2902 | 26V or ± 13V |
| Differential Input Voltage | 32V |
| LP2902 | 26V |
| Input Voltage (Note 1) | −0.3V to 32V |
| LP2902 | −0.3V to 26V |
| Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$ | Continuous |
| ESD Susceptibility (Note 9) | ±500V |

## Operating Conditions

| | Package J | Package N | Package M |
|---|---|---|---|
| Power Dissipation (Note 3) | 500 mW | 500 mW | 500 mW |
| $T_j$ Max | 150°C | 150°C | 150°C |
| $\theta_{ja}$ | 90°C/W | 90°C/W | 140°C/W |
| Operating Temp. Range | (Note 4) | (Note 4) | (Note 4) |
| Storage Temp. Range | $-65°C \leq T \leq 150°C$ | | |
| Soldering | | | |
| Information (10 sec.) | 300°C | 260°C | |
| Vapor Phase (60 sec.) | | | 215°C |
| Infrared (15 sec.) | | | 220°C |

## Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LP124 Typ | LP124 Tested Limit (Note 6) | LP124 Design Limit (Note 7) | LP2902 (Note 8) Typ | LP2902 (Note 8) Tested Limit (Note 6) | LP2902 (Note 8) Design Limit (Note 7) | LP324 Typ | LP324 Tested Limit (Note 6) | LP324 Design Limit (Note 7) | Units Limits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{os}$ | Input Offset Voltage | | 1 | 2<br>**4** | **7** | 2 | 4 | **10** | 2 | 4 | **9** | mV (Max) |
| $I_b$ | Input Bias Current | | 1 | 4<br>**8** | **8** | 2 | 20 | **40** | 2 | 10 | **20** | nA (Max) |
| $I_{os}$ | Input Offset Current | | 0.1 | 1<br>**2** | **2** | 0.5 | 4 | **8** | 0.2 | 2 | **4** | nA (Max) |
| $A_{vol}$ | Voltage Gain | $R_L = 10k$ to GND $V^+ = 30V$ | 100 | 70<br>**60** | **60** | 70 | 40 | **30** | 100 | 50 | **40** | V/mV (Min) |
| CMRR | Common Mode Rej. Ratio | $V^+ = 30V$ $0V \leq V_{cm}$ $V_{cm} < V^+ - 1.5$ | 100 | 85<br>**80** | **75** | 90 | 80 | **75** | 90 | 80 | **75** | dB (Min) |
| PSRR | Power Supply Rej. Ratio | $V^+ = 5V$ to $30V$ | 100 | 85<br>**80** | **75** | 90 | 80 | **75** | 90 | 80 | **75** | dB (Min) |
| $I_s$ | Supply Current | $R_L = \infty$ | 85 | 125<br>**150** | **200** | 85 | 150 | **250** | 85 | 150 | **250** | μA (Max) |
| $V_o$ | Output Voltage Swing | $I_L = 350\ \mu A$ to GND. $V_{cm} = 0V$ | 3.6 | 3.4<br>3.1 | **$V^+ - 1.9V$** | 3.6 | 3.4 | **$V^+ - 1.9V$** | 3.6 | 3.4 | **$V^+ - 1.9V$** | V (Min) |
| | | $I_L = 350\ \mu A$ to $V^+$ $V_{cm} = 0V$ | 0.7 | 0.8<br>**1.0** | **1.0** | 0.7 | 0.8 | **1.0** | 0.7 | 0.8 | **1.0** | V (Max) |
| $I_{out}$ Source | Output Source Current | $V_o = 3V$ $V_{in}$ (diff) = 1V | 11 | 9<br>**4** | **4** | 10 | 7 | **4** | 10 | 7 | **4** | mA (Min) |
| $I_{out}$ Sink | Output Sink Current | $V_o = 1.5V$ $V_{in}$ (diff) = 1V | 6 | 5<br>**4** | **4** | 5 | 4 | **3** | 5 | 4 | **3** | mA (Min) |
| $I_{out}$ Sink | Output Sink Current | $V_o = 1.5V$ $V_{cm} = 0V$ | 5 | 3<br>**0.5** | **1.5** | 4 | 2 | **1** | 4 | 2 | **1** | mA (Min) |
| $I_{source}$ | Output Short to GND | $V_{in}$ (diff) = 1V | 20 | 25<br>**35** | **35** | 20 | 25<br>**35** | **35** | 20 | 25<br>**35** | **35** | mA (Max) |

## Electrical Characteristics (Note 5) (Continued)

| Symbol | Parameter | Conditions | LP124 |  |  | LP2902 (Note 8) |  |  | LP324 |  |  | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Typ | Tested Limit (Note 6) | Design Limit (Note 7) | Typ | Tested Limit (Note 6) | Design Limit (Note 7) | Typ | Tested Limit (Note 6) | Design Limit (Note 7) | Limits |
| $I_{sink}$ | Output Short to $V^+$ | $V_{in}$ (diff) = 1V | 15 | 20<br>**25** | **35** | 15 | 20 | **35** | 15 | 20 | **35** | mA (Max) |
| $V_{os}$ Drift |  |  | 7 |  |  | 10 |  |  | 10 |  |  | μV/C° |
| $I_{os}$ Drift |  |  | 5 |  |  | 10 |  |  | 10 |  |  | pA/C° |
| GBW | Gain Bandwidth Product |  | 100 |  |  | 100 |  |  | 100 |  |  | KHz |
| $S_r$ | Slew Rate |  | 50 |  |  | 50 |  |  | 50 |  |  | V/mS |

**Note 1:** The input voltage is not allowed to go more than −0.3V below $V^-$ (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.

**Note 2:** Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of $V^+$. At values of supply voltage in excess of 15 $V_{DC}$, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

**Note 3:** For operation at elevated temperatures, these devices must be derated based on a thermal resistance of $\theta_{ja}$ and $T_j$ max. $T_j = T_A + \theta_{ja} P_D$.

**Note 4:** The LP124 may be operated from $-55°C \leq T_A \leq +125°C$. The LP2902 may be operated from $-40°C \leq T_A \leq +85°C$, and the LP324 may be operated from $0°C \leq T_A \leq +70°C$.

**Note 5: Boldface numbers apply at temperature extremes.** All other numbers apply only at $T_A = T_j = 25°C$, $V^+ = 5V$, $V_{cm} = V/2$, and $R_L = 100k$ connected to GND unless otherwise specified.

**Note 6:** Guaranteed and 100% production tested.

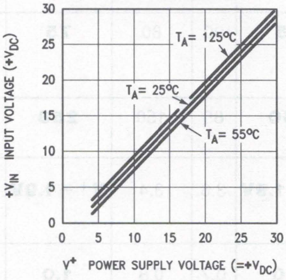
**Note 7:** Guaranteed (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP124, LP324, and 3.0V to 26V for the LP2902), and the common mode range (0V to $V^+ - 1.5V$), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

**Note 8:** The LP2902 operating supply range is 3V to 26V, and is not tested above 26V.

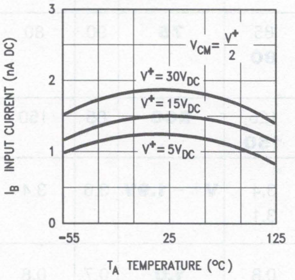
**Note 9:** The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

## Typical Performance Curves

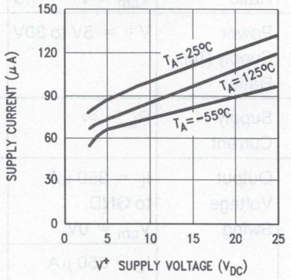
### Input Voltage Range



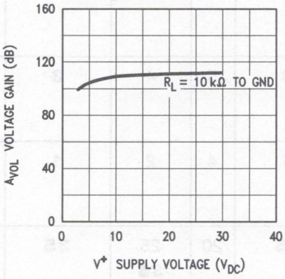
### Input Current



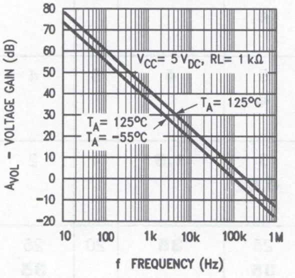
### Supply Current



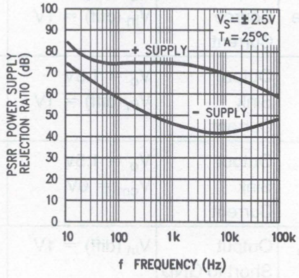
### Voltage Gain



### Open Loop Frequency Response



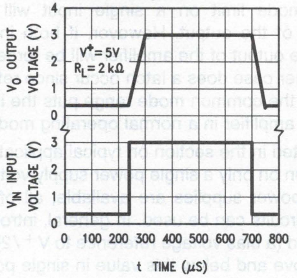
### Power Supply Rejection Ratio



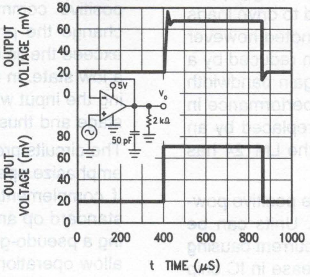
TL/H/8562-18

## Typical Performance Curves (Continued)

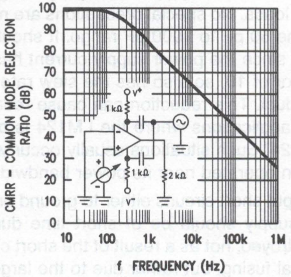
**Voltage Follower Pulse Response**



**Voltage Follower Pulse Response (Small Signal)**

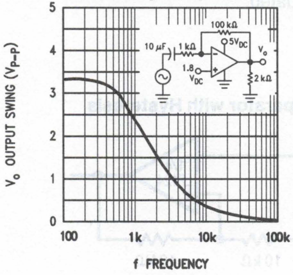


**Common Mode Rejection Ratio**

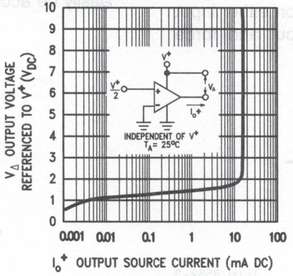


TL/H/8562–20

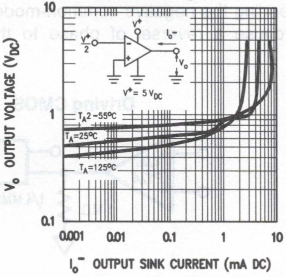
**Large Signal Frequency Response**



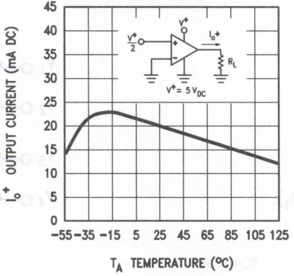
**Output Characteristics Current Sourcing**



**Output Characteristics Current Sinking**



**Current Limiting**



TL/H/8562–19

## Application Hints

The LP124 series is a micro-power pin-for-pin equivalent to the LM124 op amps. Power supply current, input bias current, and input offset current have all been reduced by a factor of 10 over the LM124. Like its predecessor, the LP124 series op amps can operate on single supply, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 $V_{DC}$.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or the unit is not inadvertently installed backwards in the test socket as an unlimited current surge through the resulting forward diode within the IC could destroy the unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than $V^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

The amplifiers have a class B output stage which allows the amplifiers to both source and sink output currents. In applications where crossover distortion is undesirable, a resistor

## Application Hints (Continued)

should be used from the output of the amplifier to ground. The resistor biases the output into class A operation.

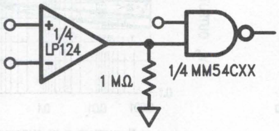
The LP124 has improved stability margin for driving capacitive loads. No special precautions are needed to drive loads in the 50 pF to 1000 pF range. It should be noted however that since the power supply current has been reduced by a factor of 10, so also has the slew rate and gain bandwidth product. This reduction can cause reduced performance in AC applications where the LM124 is being replaced by an LP124. Such situations usually occur when the LM124 has been operated near its power bandwidth.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example: If all four amplifiers were simultaneously shorted to ground on a 10V supply the junction temperature would rise by 110°C.

Exceeding the negative common-mode limit on either input will cause a reversal of phase to the output and force the amplifier to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a low state. In neither case does a latch occur since returning the input within the common mode range puts the input stage and thus the amplifier in a normal operating mode.

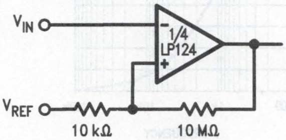
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference to V+/2) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

**Driving CMOS**



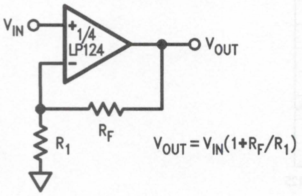
TL/H/8562-3

**Comparator with Hysteresis**



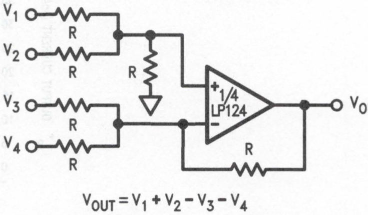
TL/H/8562-6

**Non-Inverting Amplifier**



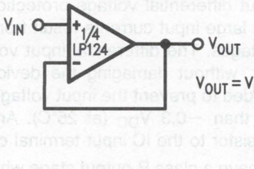
TL/H/8562-4

**Adder/Subtractor**



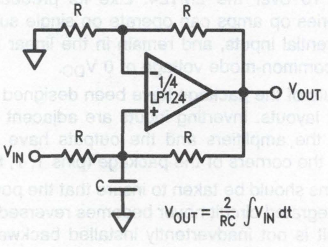
TL/H/8562-7

**Unity Gain Buffer**



TL/H/8562-5

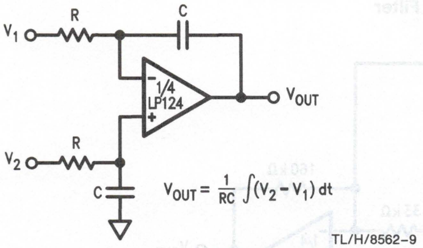
**Positive Integrator**



TL/H/8562-8

## Application Hints (Continued)

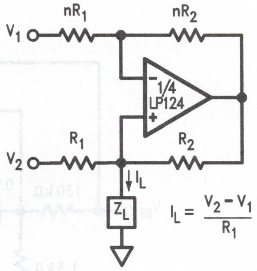
### Differential Integrator


R
C
V1
1/4 LP124
VOUT
R
V2
C

$$V_{OUT} = \frac{1}{RC}\int(V_2 - V_1)\,dt$$

TL/H/8562–9

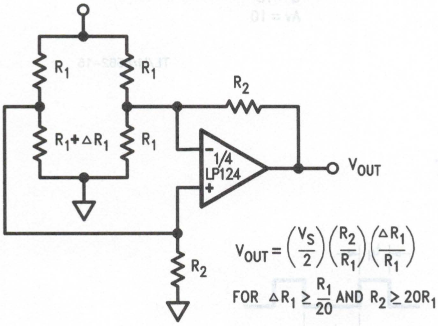
### Howland Current Pump


nR1
nR2
V1
1/4 LP124
R1
R2
V2
IL
ZL

$$I_L = \frac{V_2 - V_1}{R_1}$$

TL/H/8562–10

### Bridge Current Amplifier

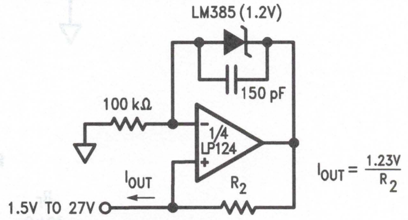

R1
R1
R2
R1+ΔR1
R1
1/4 LP124
VOUT
R2

$$V_{OUT} = \left(\frac{V_S}{2}\right)\left(\frac{R_2}{R_1}\right)\left(\frac{\Delta R_1}{R_1}\right)$$

FOR $\Delta R_1 \geq \frac{R_1}{20}$ AND $R_2 \geq 20R_1$

TL/H/8562–11

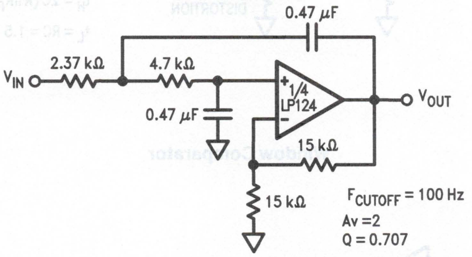
### $\mu$ Power Current Source


LM385 (1.2V)
150 pF
100 kΩ
1/4 LP124
IOUT
R2
1.5V TO 27V

$$I_{OUT} = \frac{1.23V}{R_2}$$

TL/H/8562–12

### Lowpass Filter


0.47 µF
VIN
2.37 kΩ
4.7 kΩ
1/4 LP124
VOUT
0.47 µF
15 kΩ
15 kΩ

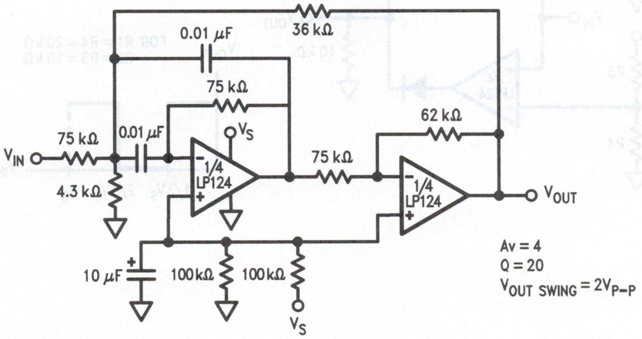
$F_{CUTOFF} = 100$ Hz

$A_V = 2$

$Q = 0.707$

TL/H/8562–13

### 1 kHz Bandpass Active Filter


36 kΩ
0.01 µF
75 kΩ
VS
62 kΩ
75 kΩ
0.01 µF
VIN
1/4 LP124
75 kΩ
1/4 LP124
VOUT
4.3 kΩ
10 µF
100kΩ
100kΩ
VS

$A_V = 4$

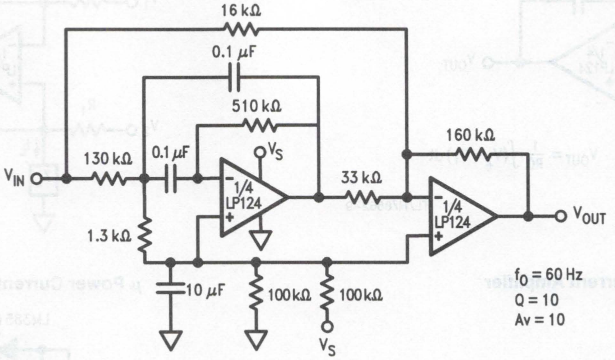
$Q = 20$

$V_{OUT\ SWING} = 2V_{P-P}$

TL/H/8562–14

## Application Hints (Continued)

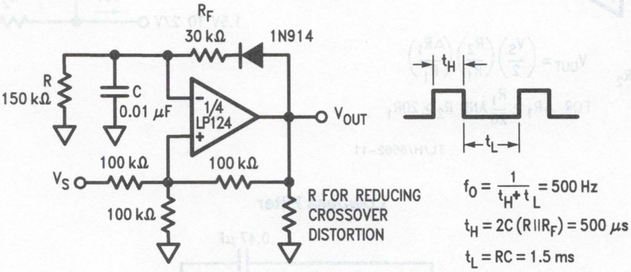
### Band-Reject Filter


16 kΩ
0.1 μF
510 kΩ
$V_S$
$V_{IN}$
130 kΩ
0.1 μF
1/4 LP124
33 kΩ
160 kΩ
1/4 LP124
$V_{OUT}$
1.3 kΩ
10 μF
100kΩ
100kΩ
$V_S$

$f_O = 60$ Hz
$Q = 10$
$A_V = 10$

TL/H/8562–15

### Pulse Generator


$R_F$
30 kΩ
1N914
R
150 kΩ
C
0.01 μF
1/4 LP124
$V_{OUT}$
$V_S$
100 kΩ
100 kΩ
100 kΩ
R FOR REDUCING CROSSOVER DISTORTION
$t_H$
$t_L$

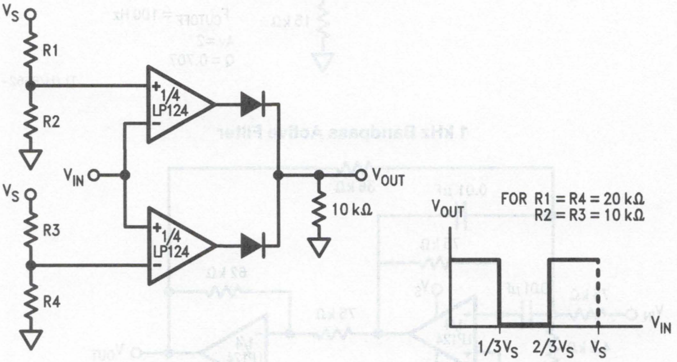
$f_O = \frac{1}{t_H + t_L} = 500$ Hz

$t_H = 2C\,(R \| R_F) = 500\ \mu s$

$t_L = RC = 1.5$ ms

TL/H/8562–16

### Window Comparator

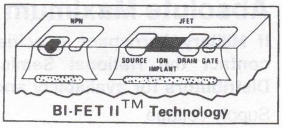

$V_S$
R1
R2
1/4 LP124
$V_{IN}$
$V_{OUT}$
$V_S$
R3
R4
1/4 LP124
10 kΩ
$V_{OUT}$
$V_{IN}$
$1/3V_S$
$2/3V_S$
$V_S$

FOR R1 = R4 = 20 kΩ
R2 = R3 = 10 kΩ

TL/H/8562–17

**National Semiconductor Corporation**

**PRELIMINARY**



# TL081CP Wide Bandwidth JFET Input Operational Amplifier

## General Description

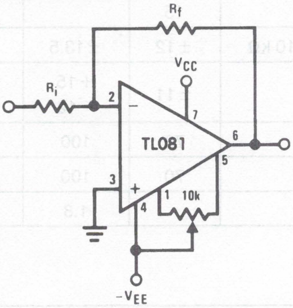
The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

## Features

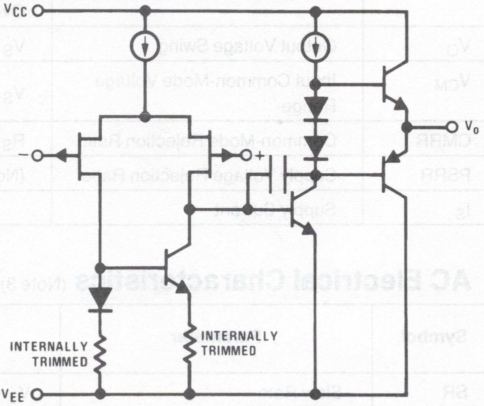
| | |
|---|---|
| ■ Internally trimmed offset voltage | 15 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise voltage | 25 nV/$\sqrt{Hz}$ |
| ■ Low input noise current | 0.01 pA/$\sqrt{Hz}$ |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/μs |
| ■ Low supply current | 1.8 mA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz−20 kHz | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 μs |

## Typical Connection



TL/H/8358–1

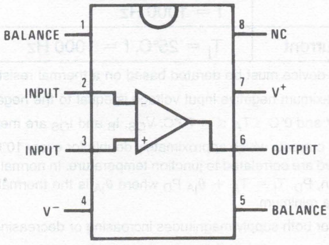
## Simplified Schematic



TL/H/8358–2

## Connection Diagram

**Dual-In-Line Package**



TL/H/8358–4

**Order Number TL081CP**
**See NS Package Number N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Notes 1 and 6) | 670 mW |
| Operating Temperature Range | 0°C to +70°C |
| $T_{j(MAX)}$ | 115°C |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 2) | ±15V |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 260°C |
| $\theta_{jA}$ | 120°C/W |

ESD rating to be determined.

## DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | TL081C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S = 10\ k\Omega$, $T_A = 25°C$ | | 5 | 15 | mV |
| | | Over Temperature | | | 20 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\ k\Omega$ | | 10 | | $\mu V/°C$ |
| $I_{OS}$ | Input Offset Current | $T_j = 25°C$, (Notes 3, 4) | | 25 | 100 | pA |
| | | $T_j \le 70°C$ | | | 4 | nA |
| $I_B$ | Input Bias Current | $T_j = 25°C$, (Notes 3, 4) | | 50 | 200 | pA |
| | | $T_j \le 70°C$ | | | 8 | nA |
| $R_{IN}$ | Input Resistance | $T_j = 25°C$ | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S = \pm 15V$, $T_A = 25°C$<br>$V_O = \pm 10V$, $R_L = 2\ k\Omega$ | 25 | 100 | | V/mV |
| | | Over Temperature | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | ±11 | +15<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S \le 10\ k\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 5) | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | 1.8 | 2.8 | mA |

## AC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | TL081C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| SR | Slew Rate | $V_S = \pm 15V$, $T_A = 25°C$ | | 13 | | $V/\mu s$ |
| GBW | Gain Bandwidth Product | $V_S = \pm 15V$, $T_A = 25°C$ | | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A = 25°C$, $R_S = 100\Omega$,<br>f = 1000 Hz | | 25 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Equivalent Input Noise Current | $T_j = 25°C$, f = 1000 Hz | | 0.01 | | $pA/\sqrt{Hz}$ |

**Note 1:** For operating at elevated temperature, the device must be derated based on a thermal resistance of 120°C/W junction to ambient for N package.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 3:** These specifications apply for $V_S = \pm 15V$ and $0°C \le T_A \le +70°C$. $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM} = 0$.

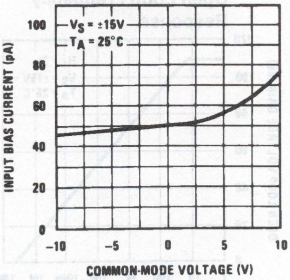
**Note 4:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 5:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$.

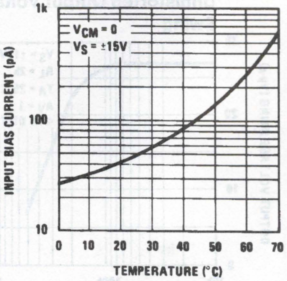
**Note 6:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

## Typical Performance Characteristics

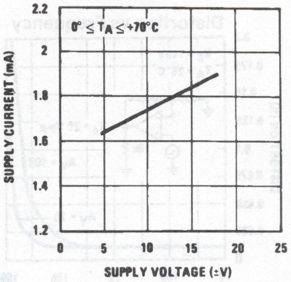
Input Bias Current



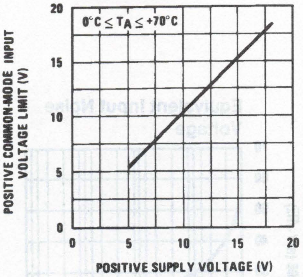
Input Bias Current



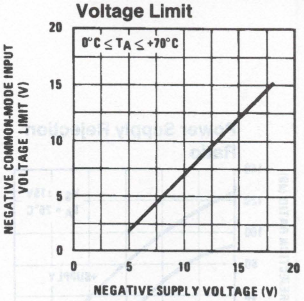
Supply Current



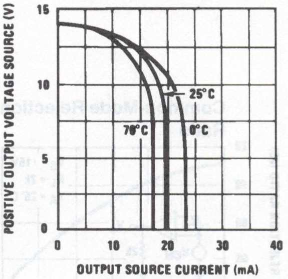
Positive Common-Mode Input Voltage Limit



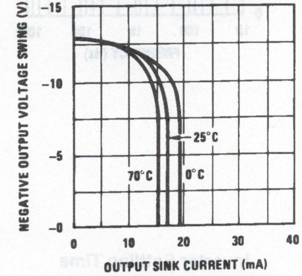
Negative Common-Mode Input Voltage Limit



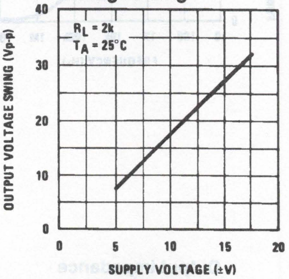
Positive Current Limit



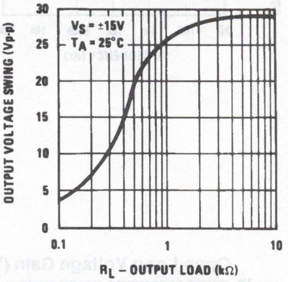
Negative Current Limit



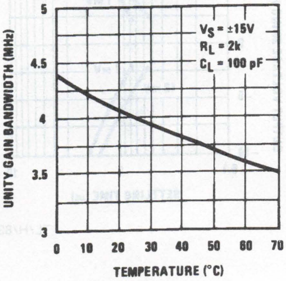
Voltage Swing



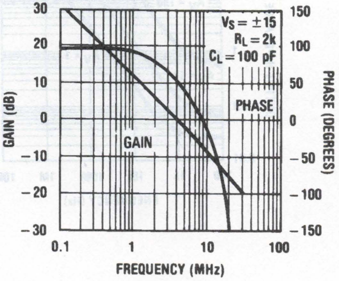
Output Voltage Swing



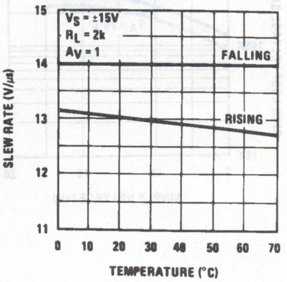
Gain Bandwidth



Bode Plot



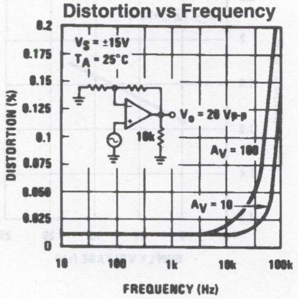
Slew Rate



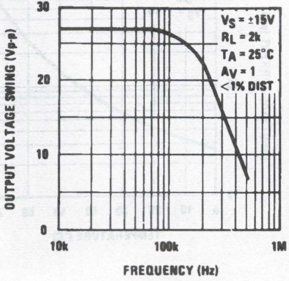
TL/H/8358–5

## Typical Performance Characteristics (Continued)

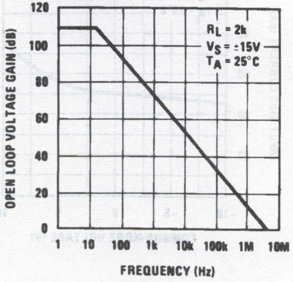
Distortion vs Frequency



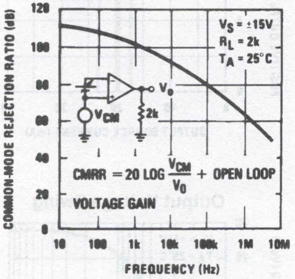
Undistorted Output Voltage Swing



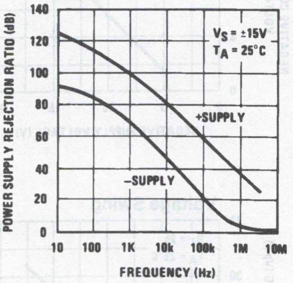
Open Loop Frequency Response



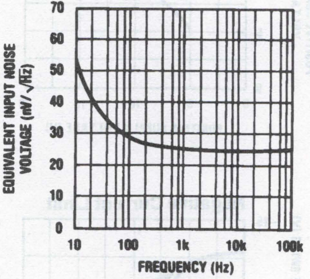
Common-Mode Rejection Ratio



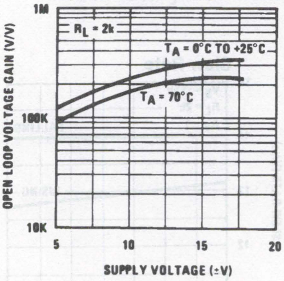
Power Supply Rejection Ratio



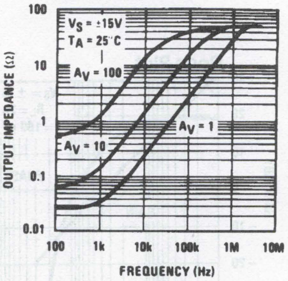
Equivalent Input Noise Voltage



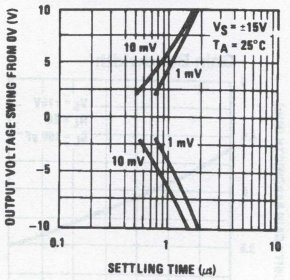
Open Loop Voltage Gain (V/V)



Output Impedance

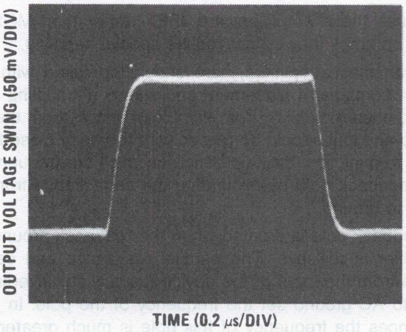


Inverter Settling Time

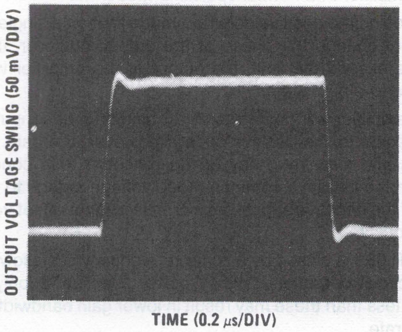


TL/H/8358–6

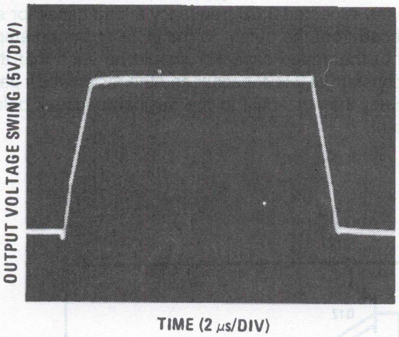
## Pulse Response


Small Signal Inverting

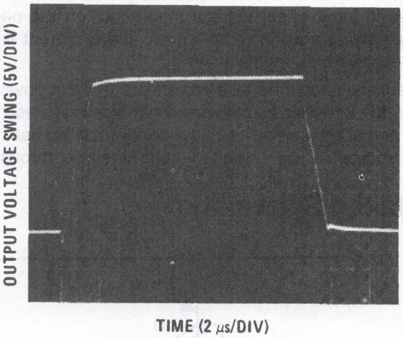
TL/H/8358–7


Small Signal Non-Inverting

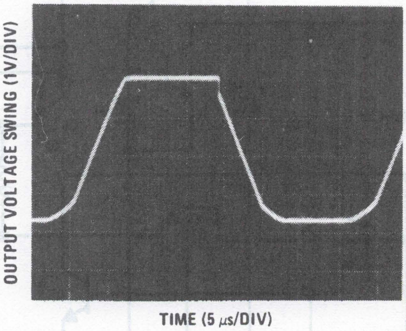
TL/H/8358–13


Large Signal Inverting

TL/H/8358–14


Large Signal Non-Inverting

TL/H/8358–15


Current Limit ($R_L = 100\Omega$)

TL/H/8358–16

## Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

## Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

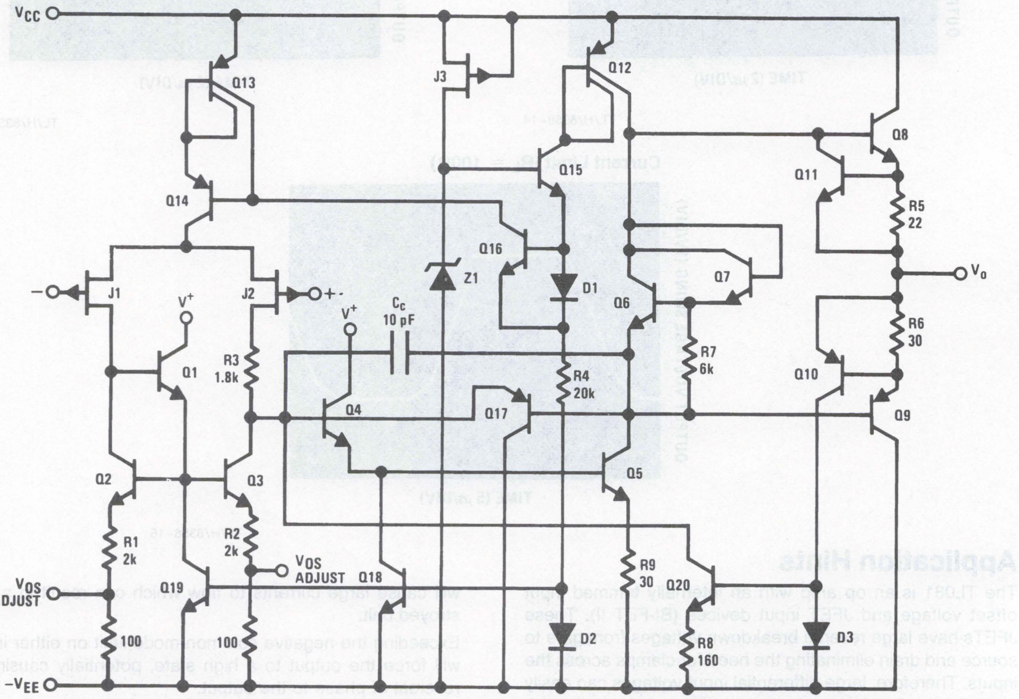
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

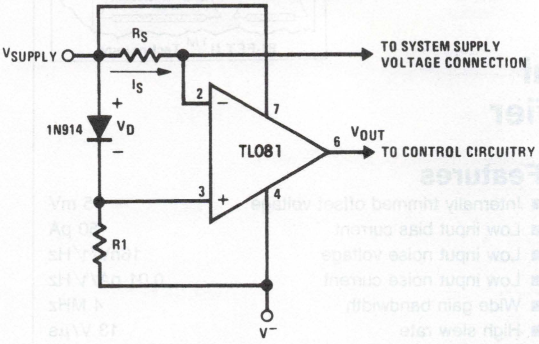
## Detailed Schematic



TL/H/8358–8

## Typical Applications

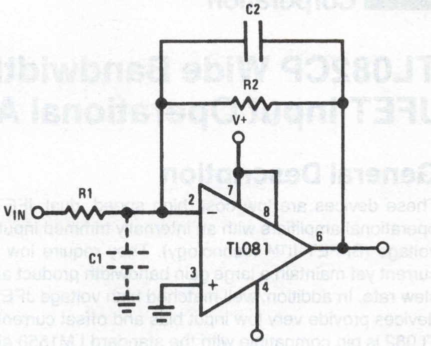
### Supply Current Indicator/Limiter


VSUPPLY
RS
IS
+
1N914
VD
−
R1
TO SYSTEM SUPPLY VOLTAGE CONNECTION
2
−
7
TL081
6
VOUT
TO CONTROL CIRCUITRY
3
+
4
V−

TL/H/8358–9

- $V_{OUT}$ switches high when $R_S I_S > V_D$

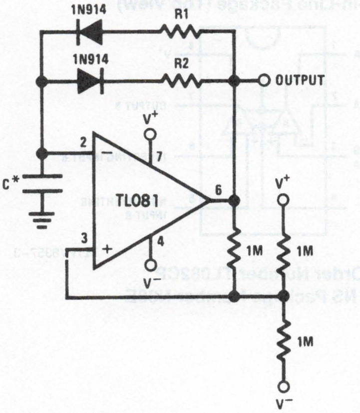
### Hi-$Z_{IN}$ Inverting Amplifier


C2
R2
V+
R1
VIN
C1
2
7
8
TL081
6
3
+
4
V−

TL/H/8358–10

Parasitic input capacitance C1 ≅ (3 pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

### Ultra-Low (or High) Duty Cycle Pulse Generator


1N914
R1
1N914
R2
OUTPUT
V+
2
−
C*
TL081
6
3
+
4
V−
V+
1M
1M
1M
V−

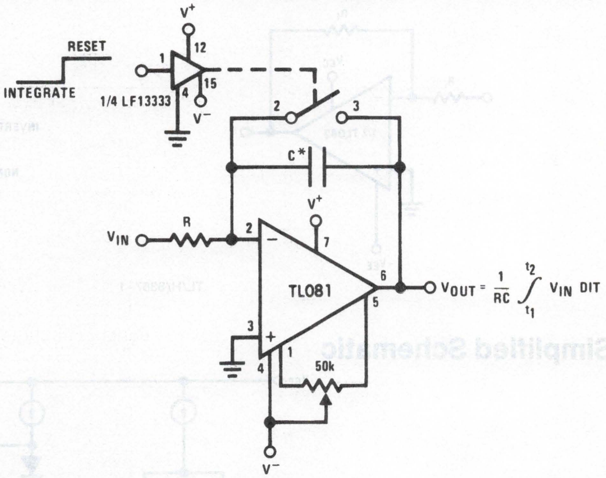
TL/H/8358–11

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

### Long Time Integrator

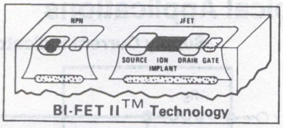

RESET
INTEGRATE
V+
1
12
1/4 LF13333
4
15
V−
2
3
C*
V+
R
VIN
2
−
7
TL081
6
5
3
+
1
4
50k
V−
$V_{OUT} = \frac{1}{RC}\int_{t_1}^{t_2} V_{IN}\,dt$

TL/H/8358–12

- *Low leakage capacitor
- 50k pot used for less sensitive $V_{OS}$ adjust

**National Semiconductor Corporation**

**PRELIMINARY**


NPN
JFET
SOURCE
ION IMPLANT
DRAIN
GATE
BI-FET II™ Technology

# TL082CP Wide Bandwidth Dual JFET Input Operational Amplifier

## General Description

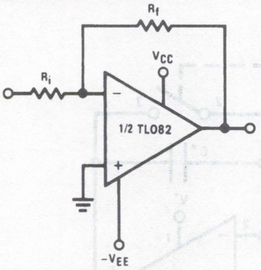
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

## Features

| | |
|---|---|
| ■ Internally trimmed offset voltage | 15 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise voltage | $16 nV/\sqrt{Hz}$ |
| ■ Low input noise current | $0.01 pA/\sqrt{Hz}$ |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/$\mu$s |
| ■ Low supply current | 3.6 mA |
| ■ High input impedance | $10^{12}\Omega$ |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp − p, BW = 20 Hz−20 kHz | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 $\mu$s |

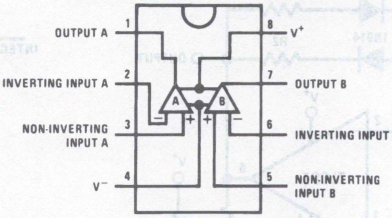
## Typical Connection


$R_f$
$R_i$
$V_{CC}$
−
+
1/2 TL082
$-V_{EE}$

TL/H/8357–1

## Connection Diagram

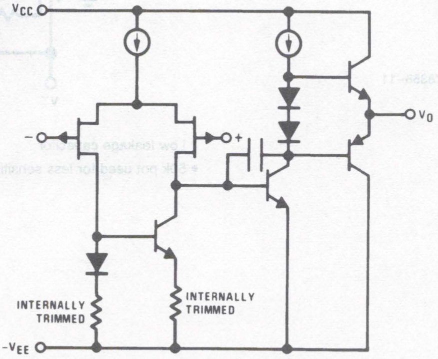
### Dual-In-Line Package (Top View)


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V⁻ 4
8 V⁺
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B
−
+
+
−

TL/H/8357–3

**Order Number TL082CP**
**See NS Package Number N08E**

## Simplified Schematic


$V_{CC}$
$V_O$
−
+
INTERNALLY TRIMMED
INTERNALLY TRIMMED
$-V_{EE}$

TL/H/8357–2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation | (Note 1) |
| Operating Temperature Range | 0°C to +70°C |
| $T_{j(MAX)}$ | 150°C |
| Differential Input Voltage | ±30V |
| Input Voltage Range (Note 2) | ±15V |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 260°C |

ESD rating to be determined.

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | TL082C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OS}$ | Input Offset Voltage | $R_S$ = 10 kΩ, $T_A$ = 25°C | | 5 | 15 | mV |
| | | Over Temperature | | | 20 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S$ = 10 kΩ | | 10 | | µV/°C |
| $I_{OS}$ | Input Offset Current | $T_j$ = 25°C, (Notes 4, 5) | | 25 | 200 | pA |
| | | $T_j$ ≤ 70°C | | | 4 | nA |
| $I_B$ | Input Bias Current | $T_j$ = 25°C, (Notes 4, 5) | | 50 | 400 | pA |
| | | $T_j$ ≤ 70°C | | | 8 | nA |
| $R_{IN}$ | Input Resistance | $T_j$ = 25°C | | $10^{12}$ | | Ω |
| $A_{VOL}$ | Large Signal Voltage Gain | $V_S$ = ±15V, $T_A$ = 25°C<br>$V_O$ = ±10V, $R_L$ = 2 kΩ | 25 | 100 | | V/mV |
| | | Over Temperature | 15 | | | V/mV |
| $V_O$ | Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 10 kΩ | ±12 | ±13.5 | | V |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V_S$ = ±15V | ±11 | +15<br>−12 | | V<br>V |
| CMRR | Common-Mode Rejection Ratio | $R_S$ ≤ 10 kΩ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 70 | 100 | | dB |
| $I_S$ | Supply Current | | | 3.6 | 5.6 | mA |

## AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | TL082C | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A$ = 25°C, f = 1Hz-20 kHz (Input Referred) | | −120 | | dB |
| SR | Slew Rate | $V_S$ = ±15V, $T_A$ = 25°C | 8 | 13 | | V/µs |
| GBW | Gain Bandwidth Product | $V_S$ = ±15V, $T_A$ = 25°C | | 4 | | MHz |
| $e_n$ | Equivalent Input Noise Voltage | $T_A$ = 25°C, $R_S$ = 100Ω, f = 1000 Hz | | 25 | | nV/√Hz |
| $i_n$ | Equivalent Input Noise Current | $T_j$ = 25°C, f = 1000 Hz | | 0.01 | | pA/√Hz |

**Note 1:** For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

**Note 2:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 3:** The power dissipation limit, however, cannot be exceeded.

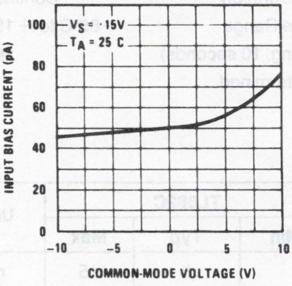
**Note 4:** These specifications apply for $V_S$ = ±15V and 0°C ≤ $T_A$ ≤ +70°C. $V_{OS}$, $I_B$ and $I_{OS}$ are measured at $V_{CM}$ = 0.

**Note 5:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_j$. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D$. $T_j = T_A + \theta_{jA} P_D$ where $\theta_{jA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

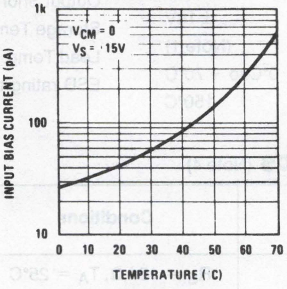
**Note 6:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S$ = ±6V to ±15V.

# Typical Performance Characteristics

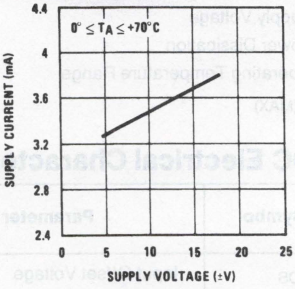
**Input Bias Current**



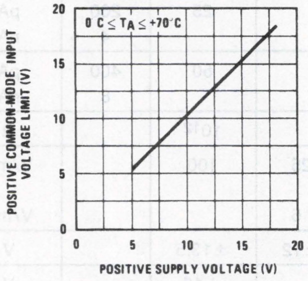
**Input Bias Current**



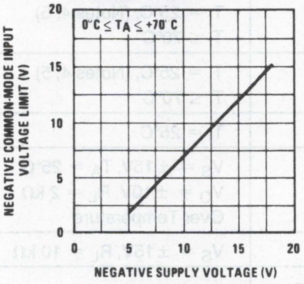
**Supply Current**



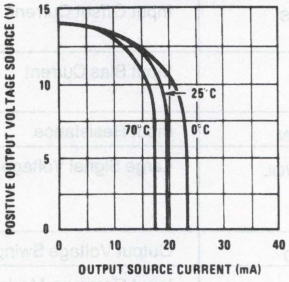
**Positive Common-Mode Input Voltage Limit**



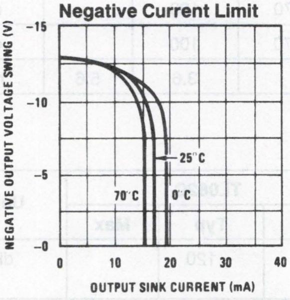
**Negative Common-Mode Input Voltage Limit**



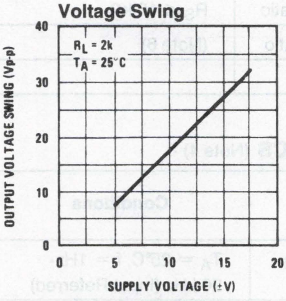
**Positive Current Limit**



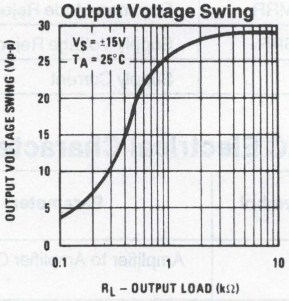
**Negative Current Limit**



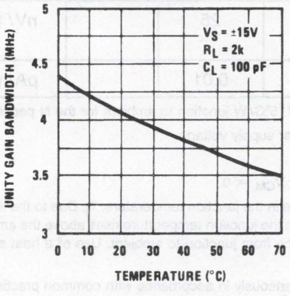
**Voltage Swing**



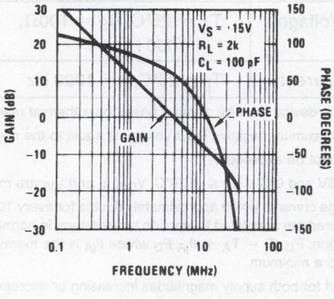
**Output Voltage Swing**



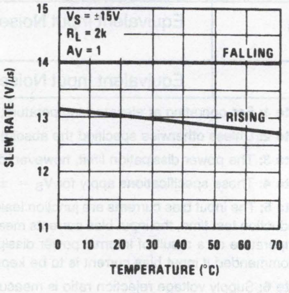
**Gain Bandwidth**



**Bode Plot**



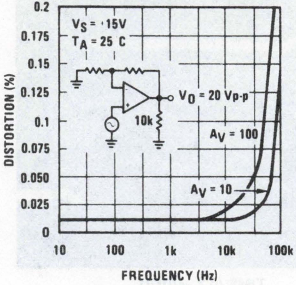
**Slew Rate**



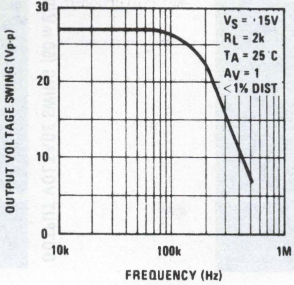
TL/H/8357-4

## Typical Performance Characteristics (Continued)

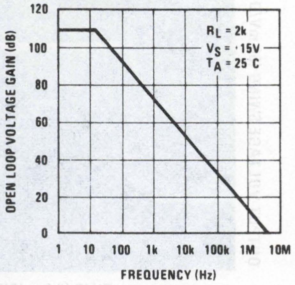
### Distortion vs Frequency



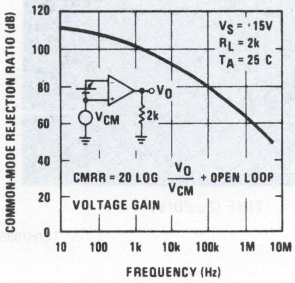
### Undistorted Output Voltage Swing



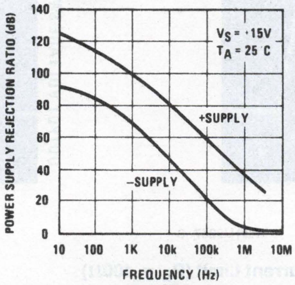
### Open Loop Frequency Response



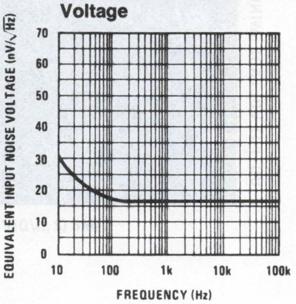
### Common-Mode Rejection Ratio



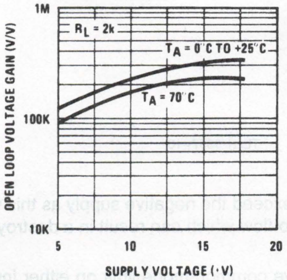
### Power Supply Rejection Ratio



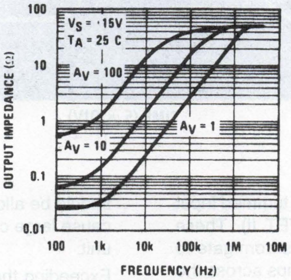
### Equivalent Input Noise Voltage



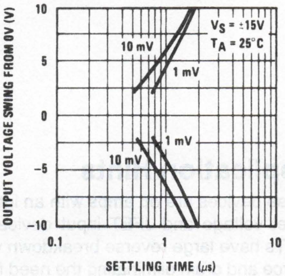
### Open Loop Voltage Gain (V/V)



### Output Impedance



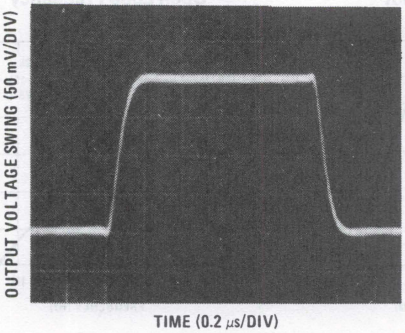
### Inverter Settling Time



TL/H/8357–5

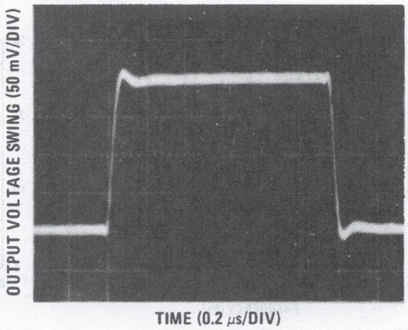
## Pulse Response

### Small Signal Inverting



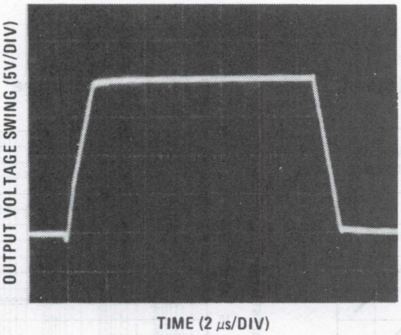
TL/H/8357-6

### Small Signal Non-Inverting



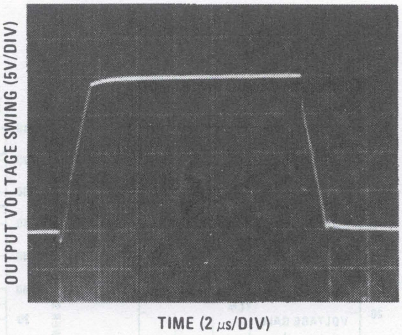
TL/H/8357-7

### Large Signal Inverting



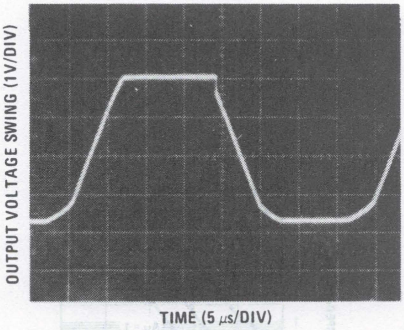
TL/H/8357-8

### Large Signal Non-Inverting



TL/H/8357-9

### Current Limit ($R_L$ = 100Ω)



TL/H/8357-10

## Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

## Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

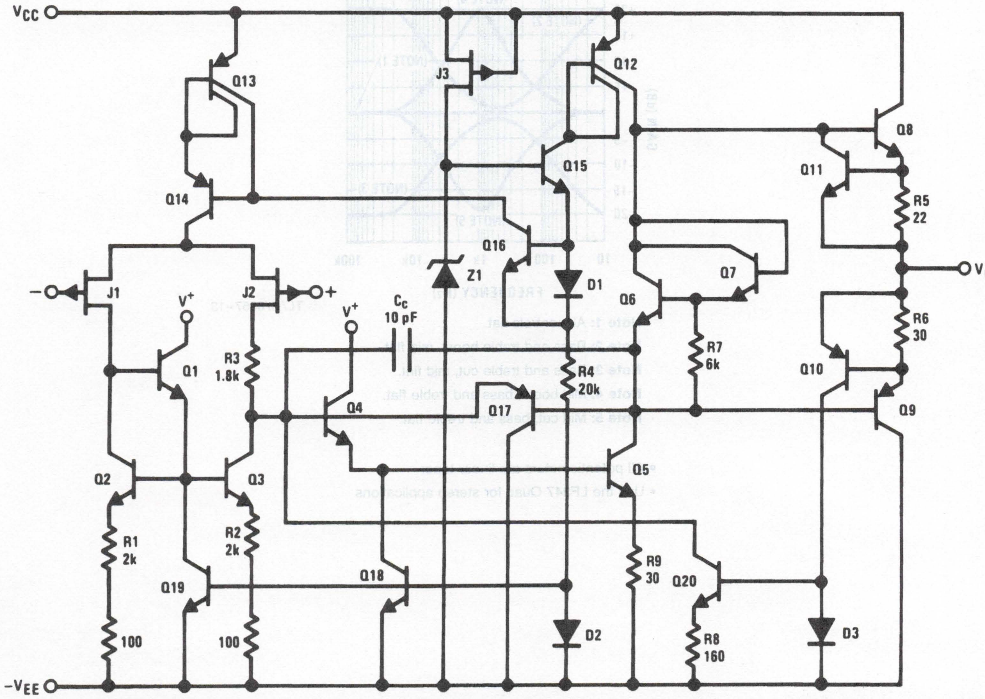
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

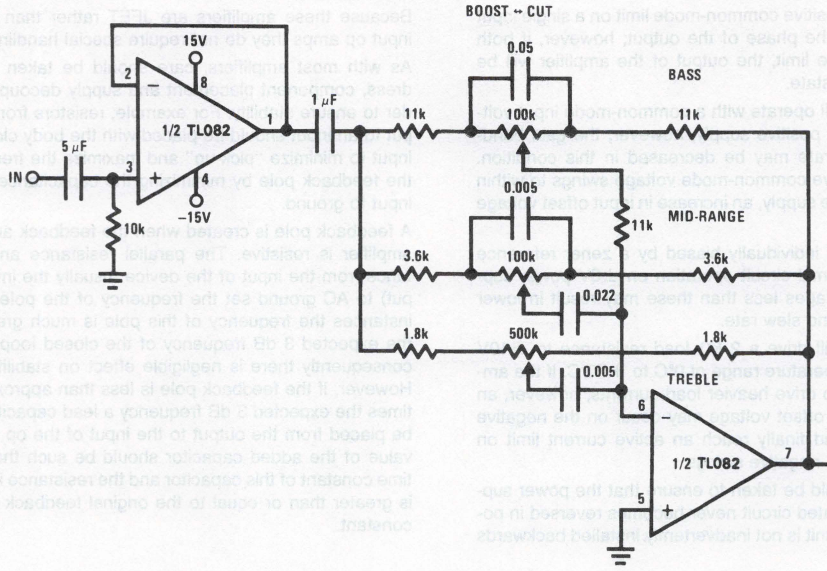
## Detailed Schematic



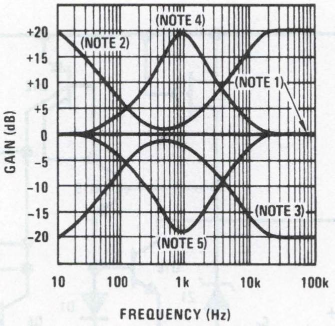
TL/H/8357–11

## Typical Applications

### Three-Band Active Tone Control


BOOST ↔ CUT
0.05
BASS
15V
8
2
1 µF
1
1/2 TL082
11k
100k
11k
5 µF
3
IN
+
4
−15V
0.005
11k
MID-RANGE
10k
3.6k
100k
3.6k
0.022
1.8k
500k
1.8k
0.005
TREBLE
6
1/2 TL082
7
OUT
5
+

TL/H/8357-12



TL/H/8357-13

**Note 1:** All controls flat.

**Note 2:** Bass and treble boost, mid flat.

**Note 3:** Bass and treble cut, mid flat.

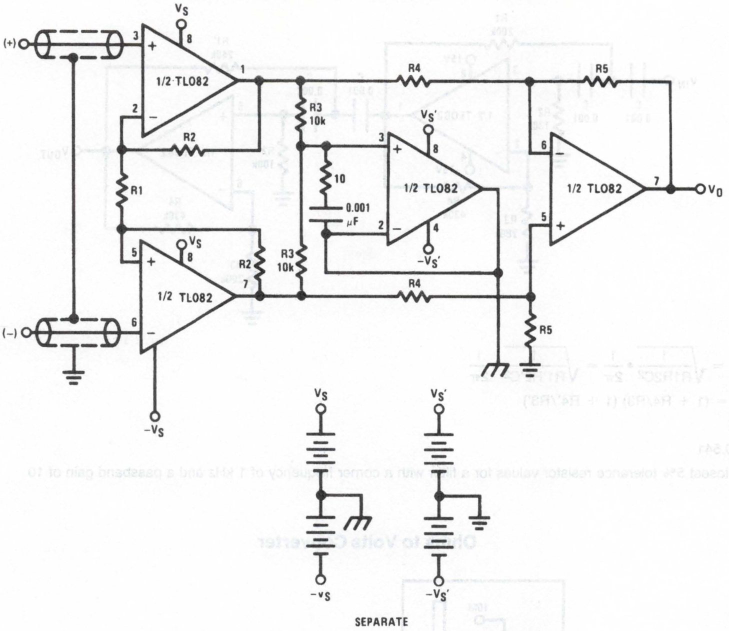
**Note 4:** Mid boost, bass and treble flat.

**Note 5:** Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

## Typical Applications (Continued)

### Improved CMRR Instrumentation Amplifier


VS
(+)
3
8
+
1
1/2 TL082
2
−
R2
R1
R4
R5
R3
10k
VS'
3
+
8
10
6
−
1/2 TL082
1/2 TL082
7
VO
0.001
μF
2
−
4
5
+
−VS'
5
+
VS
8
R2
R3
10k
7
R4
1/2 TL082
R5
6
(−)
−
−VS
VS
VS'
−VS
−VS'
SEPARATE

TL/H/8357–14

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

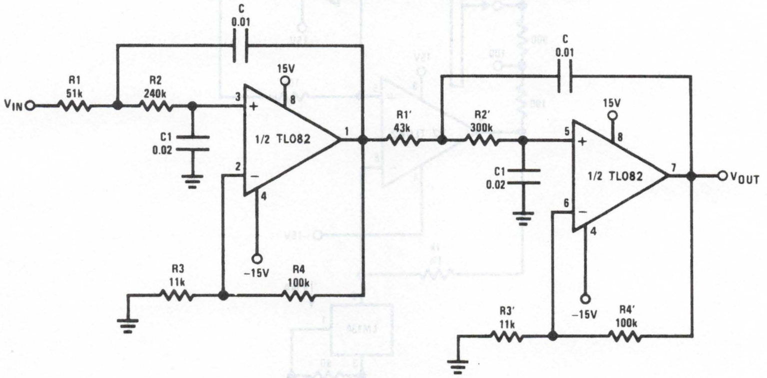
$\not\perp$ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With $A_{V_T}$ = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

### Fourth Order Low Pass Butterworth Filter

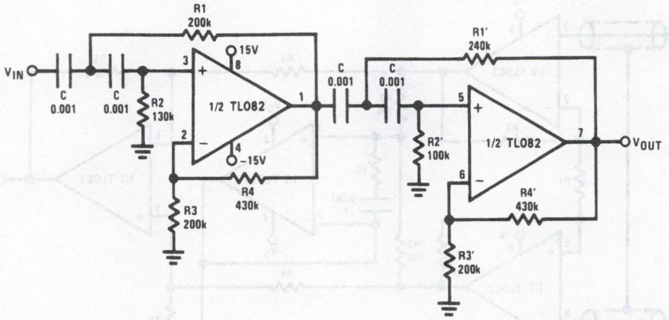

C
0.01
R1
51k
R2
240k
VIN
15V
3
+
8
C1
0.02
1/2 TL082
1
2
−
4
−15V
R3
11k
R4
100k
R1'
43k
R2'
300k
C
0.01
15V
5
+
8
C1
0.02
1/2 TL082
7
VOUT
6
−
4
−15V
R3'
11k
R4'
100k

TL/H/8357–15

- Corner frequency ($f_c$) = $\sqrt{\dfrac{1}{R1R2CC1}} \bullet \dfrac{1}{2\pi} = \sqrt{\dfrac{1}{R1'R2'CC1}} \bullet \dfrac{1}{2\pi}$
- Passband gain ($H_O$) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

## Typical Applications (Continued)

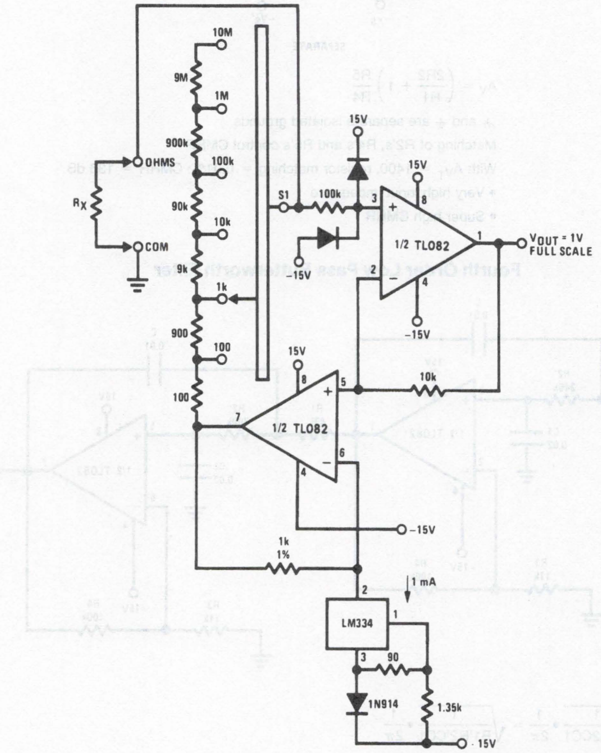
### Fourth Order High Pass Butterworth Filter


R1
200k
15V
3
8
$V_{IN}$
C
0.001
C
0.001
R2
130k
1/2 TL082
1
2
4
−15V
R4
430k
R3
200k
C
0.001
C
0.001
R1'
240k
5
R2'
100k
1/2 TL082
7
$V_{OUT}$
6
R4'
430k
R3'
200k

TL/H/8357-16

- Corner frequency ($f_C$) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain ($H_O$) = $(1 + R4/R3)\,(1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

### Ohms to Volts Converter


10M
9M
1M
900k
OHMS
100k
$R_X$
90k
10k
COM
9k
1k
900
100
100
15V
15V
S1
100k
3
8
1/2 TL082
1
$V_{OUT}$ = 1V FULL SCALE
−15V
2
4
−15V
15V
8
5
7
1/2 TL082
6
10k
4
−15V
1k
1%
2
1 mA
LM334
1
3
90
1N914
1.35k
· 15V

TL/H/8357-17

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where $R_{LADDER}$ is the resistance from switch S1 pole to pin 7 of the TL082CP.

# Section 3

# Buffers

## Section 3 Contents

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***Devices Not Covered In Last Publication**

National Semiconductor Corporation

# Buffers
# Definition of Terms

**Bandwidth:** That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

**Common-Mode Rejection Ratio:** The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

**Harmonic Distortion:** That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\%\ \text{harmonic distortion} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

**Input Bias Current:** The average of the two input currents.

**Input Common-Mode Voltage Range:** The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

**Input Impedance:** The ratio of input voltage to input current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Input Offset Current:** The difference in the currents into the two input terminals when the output is at zero.

**Input Offset Voltage:** That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Input Voltage Range:** The range of voltages on the input terminals for which the amplifier operates within specifications.

**Large-Signal Voltage Gain:** The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**Output Impedance:** The ratio of output voltage to output current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Output Resistance:** The small signal resistance seen at the output with the output voltage near zero.

**Output Voltage Swing:** The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Offset Voltage Temperature Drift:** The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

**Power Supply Rejection:** The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Settling Time:** The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**Slew Rate:** The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

**Supply Current:** The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

**Transient Response:** The closed-loop step-function response of the amplifier under small-signal conditions.

**Unity Gain Bandwidth:** The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

**Voltage Gain:** The ratio of output voltage to input voltage under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

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# Buffers Selection Guide (Notes 1 and 2)

| Device Type | −3 dB MHz (Typ) | $V_{OS}$ mV (Max) | $I_S$ mA (Max) | Voltage Gain (Typ) | $V_{OUT}$ V (Min) | S. R. V/µs (Typ) | $I_{OUT}$ mA (Typ) |
|---|---|---|---|---|---|---|---|
| LM110, 210, 310 | 20 | 7.5 | 5.5 | 0.9999 | ±10 | 3.0 | 10 |
| LH4001 | 25 | 500 | 10 | 0.97 | ±10 | 125 | 200 |
| LH0002 | 30 | ±30 | 10 | 0.97 | ±10 | 100 | 200 |
| LH0033 | 100 | 20 | 24 | 0.98 | ±9 | 1400 | 100 |
| LH4002 | 200 | 50 | 35 | 0.85 | ±3 | 1250 | 40 |
| LH0063 | 200 | ±50 | 65 | 0.93 | ±10 | 2400 | 250 |

*Not specified

**Note 1:** Datasheet should be referred to for test conditions and more detailed information.

**Note 2:** 200°C Temp Range Parts are available. Consult local sales office for information.

**National Semiconductor Corporation**

# LH0002/LH0002C Current Amplifier

## General Description

The LH0002/LH0002C is a general purpose current amplifier.

## Features

- High input impedance 400 kΩ
- Low output impedance 6Ω
- High power efficiency
- Low harmonic distortion
- DC to 30 MHz bandwidth
- Output voltage swing that approaches supply voltage
- 400 mA pulsed output current
- Slew rate is typically 200 V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

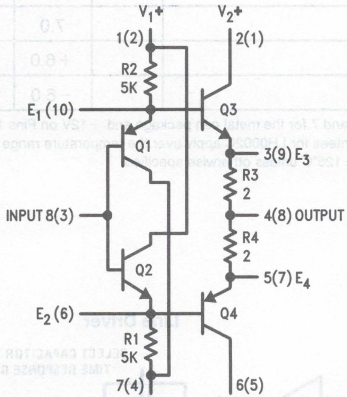
The LH0002 is available in an 8-lead low-profile TO-5 header and a 20-pin leadless chip carrier; the LH0002C is also available in an 8-lead TO-5, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

## Applications

- Line driver
- 30 MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

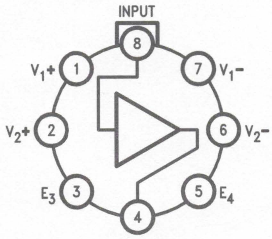
## Schematic and Connection Diagrams


$V_1$+
$V_2$+
1(2)
2(1)
R2
5K
$E_1$(10)
Q3
Q1
3(9) $E_3$
R3
2
INPUT 8(3)
4(8) OUTPUT
R4
2
Q2
5(7) $E_4$
$E_2$(6)
Q4
R1
5K
7(4)
6(5)
$V_1$−
$V_2$−

TL/H/5560-1

Pin numbers in parentheses denote pin connections for dual-in-line package.

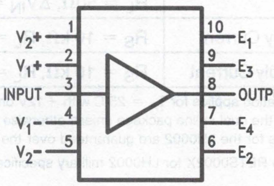
**Metal Can Package**


INPUT
8
$V_1$+
1
7
$V_1$−
$V_2$+
2
6
$V_2$−
$E_3$
3
5
$E_4$
4
OUTPUT

TL/H/5560-3

**Order Number LH0002H or LH0002CH**
**See NS Package Number H08D**

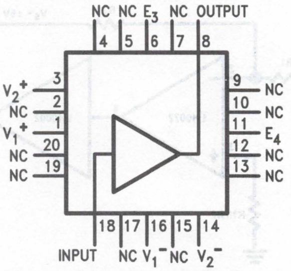
**Dual-In-Line Package**


$V_2$+
1
10
$E_1$
$V_1$+
2
9
$E_3$
INPUT
3
8
OUTPUT
$V_1$−
4
7
$E_4$
$V_2$−
5
6
$E_2$

TL/H/5560-2

**Order Number LH0002CN**
**See NS Package Number N10A**

**Leadless Chip Carrier**


NC
NC
$E_3$
NC
OUTPUT
4
5
6
7
8
$V_2$+
3
NC
2
$V_1$+
1
NC
20
NC
19
9
NC
10
NC
11
$E_4$
12
NC
13
NC
18
17
16
15
14
INPUT
NC
$V_1$−
NC
$V_2$−

TL/H/5560-6

**Order Number LH0002E**
**See NS Package Number E20A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 2)**

| | |
|---|---|
| Supply Voltage | ±22V |
| Power Dissipation Ambient | 600 mW |
| Input Voltage | (Equal to Power Supply Voltage) |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | |
| LH0002 | −55°C to +125°C |
| LH0002C | 0°C to +85°C |
| Steady State Output Current | ±100 mA |
| Pulsed Output Current (50 ms On/1 sec. Off) | ±400 mA |
| Lead Temperature Soldering (10 seconds) | |
| Metal Can | 300°C |
| Plastic | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Note 1)

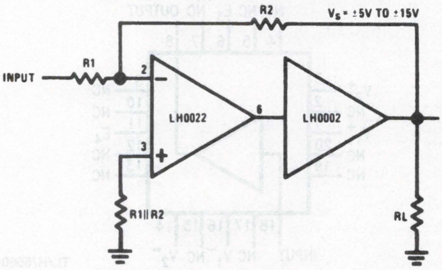
| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Voltage Gain | $R_S = 10\ k\Omega, R_L = 1.0\ k\Omega, V_{IN} = \pm 10V$ | 0.95 | 0.97 | | |
| AC Current Gain | $V_{IN} = 1.0$ Vrms, f = 1.0 kHz | | 40 | | A/mA |
| Input Impedance | $R_S = 200\ k\Omega, V_{IN} = \pm 1.0V, R_L = 1.0\ k\Omega$ | 180 | 400 | | kΩ |
| Output Impedance | $V_{IN} = \pm 1.0V, R_L = 50\Omega, R_S = 10\ k\Omega$ | | 6.0 | 10 | Ω |
| Output Voltage Swing | $R_L = 1.0\ k\Omega, V_{IN} = \pm 12V$ | ±10 | ±11 | | V |
| Output Voltage Swing | $V_S = \pm 15V, V_{IN} = \pm 12V, R_S = 50\Omega, R_L = 100\Omega, T_A = 25°C$ | ±10 | | | V |
| DC Output Offset Voltage | $R_S = 300\Omega, R_L = 1.0\ k\Omega$ | | ±10 | ±30 | mV |
| DC Input Offset Current | $R_S = 10\ k\Omega, R_L = 1.0\ k\Omega$ | | ±6.0 | ±10 | μA |
| Harmonic Distortion | $V_{IN} = 5.0$ Vrms, f = 1.0 kHz | | 0.1 | | % |
| Rise Time | $R_L = 50\Omega, \Delta V_{IN} = 100$ mV | | 7.0 | 12 | ns |
| Positive Supply Current | $R_S = 10\ k\Omega, R_L = 1.0\ k\Omega$ | | +6.0 | +10 | mA |
| Negative Supply Current | $R_S = 10\ k\Omega, R_L = 1.0\ k\Omega$ | | −6.0 | −10 | mA |

**Note 1:** Specification applies for $T_A = 25°C$ with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to +125°C unless otherwise specified.

**Note 2:** Refer to RETS0002X for LH0002 military specifications.

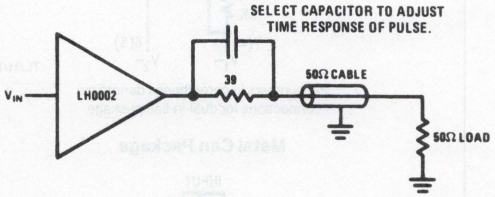
## Typical Applications

**High Current Operational Amplifier**



TL/H/5560-4

**Line Driver**

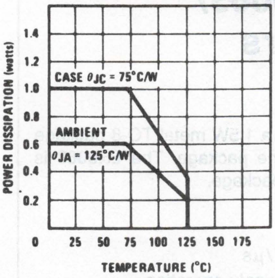


TL/H/5560-5

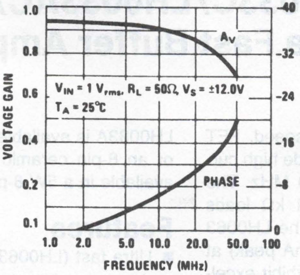
*Previously called NH0002/NH0002C

## Typical Performance Characteristics

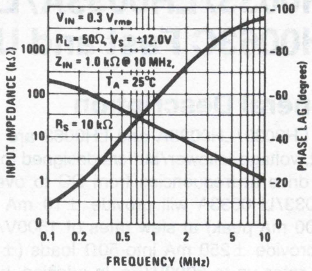
**Maximum Power Dissipation**



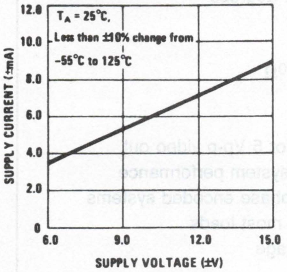
**Frequency Response**



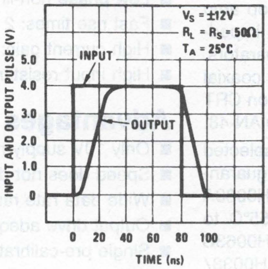
**Input Impedance (Magnitude & Phase)**



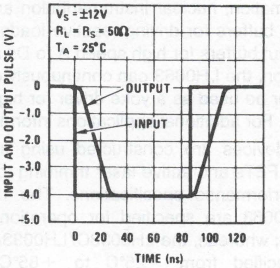
**Supply Current**



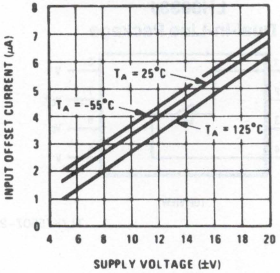
**Positive Pulse**



**Negative Pulse**



**Input Offset Current**



TL/H/5560-7

**National Semiconductor Corporation**

# LH0033/LH0033A/LH0033C/LH0033AC/LH0063/LH0063C Fast and Ultra Fast Buffer Amplifiers

## General Description

The LH0033/LH0033A and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033A will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063 will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033/LH0033A and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C/LH0033AC and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033A is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

## Features

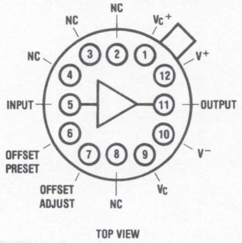
- Ultra fast (LH0063): 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ±10V with 50Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High current gain: 120 dB
- High input resistance: $10^{10}\Omega$

## Advantages

- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

## Connection Diagrams

**LH0033G**
**Metal Can Package**

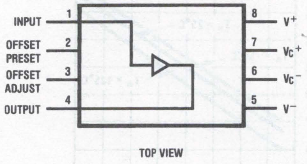

NC
NC
Vc+
NC
3
2
1
V+
4
12
INPUT
5
11
OUTPUT
6
10
OFFSET PRESET
7
8
9
V−
OFFSET ADJUST
NC
Vc
TOP VIEW

TL/K/5507-1

Case is electrically isolated

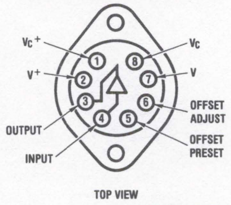
**Order Number LH0033G, LH0033AG, LH0033CG, LH0033ACG, LH0063K, LH0063CK, LH0033J or LH0033CJ**
**See NS Package Number G12B, HY08A or K08A**

**LH0033J**
**Dual-In-Line Package**


INPUT
1
OFFSET PRESET
2
OFFSET ADJUST
3
OUTPUT
4
8
V+
7
Vc+
6
Vc−
5
V−
TOP VIEW

TL/K/5507-2

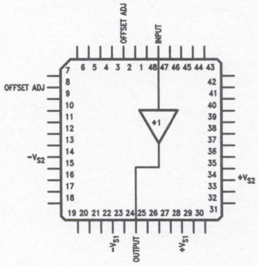
**LH0063K**
**Metal Can Package**


Vc+
Vc
V+
V
1
8
2
7
3
6
4
5
OFFSET ADJUST
OUTPUT
OFFSET PRESET
INPUT
TOP VIEW

TL/K/5507-3

Case is electrically isolated

**Leadless Chip Carrier**


OFFSET ADJ
INPUT
7 6 5 4 3 2 1 48 47 46 45 44 43
OFFSET ADJ
8
9
10
11
12
13
14
−VS2
15
16
17
18
42
41
40
39
38
37
36
35
34
+VS2
33
32
31
+1
19 20 21 22 23 24 25 26 27 28 29 30
−VS1
OUTPUT
+VS1

TL/K/5507-27

**Order Number LH0033E**
**See NS Package Number E48B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Notes 5 & 7)**

| | |
|---|---|
| Supply Voltage ($V^+-V^-$) | 40V |
| Maximum Power Dissipation (See Curves) | |
| LH0063/LH0063C | 5W |
| LH0033A/LH0033AC/LH0033/LH0033C | 1.5W |
| Maximum Junction Temperature | 175°C |
| Input Voltage | $\pm V_S$ |
| Continuous Output Current | |
| LH0063/LH0063C | ±250 mA |
| LH0033A/LH0033AC/LH0033/LH0033C | ±100 mA |
| Peak Output Current | |
| LH0063/LH0063C | ±500 mA |
| LH0033A/LH0033AC/<br>LH0033/LH0033C | ±250 mA |
| Operating Temperature Range | |
| LH0033A/LH0033 and LH0063 | −55°C to +125°C |
| LH0033AC/LH0033C and LH0063C | −25°C to +85°C |
| Storage Temperature Range | −65° to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |
| ESD rating to be determined. | |

## DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified, (Note 1)

| Parameter | Conditions | LH0033A | | | LH0033AC | | | LH0033 | | | LH0033C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Offset Voltage | $R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2) | | 1 | 5 | | 6 | 15 | | 5.0 | 10 | | 12 | 20 | mV |
| | $R_S = 100\Omega$ | | | 10 | | | 20 | | | 15 | | | 25 | mV |
| Average Temperature Coefficient of Offset Voltage | $R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3) | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | μV/°C |
| Input Bias Current | $V_{IN} = 0V$ | | | | | | | | | | | | | |
| | $T_J = 25°C$ (Note 2) | | | 100 | | | 250 | | | 250 | | | 500 | pA |
| | $T_A = 25°C$ (Note 4) | | | 1.5 | | | 2.5 | | | 2.5 | | | 5.0 | nA |
| | $T_J = T_A = T_{MAX}$ | | | 7.5 | | | 10 | | | 10 | | | 20 | nA |
| Voltage Gain | $V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$ | 0.97 | 0.98 | 1.00 | 0.96 | 0.98 | 1.00 | 0.97 | 0.98 | 1.00 | 0.96 | 0.98 | 1.00 | V/V |
| Input Impedance | $R_L = 1\ k\Omega$ | $10^{10}$ | $10^{11}$ | | $10^{10}$ | $10^{11}$ | | $10^{10}$ | $10^{11}$ | | $10^{10}$ | $10^{11}$ | | Ω |
| Output Impedance | $V_{IN} = \pm 1.0V$, $R_L = 1.0k$ | | 6.0 | 10 | | 6.0 | 10 | | 6.0 | 10 | | 6.0 | 10 | Ω |
| Output Voltage Swing | $V_I = \pm 14V$, $R_L = 1.0k$ | ±12 | | | ±12 | | | ±12 | | | ±12 | | | V |
| | $V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$ | ±9.0 | | | ±9.0 | | | ±9.0 | | | ±9.0 | | | V |
| Supply Current | $V_{IN} = 0V$ (Note 5) | | 20 | 22 | | 21 | 24 | | 20 | 22 | | 21 | 24 | mA |
| Power Consumption | $V_{IN} = 0V$ | | 600 | 660 | | 630 | 720 | | 600 | 660 | | 630 | 720 | mW |

## AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ K\Omega$ (Note 6)

| Parameter | Conditions | LH0033A | | | LH0033AC | | | LH0033 | | | LH0033C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | $V_{IN} = \pm 10V$ | 1000 | 1500 | | 1000 | 1400 | | 1000 | 1500 | | 1000 | 1400 | | V/μs |
| Bandwidth | $V_{IN} = 1.0$ Vrms | | 100 | | | 100 | | | 100 | | | 100 | | MHz |
| Phase Non-Linearity | BW = 1.0Hz to 20 MHz | | 2.0 | | | 2.0 | | | 2.0 | | | 2.0 | | degrees |
| Rise Time | $\Delta V_{IN} = 0.5V$ | | 2.9 | | | 3.2 | | | 2.9 | | | 3.2 | | ns |
| Propagation Delay | $\Delta V_{IN} = 0.5V$ | | 1.2 | | | 1.5 | | | 1.2 | | | 1.5 | | ns |
| Harmonic Distortion | f > 1 kHz | | <0.1 | | | <0.1 | | | <0.1 | | | <0.1 | | % |

**Note 1:** LH0033 and LH0033A are 100% production tested as specified at 25° C, 125°C, and−55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

**Note 2:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, $V_{OS}$ may change one to several mV, and $I_B$ will change significantly during warm-up. Refer to $I_B$ vs temperature graph for expected values.

**Note 3:** LH0033 and LH0033A are 100% production tested for this parameter. LH0033AC/C are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and $T_{MAX}$.

**Note 4:** Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

**Note 5:** Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

**Note 6:** Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

**Note 7:** Refer to RETS0033AG for the LH0033AG and RETS0033G for the LH0033G military specifications.

## DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 1)

| Parameter | Conditions | LH0063 | | | LH0063C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Offset Voltage | $R_S \le 100 k\Omega$, $T_J = 25°C$, $R_L = 100\Omega$ (Note 2) | | 10 | 25 | | 10 | 50 | mV |
| | | | | 100 | | | 100 | mV |
| Average Temperature Coefficient of Output Offset Voltage | $R_S \le 100\ k\Omega$ | | 300 | | | 300 | | $\mu V/°C$ |
| Input Bias Current | $T_J = 25°C$ (Note 2) | | 10 | 30 | | 10 | 30 | nA |
| | | | | 100 | | | 100 | nA |
| Voltage Gain | $V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 1\ k\Omega$ | 0.94 | 0.96 | 1.0 | 0.94 | 0.96 | 1.0 | V/V |
| Voltage Gain | $V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 50\Omega$<br>$T_J = 25°C$ | 0.92 | 0.93 | 0.98 | 0.91 | 0.93 | 0.98 | V/V |
| Input Capacitance | Case Shorted to Output | | 8.0 | | | 8.0 | | pF |
| Output Impedance | $V_{OUT} = \pm 10V$, $R_S \le 100\ k\Omega$, $R_L = 50\Omega$ | | 1.0 | 4.0 | | 1.0 | 4.0 | $\Omega$ |
| Output Current Swing | $V_{IN} = \pm 10V$, $R_S \le 100\ k\Omega$ | 0.2 | 0.25 | | 0.2 | 0.25 | | A |
| Output Voltage Swing | $R_L = 50\Omega$ | ±10 | ±13 | | ±10 | ±13 | | V |
| Output Voltage Swing | $V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$ | 5.0 | 7.0 | | 5.09 | 7.0 | | Vp-p |
| Supply Current | $T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$ (Note 3) | | 35 | 65 | | 35 | 65 | mA |
| Supply Current | $V_S = \pm 5.0V$ (Note 3) | | 50 | | | 50 | | mA |
| Power Consumption | $T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$ | | 1.05 | 1.95 | | 1.05 | 1.95 | W |
| Power Consumption | $V_S = \pm 5.0V$ | | 500 | | | 500 | | mW |

## AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 4)

| Parameter | Conditions | LH0063 | | | LH0063C | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | $R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$ | | 6000 | | | 6000 | | $V/\mu s$ |
| Slew Rate | $R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$ | 2000 | 2400 | | 2000 | 2400 | | $V/\mu s$ |
| Bandwidth | $V_{IN} = 1.0$ Vrms | | 200 | | | 200 | | MHz |
| Phase Non-Linearity | BW = 1.0 Hz to 20 MHz | | 2.0 | | | 2.0 | | degrees |
| Rise Time | $\Delta V_{IN} = 0.5V$ | | 1.6 | | | 1.9 | | ns |
| Propagation Delay | $\Delta V_{IN} = 0.5V$ | | 1.9 | | | 2.1 | | ns |
| Harmonic Distortion | | | <0.1 | | | <0.1 | | % |

**Note 1:** LH0063 is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

**Note 2:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, $V_{OS}$ may change one to several mV, and $I_B$ ans $I_{OS}$ will change significantly during warm-up. Refer to $I_B$ and $I_{OS}$ vs temperature graph for expected values.

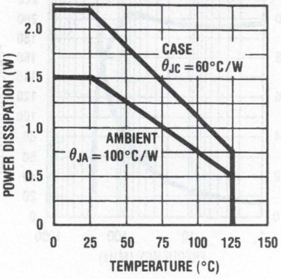
**Note 3:** Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

**Note 4:** Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

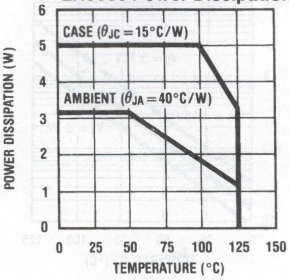
**Note 5:** Refer to RETS0063K for the LH0063K military specifications.

## Typical Performance Characteristics

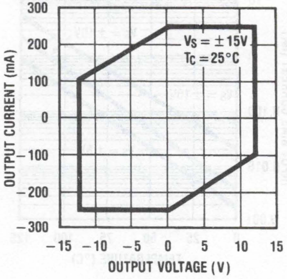
### LH0033 Power Dissipation



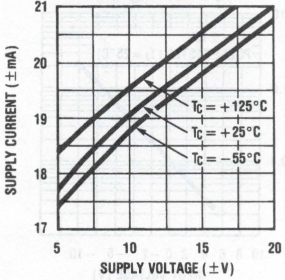
### LH0063 Power Dissipation



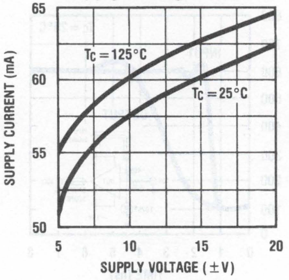
### LH0063 DC Safe Operating Area



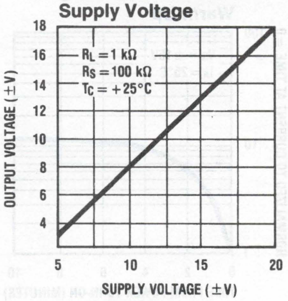
### LH0033 Supply Current vs Supply Voltage



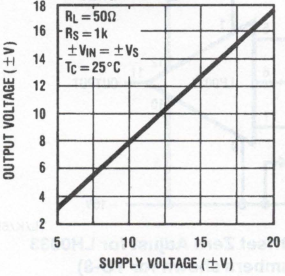
### LH0063 Supply Current vs Supply Voltage



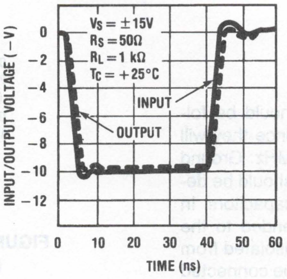
### LH0033 Output Voltage vs Supply Voltage



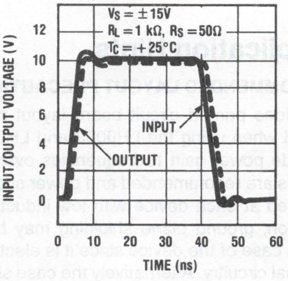
### LH0063 Output Voltage vs Supply Voltage



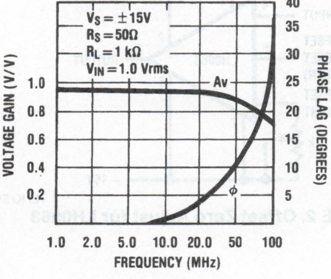
### LH0033 Negative Pulse Response



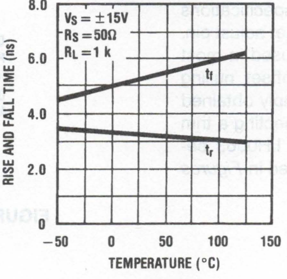
### LH0033 Positive Pulse Response



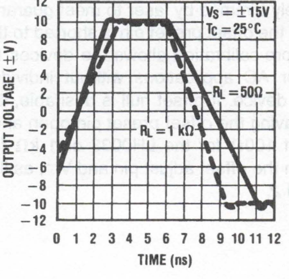
### LH0033 Frequency Response



### LH0033 Rise and Fall Time vs Temperature



### LH0063 Large Signal Pulse Response



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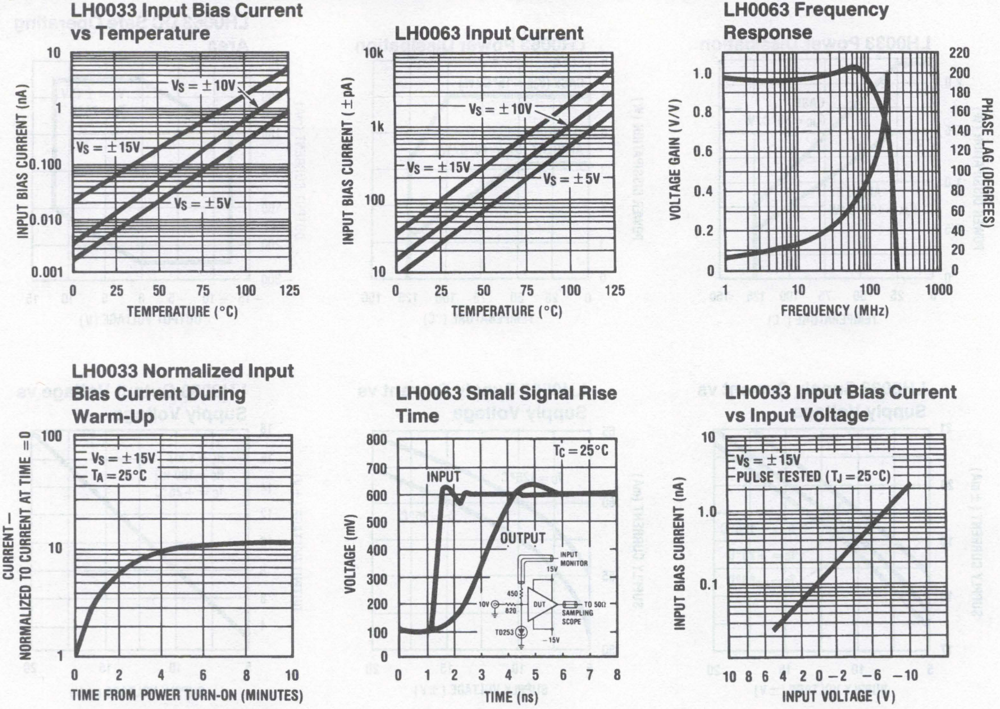
## Typical Performance Characteristics (Continued)



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## Application Hints

### RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

### OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V−, as illustrated in *Figures 1* and *2*.

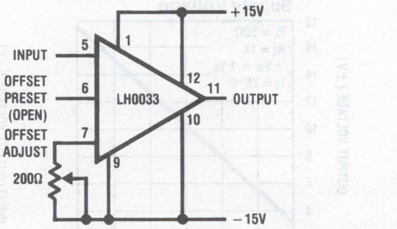
+15V
INPUT
5
1
OFFSET PRESET (OPEN)
6
12
11
LH0033
OUTPUT
10
OFFSET ADJUST
7
9
200Ω
−15V

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**FIGURE 1. Offset Zero Adjust for LH0033 (Pin numbers shown for TO-8)**

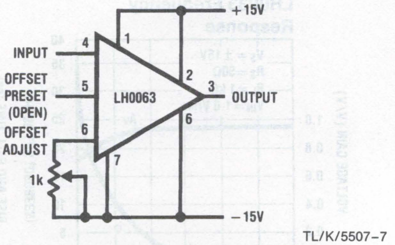
+15V
INPUT
4
1
OFFSET PRESET (OPEN)
5
2
3
LH0063
OUTPUT
6
OFFSET ADJUST
6
7
1k
−15V

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**FIGURE 2. Offset Zero Adjust for LH0063**

## Application Hints (Continued)

### OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1-A_V)\frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

$A_V$ = No load voltage gain, typically 0.99

$V^+$ = Positive supply voltage

$V^-$ = Negative supply voltage

For the above example, $\Delta V_O$ would be −35mV. This may be adjusted to zero as described in *Figure 2.* For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

### SHORT CIRCUIT PROTECTION

In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between $V^+$ and $V_C^+$ pins and $V^-$ and $V_C^-$ pins as illustrated in *Figures 3 and 4.* Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where:

$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

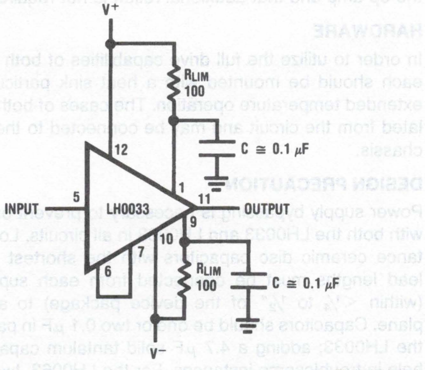

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**FIGURE 3. LH0033 Using Resistor Current Limiting**

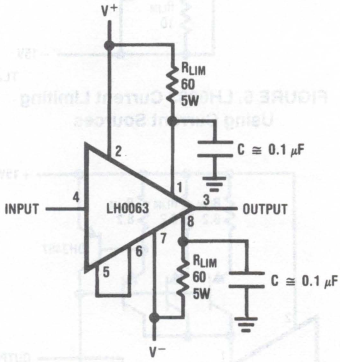

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**FIGURE 4. LH0063 Using Resistor Current Limiting**

## Application Hints (Continued)

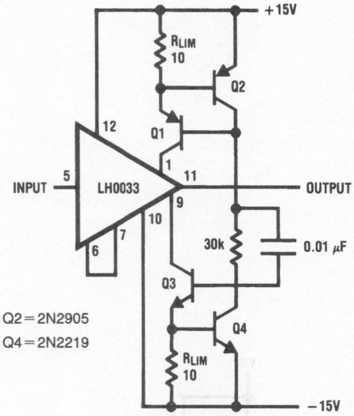
The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling $V_C+$ and $V_C-$ pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5* and *6*. In *Figures 5* and *6*, the current sources are saturated during normal operation, thus apply full supply voltage to the $V_C$ pins. Under fault conditions, the voltage decreases as required by the overload.

For *Figure 5:*

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\ mA} = 10\Omega$$

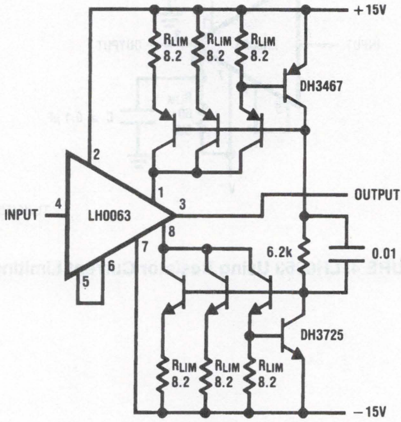
In *Figure 6*, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200\ mA)} = 8.2\Omega$$



TL/K/5507–10

**FIGURE 5. LH0033 Current Limiting Using Current Sources**



TL/K/5507–11

**FIGURE 6. LH0063 Current Limiting Using Current Sources**

### CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_V/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_D\text{pkg.} \geq P_{DC} + P_{AC}$$

$$P_D\text{pkg.} \geq (V+ - V-) \times I_S + P_{AC}$$

$$P_{AC} \cong (Vp\text{-}p)^2 \times f \times C_L$$

where:

Vp-p = Peak-to-peak output voltage swing
f = Frequency
$C_L$ = Load Capacitance

### OPERATION WITHIN AN OP AMP LOOP

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

### HARDWARE

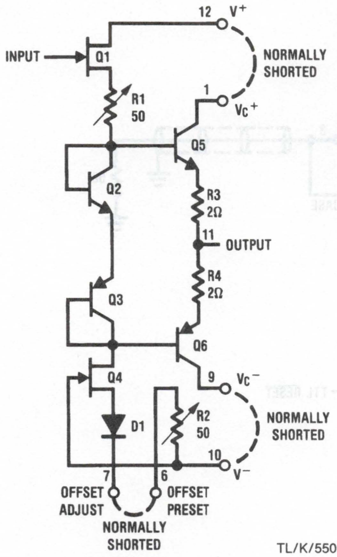
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

### DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within <¼ to ½″ of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel for the LH0033; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel will be necessary on each supply lead.

# Schematic Diagrams

**LH0033/LH0033A**


12
V+
INPUT
Q1
NORMALLY SHORTED
R1 50
1
VC+
Q5
Q2
R3 2Ω
11
OUTPUT
R4 2Ω
Q3
Q6
Q4
9
VC−
D1
R2 50
NORMALLY SHORTED
10
V−
7
6
OFFSET ADJUST
OFFSET PRESET
NORMALLY SHORTED

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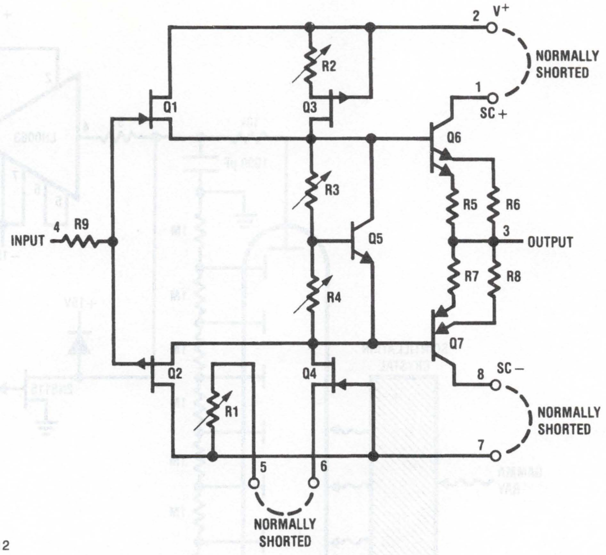
**LH0063**

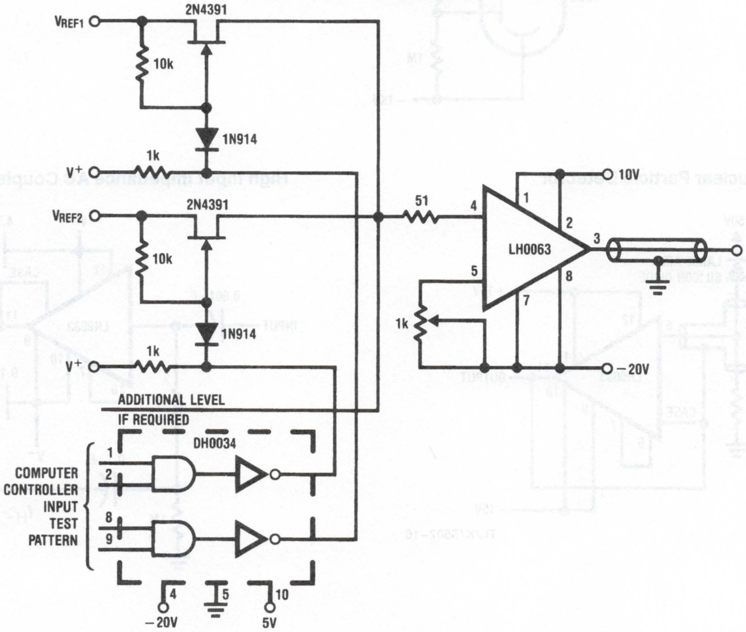

2
V+
NORMALLY SHORTED
R2
Q1
Q3
1
SC+
Q6
R3
R5
R6
INPUT
4
R9
3
OUTPUT
Q5
R7
R8
R4
Q7
Q2
Q4
8
SC−
R1
NORMALLY SHORTED
7
5
6
NORMALLY SHORTED

TL/K/5507-13

Pin numbers shown for TO-8 ("G") package.

# Typical Applications

### High Speed Automatic Test Equipment Forcing Function Generator


VREF1
2N4391
10k
1N914
1k
V+
VREF2
2N4391
10k
1N914
1k
V+
ADDITIONAL LEVEL IF REQUIRED
DH0034
1
2
8
9
COMPUTER CONTROLLER INPUT TEST PATTERN
4
−20V
5
10
5V
51
4
1
10V
2
LH0063
3
5
8
7
1k
−20V

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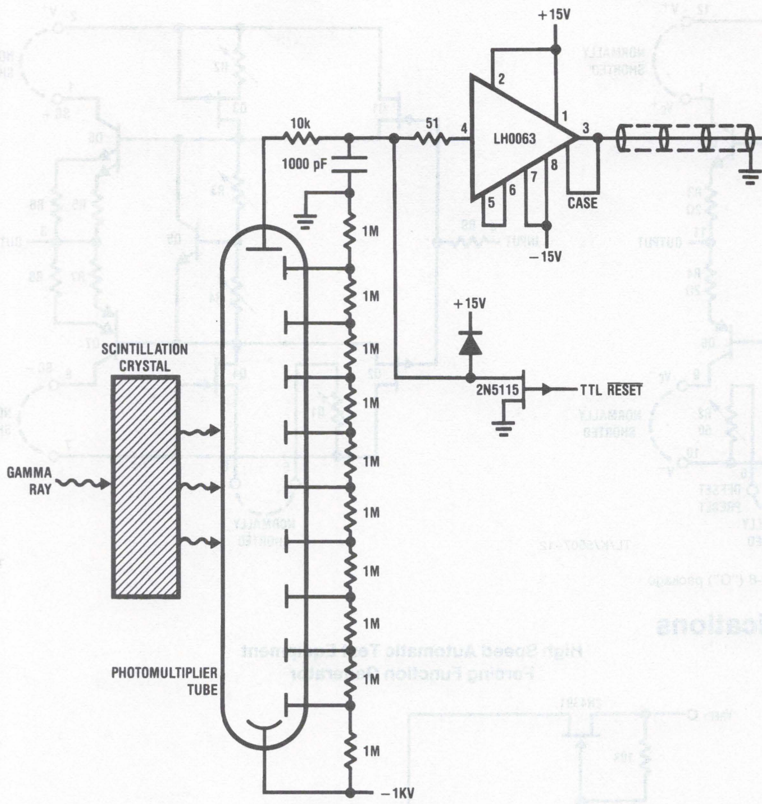
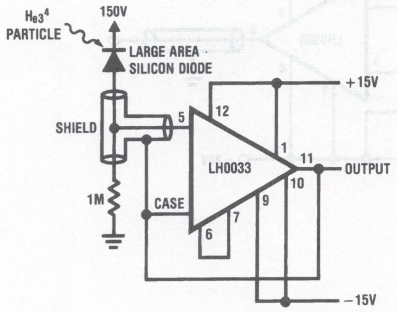
## Typical Applications (Continued)

### Gamma Ray Pulse Integrator


+15V
2
1
3
4
LH0063
10k
51
1000 pF
5
6
7
8
CASE
−15V
50
+15V
2N5115
TTL RESET
1M
1M
1M
1M
1M
1M
1M
1M
1M
1M
SCINTILLATION CRYSTAL
GAMMA RAY
PHOTOMULTIPLIER TUBE
−1KV

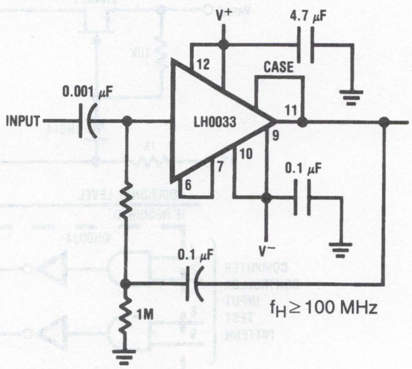
TL/K/5507–15

### Nuclear Particle Detector


$He_3^4$ PARTICLE
150V
LARGE AREA SILICON DIODE
SHIELD
1M
5
12
1
11
10
9
7
6
LH0033
CASE
+15V
OUTPUT
−15V

TL/K/5507–16

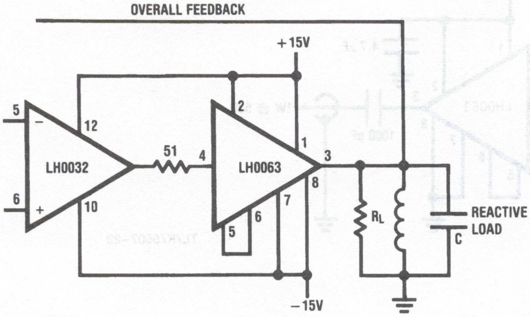
### High Input Impedance AC Coupled Amplifier


V+
4.7 µF
12
CASE
0.001 µF
INPUT
LH0033
11
9
10
7
6
0.1 µF
V−
0.1 µF
1M
$f_H \geq 100$ MHz

TL/K/5507–17

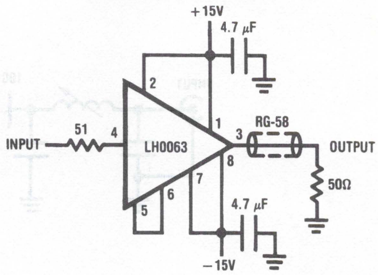
## Typical Applications (Continued)

### Isolation Buffer


OVERALL FEEDBACK
+15V
5
6
−
+
LH0032
12
10
51
4
2
LH0063
1
3
8
7
6
5
RL
REACTIVE LOAD
C
−15V

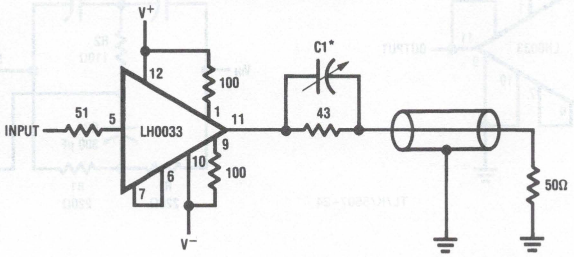
TL/K/5507–18

### Coaxial Cable Driver


+15V
4.7 µF
2
INPUT
51
4
LH0063
1
3
RG-58
OUTPUT
8
7
6
5
50Ω
4.7 µF
−15V

TL/K/5507–19

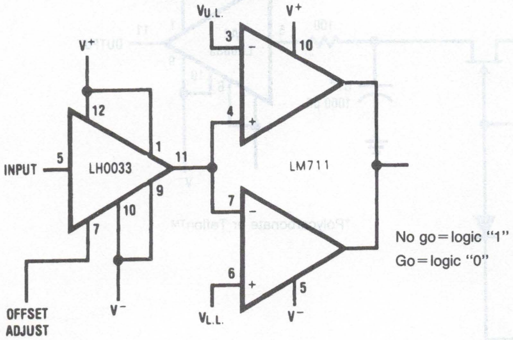
### Coaxial Cable Driver


V+
12
100
C1*
INPUT
51
5
LH0033
1
11
43
9
10
100
6
7
50Ω
V−

TL/K/5507–20

*Select C1 for optimum pulse response

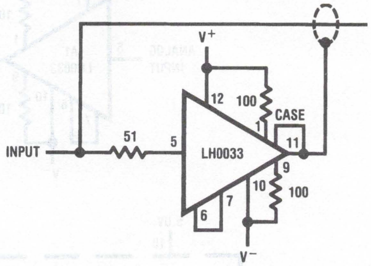
### High Input Impedance Comparator with Offset Adjust


VU.L.
V+
3
−
10
V+
4
+
12
LM711
INPUT
5
LH0033
1
11
9
7
−
10
7
6
+
5
OFFSET ADJUST
V−
VL.L.
V−

No go = logic "1"
Go = logic "0"

TL/K/5507–21

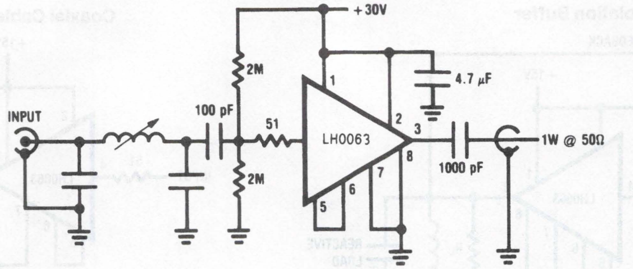
### Instrumentation Shield/Line Driver


V+
12
100
CASE
1
INPUT
51
5
LH0033
11
9
10
100
7
6
V−

TL/K/5507–22

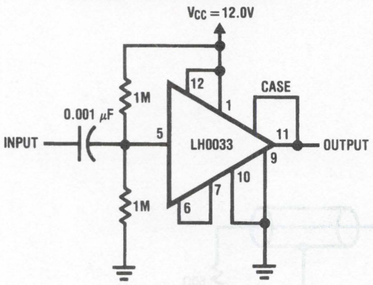
## Typical Applications (Continued)

### 1W CW Final Amplifier


+30V
2M
1
4.7 μF
INPUT
100 pF
51
LH0063
2
3
8
1W @ 50Ω
1000 pF
2M
7
6
5

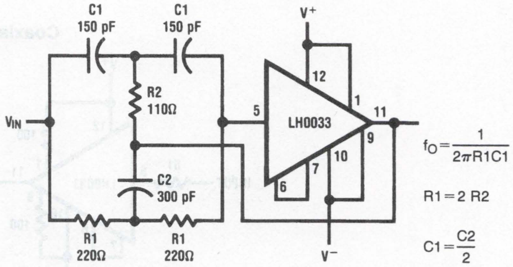
TL/K/5507-23

### Single Supply AC Amplifier


$V_{CC}$ = 12.0V
12
1M
CASE
0.001 μF
1
INPUT
5
LH0033
11
OUTPUT
9
10
7
1M
6

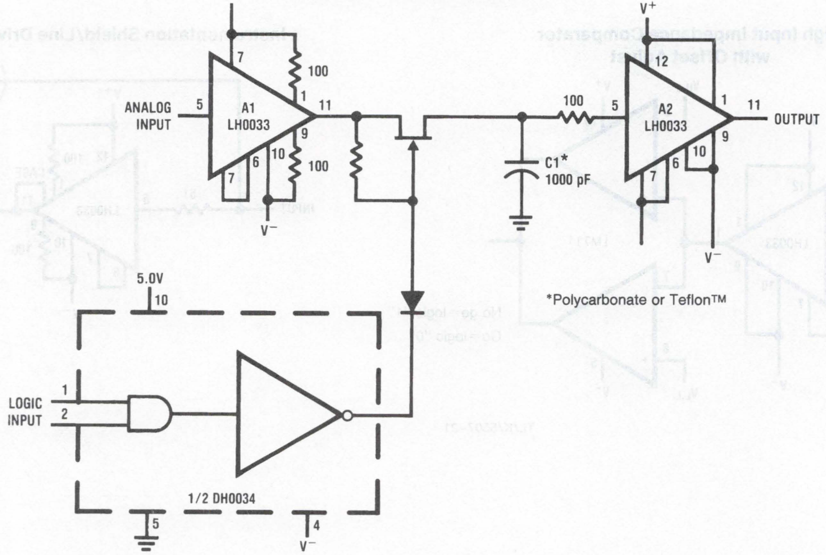
TL/K/5507-24

### 4.5 MHz Notch Filter


C1
150 pF
C1
150 pF
V+
12
R2
110Ω
5
LH0033
1
11
$V_{IN}$
9
C2
300 pF
10
7
6
R1
220Ω
R1
220Ω
V−
$f_O = \frac{1}{2\pi R1C1}$
R1 = 2 R2
$C1 = \frac{C2}{2}$

TL/K/5507-25

### High Speed Sample and Hold


V+
7
100
ANALOG INPUT
5
A1
LH0033
1
11
9
6
10
100
7
V−
V+
12
100
5
A2
LH0033
1
11
OUTPUT
9
10
6
7
V−
C1*
1000 pF
5.0V
10
LOGIC INPUT
1
2
1/2 DH0034
5
4
V−

*Polycarbonate or Teflon™

TL/K/5507-26

**National Semiconductor Corporation**

# LH4001 Wideband Current Buffer

## General Description

The LH4001 is a high speed unity gain buffer designed to provide high current drive capability at frequencies from DC to over 25 MHz. It is capable of providing a continuous output current of ±100 mA and a peak of ±200 mA.

The LH4001 is designed to fulfill a wide range of applications such as impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high speed line drivers. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased to ±100 mA.

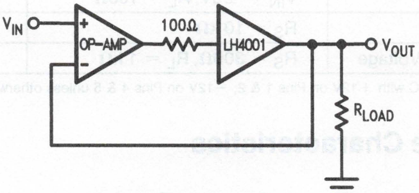
## Features

- DC to 25 MHz bandwidth
- 125 V/μs slew rate
- Drives ±10V into 50Ω
- Operates from ±5 to ±20V supplies
- Output swing approaches supply voltage

## Applications

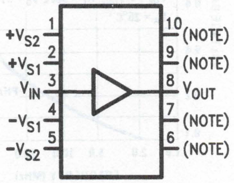
- Boost op amp output
- Buffer amplifiers
- Isolate capacitive loads
- Drive long cables

## Typical Applications and Connection Diagram



TL/K/8628-1

**Dual-In-Line Package**



TL/K/8628-2

**Top View**

***Note:** Electrically connected internally. No connection should be made to these pins.

**Order Number LH4001CN**
**See NS Package Number N10A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±22V |
| Continuous Output Current, $I_O$ | ±100 mA |
| Peak Output Current, $I_{O(peak)}$ (50 ms On/1 Sec Off) | ±200 mA |
| Input Voltage Range, $V_{IN}$ | $\pm V_S$ |
| Power Dissipation Ambient | 500 mW |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Operating Temperature Range, $T_A$ | 0°C to +70°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temp. (Soldering, <10 seconds) | 260°C |

ESD rating is to be determined.

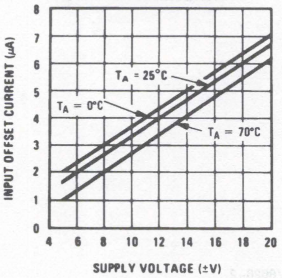
## Electrical Characteristics (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $A_V$ | Voltage Gain | $R_S = 10\ k\Omega, R_L = 1\ k\Omega$<br>$V_{IN} = \pm 10V$ | 0.95 | 0.97 | 1 | V/V |
| $R_{IN}$ | Input Impedance | $R_S = 200\ k\Omega, R_L = 1\ k\Omega$<br>$V_{IN} = \pm 1.0V$ | 180 | 400 | | kΩ |
| $R_{OUT}$ | Output Impedance | $R_S = 10\ k\Omega, R_L = 50\Omega$<br>$V_{IN} = \pm 1.0V$ | | 6 | 10 | Ω |
| $V_O$ | Output Swing | $V_S = \pm 15V, R_S = 50\Omega$<br>$R_L = 1\ k\Omega, V_{IN} = \pm 12V$ | ±10 | ±11 | | V |
| $I_B$ | Input Bias Current | $R_S = 10\ k\Omega, R_L = 1\ k\Omega$ | | ±10 | ±50 | μA |
| $t_r$ | Rise Time | $R_L = 100\Omega, \Delta V_{IN} = 100\ mV$ | | 7 | | ns |
| SR | Slew Rate | $V_{IN} = \pm 5V, R_L = 100\Omega$ | | 125 | | V/μs |
| $I_S$ | Supply Current | $R_S = 10\ k\Omega$ | | ±6 | ±10 | mA |
| $V_{OS}$ | DC Output Offset Voltage | $R_S = 300\Omega, R_L = 1\ k\Omega$ | | ±10 | ±50 | mV |

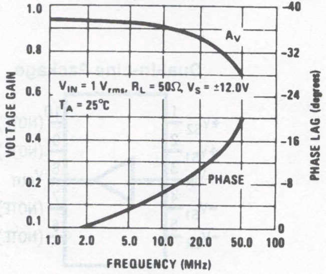
**Note 1:** Specification applies for $T_A = 25°C$ with +12V on Pins 1 & 2; −12V on Pins 4 & 5 unless otherwise specified.

## Typical Performance Characteristics

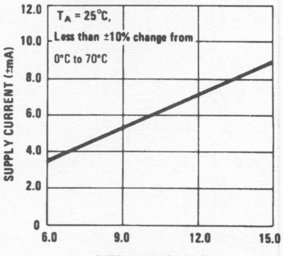
### Input Offset Current



### Frequency Response

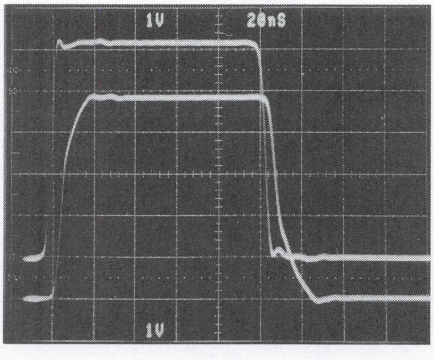


### Supply Current



TL/K/8628–3

### Pulse Response



TL/K/8628–10

$V_{IN} = \pm 2.5V, R_S = R_L = 50\Omega$

## Applications Information

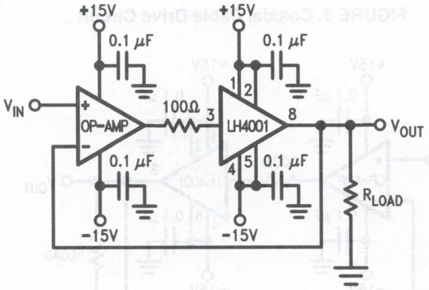
*Figure 1* shows a simple implementation of a non-inverting buffer amplifier of unity gain. Popular industry standard operational amplifiers such as LF156, LF351, LF411, LF441, LM11, LM741, etc. can be used in this configuration. Due to the high bandwidth of the LH4001, it is suitable for use with most monolithic op amps.

*Figure 2* shows an implementation of an inverting amplifier with output current capability in excess of ±100 mA. The gain of this amplifier is determined by the values of $R_F$ and $R_{IN}$. The resistor between the non-inverting input and ground is used to minimize the output offset voltage resulting from the input bias current.

Because of its high current drive capability, the LH4001 buffer amplifier is suitable for driving terminated or unterminated co-axial cables, and high current or reactive loads.

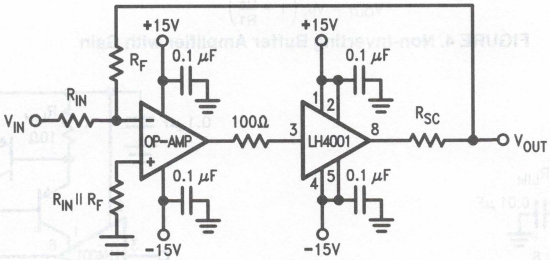
*Figure 3* shows a co-axial cable drive circuit. The 43Ω resistor matches the driving source to the cable, however, its inclusion rarely will result in substantial improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

*Figure 4* shows a non-inverting amplifier with gain and output current capability in excess of ±100 mA. It is capable of providing ±10 mA into a 1 kΩ load or ±100 mA into a 100Ω load (±10V swing). *Figures 5* and *6* show two different methods of providing current limit or short circuit protection for the LH4001. In *Figure 6,* the 10Ω resistor limits the output current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to occur.



TL/K/8628-4

**FIGURE 1. Non-Inverting Buffer Amplifier**

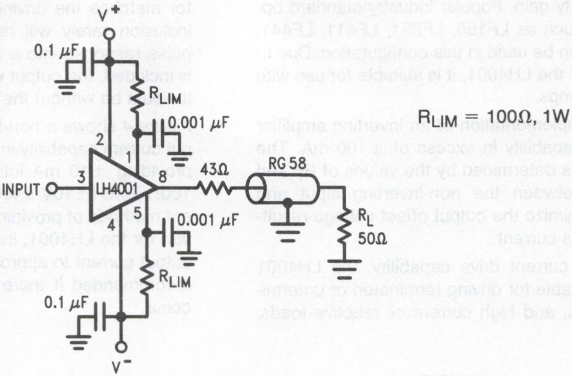


$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$$

TL/K/8628-6

**FIGURE 2. Inverting Buffer Amplifier with Current Limit**

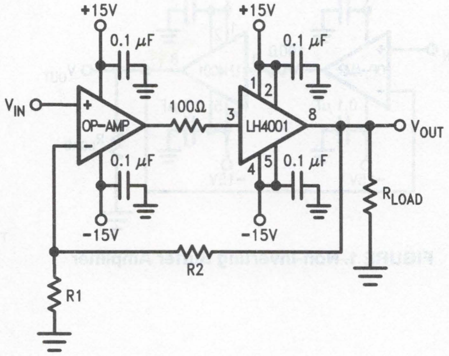
## Applications Information (Continued)


V+
0.1 µF
RLIM
0.001 µF
2
1
INPUT
3
LH4001
8
43Ω
RG 58
4
5
0.001 µF
RL
50Ω
RLIM
0.1 µF
V−

$R_{LIM} = 100\Omega$, 1W

TL/K/8628-7

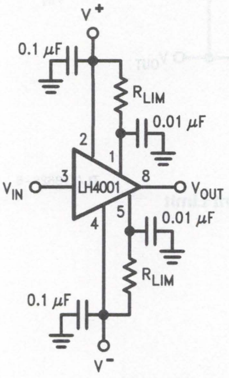
FIGURE 3. Coaxial Cable Drive Circuit


+15V
0.1 µF
+15V
0.1 µF
VIN
+
OP-AMP
−
100Ω
1
2
3
LH4001
8
VOUT
0.1 µF
4
5
0.1 µF
RLOAD
−15V
−15V
R2
R1

TL/K/8628-5

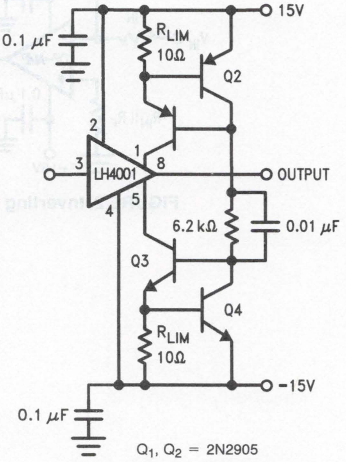
$$V_{OUT} = V_{IN}\left(1 + \frac{R2}{R1}\right)$$

FIGURE 4. Non-Inverting Buffer Amplifier with Gain


V+
0.1 µF
RLIM
0.01 µF
2
1
VIN
3
LH4001
8
VOUT
4
5
0.01 µF
RLIM
0.1 µF
V−

TL/K/8628-8

FIGURE 5. LH4001 Using Resistor Current Limiting


15V
0.1 µF
RLIM
10Ω
Q2
2
1
3
LH4001
8
OUTPUT
5
4
6.2 kΩ
0.01 µF
Q3
Q4
RLIM
10Ω
−15V
0.1 µF

$Q_1$, $Q_2$ = 2N2905

$Q_3$, $Q_4$ = 2N2219

TL/K/8628-9

FIGURE 6. Current Limit Using Current Sources

**National Semiconductor Corporation**

**PRELIMINARY**

# LH4002 Wideband Video Buffer

## General Description

The LH4002 is a high speed voltage follower designed to drive video signals from DC up to 200 MHz. At voltage supplies of ±5V, the LH4002 will provide up to 40 mA into 50Ω at slew rates in excess of 1000 V/µs.

The device is intended to fulfill a wide range of high speed applications including video distribution, impedance transformation, and load isolation. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased.

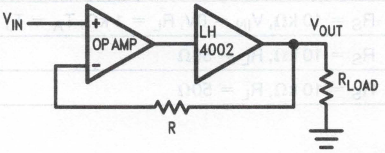
## Features

- DC to 200 MHz Bandwidth with $V_S = \pm 5V$
- 1250 V/µs Slew Rate into 50Ω
- 150 MHz Bandwidth with $V_S = \pm 5V$, $R_L = 50\Omega$ and Voltage Swing $= 2\ V_{P-P}$

## Applications

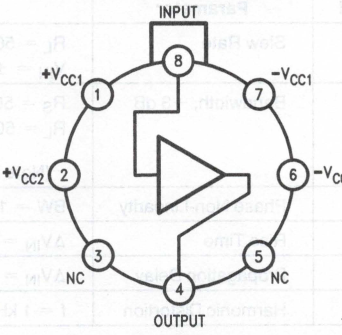
- Wideband Buffer Amplifiers
- Wideband Line Driver

## Typical Applications and Connection Diagrams


$V_{IN}$
OP AMP
+
−
LH 4002
$V_{OUT}$
$R_{LOAD}$
R

TL/K/8686-1

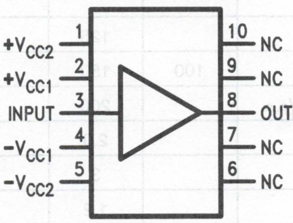
**Metal Can Package**


INPUT
8
$+V_{CC1}$
1
$-V_{CC1}$
7
$+V_{CC2}$
2
6
$-V_{CC2}$
3
NC
5
NC
4
OUTPUT

TL/K/8686-3

**Top View**

**Dual-In-Line Package**

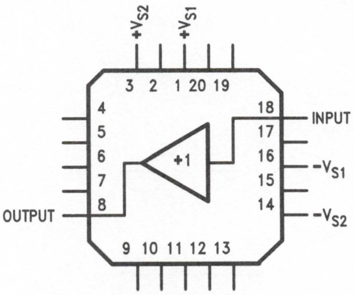

$+V_{CC2}$
1
$+V_{CC1}$
2
INPUT
3
$-V_{CC1}$
4
$-V_{CC2}$
5
10
NC
9
NC
8
OUTPUT
7
NC
6
NC

TL/K/8686-2

**Top View**

**Order Number LH4002CN**
**See NS Package Number N10A**

**Order Number LH4002CH or LH4002H**
**See NS Package Number H08D**


$+V_{S2}$
$+V_{S1}$
3 2 1 20 19
4
5
6
7
8
OUTPUT
+1
18
INPUT
17
16
$-V_{S1}$
15
14
$-V_{S2}$
9 10 11 12 13

TL/K/8686-13

**Order Number LH4002E**
**See NS Package Number E20A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±6V |
| Input Voltage Range, $V_{IN}$ | $\pm V_S$ |
| Continuous Output Current, $I_O$ | ±60 mA |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Operating Temperature Range, $T_A$ | |
| LH4002 | −55°C to +125°C |
| LH4002C | −25°C to +85°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

ESD rating is to be determined.

## DC Electrical Characteristics $V_{CC} = \pm 5V, T_{min} \leq T_A \leq T_{max}$ unless otherwise stated.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $T_A = T_J = 25°C$<br>$R_S = 150\Omega, R_L = 50\Omega$ | | | 20 | 50 | mV |
| $I_B$ | Input Bias Current | $R_S = 1\ k\Omega, R_L = 50\Omega$ | | | 100 | 200 | µA |
| $A_V$ | DC Voltage Gain | $R_S = 10\ k\Omega, R_L = 1.0\ k\Omega, V_{IN} = \pm 2V$ | | 0.95 | 0.97 | | V/V |
| $V_O$ | Output Voltage Swing | $R_S = 150\Omega, V_{IN} = \pm 2.5V$ | $R_L = 1\ k\Omega$ | ±2.2 | ±2.4 | | V |
| | | | $T_A = 25°C, R_L = 50\Omega$ | ±2.0 | ±2.2 | | V |
| $I_S$ | Supply Current | $R_S = 10\ k\Omega, V_{IN} = 0V, R_L = 1\ k\Omega, T_A = T_J = 25°C$ | | | 20 | 35 | mA |
| $R_{OUT}$ | Output Resistance | $R_S = 10\ k\Omega, R_L = 50\Omega$ | | | 6 | 10 | Ω |
| $R_{IN}$ | Input Resistance | $R_S = 10\ k\Omega, R_L = 50\Omega$ | | 10 | 18 | | kΩ |

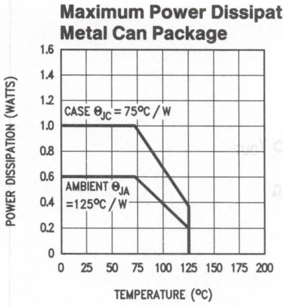
## AC Electrical Characteristics $V_{CC} = \pm 5V, T_A = 25°C.$

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $S_R$ | Slew Rate | $R_L = 50\Omega, R_S = 50\Omega$<br>$V_{IN} = \pm 2V$ | | 1000 | 1250 | | V/µs |
| $f_{3dB}$ | Bandwidth, −3 dB | $R_S = 50\Omega$<br>$R_L = 50\Omega$<br>(Note 2) | $V_{OUT} = 4V_{P-P}$ | 100 | 125 | | MHz |
| | | | $V_{OUT} = 2V_{P-P}$ | | 150 | | MHz |
| | | | $V_{OUT} = 100\ mV_{P-P}$ | | 200 | | MHz |
| | Phase Non-Linearity | BW = 1.0–20 MHz | | | 2.0 | | degrees |
| $t_r$ | Rise Time | $\Delta V_{IN} = 0.5V$ | | | 3 | | ns |
| $t_d$ | Propagation Delay | $\Delta V_{IN} = 0.5V$ | | | 1.2 | | ns |
| THD | Harmonic Distortion | f = 1 kHz | | | 0.1 | | % |

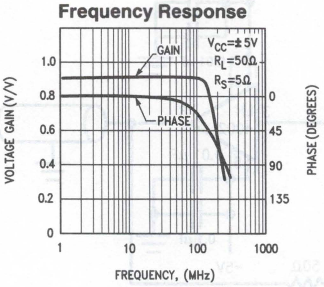
**Note 1:** Under normal operating conditions $+V_{CC1}$ and $+V_{CC2}$ should be connected together, and $-V_{CC1}$ and $-V_{CC2}$ should be connected together.

**Note 2:** Guaranteed by design. This parameter is sample tested.

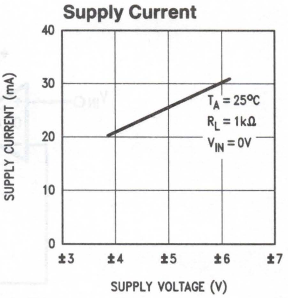
## Typical Performance Characteristics



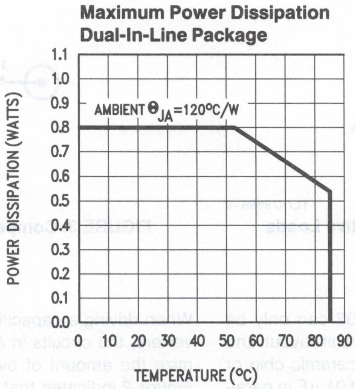
TL/K/8686-4



TL/K/8686-5

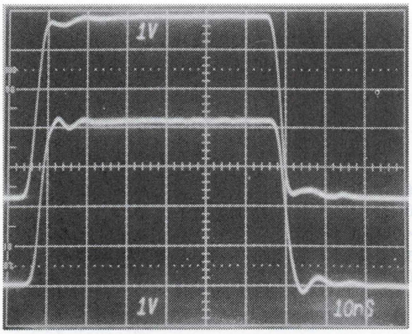


TL/K/8686-6



TL/K/8686-12

## Pulse Response

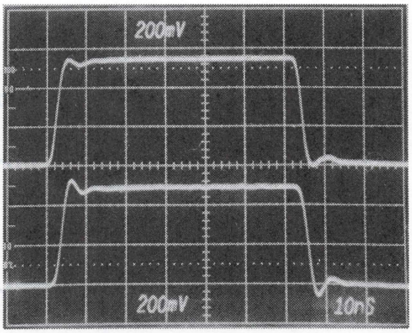


TL/K/8686-7

TOP TRACE
= INPUT

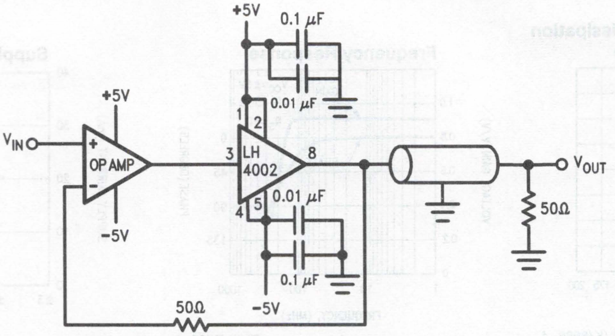
BOTTOM TRACE
= OUTPUT

$V_S = \pm 5V$
$R_L = 50\Omega$



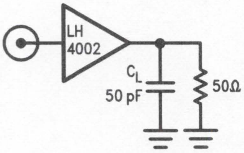
TL/K/8686-8

## Typical Applications


+5V
0.1 μF
0.01 μF
+5V
V_IN
+
OP AMP
−
−5V
1
2
3
LH
4002
8
5
4
0.01 μF
0.1 μF
−5V
50Ω
V_OUT
50Ω

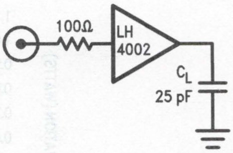
TL/K/8686-11

FIGURE 1. Wideband Unity Gain Amplifier Using LH4002CN


LH
4002
C_L
50 pF
50Ω

TL/K/8686-9

FIGURE 2. Compensation for Capacitive Loads


100Ω
LH
4002
C_L
25 pF

TL/K/8686-10

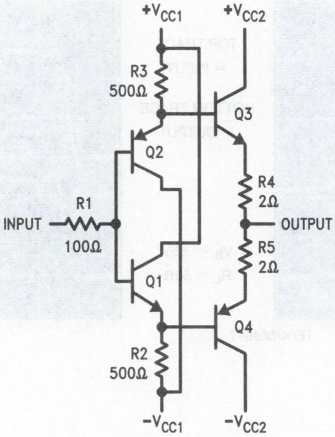
FIGURE 3. Compensation for Capacitive Loads

## Applications Information

The high speed performance of the LH4002 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.01 μF in parallel with 0.1 μF should be connected with the shortest practical lead length between device supply leads and a ground plane. Failure to follow these rules can result in oscillations.

When driving a capacitive load such as inputs to flash converters, the circuits in *Figure 2* and *3* can be used to minimize the amount of overshoot and ringing at the outputs. *Figure 2* indicates that a 50Ω should be placed in parallel with the load and *Figure 3* recommends that a 100Ω resistor be placed in series with the input to the LH4002.

## Schematic Diagram


+V_CC1
+V_CC2
R3
500Ω
Q3
Q2
R4
2Ω
R1
INPUT
100Ω
OUTPUT
R5
2Ω
Q1
Q4
R2
500Ω
−V_CC1
−V_CC2

TL/K/8686-14

National Semiconductor Corporation

**PRELIMINARY**

# LH4003/LH4003C Precision RF Closed Loop Buffer

## General Description

The LH4003 is a precision RF buffer optimized for unity gain applications. The LH4003 features a small signal bandwidth of 250 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4003 is useful in applications such as video buffering, cable driving, and flash converter input conditioning.

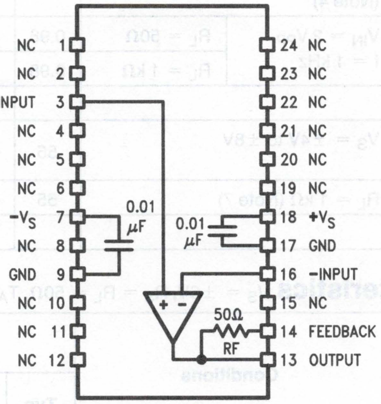
## Features

- Operation from ±6V supplies
- Drive 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.97 gain accuracy into 50Ω

## Applications

- Line drivers
- Video buffers

## Block and Connection Diagram


NC 1
NC 2
+INPUT 3
NC 4
NC 5
NC 6
−V_S 7
NC 8
GND 9
NC 10
NC 11
NC 12
24 NC
23 NC
22 NC
21 NC
20 NC
19 NC
18 +V_S
17 GND
16 −INPUT
15 NC
14 FEEDBACK
13 OUTPUT
0.01 μF
0.01 μF
+ −
50Ω
RF

**Note 1:** NC = No Connection

**Note 2:** Pins 9 & 17 Internally Connected

TL/K/9243-1

**Top View**

**Order Number LH4003D, LH4003CD**
**See NS Package Number D24D**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, Vs | ±8V |
| Power Dissipation, $P_D$ | |
| $T_A = 25°C$, derate linearly at 62.5°C/W | 2W |
| $T_C = 25°C$, derate linearly at 33.3°C/W | 3.75W |
| Input Common Mode Voltage Range, $V_{CM}$ | ±Vs |
| Output Current, $I_O$ | ±100 mA |
| Output Short Circuit Duration | Continuous |
| Operating Temperature Range, $T_A$ | |
| LH4003CD | −25°C to +85°C |
| LH4003D | −55°C to +125°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

## DC Electrical Characteristics $V_S = \pm6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Notes 1, 6)

| Symbol | Parameter | Conditions | | LH4003C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $V_{OS}$ | Output Offset Voltage | $T_A = T_J = 25°C$ (Note 4) | | 5 | 15 | | mV |
| $V_{OS/\Delta T}$ | Offset Voltage Drift | | | 100 | | | μV/°C |
| $I_B$ | Input Bias Current | $R_S = 300\Omega$, $T_A = T_J = 25°C$ (Note 4) | | 100 | 200 | | μA |
| $A_V$ | Voltage Gain | $V_{IN} = 2\ V_{PP}$ f = 1 kHz | $R_L = 50\Omega$ | 0.98 | 0.95 | | $V/V_{(Min)}$ |
| | | | $R_L = 1\ k\Omega$ | 0.98 | 0.95 | | |
| $V_O$ | Output Voltage Swing | | | | ±3 | | $V_{(Min)}$ |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm4V$ to $\pm8V$ | | 55 | 45 | | $dB_{(Min)}$ |
| $I_S$ | Supply Current | $R_L = 1\ k\Omega$ (Note 7) | | 55 | 65 | | mA |
| $P_D$ | Power Dissipation | | | | | 780 | mW |

## AC Electrical Characteristics $V_S = \pm6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Note 1)

| Symbol | Parameter | Conditions | | LH4003C | | | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $t_r$ | Small Signal Rise Time | $\Delta V_{IN} = 0.5V$ | | 2 | | | ns |
| $t_s$ | Settling Time to 0.1% | $V_{IN} = \pm3V$ | | 80 | | | |
| SR | Slew Rate | $V_{IN} = -3V$ to $+3V$ | 10%–90% | 1000 | | 800 | V/μs (Min) |
| | | $V_{IN} = +3V$ to $-3V$ | 10%–90% | 1200 | | 1000 | |
| $f_{-3\ dB}$ | Small Signal Bandwidth | $V_{OUT} = 100$ mVp-p | | 250 | 200 | | MHz (Min) |
| | Full Power Bandwidth | $V_{IN} = \pm2V$, (Note 5) | | 65 | | | MHz |
| | Harmonic Distortion | Second Order, $V_{OUT} = 4V$ p-p, $f_{IN} = 10$ MHz | | −60 | | | dB |

## DC Electrical Characteristics $V_S$ = ±6V, $R_S$ = $R_L$ = 50Ω, $T_A$ = 25°C unless otherwise noted. (Notes 1, 6)

| Symbol | Parameter | Conditions | | LH4003 Typ | LH4003 Tested Limit (Note 2) | LH4003 Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Output Offset Voltage | $T_A$ = $T_J$ = 25°C (Note 4) | | 2 | 15<br>**20** | | mV |
| $V_{OS/\Delta T}$ | Offset Voltage Drift | | | 100 | | | μV/°C |
| $I_B$ | Input Bias Current | $R_S$ = 300Ω | $T_A$ = $T_J$ = 25°C, (Note 4) | 100 | 200<br>**200** | | μA |
| $A_V$ | Voltage Gain | $V_{IN}$ = 2 $V_{PP}$<br>f = 1 kHz | $R_L$ = 50Ω | 0.98 | 0.95 | **0.93** | $V/V_{(Min)}$ |
| | | | $R_L$ = 1 kΩ | 0.98 | 0.95<br>**0.93** | | |
| $V_O$ | Output Voltage Swing | $A_V$ = +1 | | | ±3 | **±3** | V (Min) |
| PSRR | Power Supply Rejection Ratio | $V_S$ = ±4V to ±8V | | 55 | 45<br>**40** | | dB (Min) |
| $I_S$ | Supply Current | $R_L$ = 1 kΩ (Note 7) | | 55 | 65 | **80** | mA |
| $P_D$ | Power Dissipation | | | | | 780 | mW |

## AC Electrical Characteristics $V_S$ = ±6V, $R_S$ = $R_L$ = 50Ω, $T_A$ = 25°C unless otherwise noted. (Note 1)

| Symbol | Parameter | Conditions | | LH4003 Typ | LH4003 Tested Limit (Note 2) | LH4003 Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $t_r$ | Small Signal Rise Time | $\Delta V_{IN}$ = 0.5V | | 2 | | | ns |
| $t_s$ | Settling Time to 0.1% | $V_{IN}$ = ±3V | | 80 | | | ns |
| SR | Slew Rate | $V_{IN}$ = −3V to +3V | 10%–90% | 1000 | | 800 | V/μs (Min) |
| | | $V_{IN}$ = +3V to −3V | 10%–90% | 1200 | | 1000 | |
| $f_{-3\,dB}$ | Small Signal Bandwidth | $V_{OUT}$ = 100 mVp-p | | 250 | 200 | | MHz (Min) |
| | Full Power Bandwidth | $V_{IN}$ = ±2V, (Note 5) | | 65 | | | MHz |
| | Harmonic Distortion | Second Order, $V_{OUT}$ = 4V p-p,<br>$f_{IN}$ = 10 MHz | | −60 | | | dB |

**Note 1:** These measurements are taken with the LH4003 strapped for a gain of +1.

**Note 2:** Tested limits are guaranteed and 100% tested in production.

**Note 3:** Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

**Note 4:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J$ = 25°C. See Typical Performance Characteristics for information.

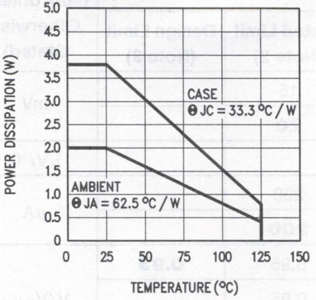
**Note 5:** Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate / (2 πV peak).

**Note 6: Boldface limits are guaranteed over full temperature.** Operating ambient temperature range of LH4003C is −25°C to +85°C, and LH4003 is −55°C to +125°C.

**Note 7:** When the LH4003 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with $V_S$ of ±6V is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

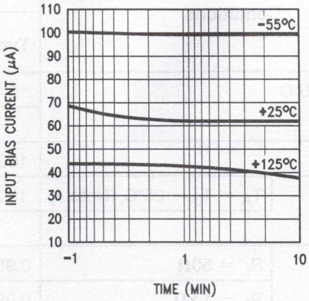
# Typical Performance Characteristics

**Maximum Power Dissipation**



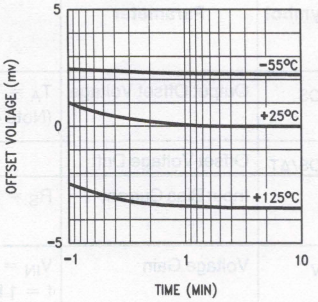
TL/K/9243-2

**Input Bias Current vs Time**



TL/K/9243-10

**Offset Voltage (Typical) vs Time**



TL/K/9243-11

# Application Information

The unity gain follower configuration shown in *Figure 1,* offers a 250 MHz small signal bandwidth to the −3dB point and the minimum slew rate of 800 V/μs insures a full power bandwidth of 65 MHz for a 4V peak-to-peak signal, according to the formula:

$$B = SR/2\pi Vp$$

Where SR is the slew rate in μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.

## DRIVING CAPACITIVE LOADS

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4003 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time of 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).

## LAYOUT CONSIDERATIONS

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz required special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4003 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 μF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5.*

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.

## INPUT CAPACITANCE

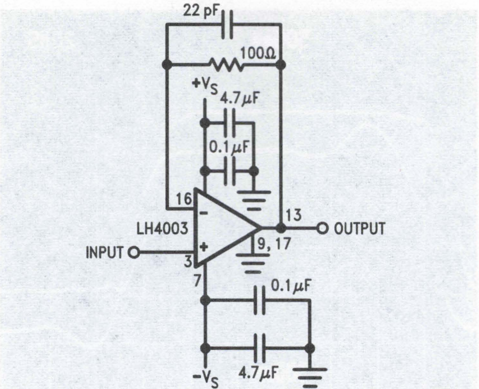
The input capacitance of the LH4003 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500 ohms should not be utilized in the feedback network and high source impedance should be avoided.

## BIAS CURRENT

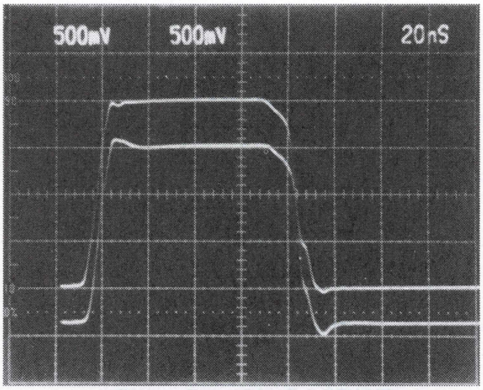
The input bias current is typically 100 μA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.

## Typical Applications


22 pF
100Ω
+V_S
4.7μF
0.1μF
16
LH4003
13
OUTPUT
INPUT
3
9, 17
7
0.1μF
-V_S
4.7μF

TL/K/9243-3

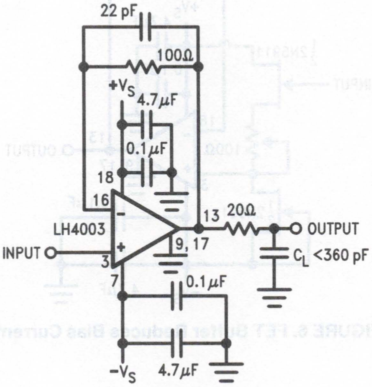
**FIGURE 1. Unity Gain Follow, Typical BW 3dB = 250 MHz**



TL/K/9243-4

**Note:** Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = R_L = 50\Omega$.

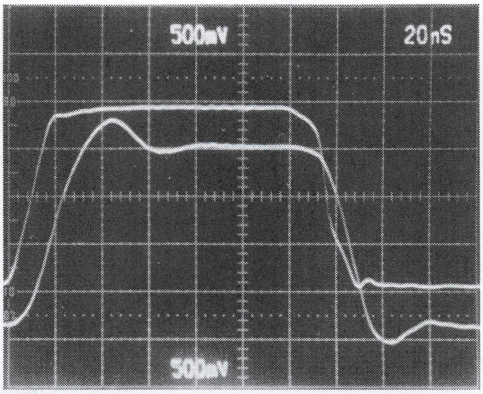
**FIGURE 2. Pulse Response of Follower**


22 pF
100Ω
+V_S
4.7μF
0.1μF
18
16
LH4003
INPUT
3
13
20Ω
OUTPUT
9, 17
C_L <360 pF
7
0.1μF
-V_S
4.7μF

TL/K/9243-6

**FIGURE 3. Driving Capacitance**

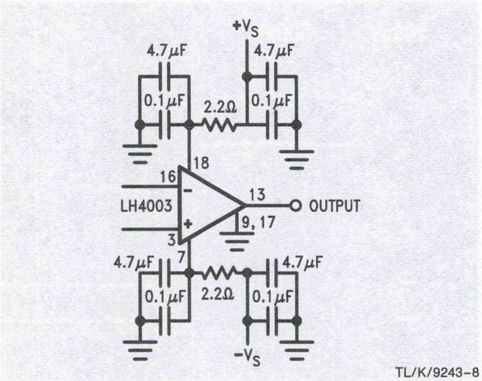
## Typical Applications (Continued)



TL/K/9243-7

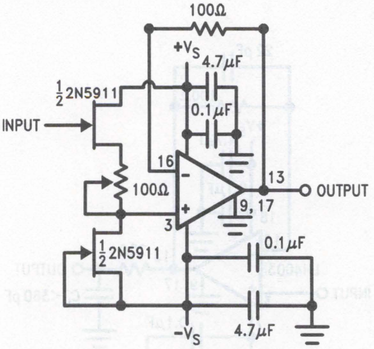
**Note:** Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = 50\Omega$, $R_{ISO} = 20\Omega$ and $C_L = 300$ pF.

**FIGURE 4. Pulse Response when Driving Capacitance.**


+VS
4.7μF
4.7μF
0.1μF
2.2Ω
0.1μF
18
16
13
LH4003
OUTPUT
9, 17
3
7
4.7μF
4.7μF
0.1μF
2.2Ω
0.1μF
-VS

TL/K/9243-8

**FIGURE 5. Dual Stage Decoupling**


100Ω
+VS
4.7μF
1/2 2N5911
0.1μF
INPUT
16
13
OUTPUT
100Ω
9, 17
3
1/2 2N5911
0.1μF
-VS
4.7μF

TL/K/9243-9

**FIGURE 6. FET Buffer Reduces Bias Current**

**National Semiconductor Corporation**

**PRELIMINARY**

# LH4004/LH4004C Wideband FET-Input Buffer/Amplifier

## General Description

The LH4004 is an FET input, high speed differential amplifier optimized for unity gain applications. It eliminates most of the drawbacks of conventional open loop buffers and does not require compensation for unity and other low gain operations. It is an ideal choice for video distribution, driving flash converters, and summing amplifiers. Furthermore, the bandwidth does not decrease with increasing gain. At a closed loop gain of 4, the LH4004 still offers a 75 MHz bandwidth.

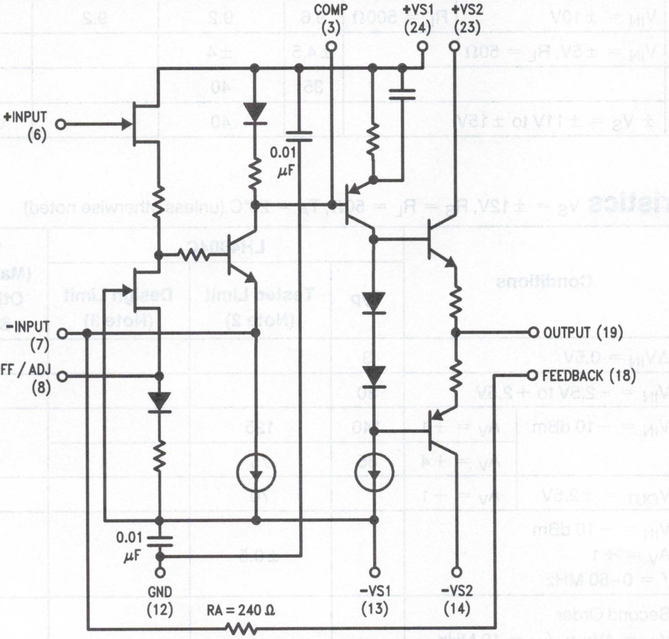
## Applications

- Unity gain buffer
- Low gain op amp

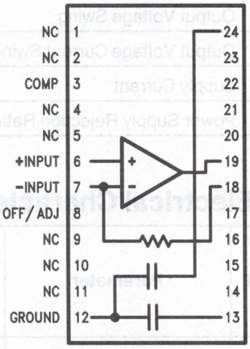
## Features

- ±0.5 dB gain flatness
- 500 V/μs slew rate
- Drives 50Ω directly
- 140 MHz bandwidth
- No external components required for unity gain operation
- Internal power supply bypassing

## Simplified Schematic and Connection Diagram


COMP (3)
+VS1 (24)
+VS2 (23)
+INPUT (6)
0.01 μF
−INPUT (7)
OFF / ADJ (8)
OUTPUT (19)
FEEDBACK (18)
0.01 μF
GND (12)
RA = 240 Ω
−VS1 (13)
−VS2 (14)

TL/K/8831–1


NC 1
NC 2
COMP 3
NC 4
NC 5
+INPUT 6
−INPUT 7
OFF/ADJ 8
NC 9
NC 10
NC 11
GROUND 12
24 +VS1
23 +VS2
22 NC
21 NC
20 NC
19 OUTPUT
18 FEEDBACK
17 NC
16 NC
15 NC
14 −VS2
13 −VS1

TL/K/8831–2

**Top View**

**Order Number LH4004CD or LH4004D**

**See NS Package Number D24D**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±15V |
| Power Dissipation, $P_D$ | |
| $T_A = 25°C$, derate linearly at 80°C/W | 1.8W |
| $T_C = 25°C$, derate linearly at 40°C/W | 3.75W |
| Input Voltage Range, $V_{IN}$ | $\pm V_S$ |
| Operating Temperature Range, $T_A$ | |
| LH4004CD | −25°C to +85°C |
| LH4004D | −55°C to +125°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temperature (Soldering, <10 sec) | 300°C |

ESD rating is to be determined.

## DC Electrical Characteristics $V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted (Note 1)

| Symbol | Parameter | Conditions | | LH4004C Typ | LH4004C Tested Limit (Note 2) | LH4004C Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{IN} = 0V$, $T_A = T_J = 25°C$ (Note 4) | | 8 | 15 | | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | | | 300 | | | $\mu V/°C$ |
| $I_B$ | Input Bias Current | $T_J = 25°C$, Pin 6 (Note 4) | | | 400 | | pA |
| | Gain Accuracy | $V_{IN} = \pm 1V$<br>$A_V = +1$ | $R_L = 500\Omega$ | 0.98 | 0.96 | **0.93** | V/V (Min) |
| | | | $R_L = 50\Omega$ | 0.98 | 0.96 | **0.93** | |
| $V_O$ | Output Voltage Swing | $V_{IN} = \pm 10V$ | $R_L = 500\Omega$ | 9.6 | 9.2 | 9.2 | V (Min) |
| $V_O$ | Output Voltage Current Swing | $V_{IN} = \pm 5V$, $R_L = 50\Omega$ | | ±4.5 | ±4 | | V (Min) |
| $I_S$ | Supply Current | | | 35 | 40 | | mA |
| PSRR | Power Supply Rejection Ratio | $\pm V_S = \pm 11V$ to $\pm 15V$ | | | 40 | | dB (Min) |

## AC Electrical Characteristics $V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ (unless otherwise noted)

| Symbol | Parameter | Conditions | | LH4004C Typ | LH4004C Tested Limit (Note 2) | LH4004C Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $t_r$ | Small Signal Rise Time | $\Delta V_{IN} = 0.5V$ | | 3 | | | ns |
| $t_s$ | Settling Time to 0.5% | $V_{IN} = -2.5V$ to $+2.5V$ | | 30 | | | ns |
| $f_{-3dB}$ | Small Signal Bandwidth | $V_{IN} = -10$ dBm | $A_V = +1$ | 140 | 125 | | MHz (Min) |
| | | | $A_V = +4$ | 85 | 75 | | |
| | Large Signal Bandwidth | $V_{OUT} = \pm 2.5V$ | $A_V = +1$ | | 70 | | MHz |
| | Gain Flatness | $V_{IN} = -10$ dBm<br>$A_V = +1$<br>$f = 0$–50 MHz | | | ±0.5 | | dB |
| | Harmonic Distortion | Second Order<br>$V_{IN} = 4Vp\text{-}p$, $f_{IN} = 10$ MHz | | | | | dB |
| SR | Slew Rate | $V_{IN} = -2.5V$ to $+2.5V$ | | 1500 | | 1200 | $V/\mu s$ (Min) |
| | | $V_{IN} = +2.5V$ to $-2.5V$ | | 600 | | 500 | |

## DC Electrical Characteristics

$V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted (Notes 1 & 5)

| Symbol | Parameter | Conditions | | LH4004 Typ | LH4004 Tested Limit (Note 2) | LH4004 Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $T_A = T_J = 25°C$ (Note 4) | | 8 | 15 | | mV |
| $V_{OS}/\Delta T$ | Offset Voltage Drift | | | 300 | | | μV/°C |
| $I_B$ | Input Bias Current | $T_A = T_J = 25°C$, Pin 6 (Note 4) | | | 400 | | pA |
| | | | | | **400** | | nA |
| | Gain Accuracy | $V_{IN} = \pm 1V$<br>$A_V = +1$ | $R_L = 500\Omega$ | 0.98 | 0.96<br>**0.93** | | V/V (Min) |
| | | | $R_L = 50\Omega$ | 0.98 | 0.96<br>**0.93** | | |
| $V_O$ | Output Voltage Swing | $V_{IN} = \pm 10V$ | $R_L = 500\Omega$ | 9.6 | 9.2 | | V (Min) |
| $V_O$ | Output Voltage Swing | $V_{IN} = \pm 5V$, $R_L = 50\Omega$ | | ±4.5 | **±4** | | V (Min) |
| $I_S$ | Supply Current | | | 35 | 40 | | |
| PSRR | Power Supply Rejection Ratio | | | | **40** | | dB (Min) |

## AC Electrical Characteristics

$V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | Conditions | | LH4004 Typ | LH4004 Tested Limit (Note 2) | LH4004 Design Limit (Note 3) | Units (Max Unless Otherwise Stated) |
|---|---|---|---|---|---|---|---|
| $t_r$ | Small Signal Rise Time | $\Delta V_{IN} = 0.5V$ | | 3 | | | ns |
| $t_s$ | Settling Time to 0.5% | $V_{IN} = -2.5V$ to $+2.5V$ | | 30 | | | ns |
| $f_{-3dB}$ | Small Signal Bandwidth | $V_{IN} = -10$ dBm | $A_V = +1$ | | 125 | | MHz (Min) |
| | | | $A_V = +4$ | | 75 | | |
| | Large Signal Bandwidth | $V_{OUT} = \pm 2.5V$ | $A_V = +1$ | | 70 | | MHz |
| | Gain Flatness | $V_{IN} = 100$ mV p-p<br>$A_V = +1$<br>$f = 0–50$ MHz | | | ±0.5 | | dB |
| | Harmonic Distortion | Second Order<br>$V_{IN} = 4V$ p-p, $f_{IN} = 10$ MHz | | | | | dB |
| SR | Slew Rate | $V_{IN} = -2.5V$ to $+2.5V$ | | 1500 | | 1200 | V/μs (Min) |
| | | $V_{IN} = +2.5V$ to $-2.5V$ | | 600 | | 500 | |

**Note 1: Boldface limits are guaranteed over full temperature range.** Operating ambient temperature range of LH4004C is −25°C to +85°C, and LH4004 is −55°C to +125°C.

**Note 2:** Tested limits are guaranteed and 100% production tested.

**Note 3:** Design limits are guaranteed (but not 100% production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality levels.

**Note 4:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

**Note 5:** When the LH4004 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with $V_S$ of ±12V is 960 mW, whereas the package is only rated to 800 mW without a heatsink at 125°C.

## Application Hints

The front page figure shows the simplified schematic which includes the feedback resistor and the decoupling capacitors.

The essential difference from other op amps is that both inputs are radically different, the non-inverting input goes to a FET buffer follower and the inverting input is connected to the second stage emitter node. This topology is responsible for the unique bandwidth characteristic and transfer function of the amplifier.

Let's consider the connection diagram of *Figure 1.* The typical transfer function in the case of a classical op amp would be:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K(s)}{1 + K(s)/B}$$

where $B = \frac{R_A + R_B}{R_B}$ and K(s) is the open loop gain of the amplifier and is frequency dependent. By rearranging the formula, we find;

$$(1) \quad \frac{V_{OUT}}{V_{IN}} = B * \frac{K(s)}{K(s) + B}$$

For the LH4004, a small signal analysis shows that the difference between the two inputs turns the previous typical equation into:

$$(2) \quad \frac{V_{OUT}}{V_{IN}} = B * \frac{K(s)}{K(s) + B + m\,R_A}$$

where m is an internal parameter to the device and K(s) is approximately 70 dB at DC with a 50Ω load.

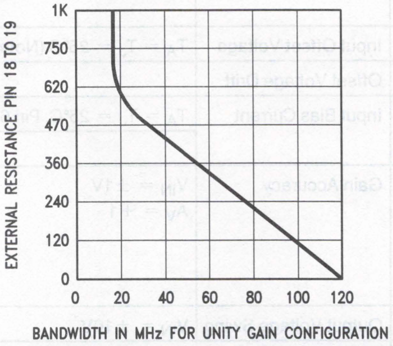
In both equations, the second term is negligible when the open loop gain of the amplifier, K(s), approaches infinity, but in equation (1), when the signal frequency reaches a point where K(s) is small, say K(s) = 10 or less, then the term will be very sensitive to the value of the closed loop gain B and $V_{OUT}/V_{IN}$ will fall earlier as B increases.

In equation (2), m is approximately 0.19 and $R_A$ is provided inside the package, with a value which has been chosen to be 240Ω. The term $mR_A$ is therefore equal to 46 and will dominate the term B as long as it is kept below 5. The result is that $V_{OUT}/V_{IN}$ will not be as dependent on B as with traditional topologies. The gain will still fall with the open loop gain K(s) as the frequency increases, but the roll off will be virtually independent of the closed loop gain B.

Resistor $R_B$ sets the overall closed loop gain, but has very little effect on stability and bandwidth. Another peculiarity of the LH4004 is that the loop compensation can be accomplished by changing the value of resistor $R_A$ *(Figure 2).* Even though this such as settling time, overshoot and phase margin, it will not affect the slew rate. Although this resistive compensation scheme is adequate in most cases, an alternate method is to place a capacitor between pins 3 and 19 *(Figure 3).* This method of compensation also reduces the device slew rate *(Figure 4).*

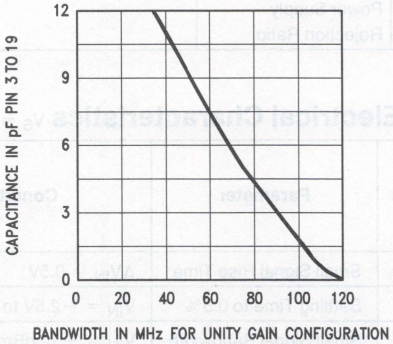
## Low Gain Operation

The small amount of stray capacitance present at the inverting input can cause peaking which increases with decreasing gain. The gain set resistor $R_B$ (in *Figure 1* ) is effectively in parallel with this capacitance and so a frequency domain pole results. With a small $R_B$, this pole is at a high frequency and it affects the closed loop gain of the LH4004 only slightly. At lower values of gain, this pole becomes significant. For example, at a gain of +2, the gain may peak as much as 1.5 dB to 2 dB at 100 MHz.



TL/K/8831-10

**FIGURE 2. Bandwidth vs $R_{ext}$**



TL/K/8831-11

**FIGURE 3. Bandwidth vs $C_{ext}$**

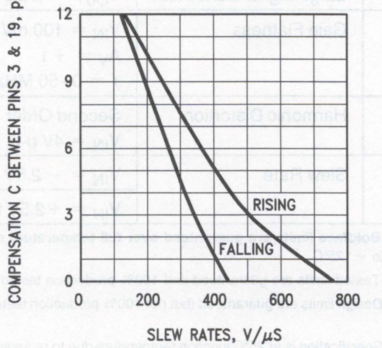


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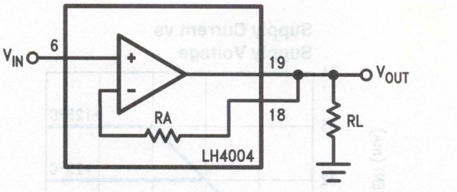
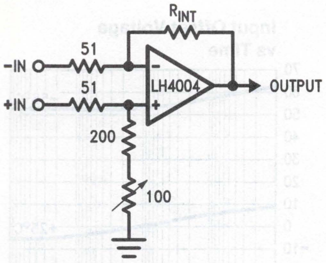
**FIGURE 4. Slew Rates vs Compensation C**

## Typical Applications


$V_{IN}$
6
+
−
19
18
RA
LH4004
$V_{OUT}$
RL

TL/K/8831-4

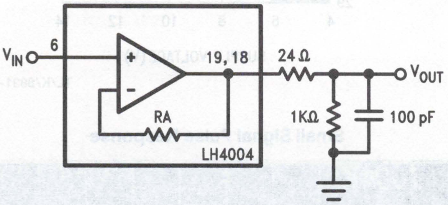
**FIGURE 5. Unity Gain Buffer**


$R_{INT}$
−IN
51
+IN
51
LH4004
−
+
OUTPUT
200
100

**Note:** Adjust pot for best CMRR.

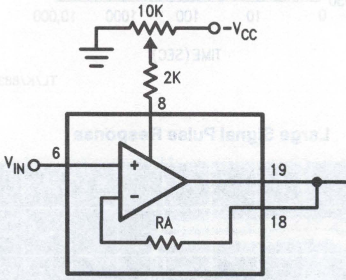
TL/K/8831-12

**FIGURE 6. Differential Amplifier**


$V_{IN}$
6
+
−
19, 18
24 Ω
RA
LH4004
1KΩ
100 pF
$V_{OUT}$

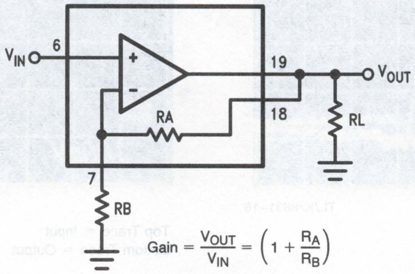
TL/K/8831-5

**FIGURE 7. Driving Capacitive Loads**


10K
$-V_{CC}$
2K
8
$V_{IN}$
6
+
−
19
18
RA
$V_{OUT}$

TL/K/8831-6

**FIGURE 8. Offset Adjust**


$V_{IN}$
6
+
−
RA
19
18
$V_{OUT}$
RL
7
RB

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_A}{R_B}\right)$$

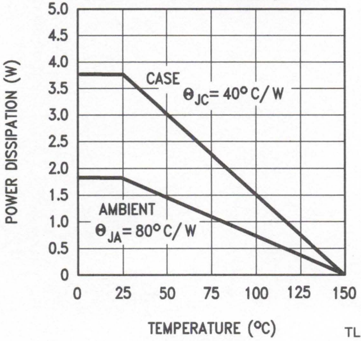
$R_A = 240\Omega$

TL/K/8831-7

**FIGURE 9. LH4004 Used in Amplifier Applications**

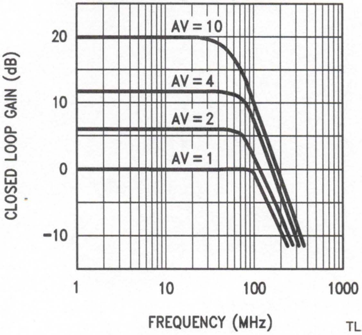
## Typical Performance Characteristics

### Maximum Power Dissipation



TL/K/8831-8

### Closed Loop Response



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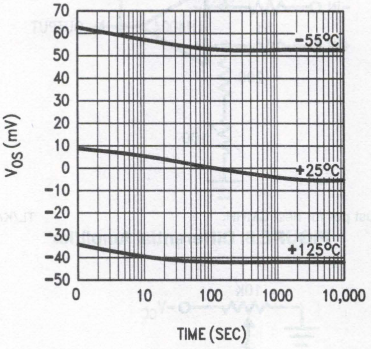
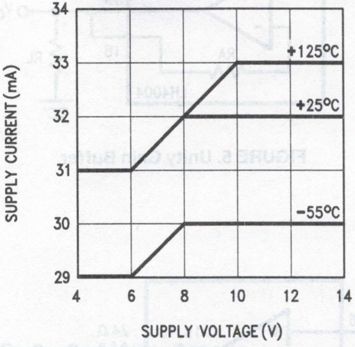
## Typical Performance Characteristics (Continued)

**Input Offset Voltage vs Time**



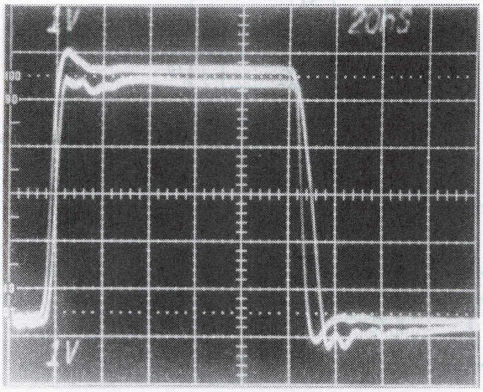
TL/K/8831-14

**Supply Current vs Supply Voltage**



TL/K/8831-15

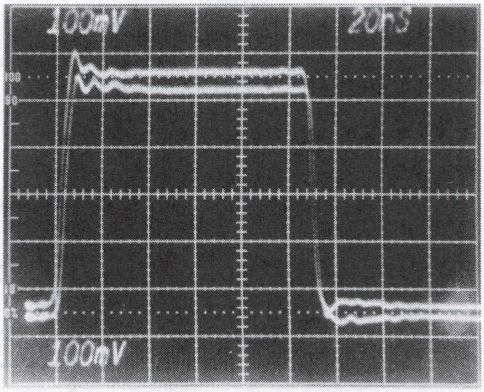
**Large Signal Pulse Response**



TL/K/8831-16

Top Trace = Input
Bottom Trace = Output

**Small Signal Pulse Response**



TL/K/8831-17

Top Trace = Input
Bottom Trace = Output

**National Semiconductor Corporation**

**PRELIMINARY**

# LH4006/LH4006C Precision RF Closed Loop Buffer

## General Description

The LH4006 is a precision RF buffer optimized for unity gain applications. It features a small signal bandwidth of 350 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4006 is useful in applications such as video buffering, cable driving, and flash converter input conditioning. The high bandwidth also allows the LH4006 to be used in RF/IF signal conditioning such as amplification or down conversion.

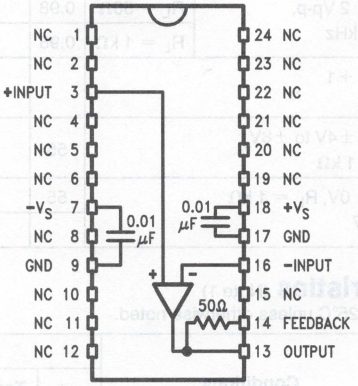
## Features

- Operation from ±6V supplies
- Drives 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.95 gain accuracy into 50Ω

## Applications

- Line drivers
- Video buffers
- Pulse amplifiers

## Connection Diagram



NC 1
NC 2
+INPUT 3
NC 4
NC 5
NC 6
$-V_S$ 7
NC 8
GND 9
NC 10
NC 11
NC 12
24 NC
23 NC
22 NC
21 NC
20 NC
19 NC
18 $+V_S$
17 GND
16 −INPUT
15 NC
14 FEEDBACK
13 OUTPUT
0.01 μF
0.01 μF
+
−
50Ω

TL/K/9255-1

**Top View**

**Note 1:** NC = not connected.

**Note 2:** Pins 9 & 17 are internally connected.

**Order Number LH4006D & LH4006CD**
**See NS Package Number D24D**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, $V_S$ | ±8V |
| Power Dissipation, $P_D$ | |
| $T_C = 25°C$, Derate Linearly at 33.3°C/W | 3.75W |
| $T_A = 25°C$, Derate Linearly at 62.5°C/W | 2W |
| Input Common Mode Voltage Range, $V_{CM}$ | $\pm V_S$ |
| Output Current, $I_O$ | ±100 mA |
| Output Short Circuit Duration | Continuous |
| Operating Temperature Range, $T_A$ | |
| LH4006CD | −25°C to +85°C |
| LH4006D | −55°C to +125°C |
| Storage Temperature Range, $T_{STG}$ | −65°C to +150°C |
| Maximum Junction Temperature, $T_J$ | 150°C |
| Lead Temperature (Soldering < 10 sec.) | 300°C |
| ESD Rating to be determined. | |

## DC Electrical Characteristics (Notes 1 & 6)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

| Symbol | Parameter | Conditions | | LH4006C Typ | LH4006C Tested Limit (Note 2) | LH4006C Design Limit (Note 3) | Units (Max unless otherwise stated) |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Output Offset Voltage | $T_A = T_J = 25°C$, Note 4 | | 5 | 15 | | mV |
| $V_{OS/\Delta T}$ | Offset Voltage Drift | | | 100 | | | μV/°C |
| $I_B$ | Input Bias Current | $R_S = 300\Omega$, Note 4 | | 100 | 300 | | μA |
| $A_V$ | Voltage Gain | $V_{IN} = 2$ Vp-p,<br>f = 1 kHz | $R_L = 50\Omega$ | 0.98 | 0.95 | | V/V<br>(min) |
| | | | $R_L = 1\ k\Omega$ | 0.98 | 0.95 | | |
| $V_O$ | Output Voltage Swing | $A_V = +1$ | | | ±3 | | V<br>(min) |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 4V$ to $\pm 8V$<br>$R_L = 1\ k\Omega$ | | 55 | 45 | | dB<br>(min) |
| $I_S$ | Supply Current | $V_{IN} = 0V$, $R_L = 1\ k\Omega$<br>Note 7 | | 55 | 65 | | mA |
| $P_D$ | Power Dissipation | | | | | 780 | mW |

## AC Electrical Characteristics (Note 1)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

| Symbol | Parameter | Conditions | | LH4006C Typ | LH4006C Tested Limit (Note 2) | LH4006C Design Limit (Note 3) | Units (Max unless otherwise stated) |
|---|---|---|---|---|---|---|---|
| tr | Small Signal Rise Time | $\Delta V_{IN} = 0.5V$ | | 2 | | | ns |
| ts | Settling Time to 0.1% | $V_{IN} = \pm 3V$ | | 80 | | | |
| SR | Slew Rate | $V_{IN} = -3V$ to $+3V$ | 10%–90% | 1000 | | | V/μs<br>(min) |
| | | $V_{IN} = +3V$ to $-3V$ | 10%–90% | 1200 | | | |
| $f_{-3\ dB}$ | Small Signal Bandwidth | $V_{OUT} = 100$ mVp-p | $A_V = +1$ | 350 | 300 | | MHz<br>(min) |
| | Full Power Bandwidth | $V_{IN} = \pm 2V$, Note 5 | | 80 | | | |
| | Second Order Harmonic Distortion | $V_{OUT} = 4$ Vp-p,<br>$f_{IN} = 10$ MHz | | −60 | | | dB |

## DC Electrical Characteristics (Notes 1 & 6)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

| Symbol | Parameter | Conditions | | LH4006 | | | Units (Max unless otherwise stated) |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| $V_{OS}$ | Output Offset Voltage | $T_A = T_J = 25°C$ | | 2 | 15 | | mV |
| | | | | | **25** | | |
| $V_{OS/\Delta T}$ | Offset Voltage Drift | $V_{IN} = 0V$ | | 100 | | | $\mu V/°C$ |
| $I_B$ | Input Bias Current | $R_S = 300\Omega$<br>$T_A = T_J = 25°C$, Note 4 | | 100 | 300 | | $\mu A$ |
| | | | | | **400** | | |
| $A_V$ | Voltage Gain | $V_{IN} = 2$ Vp-p, f = 1 kHz | $R_L = 50\Omega$ | 0.98 | 0.95<br>**0.93** | | V/V (min) |
| | | | $R_L = 1 k\Omega$ | 0.98 | 0.95<br>**0.93** | | |
| $V_O$ | Output Voltage Swing | $A_V = +1$ | | | ±3 | **±3** | V (min) |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 4V$ to $+8V$ | | 55 | 45<br>**40** | | dB (min) |
| $I_S$ | Supply Current | $V_{IN} = 0V$, $R_L = 1 k\Omega$ (Note 7) | | 55 | 65 | **80** | mA |
| $P_D$ | Power Dissipation | | | | | 780 | mW |

## AC Electrical Characteristics (Note 1)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

| Symbol | Parameter | Conditions | | LH4006 | | | Units (Max unless otherwise stated) |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Tested Limit (Note 2) | Design Limit (Note 3) | |
| tr | Small Signal Rise Time | $\Delta V_{IN} = 0.5V$ | | 2 | | | ns |
| ts | Settling Time to 0.1% | $V_{IN} = \pm 3V$ | | 80 | | | |
| SR | Slew Rate | $V_{IN} = -3V$ to $+3V$ | 10%–90% | 1000 | | | V/$\mu$s (min) |
| | | $V_{IN} = +3V$ to $-3V$ | 10%–90% | 1200 | | | |
| $f_{-3 dB}$ | Small Signal Bandwidth | $V_{OUT} = 100$ mVp-p | $A_V = +1$ | 350 | 300 | | MHz (min) |
| | Full Power Bandwidth | $V_{IN} = \pm 2V$, Note 5 | | 80 | | | |
| | Second Order Harmonic Distortion | $V_{OUT} = 4$ Vp-p, $f_{IN} = 10$ MHz | | −60 | | | dB |

**Note 1:** These measurements are taken with the LH4006 strapped for a gain of +1.

**Note 2:** Tested limits are guaranteed and 100% tested in production.

**Note 3:** Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

**Note 4:** Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual value may be higher at operating junction temperature.

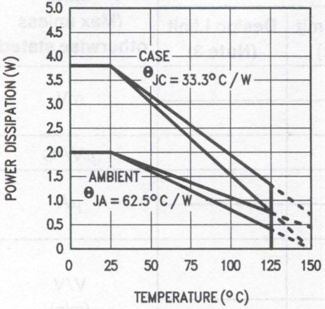
**Note 5:** Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate/(2 $\pi$V peak).

**Note 6:** **Boldface limits are guaranteed over full temperature.** Operating ambient temperature range of LH4006C is −25°C to +85°C, and LH4006 is −55°C to +125°C.

**Note 7:** When the LH4006 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with $V_S$ of ±6V is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

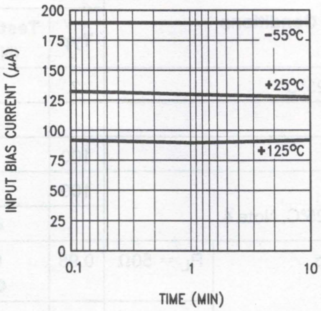
## Typical Performance Characteristics

**Maximum Power Dissipation**



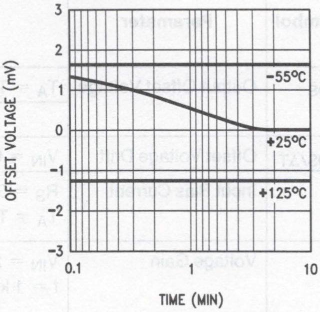
TL/K/9255-2

**Input Bias Current vs Time**



TL/K/9255-10

**Offset Voltage (Typical) vs Time**



TL/K/9255-11

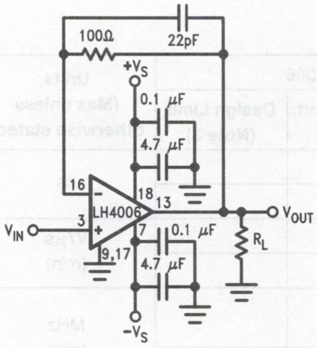
## Application Information

The unity gain follower configuration shown in *Figure 1*, offers a 350 MHz small signal bandwidth to the −3 dB point and the minimum slew rate of 1000 V/μs insures a full power bandwidth of 80 MHz for a 4V peak to peak signal, according to the formula:

$$B = \frac{SR}{2\pi Vp}$$

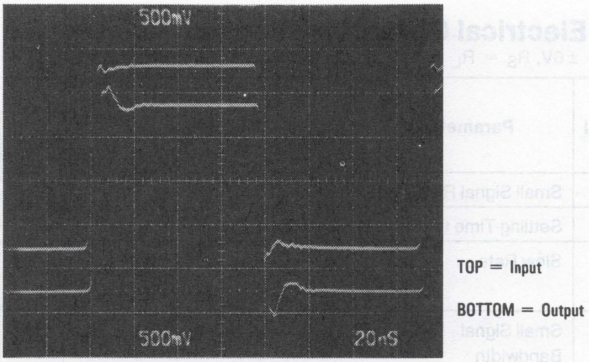
Where SR is the slew rate in V/μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.



TL/K/9255-3

**FIGURE 1. Unity Gain Follower**



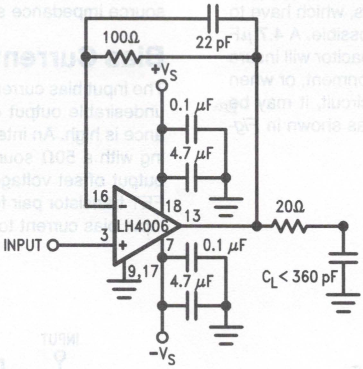
TL/K/9255-5

$V_{CC} = \pm 6V$, $R_S = R_L = 50\Omega$.

**FIGURE 2. Follower/Buffer Pulse Response**

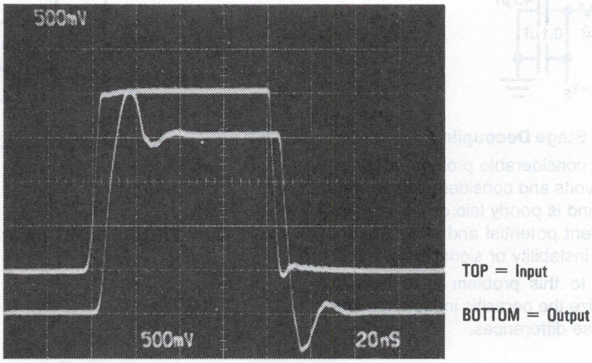
## Driving Capacitive Loads

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4006 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time to 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).



TL/K/9255-6

**FIGURE 3. Driving Capacitance**



TL/K/9255-7

$V_{CC} = \pm 6$ Volts

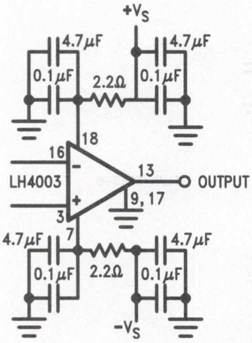
$C_L = 360$ pF

**FIGURE 4. Pulse Response When Driving Capacitance**

## Layout Considerations

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz requires special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4006 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 µF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5*.



TL/K/9255-8

**FIGURE 5. Dual Stage Decoupling**

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.

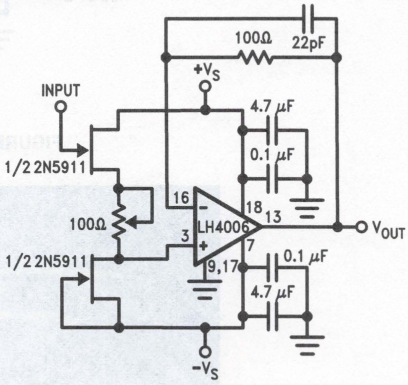
## Input Capacitance

The input capacitance of the LH4006 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500Ω should not be used in the feedback network and high source impedance should be avoided.

## Bias Current

The input bias current is typically 100 µA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.



TL/K/9255-9

**FIGURE 6. FET Input Follower Buffer**

**National Semiconductor Corporation**

# LM102/LM302 Voltage Followers

## General Description

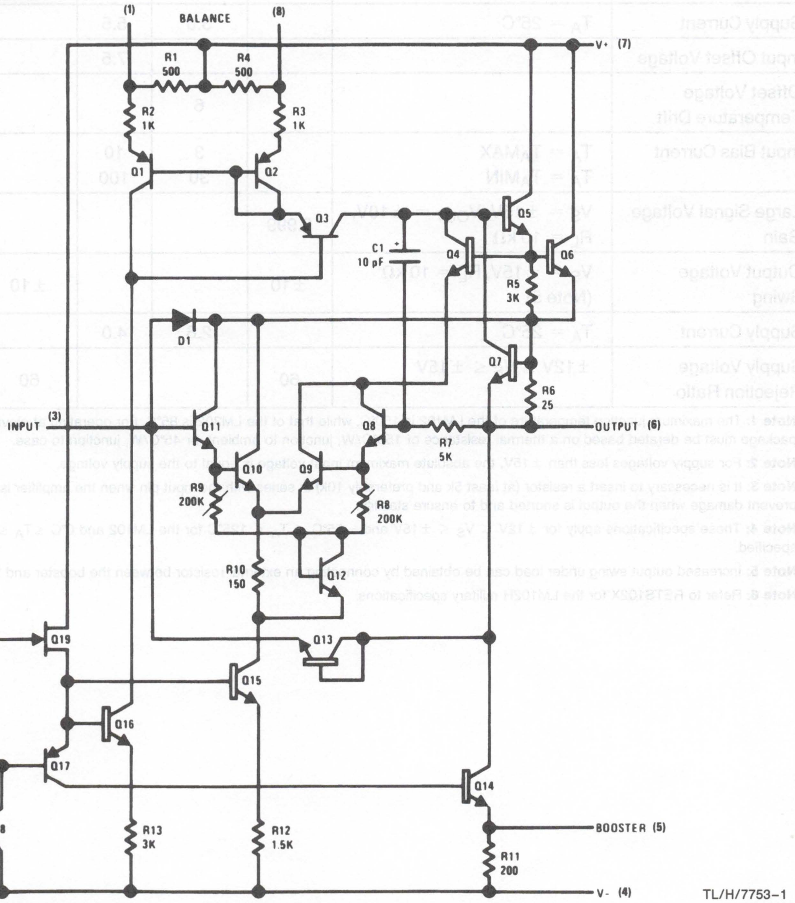
The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift.

The LM102, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response—all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

## Features

- Fast slewing — 10V/$\mu$s
- Low input current — 10 nA (max)
- High input resistance — 10,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1K potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications

## Schematic Diagram


(1)
BALANCE
(8)
R1 500
R4 500
R2 1K
R3 1K
Q1
Q2
Q3
C1 10 pF
Q4
Q5
Q6
R5 3K
V+ (7)
D1
Q7
R6 25
INPUT (3)
Q11
Q8
R7 5K
OUTPUT (6)
Q10
Q9
R9 200K
R8 200K
R10 150
Q12
Q13
Q19
Q15
Q16
Q17
Q14
BOOSTER (5)
Q18
R13 3K
R12 1.5K
R11 200
V- (4)

TL/H/7753-1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Note 1) | 500 mW |
| Input Voltage (Note 2) | ±15V |
| Output Short Circuit Duration (Note 3) | Indefinite |

| | |
|---|---|
| Operating Free Air Temperature Range | |
| LM102 | −55°C to +125°C |
| LM302 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM102 | | | LM302 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Type | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 2 | 5 | | 5 | 15 | mV |
| Input Bias Current | $T_A = 25°C$ | | 3 | 10 | | 10 | 30 | nA |
| Input Resistance | $T_A = 25°C$ | $10^{10}$ | $10^{12}$ | | $10^9$ | $10^{12}$ | | Ω |
| Input Capacitance | | | | 3.0 | | 3.0 | | pF |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S$ ±15V, $V_{OUT} = \pm 10V$, $R_L = 8 k\Omega$ | 0.999 | 0.9996 | | 0.9985 | 0.9995 | 1.0 | V/V |
| Output Resistance | $T_A = 25°C$ | | 0.8 | 2.5 | | 0.8 | 2.5 | Ω |
| Supply Current | $T_A = 25°C$ | | 3.5 | 5.5 | | 3.5 | 5.5 | mA |
| Input Offset Voltage | | | | 7.5 | | | 20 | mV |
| Offset Voltage Temperature Drift | | | 6 | | | 20 | | µV/°C |
| Input Bias Current | $T_A = T_AMAX$<br>$T_A = T_AMIN$ | | 3<br>30 | 10<br>100 | | 3.0<br>20 | 15<br>50 | nA<br>nA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 10 k\Omega$ | 0.999 | | | | | | |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10 k\Omega$ (Note 5) | ±10 | | | ±10 | | | V |
| Supply Current | $T_A = 25°C$ | | 2.6 | 4.0 | | | | mA |
| Supply Voltage Rejection Ratio | $\pm 12V \le V_S \le \pm 15V$ | 60 | | | 60 | | | dB |

**Note 1:** The maximum junction temperature of the LM102 is 150°C, while that of the LM302 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

**Note 2:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

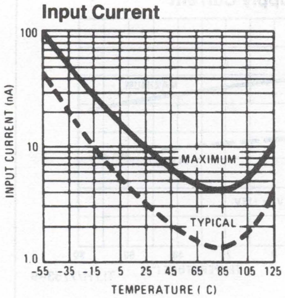
**Note 3:** It is necessary to insert a resistor (at least 5k and preferably 10k) in series with the input pin when the amplifier is driven from low impedance sources to prevent damage when the output is shorted and to ensure stability.

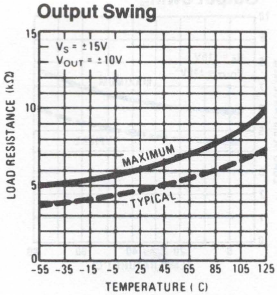
**Note 4:** These specifications apply for $\pm 12V \le V_S \le \pm 15V$ and $-55°C \le T_A \le 125°C$ for the LM102 and $0°C \le T_A \le 70°C$ for the LM302 unless otherwise specified.

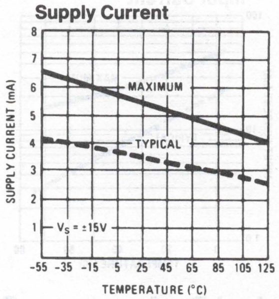
**Note 5:** Increased output swing under load can be obtained by connecting an external resistor between the booster and $V^-$ terminals. See curve.

**Note 6:** Refer to RETS102X for the LM102H military specifications.

## Guaranteed Performance Characteristics LM102

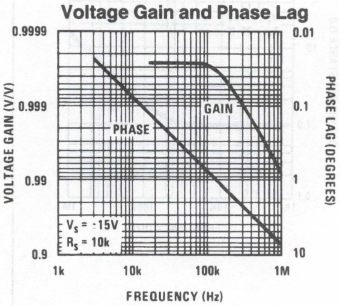

Input Current

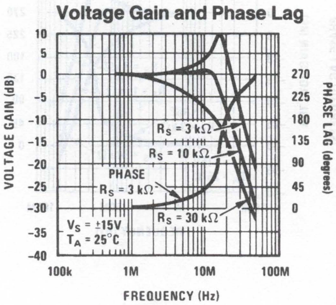

Output Swing

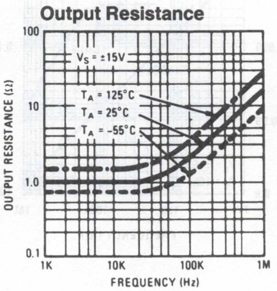

Supply Current

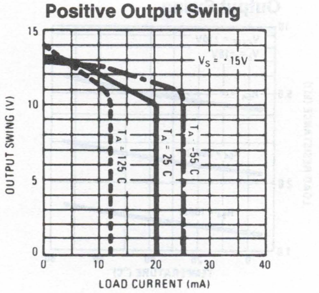
TL/H/7753-7

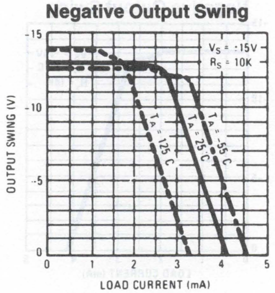
## Typical Performance Characteristics LM102

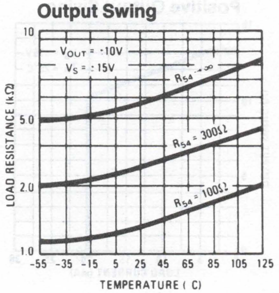

Voltage Gain and Phase Lag

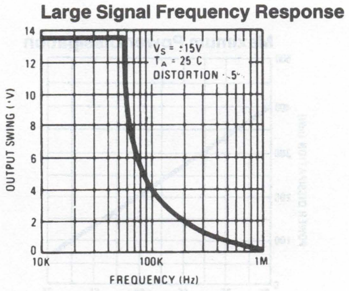

Voltage Gain and Phase Lag

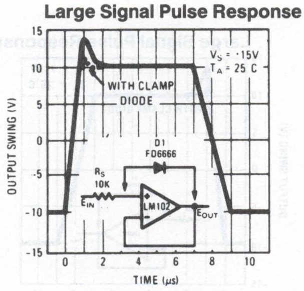

Output Resistance

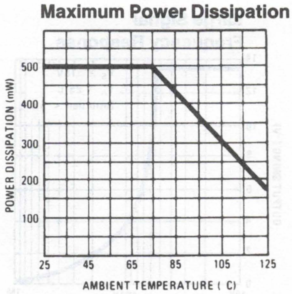

Positive Output Swing


Negative Output Swing


Output Swing

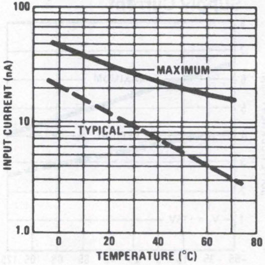

Large Signal Frequency Response

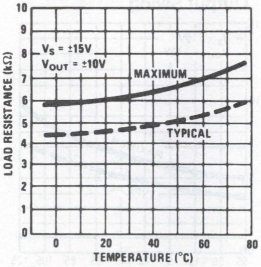

Large Signal Pulse Response

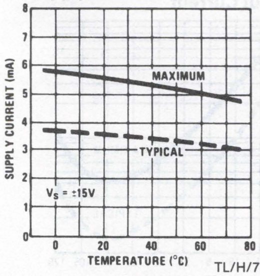

Maximum Power Dissipation

TL/H/7753-8

## Guaranteed Performance Characteristics LM302

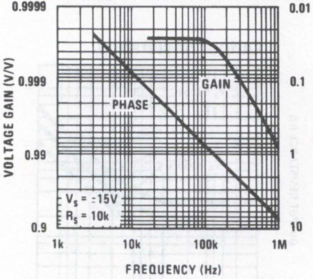

Input Current

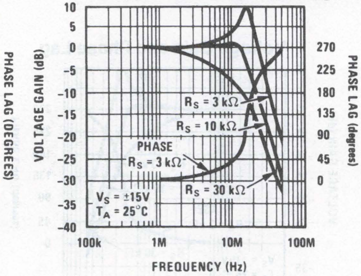

Output Swing

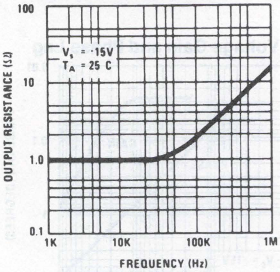

Supply Current

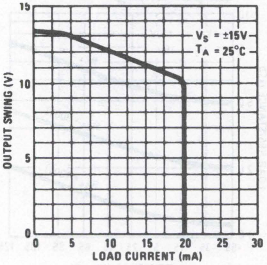
TL/H/7753-9

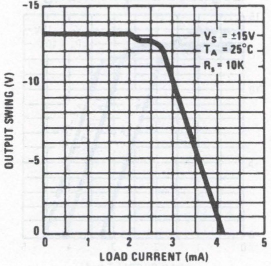
## Typical Performance Characteristics LM302

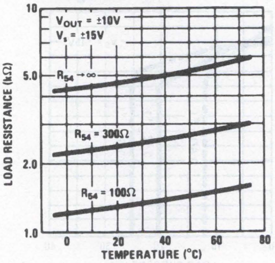

Voltage Gain and Phase Lag

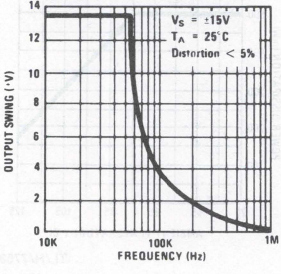

Voltage Gain and Phase Lag

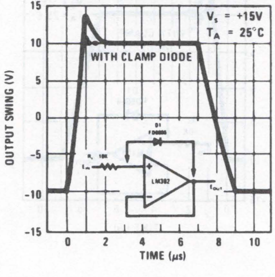

Output Resistance

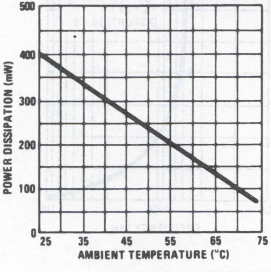

Positive Output Swing


Negative Output Swing


Output Swing


Large Signal Frequency Response

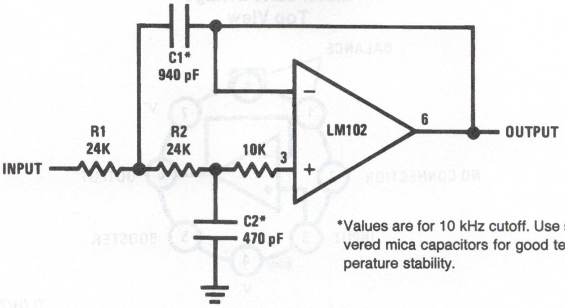

Large Signal Pulse Response


Maximum Power Dissipation

TL/H/7753-10

## Typical Applications

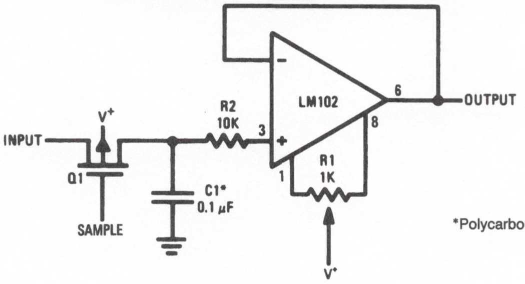
### Low Pass Active Filter


C1*
940 pF
R1
24K
R2
24K
10K
3
LM102
6
OUTPUT
INPUT
C2*
470 pF

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

TL/H/7753–3

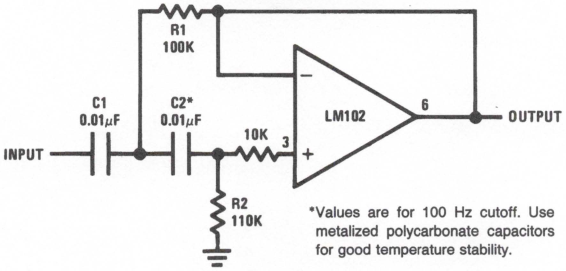
### Sample and Hold with Offset Adjustment


LM102
6
OUTPUT
R2
10K
3
8
INPUT
V+
Q1
1
R1
1K
C1*
0.1 μF
SAMPLE
V+

*Polycarbonate-dielectric capacitor.

TL/H/7753–4

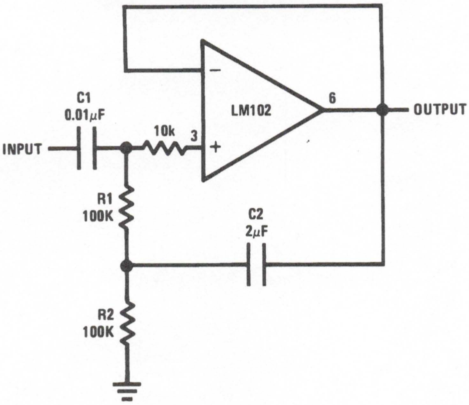
### High Pass Active Filter


R1
100K
C1
0.01μF
C2*
0.01μF
LM102
6
OUTPUT
10K
3
INPUT
R2
110K

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

TL/H/7753–5

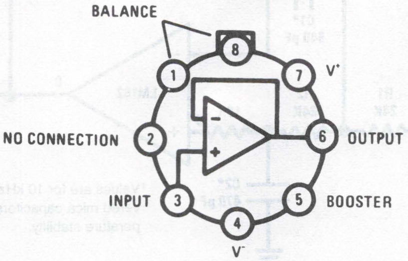
### High Input Impedance AC Amplifier


C1
0.01μF
LM102
6
OUTPUT
10k
3
INPUT
R1
100K
C2
2μF
R2
100K

TL/H/7753–6

## Connection Diagram

**Metal Can Package**
**Top View**


BALANCE
8
1
7
V⁺
NO CONNECTION
2
6
OUTPUT
−
+
INPUT
3
5
BOOSTER
4
V⁻

TL/H/7753–2

**Order Number LM102H or LM302H**
**See NS Package Number H08C**

National Semiconductor Corporation

# LM110/LM210/LM310 Voltage Follower

## General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

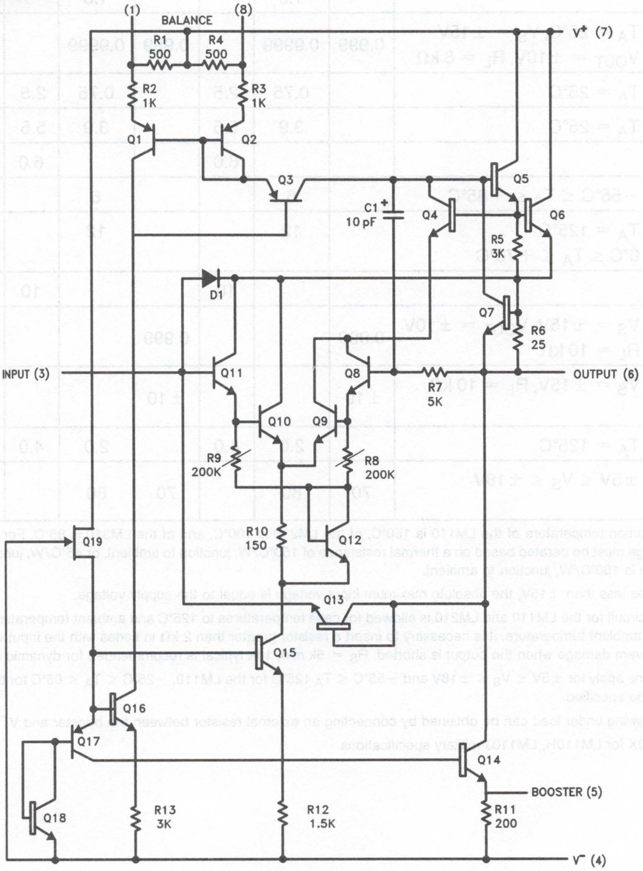
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55°C \le T_A \le +125°C$, the LM210 from $-25°C \le T_A \le +85°C$ and the LM310 from $0°C \le T_A \le +70°C$.

## Features

| | |
|---|---|
| ■ Input current | 10 nA max over temperature |
| ■ Small signal bandwidth | 20 MHz |
| ■ Slew rate | 30 V/μs |
| ■ Supply voltage range | ±5V to ±18V |

## Schematic Diagram


(1)
(8)
BALANCE
R1 500
R4 500
R2 1K
R3 1K
Q1
Q2
Q3
V+ (7)
C1 10 pF
Q4
Q5
Q6
R5 3K
D1
Q7
R6 25
INPUT (3)
Q11
Q8
R7 5K
OUTPUT (6)
Q10
Q9
R9 200K
R8 200K
Q19
R10 150
Q12
Q13
Q15
Q16
Q17
Q14
BOOSTER (5)
Q18
R13 3K
R12 1.5K
R11 200
V− (4)

TL/H/7761–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Note 1) | 500 mW |
| Input Voltage (Note 2) | ±15V |
| Output Short Circuit Duration (Note 3) | Indefinite |
| Operating Temperature Range | |
| LM110 | −55°C to +125°C |
| LM210 | −25°C to +85°C |
| LM310 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | LM110 | | | LM210 | | | LM310 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$ | | 1.5 | 4.0 | | 1.5 | 4.0 | | 2.5 | 7.5 | mV |
| Input Bias Current | $T_A = 25°C$ | | 1.0 | 3.0 | | 1.0 | 3.0 | | 2.0 | 7.0 | nA |
| Input Resistance | $T_A = 25°C$ | $10^{10}$ | $10^{12}$ | | $10^{10}$ | $10^{12}$ | | $10^{10}$ | $10^{12}$ | | Ω |
| Input Capacitance | | | 1.5 | | | 1.5 | | | 1.5 | | pF |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = \pm 15V$<br>$V_{OUT} = \pm 10V$, $R_L = 8\ k\Omega$ | 0.999 | 0.9999 | | 0.999 | 0.9999 | | 0.999 | 0.9999 | | V/V |
| Output Resistance | $T_A = 25°C$ | | 0.75 | 2.5 | | 0.75 | 2.5 | | 0.75 | 2.5 | Ω |
| Supply Current | $T_A = 25°C$ | | 3.9 | 5.5 | | 3.9 | 5.5 | | 3.9 | 5.5 | mV |
| Input Offset Voltage | | | | 6.0 | | | 6.0 | | | 10 | mV |
| Offset Voltage | $-55°C \le T_A \le +85°C$ | | 6 | | | 6 | | | | | µV/°C |
| Temperature Drift | $T_A = 125°C$ | | 12 | | | 12 | | | | | µV/°C |
| | $0°C \le T_A \le +70°C$ | | | | | | | | 10 | | µV/°C |
| Input Bias Current | | | | 10 | | | 10 | | | 10 | nA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$<br>$R_L = 10\ k\Omega$ | 0.999 | | | 0.999 | | | 0.999 | | | V/V |
| Output Voltage Swing (Note 5) | $V_S = \pm 15V$, $R_L = 10\ k\Omega$ | ±10 | | | ±10 | | | ±10 | | | V |
| Supply Current | $T_A = 125°C$ | | 2.0 | 4.0 | | 2.0 | 4.0 | | | | mA |
| Supply Voltage Rejection Ratio | $\pm 5V \le V_S \le \pm 18V$ | 70 | 80 | | 70 | 80 | | 70 | 80 | | dB |

**Note 1:** The maximum junction temperature of the LM110 is 150°C, of the LM210 is 100°C, and of the LM310 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 2:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 3:** Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to 125°C and ambient temperatures to 70°C, and for the LM310, 70°C case temperature or 55°C ambient temperature. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted. $R_S = 5k$ min, 14k typical is recommended for dynamic stability in all applications.

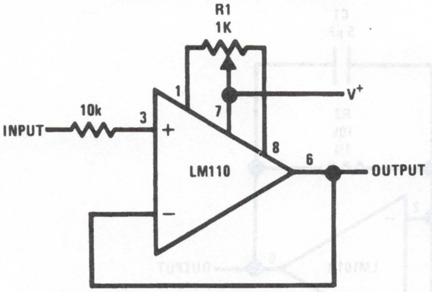
**Note 4:** These specifications apply for $\pm 5V \le V_S \le \pm 18V$ and $-55°C \le T_A\ 125°C$ for the LM110, $-25°C \le T_A \le 85°C$ for the LM210, and $0°C \le T_A \le 70°C$ for the LM310 unless otherwise specified.

**Note 5:** Increased output swing under load can be obtained by connecting an external resistor between the booster and $V^-$ terminals. See curve.

**Note 6:** Refer to RETS110X for LM110H, LM110J military specifications.

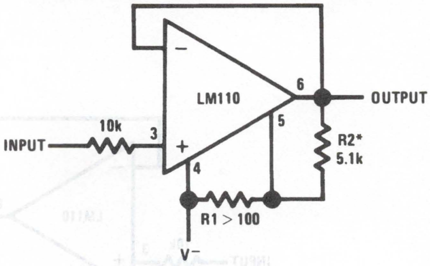
# Auxiliary Circuits

### Offset Balancing Circuit


R1
1K
V+
1
7
10k
3
INPUT
8
LM110
6
OUTPUT
+
−

TL/H/7761–2

### Increasing Negative Swing Under Load

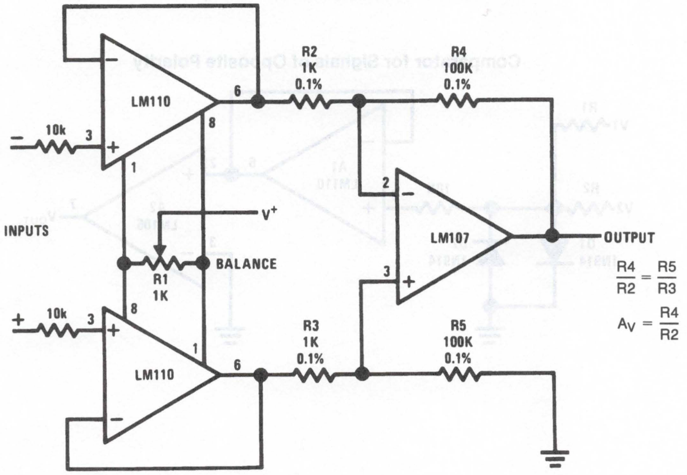

−
LM110
6
OUTPUT
10k
3
INPUT
+
5
R2*
5.1k
4
R1 > 100
V−

TL/H/7761–3

*May be added to reduce internal dissipation

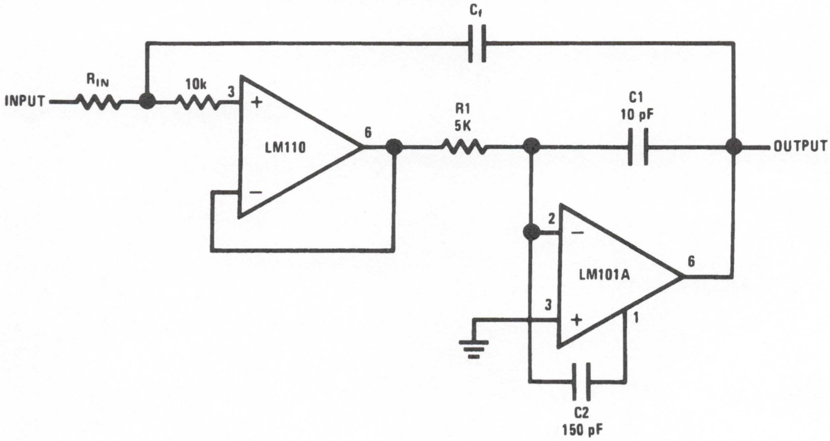
# Typical Applications

### Differential Input Instrumentation Amplifier


LM110
−
10k
3
+
6
8
1
R2
1K
0.1%
R4
100K
0.1%
V+
INPUTS
BALANCE
R1
1K
2
−
LM107
OUTPUT
3
+
R4/R2 = R5/R3
A_V = R4/R2
+
10k
3
8
1
LM110
−
6
R3
1K
0.1%
R5
100K
0.1%

TL/H/7761–4

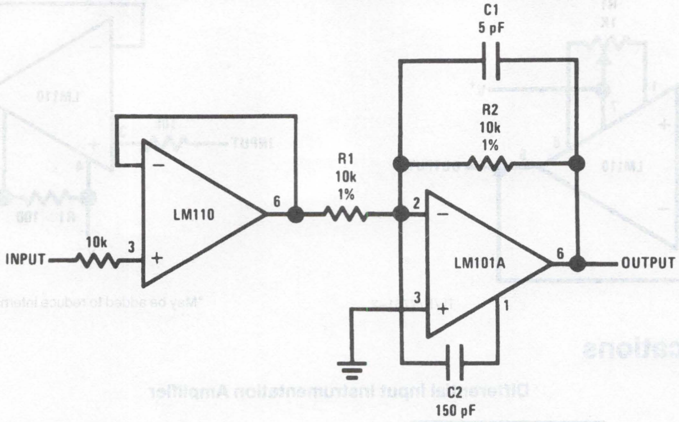
### Fast Integrator with Low Input Current


C_f
R_IN
INPUT
10k
3
+
LM110
−
6
R1
5K
C1
10 pF
OUTPUT
2
−
LM101A
6
3
+
1
C2
150 pF

TL/H/7761–5

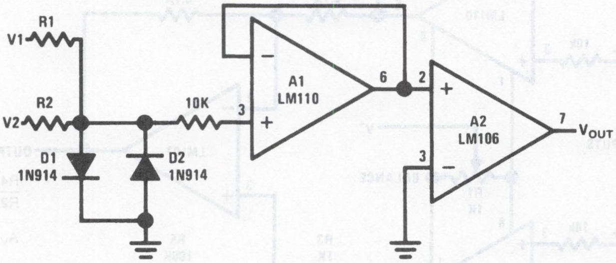
## Typical Applications (Continued)

### Fast Inverting Amplifier with High Input Impedance


C1
5 pF
R2
10k
1%
R1
10k
1%
LM110
LM101A
INPUT
10k
OUTPUT
C2
150 pF
6
2
3
1

TL/H/7761-6

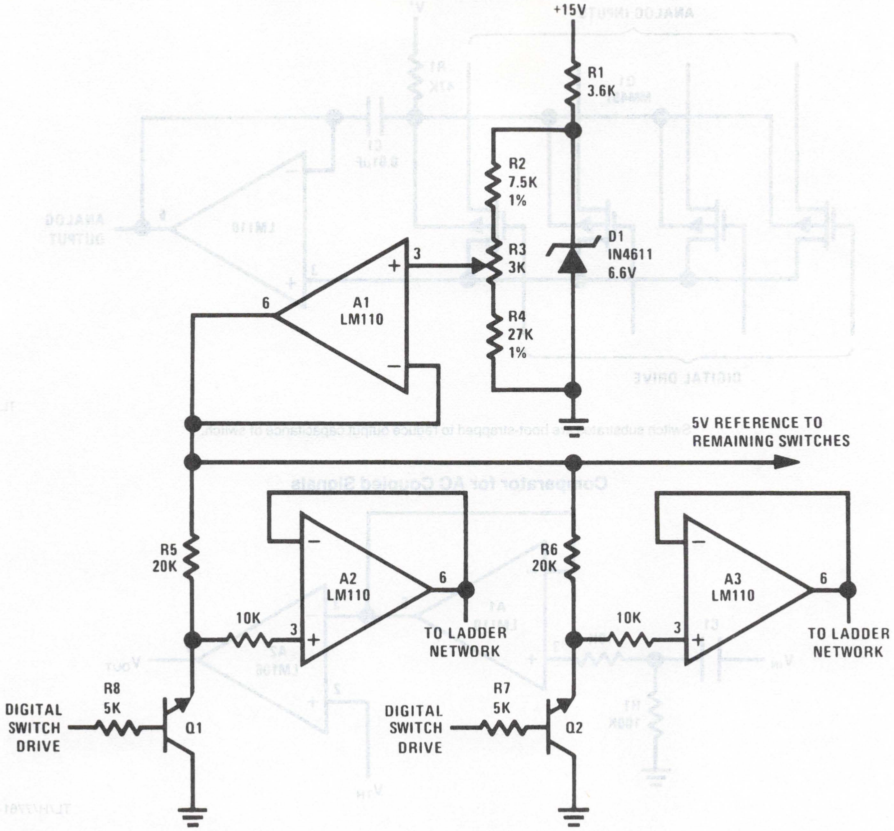
### Comparator for Signals of Opposite Polarity


R1
V1
R2
V2
10K
D1
1N914
D2
1N914
A1
LM110
A2
LM106
VOUT
6
2
3
7

TL/H/7761-7

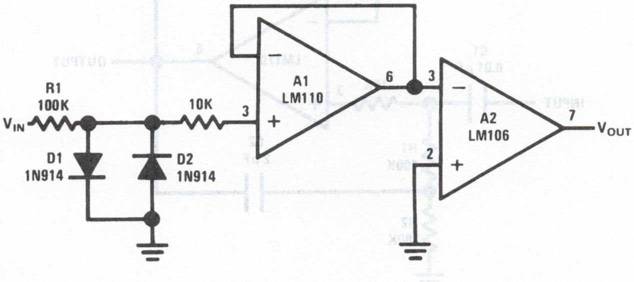
## Typical Applications (Continued)

### Driver for A/D Ladder Network


+15V
R1
3.6K
R2
7.5K
1%
R3
3K
R4
27K
1%
D1
IN4611
6.6V
3
+
A1
LM110
6
−
5V REFERENCE TO
REMAINING SWITCHES
R5
20K
−
A2
LM110
6
10K
3
+
TO LADDER
NETWORK
R6
20K
−
A3
LM110
6
10K
3
+
TO LADDER
NETWORK
DIGITAL
SWITCH
DRIVE
R8
5K
Q1
DIGITAL
SWITCH
DRIVE
R7
5K
Q2

TL/H/7761-8

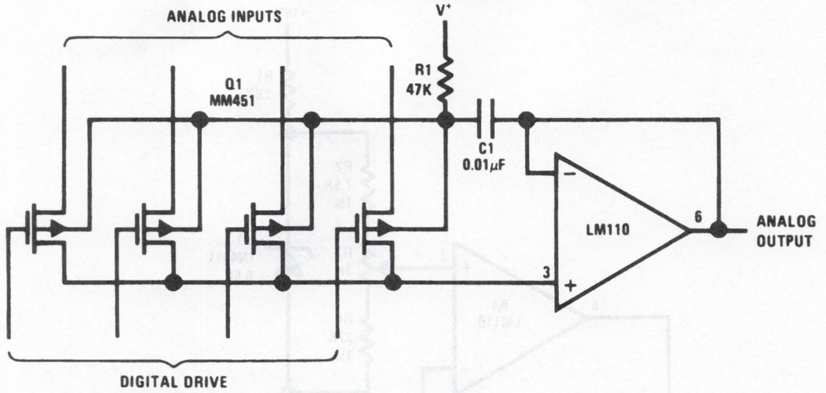
### Zero Crossing Detector


R1
100K
$V_{IN}$
D1
1N914
D2
1N914
10K
3
+
−
A1
LM110
6
3
−
A2
LM106
7
$V_{OUT}$
2
+

TL/H/7761-9

## Typical Applications (Continued)

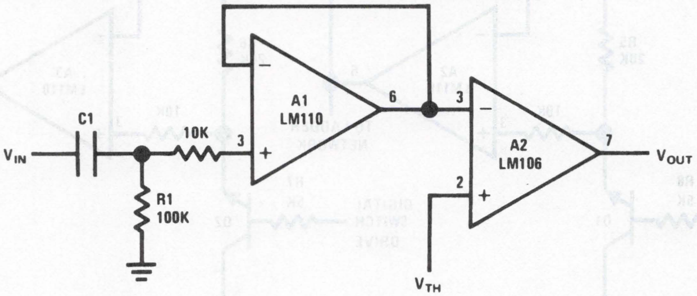
### Buffer for Analog Switch*


ANALOG INPUTS
V+
Q1
MM451
R1
47K
C1
0.01µF
LM110
6
3
−
+
ANALOG OUTPUT
DIGITAL DRIVE

TL/H/7761-10

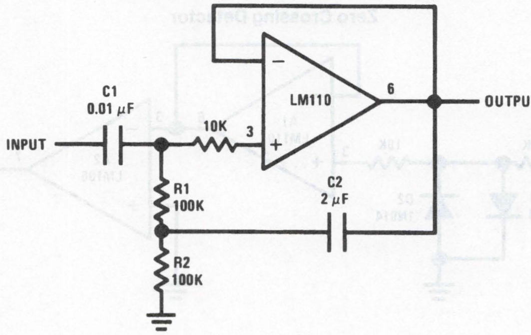
*Switch substrates are boot-strapped to reduce output capacitance of switch.

### Comparator for AC Coupled Signals


C1
V_IN
10K
R1
100K
3
+
−
A1
LM110
6
3
2
A2
LM106
7
V_OUT
V_TH

TL/H/7761-11

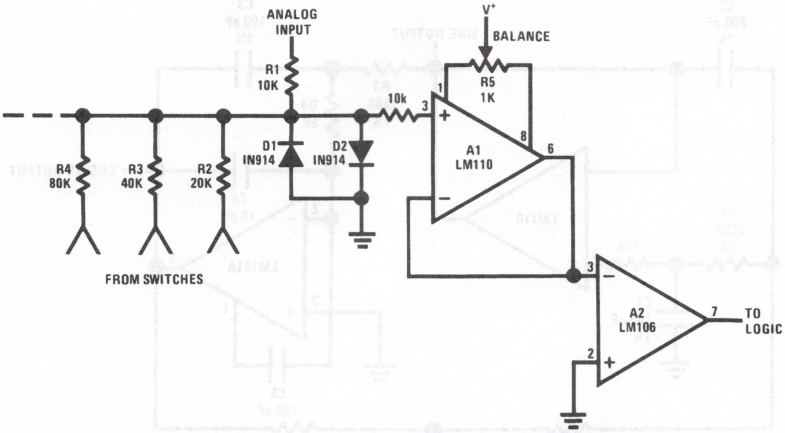
### High Input Impedance AC Amplifier


C1
0.01 µF
INPUT
10K
3
+
−
LM110
6
OUTPUT
R1
100K
C2
2 µF
R2
100K

TL/H/7761-12

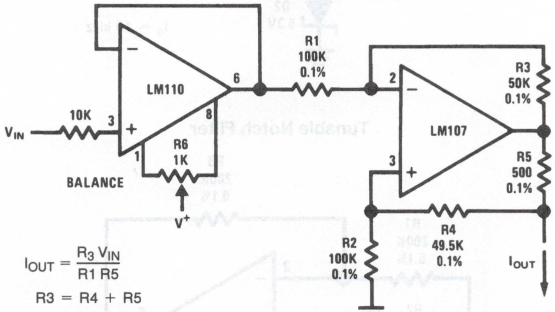
## Typical Applications (Continued)

### Comparator for A/D Converter Using a Binary-Weighted Network


ANALOG INPUT
V⁺
BALANCE
R1 10K
R5 1K
10k
1
3
+
8
6
A1 LM110
−
D1 IN914
D2 IN914
R4 80K
R3 40K
R2 20K
FROM SWITCHES
3
−
A2 LM106
7
TO LOGIC
2
+

TL/H/7761–13

### Bilateral Current Source


−
LM110
6
R1 100K 0.1%
2
−
R3 50K 0.1%
10K
3
+
8
V_IN
R6 1K
1
BALANCE
V⁺
LM107
3
+
R5 500 0.1%
R4 49.5K 0.1%
R2 100K 0.1%
I_OUT

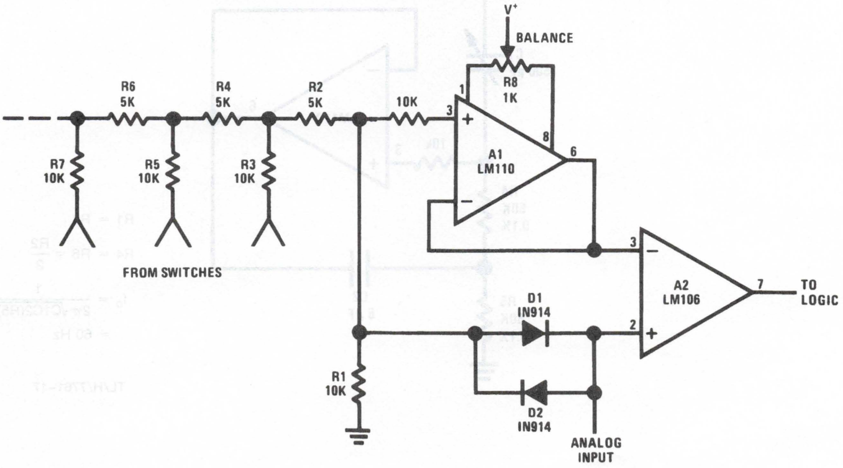
$$I_{OUT} = \frac{R_3 V_{IN}}{R1\ R5}$$

$$R3 = R4 + R5$$

$$R1 = R2$$

TL/H/7761–14

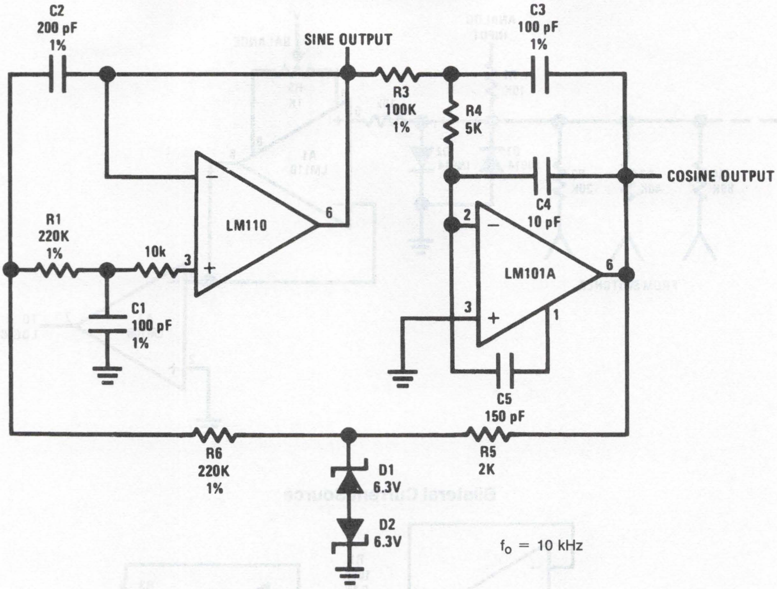
### Comparator for A/D Converter Using a Ladder Network


V⁺
BALANCE
R8 1K
R6 5K
R4 5K
R2 5K
10K
1
3
+
8
6
A1 LM110
−
R7 10K
R5 10K
R3 10K
FROM SWITCHES
3
−
A2 LM106
7
TO LOGIC
2
+
D1 IN914
D2 IN914
R1 10K
ANALOG INPUT

TL/H/7761–15

## Typical Applications (Continued)

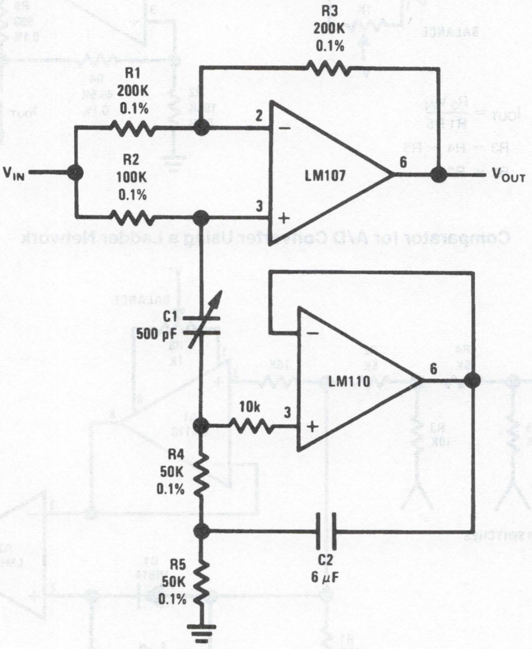
### Sine Wave Oscillator


C2
200 pF
1%
SINE OUTPUT
C3
100 pF
1%
R3
100K
1%
R4
5K
COSINE OUTPUT
C4
10 pF
LM110
LM101A
R1
220K
1%
10k
C1
100 pF
1%
C5
150 pF
R6
220K
1%
R5
2K
D1
6.3V
D2
6.3V
2
3
6
1

$f_o$ = 10 kHz

TL/H/7761–16

### Tunable Notch Filter


R3
200K
0.1%
R1
200K
0.1%
R2
100K
0.1%
$V_{IN}$
LM107
$V_{OUT}$
2
3
6
C1
500 pF
LM110
10k
R4
50K
0.1%
C2
6 µF
R5
50K
0.1%

$$R1 = R3$$

$$R4 = R6 = \frac{R2}{2}$$

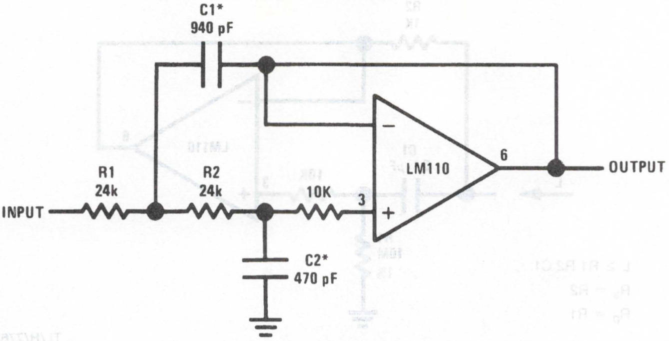
$$f_o = \frac{1}{2\pi\sqrt{C1C2(R5)^2}}$$

$$= 60\ \text{Hz}$$

TL/H/7761–17

## Typical Applications (Continued)

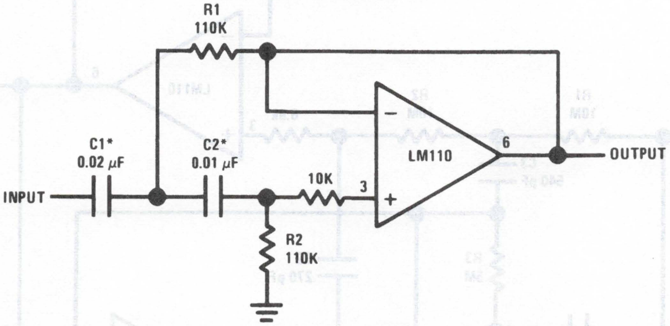
### Low Pass Active Filter


C1*
940 pF
R1
24k
R2
24k
10K
INPUT
3
6
LM110
OUTPUT
C2*
470 pF

TL/H/7761–18

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

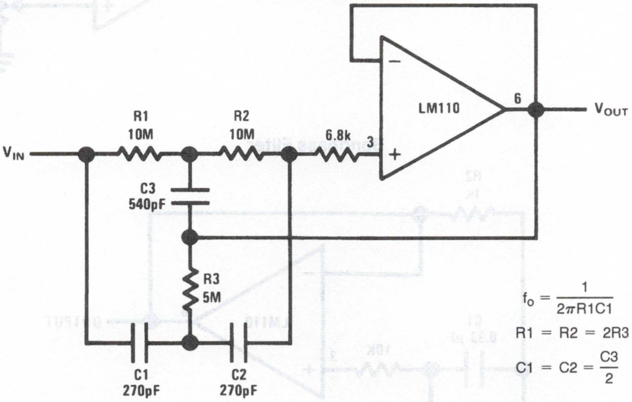
### High Pass Active Filter


R1
110K
C1*
0.02 μF
C2*
0.01 μF
10K
INPUT
3
6
LM110
OUTPUT
R2
110K

TL/H/7761–19

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

### High Q Notch Filter


LM110
6
V_OUT
R1
10M
R2
10M
6.8k
3
V_IN
C3
540pF
R3
5M
C1
270pF
C2
270pF

$$f_o = \frac{1}{2\pi R1C1}$$

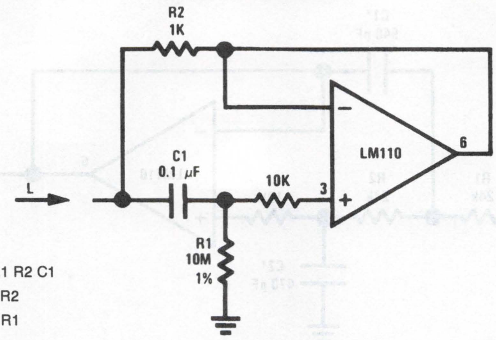
$$R1 = R2 = 2R3$$

$$C1 = C2 = \frac{C3}{2}$$

TL/H/7761–20

## Typical Applications (Continued)

### Simulated Inductor


R2
1K
LM110
6
C1
0.1 μF
10K
3
L
R1
10M
1%

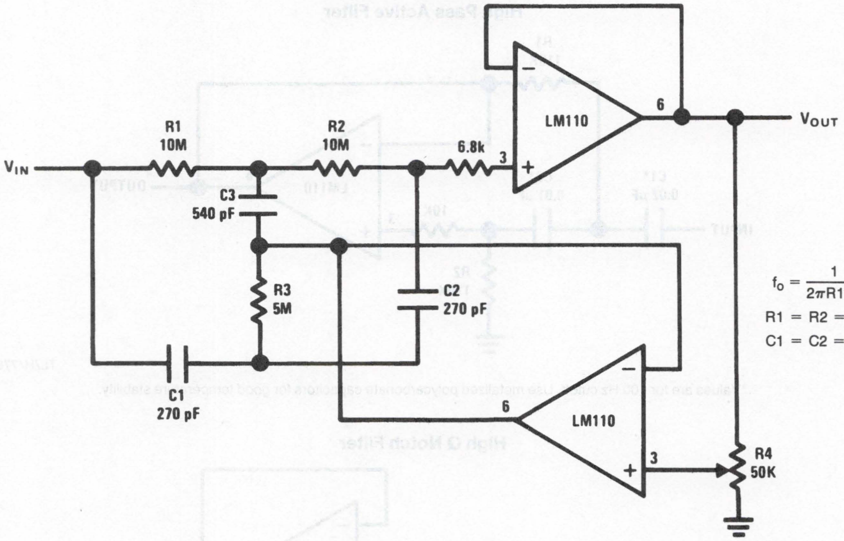
L ≥ R1 R2 C1

$R_s$ = R2

$R_p$ = R1

TL/H/7761-21

### Adjustable Q Notch Filter


LM110
6
$V_{OUT}$
R1
10M
R2
10M
6.8k
3
$V_{IN}$
C3
540 pF
R3
5M
C2
270 pF
C1
270 pF
6
LM110
3
R4
50K

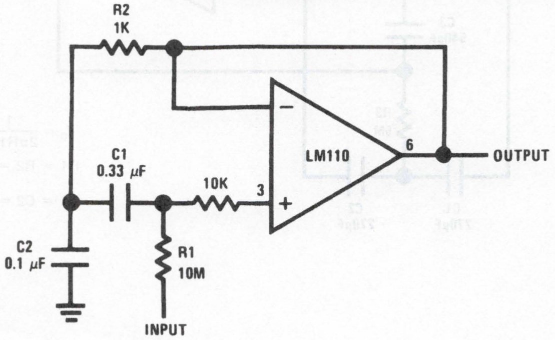
$$f_o = \frac{1}{2\pi R1C1}$$

R1 = R2 = 2R3

C1 = C2 = C3/2

TL/H/7761-22

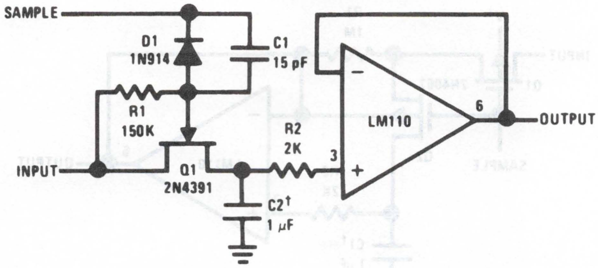
### Bandpass Filter


R2
1K
LM110
6
OUTPUT
C1
0.33 μF
10K
3
C2
0.1 μF
R1
10M
INPUT

TL/H/7761-23

## Typical Applications (Continued)

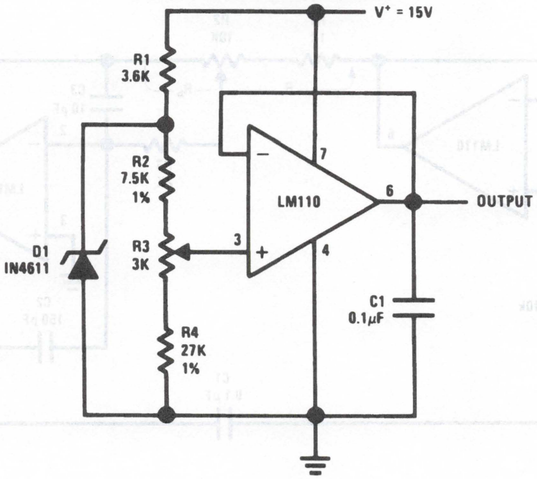
### Sample and Hold


SAMPLE
D1
1N914
C1
15 pF
R1
150K
R2
2K
INPUT
Q1
2N4391
C2†
1 μF
3
LM110
6
OUTPUT

TL/H/7761–24

†Use capacitor with polycarbonate teflon or polythylene dietetric

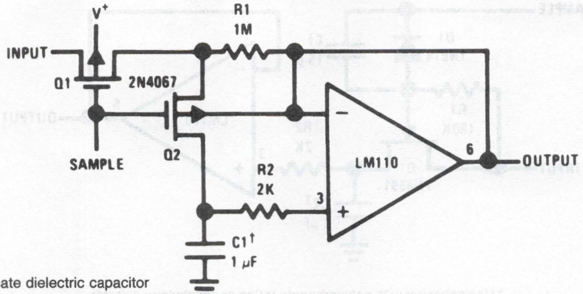
### Buffered Reference Source


V+ = 15V
R1
3.6K
R2
7.5K
1%
R3
3K
R4
27K
1%
D1
IN4611
7
LM110
6
3
4
OUTPUT
C1
0.1μF

TL/H/7761–25

## Typical Applications (Continued)

### Low Drift Sample and Hold*


V⁺
R1
1M
INPUT
Q1
2N4067
SAMPLE
Q2
−
R2
2K
LM110
6
OUTPUT
3
+
C1†
1 μF

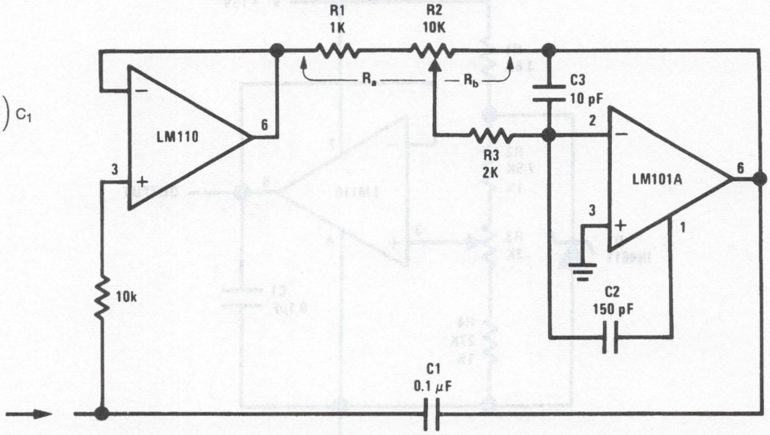
†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV/sec

TL/H/7761-26

### Variable Capacitance Multiplier

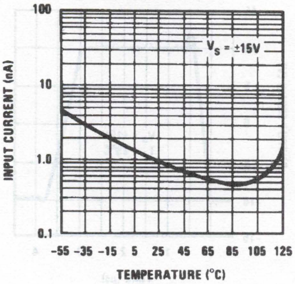
$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$


R1
1K
R2
10K
Ra
Rb
C3
10 pF
2
−
LM110
6
3
+
R3
2K
LM101A
6
3
+
1
10k
C2
150 pF
C1
0.1 μF

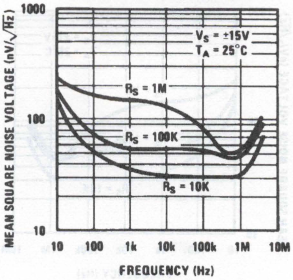
TL/H/7761-27

# Typical Performance Characteristics (LM110/LM210)

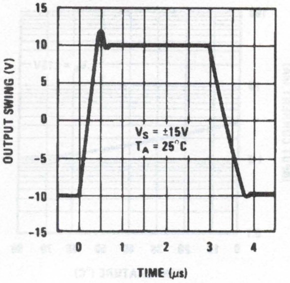
### Input Current



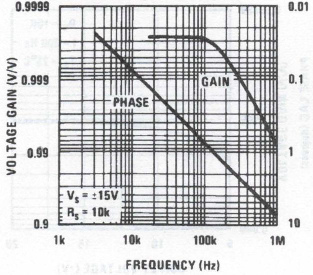
### Output Noise Voltage



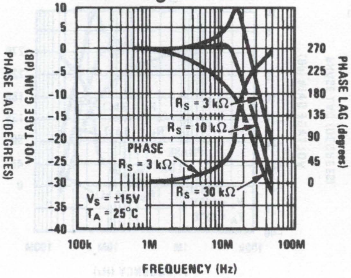
### Large Signal Pulse Response



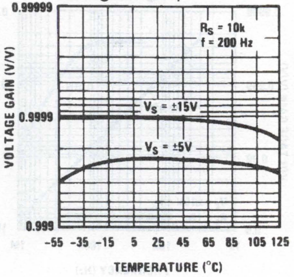
### Voltage Gain and Phase Lag



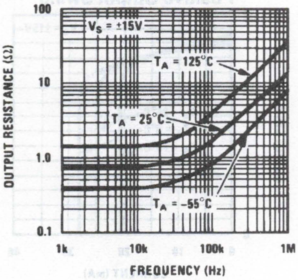
### Voltage Gain and Phase Lag



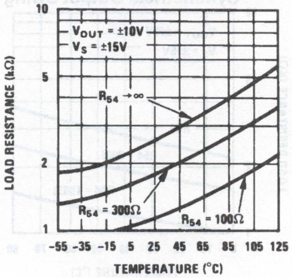
### Voltage Gain



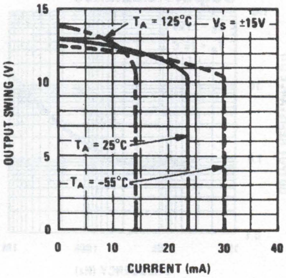
### Output Resistance



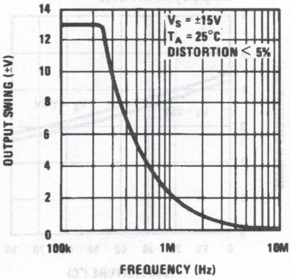
### Symmetrical Output Swing



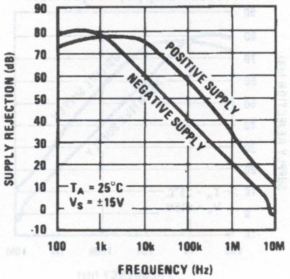
### Positive Output Swing



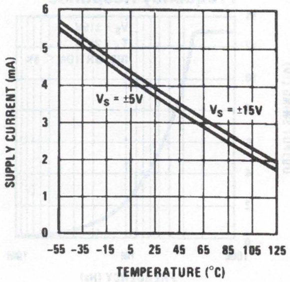
### Large Signal Frequency Response



### Power Supply Rejection



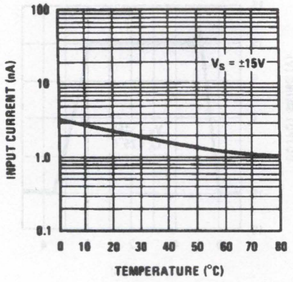
### Supply Current



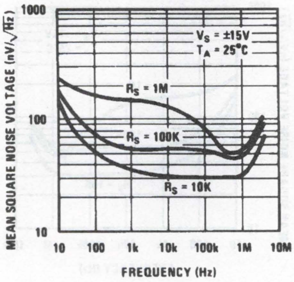
TL/H/7761-28

## Typical Performance Characteristics (LM310)

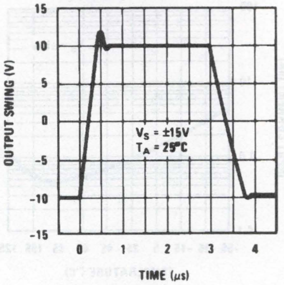
### Input Current



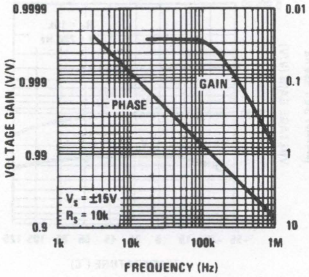
### Output Noise Voltage



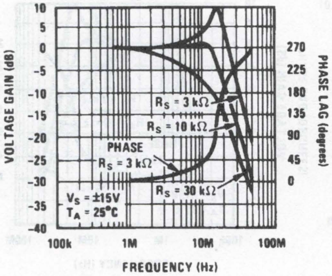
### Large Signal Pulse Response



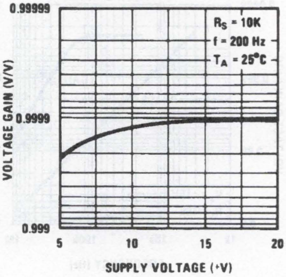
### Voltage Gain and Phase Lag



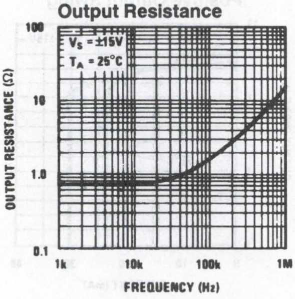
### Voltage Gain and Phase Lag



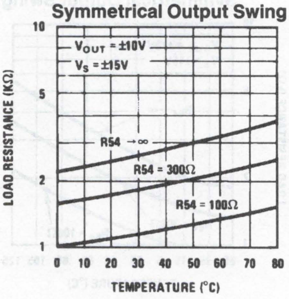
### Voltage Gain



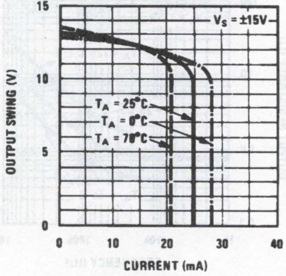
### Output Resistance



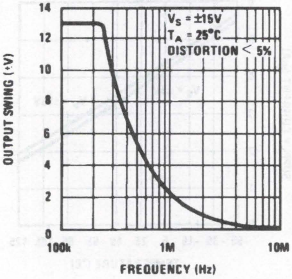
### Symmetrical Output Swing



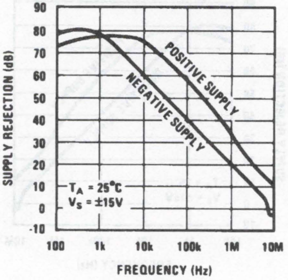
### Positive Output Swing



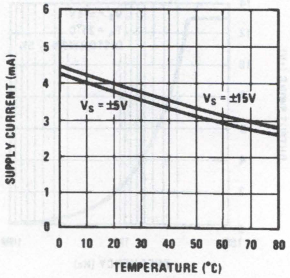
### Large Signal Frequency Response



### Power Supply Rejection



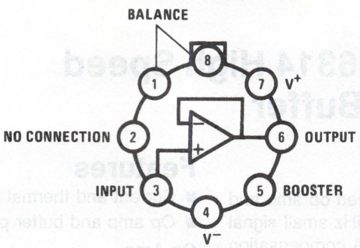
### Supply Current



TL/H/7761-29

## Connection Diagrams

**Metal Can Package**


BALANCE
8
1
7
V+
NO CONNECTION
2
6
OUTPUT
INPUT
3
5
BOOSTER
4
V−
−
+

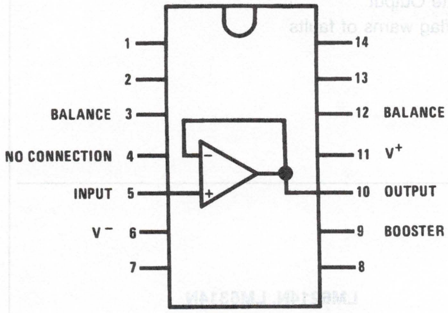
TL/H/7761–30

Package is connected to Pin 4 ($V^-$)

**Top View**

**Order Number LM110H, LM210H or LM310H**
**See NS Package Number H08C**

**Dual-In-Line Package**


1
2
BALANCE 3
NO CONNECTION 4
INPUT 5
V− 6
7
14
13
12 BALANCE
11 V+
10 OUTPUT
9 BOOSTER
8
−
+

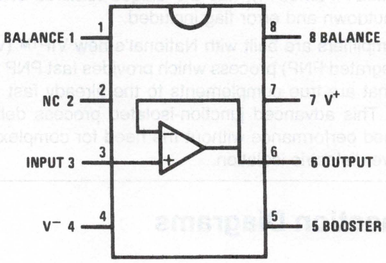
TL/H/7761–31

**Note:** Pin 6 connected to bottom of package.

**Top View**

**Order Number LM110J, LM210J or LM310J**
**See NS Package Number J14A**

**Dual-In-Line Package**


BALANCE 1
1
NC 2
2
INPUT 3
3
V− 4
4
8
8 BALANCE
7
7 V+
6
6 OUTPUT
5
5 BOOSTER
−
+

TL/H/7761–32

**Top View**

**Order Number LM310M or LM310N**
**See NS Package Number M08A or N08E**

**National Semiconductor Corporation**

**ADVANCED INFORMATION**

# LM6113/LM6214/LM6314 High Speed Op Amp Plus Power Buffer

## General Description

The LM6113 family is a combined high speed op amp and power buffer. The op amp features a 40 MHz small signal bandwidth, and a fast 240V/μs slew rate. A compensation pin is included for altering the open loop bandwidth and slew rate if desired. The op amp and buffer are pinned out separately, and can be used independently or in combination. The buffer has a 50 MHz small signal bandwidth and slews at 700V/μs into a 50Ω load and can deliver ±300 mA output current. The buffer includes protection in the form of current limit and thermal shutdown. The 16 pin plastic version, (LM6214/LM6314), has the unique features of electronic shutdown and error flag included.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

## Features

- Current and thermal limiting
- Op amp and buffer pinned out separately

**Op Amp**

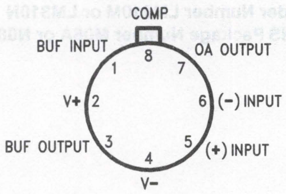
| | |
|---|---|
| ■ Wide bandwidth | 40 MHz |
| ■ High slew rate | 240V/μs |

**Buffer**

| | |
|---|---|
| ■ High slew rate (Into 50Ω) | 700V/μs |
| ■ Wide bandwidth | 50 MHz |
| ■ Electronic shutdown | |
| ■ Bi-State Output | |
| ■ Error flag warns of faults | |

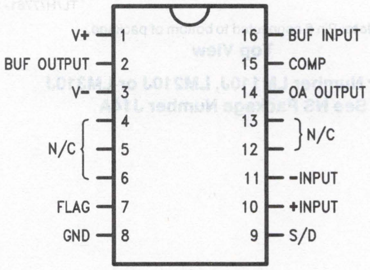
## Connection Diagrams

**LM6113H**



TL/H/9224-1

**LM6214N, LM6314N**



TL/H/9224-2

**Order Number LM6113H, LM6214N or LM6314N**
**See NS Package Number H08A or N16A**

**National Semiconductor Corporation**

**ADVANCED INFORMATION**

# LM6121/LM6221/LM6321 High Speed Buffer

## General Description

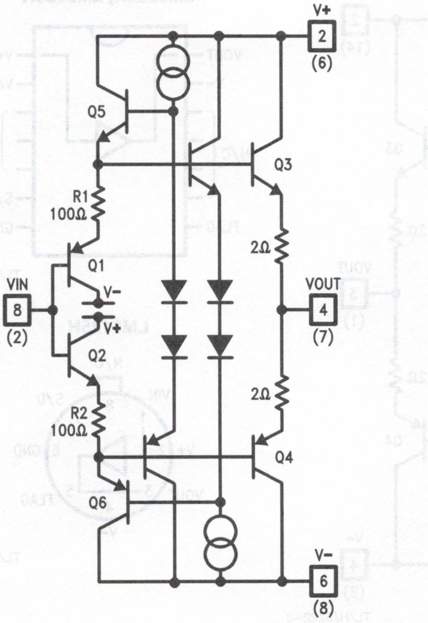
The LM6121 family of high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers can deliver ±300 mA, and do not oscillate while driving large capacitive loads. The LM6121 features performance which is superior to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true compliments to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

## Features

| | |
|---|---|
| ■ High Slew Rate (into 50Ω) | 800 V/μs |
| ■ Wide Bandwidth (into 50Ω) | 50 MHz |
| ■ Peak Output Current | ±300 mA |
| ■ High Input Impedance | 5 MΩ |
| ■ LH0002H pin compatible | |
| ■ No oscillations with Capacitive loads | |
| ■ 5V to ±16V operation | |
| ■ Current and Thermal Limiting | |
| ■ Slew Rate 100% tested | |

## Simplified Schematic

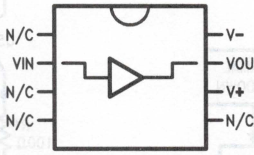


TL/H/9223-1

Numbers in ( ) are for 8 pin N DIP

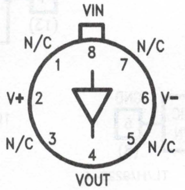
## Pin Configurations

**LM6221N**
**LM6321N**



TL/H/9223-2

**LM6121H**



TL/H/9223-3

**Order Number LM6121H, LM6221N or LM6321N**
**See NS Package Number H08A or N08E**

**National Semiconductor Corporation**

**ADVANCED INFORMATION**

# LM6125/LM6225/LM6325 High Speed Buffer

## General Description

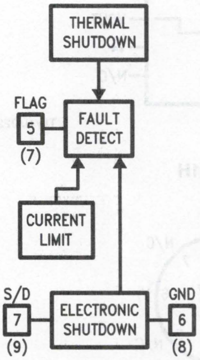
The LM6125 family of high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers can drive ±300 mA, and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers, these include: current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true compliments to the already fast NPN devices. This advanced junction-isolated process delivers high-speed performance without the need for complex and expensive dielectric isolation.

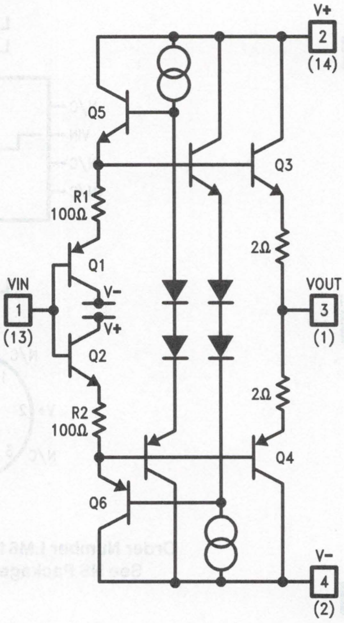
## Features

- High slew rate (into 50Ω) 800 Vμs
- Wide bandwidth (into 50Ω) 50 MHz
- Peak output current ±300 mA
- High input impedance 5 MΩ
- No oscillations with capactive loads
- Current and thermal limiting
- Electronic shutdown
- Bi-state output
- Error flag warns of faults
- Slew rate 100% tested

## Simplified Schematic


THERMAL SHUTDOWN
FLAG
5
(7)
FAULT DETECT
CURRENT LIMIT
S/D
7
(9)
ELECTRONIC SHUTDOWN
GND
6
(8)

TL/H/9222-1

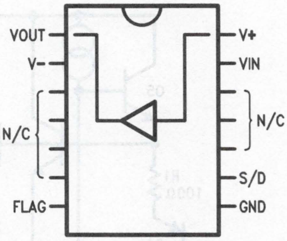

V+
2
(14)
Q5
Q3
R1
100Ω
Q1
VIN
1
(13)
V−
V+
Q2
R2
100Ω
2Ω
VOUT
3
(1)
2Ω
Q4
Q6
V−
4
(2)

Numbers in ( ) are for 14 pin N DIP.

TL/H/9222-2

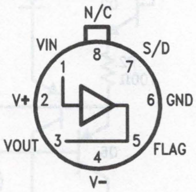
## Pin Configurations

**LM6225N, LM6325N**


VOUT
V−
N/C
FLAG
V+
VIN
N/C
S/D
GND

TL/H/9222-3

**LM6125H**


N/C
8
VIN
1
S/D
7
V+
2
6
GND
VOUT
3
5
FLAG
4
V−

TL/H/9222-4

**Order Number LM6125H, LM6225N or LM6325N**
**See NS Package Number H08A or N14A**

# Section 4

# Voltage Comparators

# Section 4 Contents

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Voltage Comparators Selection Guide . . . . . 4-4
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LM111/LM211/LM311 Voltage Comparator . . . . . 4-18
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LM139/LM239/LM339/LM139A/LM239A/LM339A, LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators . . . . . 4-37
LM160/LM260/LM360 High Speed Differential Comparator . . . . . 4-49
LM161/LM261/LM361 High Speed Differential Comparator . . . . . 4-53
LM193/LM293/LM393, LM193A, LM293A, LM393A, LM2903 Low Power Low Offset Voltage Dual Comparator . . . . . 4-58
LP165/LP365 Micropower Programmable Quad Comparator . . . . . 4-67
LP311 Voltage Comparator . . . . . 4-75
LP339 Ultra-Low Power Quad Comparator . . . . . 4-79

# Voltage Comparators Definition of Terms

**Input Bias Current:** The average of the two input currents.

**Input Offset Current:** The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

**Input Offset Voltage:** The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

**Input Voltage Range:** The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

**Logic Threshold Voltage:** The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

**Negative Output Level:** The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

**Output Leakage Current:** The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

**Output Resistance:** The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

**Output Sink Current:** The maximum negative current that can be delivered by the comparator.

**Positive Output Level:** The high output voltage level with a given load and the input drive equal to or greater than a specified value.

**Power Consumption:** The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

**Response Time:** The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

**Saturation Voltage:** The low-output voltage level with the input drive equal to or greater than a specified value.

**Strobe Current:** The current out of the strobe terminal when it is at the zero logic level.

**Strobe Output Level:** The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

**Strobe "ON" Voltage:** The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

**Strobe "OFF" Voltage:** The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

**Strobe Release Time:** The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

**Supply Current:** The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

**Voltage Gain:** The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

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Semiconductor
Corporation

# Voltage Comparators Selection Guide

| | Response Time (Typ) ns | $V_{OS}$ mV(Max) | $I_S$ mA(Max) | $I_B$ nA(Max) | Comments |
|---|---|---|---|---|---|
| $T_A = 25°C$ (Notes 1 and 2) | | | | | |
| LM361 | 12 | 5 | 25 | 30,000 | High Speed w/Strobes |
| LM360 | 16 | 5 | 32 | 20,000 | High Speed, Complementary Outputs |
| LM306 | 40 | 5 | 10 | 25,000 | High Speed, High Drive |
| LM319 | 80 | 8 | 12.5 | 1000 | High Speed Dual |
| LF311 | 200 | 10 | 7.5 | 0.15 | FET Input |
| LM311 | 200 | 10 | 7.5 | 300 | General Purpose Single |
| LM339 | 1300 | 5 | 2 | 400 | General Purpose Quad |
| LM392 | 1300 | 10 | 1 | 400 | One Comparator Plus One Op Amp |
| LM393 | 1300 | 5 | 2.5 | 250 | General Purpose Dual |
| LM2903 | 1300 | 5 | 2.5 | 250 | Automotive Dual |
| LM2901 | 1300 | 7 | 2 | 400 | Automotive Quad |
| LP365 | 4000 | 9 | 0.30 | 200 | Programmable Quad |
| LP311 | 4000 | 10 | 0.3 | 150 | Low Power Single |
| LP339 | 5000 | 9 | 0.1 | 40 | Low Power Quad |

*Not Specified

**Note 1:** Datasheet should be referred to for test conditions and more detailed information.

**Note 2:** This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

**National Semiconductor Corporation**

# LF111/LF211/LF311 Voltage Comparators

## General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

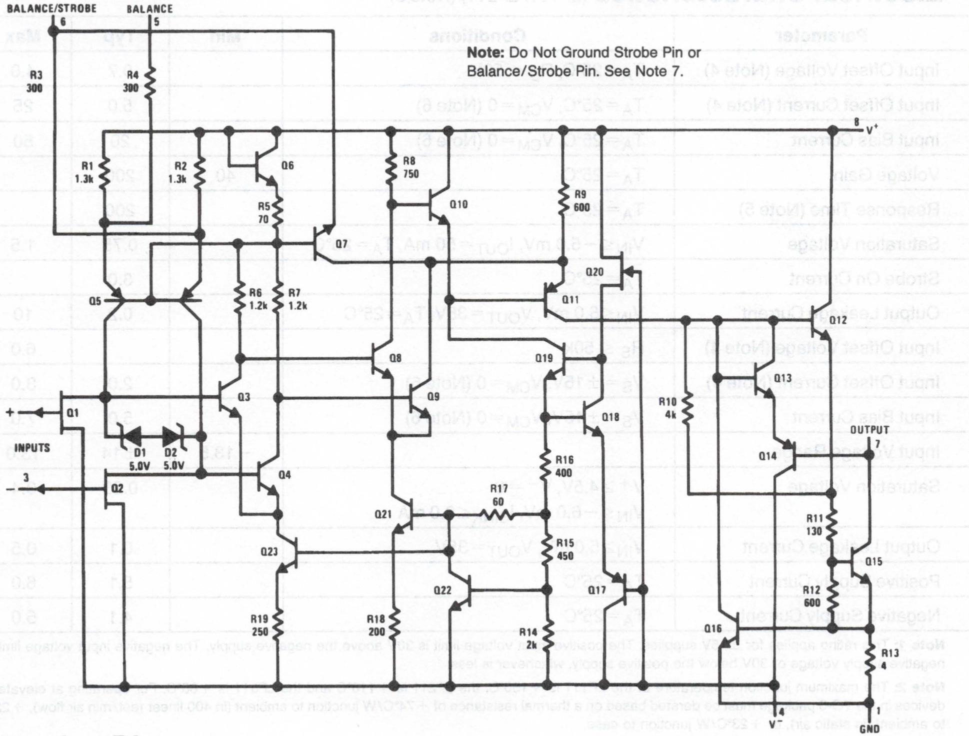
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

## Features

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

## Schematic Diagram

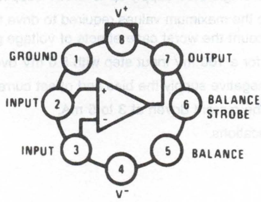

BALANCE/STROBE
6
BALANCE
5
R3 300
R4 300
R1 1.3k
R2 1.3k
Q6
R5 70
R8 750
Q10
R9 600
8
V+
Q7
Q5
R6 1.2k
R7 1.2k
Q20
Q11
Q12
Q8
Q19
Q13
+
Q1
Q3
Q9
R10 4k
Q18
INPUTS
D1 5.0V
D2 5.0V
OUTPUT
7
3
Q2
Q4
Q14
R16 400
R17 60
Q21
R11 130
Q23
R15 450
Q15
Q22
Q17
R12 600
R19 250
R18 200
R14 2k
Q16
R13
4
V-
1
GND

**Note:** Do Not Ground Strobe Pin or Balance/Strobe Pin. See Note 7.

TL/H/5703-2

## Connection Diagram

**Metal Can Package**


V+
8
GROUND
1
7
OUTPUT
INPUT
2
+
-
6
BALANCE/
STROBE
INPUT
3
5
BALANCE
4
V-

TL/H/5703-1

**Top View**

**Order Number LF111H, LF211H or LF311H**

**See NS Package Number H08C**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 8)**

| | LF111/LF211 | LF311 |
|---|---|---|
| Total Supply Voltage ($V_{84}$) | 36V | 36V |
| Output to Negative Supply Voltage ($V_{74}$) | 50V | 40V |
| Ground to Negative Supply Voltage ($V_{14}$) | 30V | 30V |
| Differential Input Voltage | ±30V | ±30V |
| Input Voltage (Note 1) | ±15V | ±15V |
| Power Dissipation (Note 2) | 500 mW | 500 mW |
| Output Short Circuit Duration | 10 seconds | 10 seconds |

| | LF111/LF211 | LF311 |
|---|---|---|
| Operating Temp. Range | | |
| LF111 | −55°C to +125°C | |
| LF211 | −25°C to +85°C | |
| LF311 | | 0°C to +70°C |
| Storage Temp. Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C | 300°C |

ESD rating to be determined.

## Electrical Characteristics (LF111/LF211) (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C$, $R_S \le 50k$ | | 0.7 | 4.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$, $V_{CM} = 0$ (Note 6) | | 5.0 | 25 | pA |
| Input Bias Current | $T_A = 25°C$, $V_{CM} = 0$ (Note 6) | | 20 | 50 | pA |
| Voltage Gain | $T_A = 25°C$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \le -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$ | | 0.75 | 1.5 | V |
| Strobe On Current | $T_A = 25°C$ | | 3.0 | | mA |
| Output Leakage Current | $V_{IN} \le 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$ | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \le 50k$ | | | 6.0 | mV |
| Input Offset Current (Note 4) | $V_S = \pm 15V$, $V_{CM} = 0$ (Note 6) | | 2.0 | 3.0 | nA |
| Input Bias Current | $V_S = \pm 15V$, $V_{CM} = 0$ (Note 6) | | 5.0 | 7.0 | nA |
| Input Voltage Range | | −13.5 | ±14 | 13.0 | V |
| Saturation Voltage | $V^+ \ge 4.5V$, $V^- = 0$<br>$V_{IN} \le -6.0$ mV, $I_{SINK} \le 8.0$ mA | | 0.23 | 0.4 | V |
| Output Leakage Current | $V_{IN} \ge 5.0$ mV, $V_{OUT} = 35V$ | | 0.1 | 0.5 | µA |
| Positive Supply Current | $T_A = 25°C$ | | 5.1 | 6.0 | mA |
| Negative Supply Current | $T_A = 25°C$ | | 4.1 | 5.0 | mA |

**Note 1:** This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

**Note 2:** The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +74°C/W junction to ambient (in 400 linear feet/min air flow), +225°C/W junction to ambient (in static air), or +23°C/W junction to case.

**Note 3:** These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \le T_A \le +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \le T_A \le +85°C$ and for the LF311 $0°C \le T_A \le +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

**Note 5:** The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

**Note 6:** For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

**Note 7:** Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

**Note 8:** Refer to RETSF111X for LF111H military specifications.

## Electrical Characteristics (LF311) (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C$, $R_S \leq 50k$ | | 2.0 | 10 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$, $V_{CM} = 0$ (Note 6) | | 5.0 | 75 | pA |
| Input Bias Current | $T_A = 25°C$, $V_{CM} = 0$ (Note 6) | | 25 | 150 | pA |
| Voltage Gain | $T_A = 25°C$ | | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$ | | 0.75 | 1.5 | V |
| Strobe On Current | $T_A = 25°C$ | | 3.0 | | mA |
| Output Leakage Current | $V_{IN} \geq 10$mV, $V_{OUT} = 35$V, $T_A = 25°C$ | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50k$ | | | 15 | mV |
| Input Offset Current (Note 4) | $V_S = \pm 15$V, $V_{CM} = 0$ (Note 6) | | 1.0 | | nA |
| Input Bias Current | $V_S = 15$V, $V_{CM} = 0$ (Note 6) | | 3.0 | | nA |
| Input Voltage Range | | | +14<br>−13.5 | | V<br>V |
| Saturation Voltage | $V^+ \geq 4.5$V, $V^- = 0$<br>$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8.0$ mA | | 0.23 | 0.4 | V |
| Positive Supply Current | $T_A = 25°C$ | | 5.1 | 7.5 | mA |
| Negative Supply Current | $T_A = 25°C$ | | 4.1 | 5.0 | mA |

**Note 1:** This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

**Note 2:** The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

**Note 3:** These specifications apply for $V_S = \pm 15$V and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

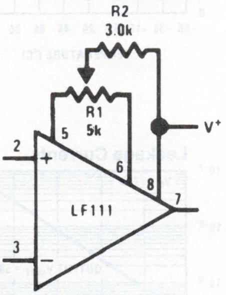
**Note 5:** The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

**Note 6:** For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

**Note 7:** Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

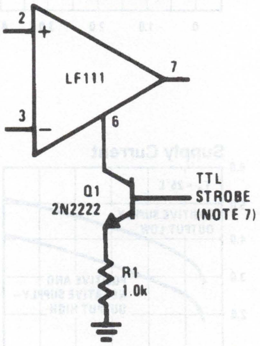
## Auxiliary Circuits

### Offset Balancing



TL/H/5703-13

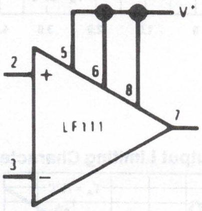
### Strobing



TL/H/5703-14

**Note:** Do Not Ground Strobe Pin.

### Increasing Input Stage Current*

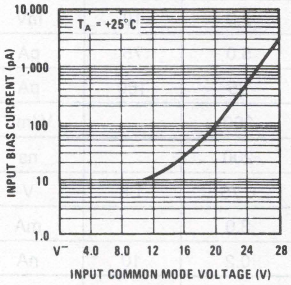


TL/H/5703-15

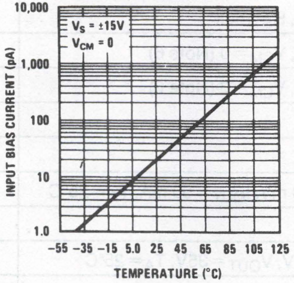
*Increases typical common mode slew from 7.0V/µs to 18V/µs

# Typical Performance Characteristics

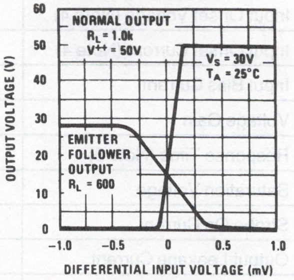
### Input Bias Current vs Common Mode



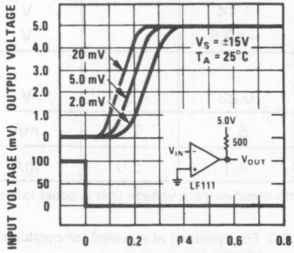
### Input Bias Current vs Temperature



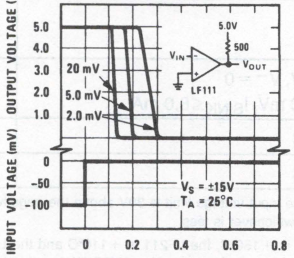
### Transfer Function



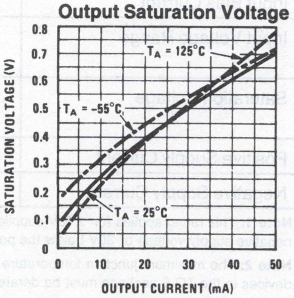
### Response Time for Various Input Overdrives



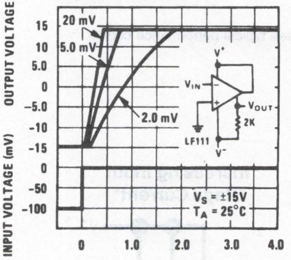
### Response Time for Various Input Overdrives



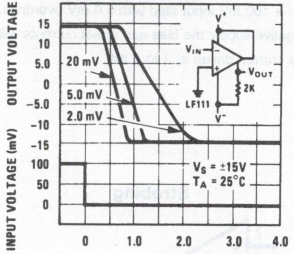
### Output Saturation Voltage



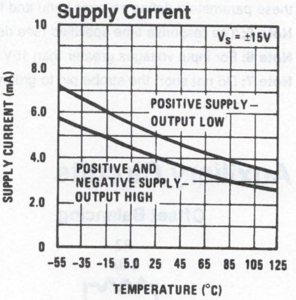
### Response Time for Various Input Overdrives



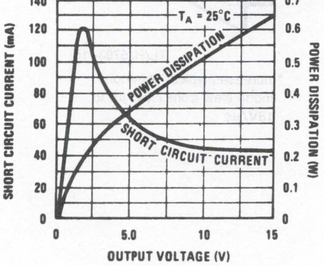
### Response Time for Various Input Overdrives



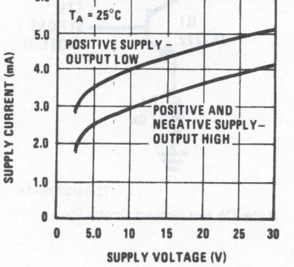
### Supply Current



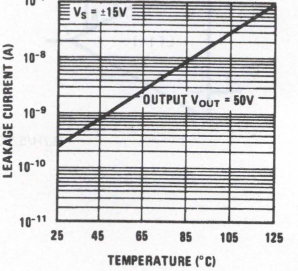
### Output Limiting Characteristics



### Supply Current



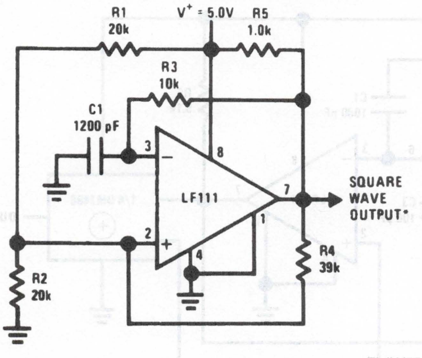
### Leakage Currents



TL/H/5703–4

# Typical Applications

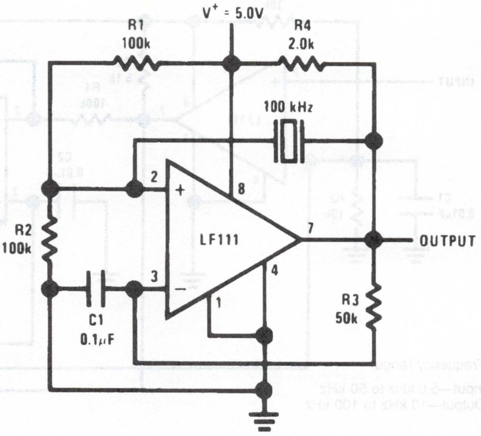
## 100 kHz Free Running Multivibrator


R1
20k
V+ = 5.0V
R5
1.0k
R3
10k
C1
1200 pF
3
8
LF111
7
1
2
4
SQUARE
WAVE
OUTPUT*
R4
39k
R2
20k

TL/H/5703-7

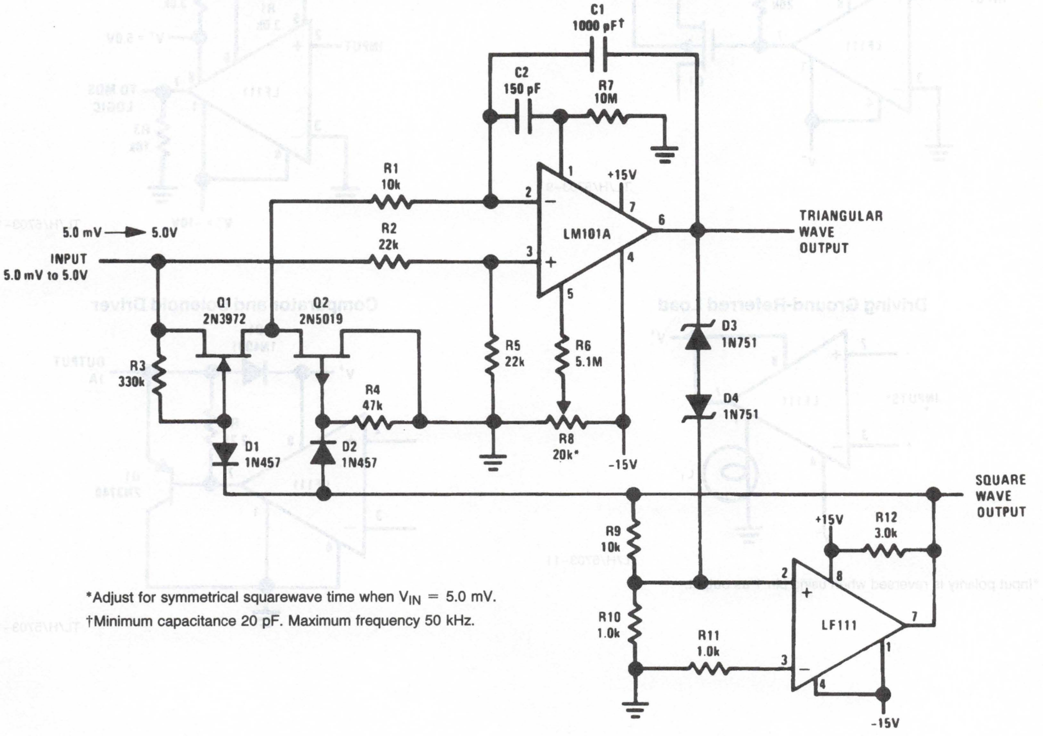
*TTL or DTL fanout of two.

## Crystal Oscillator


V+ = 5.0V
R1
100k
R4
2.0k
100 kHz
2
8
LF111
7
OUTPUT
R2
100k
3
4
1
C1
0.1μF
R3
50k

TL/H/5703-3

## 10 Hz to 10 kHz Voltage Controlled Oscillator


C1
1000 pF†
C2
150 pF
R7
10M
R1
10k
1
+15V
2
7
LM101A
6
TRIANGULAR
WAVE
OUTPUT
5.0 mV → 5.0V
INPUT
5.0 mV to 5.0V
R2
22k
3
4
5
Q1
2N3972
Q2
2N5019
D3
1N751
R3
330k
R5
22k
R6
5.1M
R4
47k
D4
1N751
D1
1N457
D2
1N457
R8
20k*
-15V
SQUARE
WAVE
OUTPUT
+15V
R12
3.0k
R9
10k
2
8
LF111
7
R10
1.0k
R11
1.0k
3
1
4
-15V

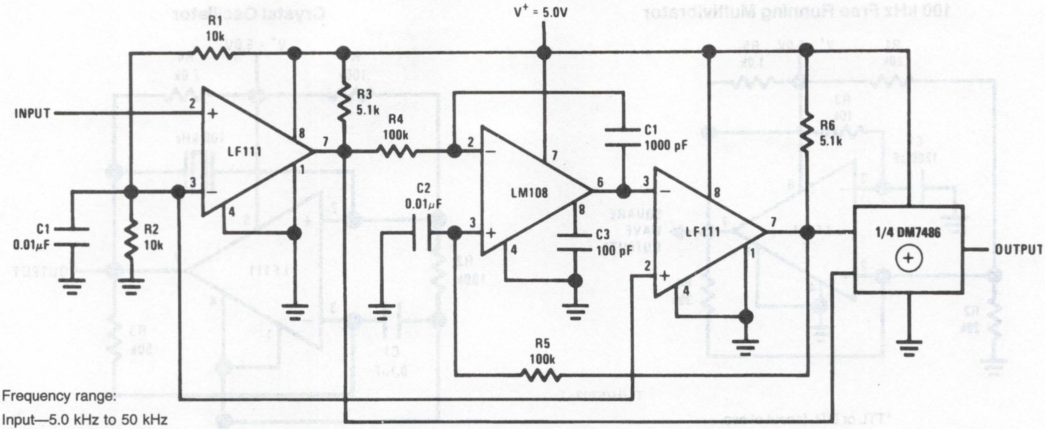
*Adjust for symmetrical squarewave time when $V_{IN}$ = 5.0 mV.

†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

TL/H/5703-5

## Typical Applications (Continued)

### Frequency Doubler

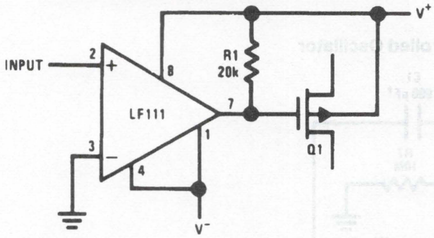

V+ = 5.0V
R1
10k
INPUT
LF111
R3
5.1k
R4
100k
C1
1000 pF
LM108
R6
5.1k
C2
0.01μF
C1
0.01μF
R2
10k
C3
100 pF
LF111
1/4 DM7486
OUTPUT
R5
100k

Frequency range:

Input—5.0 kHz to 50 kHz
Output—10 kHz to 100 kHz

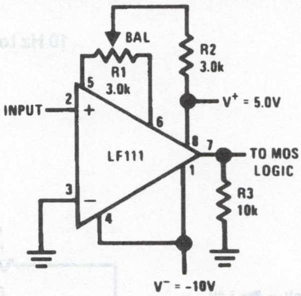
TL/H/5703–8

### Zero Crossing Detector Driving MOS Switch


V+
INPUT
LF111
R1
20k
Q1
V−

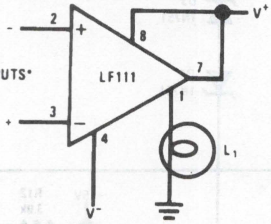
TL/H/5703–9

### Zero Crossing Detector Driving MOS Logic


BAL
R1
3.0k
R2
3.0k
INPUT
V+ = 5.0V
LF111
TO MOS LOGIC
R3
10k
V− = −10V

TL/H/5703–10

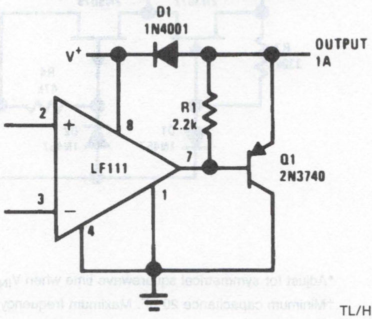
### Driving Ground-Referred Load


INPUTS*
LF111
V+
L1
V−

TL/H/5703–11

*Input polarity is reversed when using pin 1 as output.

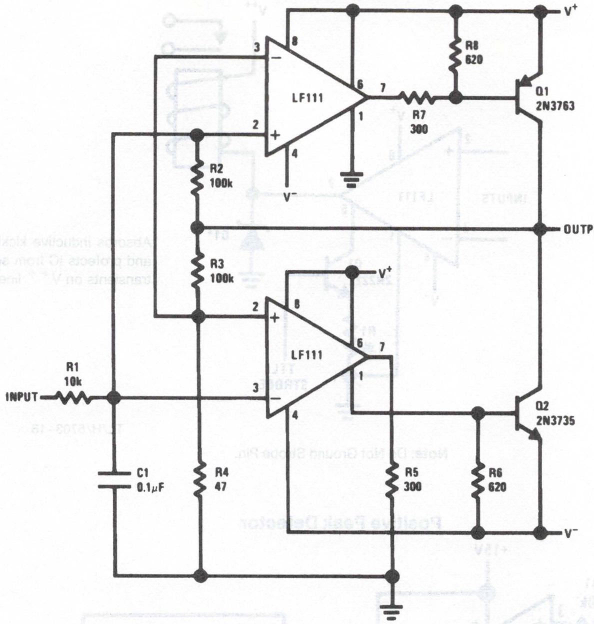
### Comparator and Solenoid Driver


D1
1N4001
V+
OUTPUT
1A
R1
2.2k
LF111
Q1
2N3740

TL/H/5703–12

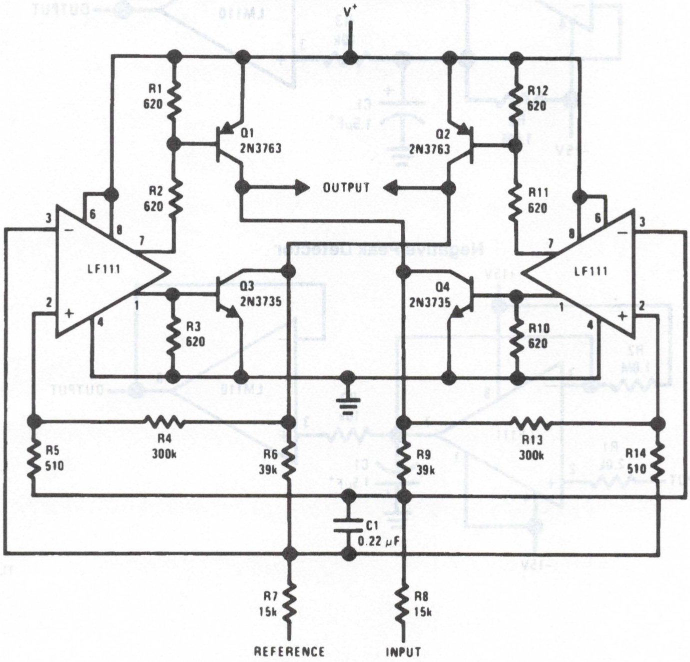
## Typical Applications (Continued)

### Switching Power Amplifier


V+
3
8
R8
620
LF111
6
7
R7
300
Q1
2N3763
2
1
4
V−
R2
100k
OUTPUT
R3
100k
V+
2
8
LF111
6
7
1
R1
10k
INPUT
3
4
Q2
2N3735
C1
0.1μF
R4
47
R5
300
R6
620
V−

TL/H/5703–16

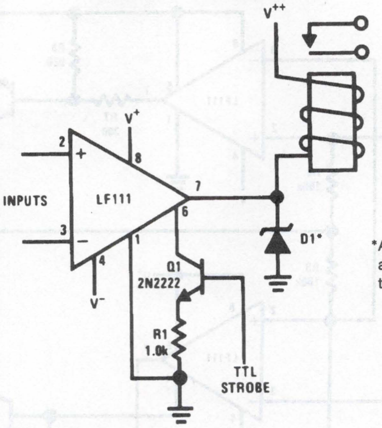
### Switching Power Amplifier


V+
R1
620
Q1
2N3763
Q2
2N3763
R12
620
R2
620
OUTPUT
R11
620
3
6
8
7
LF111
2
1
4
Q3
2N3735
Q4
2N3735
6
3
8
7
LF111
1
2
4
R3
620
R10
620
R4
300k
R13
300k
R5
510
R6
39k
R9
39k
R14
510
C1
0.22 μF
R7
15k
R8
15k
REFERENCE
INPUT

TL/H/5703–17

## Typical Applications (Continued)

### Relay Driver with Strobe

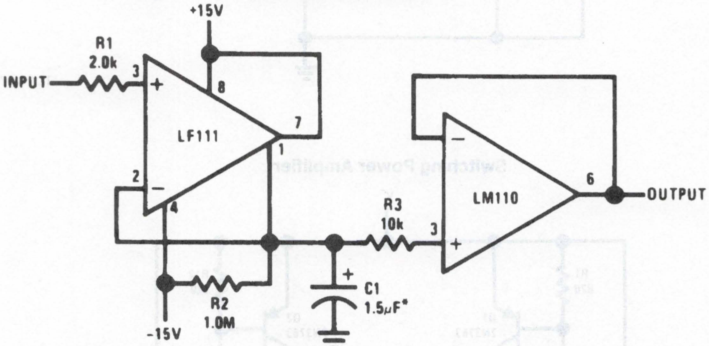

V++
V+
2
+
8
INPUTS
LF111
7
6
3
−
1
4
V−
Q1
2N2222
D1*
R1
1.0k
TTL
STROBE

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

TL/H/5703-18

**Note:** Do Not Ground Strobe Pin.

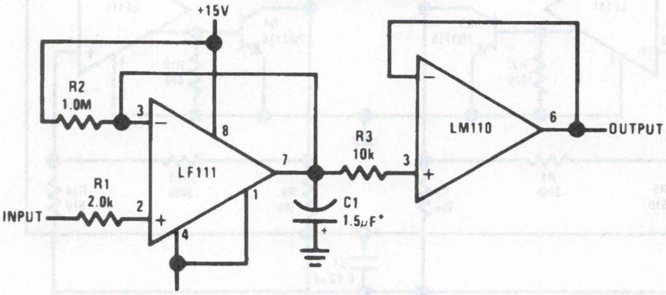
### Positive Peak Detector


+15V
R1
2.0k
INPUT
3
+
8
LF111
7
1
2
−
4
−
LM110
6
OUTPUT
R3
10k
3
+
+
C1
1.5μF*
R2
1.0M
−15V

*Solid tantalum

TL/H/5703-19

### Negative Peak Detector

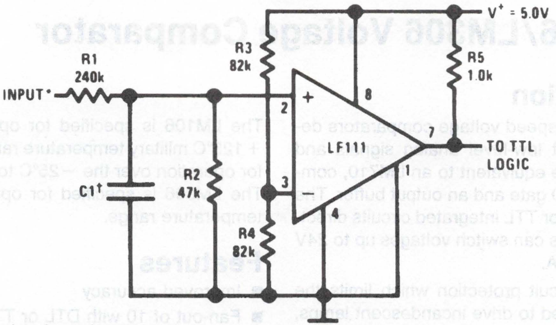

+15V
R2
1.0M
3
−
8
LF111
7
1
R1
2.0k
INPUT
2
+
4
−15V
R3
10k
C1
1.5μF*
+
−
LM110
6
OUTPUT
3
+

*Solid tantalum

TL/H/5703-20

## Typical Applications (Continued)

**TTL Interface with High Level Logic**

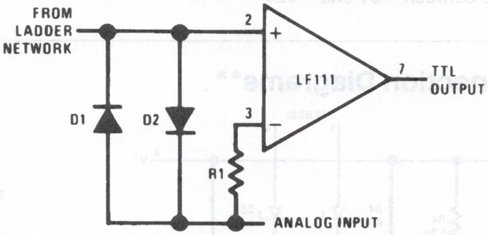

V⁺ = 5.0V
R3
82k
R5
1.0k
R1
240k
INPUT*
2
+
8
7
LF111
TO TTL
LOGIC
1
R2
47k
C1†
3
4
R4
82k

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes

TL/H/5703–21

**Using Clamp Diodes to Improve Response**


FROM
LADDER
NETWORK
2
+
LF111
7
TTL
OUTPUT
D1
D2
3
−
R1
ANALOG INPUT

TL/H/5703–6

**National Semiconductor Corporation**

# LM106/LM206/LM306 Voltage Comparator

## General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 10 mA.

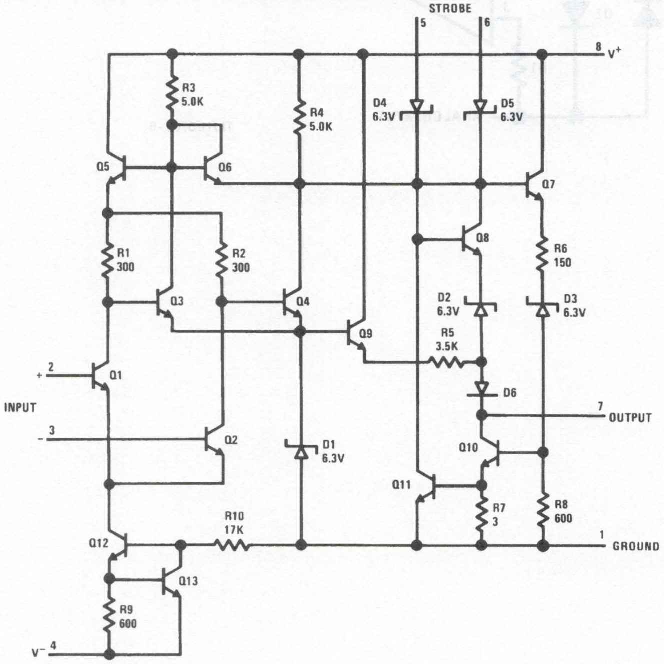
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM206 is specified for operation over the −25°C to +85°C temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

## Features

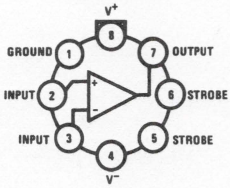
- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

## Schematic and Connection Diagrams**


STROBE
5
6
8
V+
R3
5.0K
R4
5.0K
D4
6.3V
D5
6.3V
Q5
Q6
Q7
R1
300
R2
300
Q3
Q4
Q8
R6
150
D2
6.3V
D3
6.3V
Q9
R5
3.5K
+ 2
Q1
INPUT
D6
7
OUTPUT
− 3
Q2
D1
6.3V
Q10
Q11
R7
3
R8
600
R10
17K
Q12
1
GROUND
Q13
R9
600
V− 4

TL/H/7756-1

**Metal Can**


V+
8
GROUND
1
7
OUTPUT
INPUT
2
6
STROBE
INPUT
3
5
STROBE
4
V−
+
−

TL/H/7756-2

**Top View**

**Note:** Pin 4 connected to case.

**Order Number LM106H, LM206H or LM306H**
**See NS Package Number H08A**

**Pin connections shown are for TO-5 package.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 6)**

| | |
|---|---|
| Positive Supply Voltage | 15V |
| Negative Supply Voltage | −15V |
| Output Voltage | 24V |
| Output to Negative Supply Voltage | 30V |
| Differential Input Voltage | ±5V |
| Input Voltage | ±7V |

| | |
|---|---|
| Power Dissipation (Note 1) | 600 mW |
| Output Short Circuit Duration | 10 seconds |
| Operating Temperature Range | $T_{MIN}$ $T_{MAX}$ |
| LM106 | −55°C to +125°C |
| LM206 | −25°C to +85°C |
| LM306 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 2)

| Parameter | Conditions | LM106/LM206 | | | LM306 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 3) | | 0.5 | 2.0 | | 1.6 | 5.0 | mV |
| Input Offset Current | (Note 3) | | 0.7 | 3.0 | | 1.8 | 5.0 | μA |
| Input Bias Current | | | 10 | 20 | | 16 | 25 | μA |
| Response Time | $R_L$ = 390Ω to 5V<br>$C_L$ = 15 pF, (Note 4) | | 28 | 40 | | 28 | 40 | ns |
| Saturation Voltage | $V_{IN} \le -5$ mV, $I_{OUT}$ = 100 mA | | 1.0 | 1.5 | | | | V |
| | $V_{IN} \le -7$ mV, $I_{OUT}$ = 100 mA | | | | | 0.8 | 2.0 | V |
| Output Leakage Current | $V_{IN} \ge 5$ mV, 8V ≤ $V_{OUT}$ ≤ 24V | | 0.02 | 1.0 | | | | μA |
| | $V_{IN} \ge 7$ mV, 8V ≤ $V_{OUT}$ ≤ 24V | | | | | 0.02 | 2.0 | μA |
| **THE FOLLOWING SPECIFICATIONS APPLY FOR $T_{MIN} \le T_A \le T_{MAX}$ (Note 5)** | | | | | | | | |
| Input Offset Voltage | (Note 3) | | | 3.0 | | | 6.5 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 10 | | 5 | 20 | μV/°C |
| Input Offset Current | $T_L \le T_A \le 25°C$, (Note 3) | | 1.8 | 7.0 | | 2.4 | 7.5 | μA |
| | $25°C \le T_A \le T_H$ | | 0.25 | 3.0 | | | 5.0 | μA |
| Average Temperature Coefficient of Input Offset Current | $25°C \le T_A \le T_H$ | | 5.0 | 25 | | 15 | 50 | nA/°C |
| | $T_L \le T_A \le 25°C$ | | 15 | 75 | | 24 | 100 | nA/°C |
| Input Bias Current | $T_L \le T_A \le 25°C$ | | | 45 | | 25 | 40 | μA |
| | $25°C \le T_A \le T_H$ | | | 20 | | | 25 | μA |
| Input Voltage Range | $-7V \ge V^- \ge -12V$ | ±5.0 | | | ±5.0 | | | V |
| Differential Input Voltage Range | | ±5.0 | | | ±5.0 | | | V |
| Saturation Voltage | $V_{IN} \le -5$ mV, $I_{OUT}$ = 50 mA<br>$V_{IN} \le -8$ mV For LM306 | | | 1.0 | | | 1.0 | V |
| Saturation Voltage | $V_{IN} \le -5$ mV, $I_{OUT}$ = 16 mA<br>$V_{IN} \le -8$ mV For LM306 | | | 0.4 | | | 0.4 | V |
| Positive Output Level | $V_{IN} \ge 5$ mV, $I_{OUT}$ = −400μA<br>$V_{IN} \ge 8$ mV For LM306 | 2.5 | | 5.5 | 2.5 | | 5.5 | V |
| Output Leakage Current | $V_{IN} \ge 5$ mV, 8V ≤ $V_{OUT}$ ≤ 24V<br>$V_{IN} \ge 8$ mV For LM306<br>$T_L \le T_A \le 25°C$ | | | 1.0 | | | 2.0 | μA |
| | $25°C < T_A \le T_H$ | | | 100 | | | 100 | μA |
| Strobe Current | $V_{STROBE}$ = 0.4V | | −1.7 | −3.2 | | −1.7 | −3.2 | mA |

## Electrical Characteristics (Note 2) (Continued)

| Parameter | Conditions | LM106/LM206 | | | LM306 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Strobe "ON" Voltage | | 0.9 | 1.4 | | 0.9 | 1.4 | | V |
| Strobe "OFF" Voltage | $I_{SINK} \le 16$ mA | | 1.4 | 2.2 | | 1.4 | 2.2 | V |
| Positive Supply Current | $V_{IN} = -5$ mV<br>$V_{IN} = -8$ mV for LM306 | | 5.5 | 10 | | 5.5 | 10 | mA |
| Negative Supply Current | | | −1.5 | −3.6 | | −1.5 | −3.6 | mA |

**Note 1:** The maximum junction temperature of LM106 is 150°C, LM206 is 110°C, LM306 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

**Note 2:** These specifications apply for $-3V \ge V^- \ge -12V$, $V^+ = 12V$ and $T_A = 25°C$ unless otherwise specified. All currents into device pins are considered positive.

**Note 3:** The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

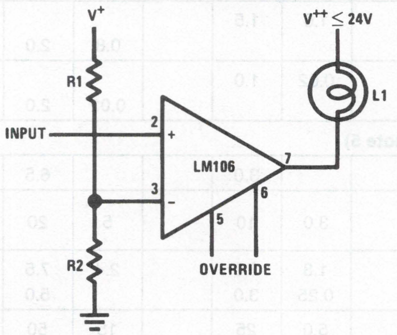
**Note 4:** The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

**Note 5:** All currents into device pins are considered positive.

**Note 6:** Refer to RETS106X for LM106 military specifications.

## Typical Applications**

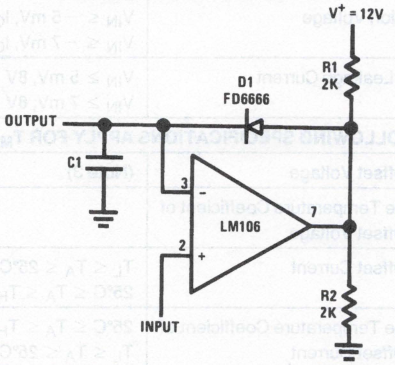
### Level Detector and Lamp Driver



V+
V++ ≤ 24V
R1
L1
INPUT
2
+
3
−
LM106
7
6
5
R2
OVERRIDE

TL/H/7756-4

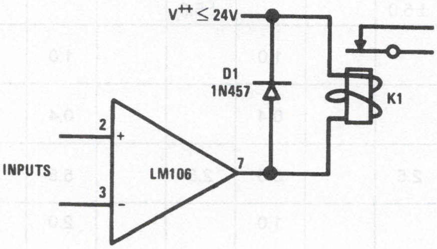
### Fast Response Peak Detector



V+ = 12V
R1
2K
D1
FD6666
OUTPUT
C1
3
−
2
+
LM106
7
R2
2K
INPUT

TL/H/7756-5

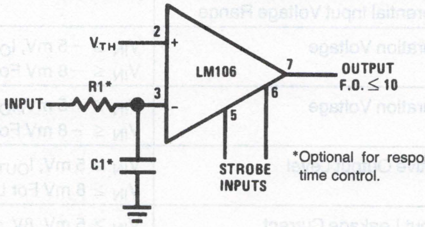
### Relay Driver



V++ ≤ 24V
D1
1N457
K1
2
+
INPUTS
3
−
LM106
7

TL/H/7756-6

### Adjustable Threshold Line Receiver



2
+
V_TH
INPUT
R1*
3
−
LM106
7
6
5
OUTPUT
F.O. ≤ 10
C1*
STROBE
INPUTS

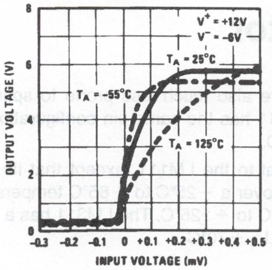
*Optional for response time control.

TL/H/7756-7

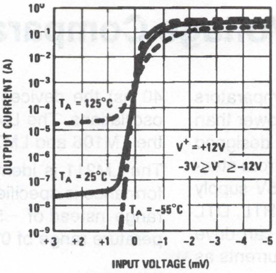
**Pin connections shown are for TO-5 package.

## Typical Performance Characteristics

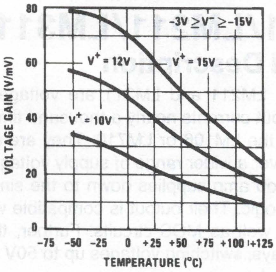
### Transfer Function



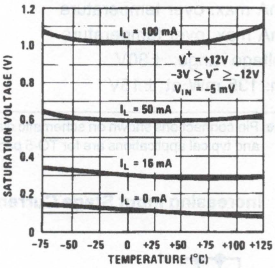
### Transconductance



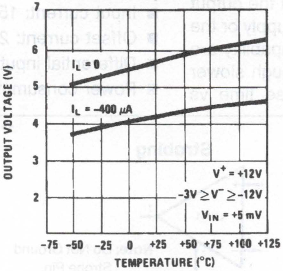
### Voltage Gain



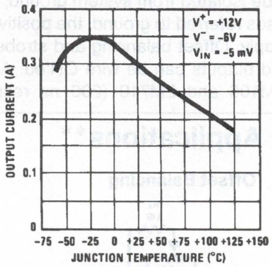
### Saturation Voltage



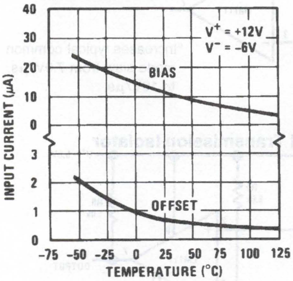
### Positive Output Level



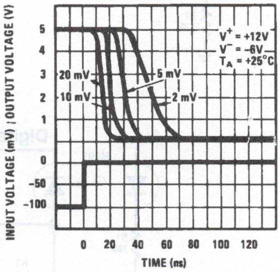
### Short Circuit Output Current



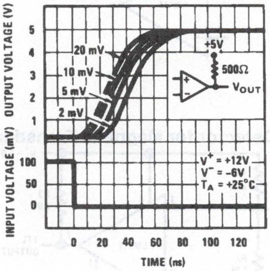
### Input Current



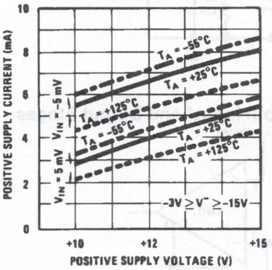
### Response Time for Various Input Overdrives



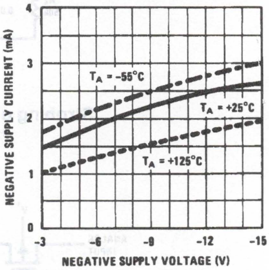
### Response Time for Various Input Overdrives



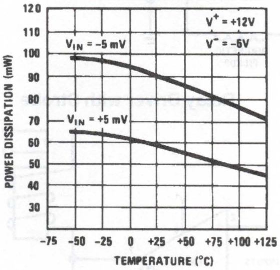
### Positive Supply Current



### Negative Supply Current



### Power Consumption



TL/H/7756–8

**National Semiconductor Corporation**

# LM111/LM211/LM311 Voltage Comparator

## General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

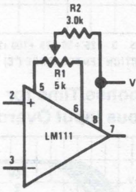
## Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

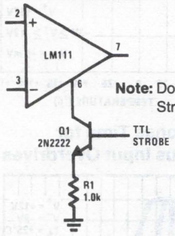
## Typical Applications**

**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.

### Offset Balancing

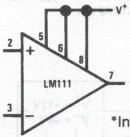

R2
3.0k
R1
5k
V+
LM111
2
3
5
6
7
+
−

### Strobing


2
3
+
−
LM111
7
6
Q1
2N2222
TTL
STROBE
R1
1.0k

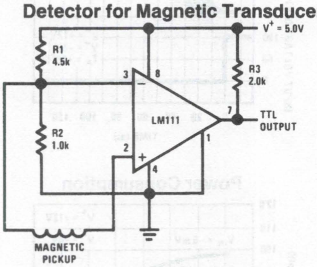
**Note:** Do Not Ground Strobe Pin.

### Increasing Input Stage Current*

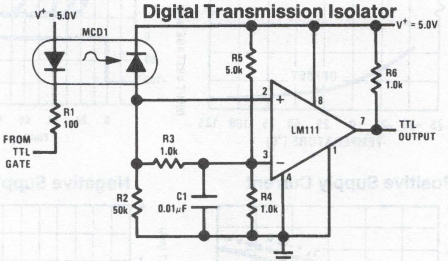

V+
2
3
+
−
5
6
8
7
LM111

*Increases typical common mode slew from 7.0V/μs to 18V/μs.

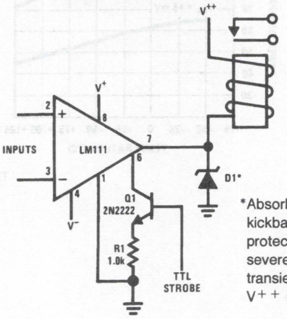
### Detector for Magnetic Transducer


V+ = 5.0V
R1
4.5k
R2
1.0k
R3
2.0k
3
8
2
4
7
1
LM111
TTL
OUTPUT
MAGNETIC
PICKUP

### Digital Transmission Isolator


V+ = 5.0V
MCD1
R1
100
FROM
TTL
GATE
V+ = 5.0V
R5
5.0k
R6
1.0k
2
8
3
4
7
1
LM111
TTL
OUTPUT
R3
1.0k
R2
50k
C1
0.01μF
R4
1.0k

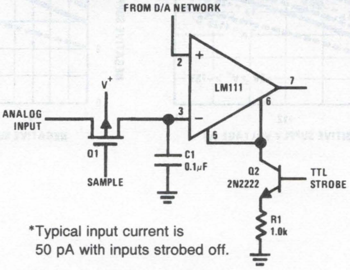
### Relay Driver with Strobe


V++
V+
2
8
3
4
7
6
1
LM111
INPUTS
V−
D1*
Q1
2N2222
R1
1.0k
TTL
STROBE

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

**Note:** Do Not Ground Strobe Pin.

### Strobing off Both Input* and Output Stages


FROM D/A NETWORK
2
3
+
−
LM111
7
6
5
V+
ANALOG
INPUT
Q1
SAMPLE
C1
0.1μF
Q2
2N2222
TTL
STROBE
R1
1.0k

*Typical input current is 50 pA with inputs strobed off.

**Note:** Do Not Ground Strobe Pin.

TL/H/5704–1

## Absolute Maximum Ratings for the LM111/LM211

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 7)**

| | |
|---|---|
| Total Supply Voltage ($V_{84}$) | 36V |
| Output to Negative Supply Voltage ($V_{74}$) | 50V |
| Ground to Negative Supply Voltage ($V_{14}$) | 30V |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 1) | ±15V |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range LM111 | −55°C to 125°C |
| LM211 | −25°C to 85°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C |
| Voltage at Strobe Pin | V+ −5V |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics for the LM111 and LM211 (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C$, $R_S \leq 50k$ | | 0.7 | 3.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$ | | 4.0 | 10 | nA |
| Input Bias Current | $T_A = 25°C$ | | 60 | 100 | nA |
| Voltage Gain | $T_A = 25°C$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA<br>$T_A = 25°C$ | | 0.75 | 1.5 | V |
| Strobe ON Current (Note 6) | $T_A = 25°C$ | 2.0 | 3.0 | 5.0 | mA |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$<br>$T_A = 25°C$, $I_{STROBE} = 3$ mA | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50$ k | | | 4.0 | mV |
| Input Offset Current (Note 4) | | | | 20 | nA |
| Input Bias Current | | | | 150 | nA |
| Input Voltage Range | $V^+ = 15V$, $V^- = -15V$, Pin 7<br>Pull-Up May Go To 5V | −14.5 | 13.8,-14.7 | 13.0 | V |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$<br>$V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA | | 0.23 | 0.4 | V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ | | 0.1 | 0.5 | μA |
| Positive Supply Current | $T_A = 25°C$ | | 5.1 | 6.0 | mA |
| Negative Supply Current | $T_A = 25°C$ | | 4.1 | 5.0 | mA |

**Note 1:** This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

**Note 2:** The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

**Note 3:** These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

**Note 5:** The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

**Note 6:** Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

**Note 7:** Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

## Absolute Maximum Ratings for the LM311

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Total Supply Voltage ($V_{84}$) | 36V |
| Output to Negative Supply Voltage $V_{74}$) | 40V |
| Ground to Negative Supply Voltage $V_{14}$) | 30V |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 1) | ±15V |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range | 0° to 70°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (soldering, 10 sec) | 260°C |
| Voltage at Strobe Pin | $V^{+}$ −5V |

Soldering Information

Dual-In-Line Package

Soldering (10 seconds) . . . . . . . . . . . . . . . . . . . . 260°C

Small Outline Package

Vapor Phase (60 seconds) . . . . . . . . . . . . . . . . . 215°C

Infrared (15 seconds) . . . . . . . . . . . . . . . . . . . . . 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics for the LM311 (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C, R_S \leq 50k$ | | 2.0 | 7.5 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$ | | 6.0 | 50 | nA |
| Input Bias Current | $T_A = 25°C$ | | 100 | 250 | nA |
| Voltage Gain | $T_A = 25°C$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA<br>$T_A = 25°C$ | | 0.75 | 1.5 | V |
| Strobe ON Current | $T_A = 25°C$ | 1.5 | 3.0 | | mA |
| Output Leakage Current | $V_{IN} \geq 10$ mV, $V_{OUT} = 35V$<br>$T_A = 25°C, I_{STROBE} = 3$ mA<br>$V^{-} = V_{GRND} = -5V$ | | 0.2 | 50 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50K$ | | | 10 | mV |
| Input Offset Current (Note 4) | | | | 70 | nA |
| Input Bias Current | | | | 300 | nA |
| Input Voltage Range | | −14.5 | 13.8, −14.7 | 13.0 | V |
| Saturation Voltage | $V^{+} \geq 4.5V, V^{-} = 0$<br>$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA | | 0.23 | 0.4 | V |
| Positive Supply Current | $T_A = 25°C$ | | 5.1 | 7.5 | mA |
| Negative Supply Current | $T_A = 25°C$ | | 4.1 | 5.0 | mA |

**Note 1:** This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

**Note 2:** The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 3:** These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

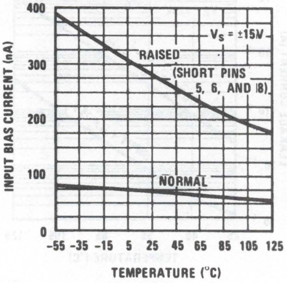
**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

**Note 5:** The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

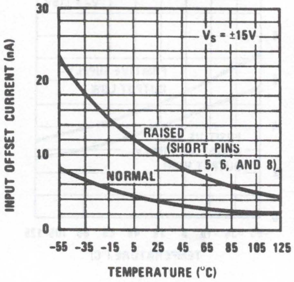
**Note 6:** Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

## LM111/LM211 Typical Performance Characteristics

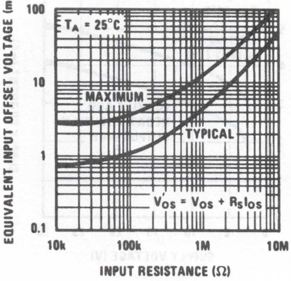
Input Bias Current



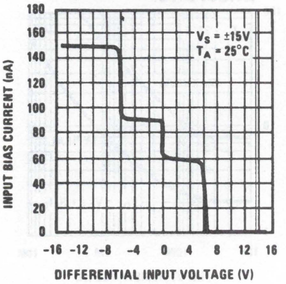
Input Offset Current



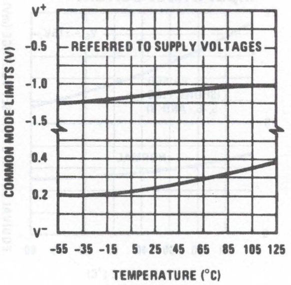
Offset Error



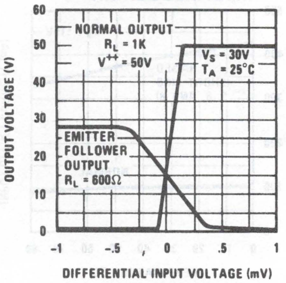
Input Characteristics



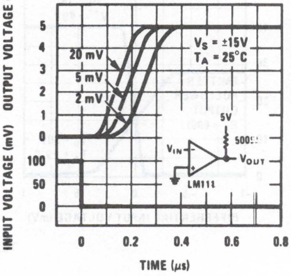
Common Mode Limits



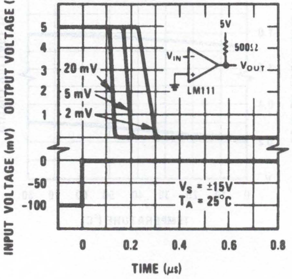
Transfer Function



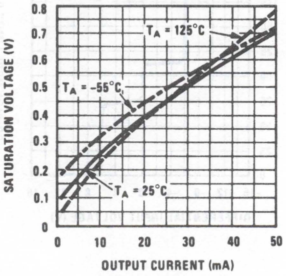
Response Time for Various Input Overdrives



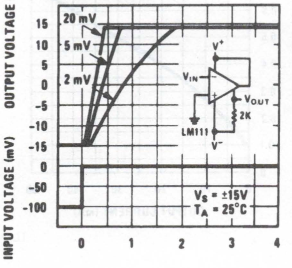
Response Time for Various Input Overdrives



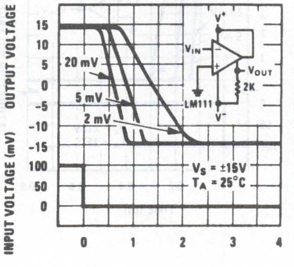
Output Saturation Voltage



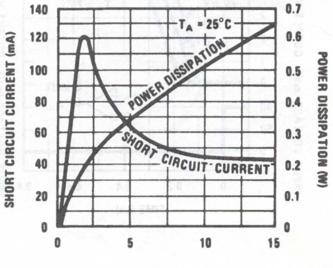
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



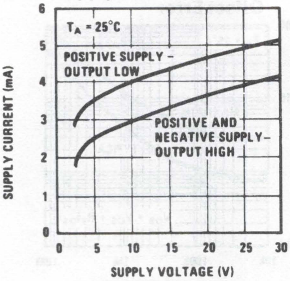
Output Limiting Characteristics



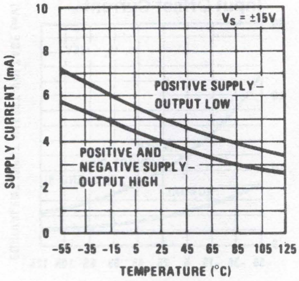
TL/H/5704-2

## LM111/LM211 Typical Performance Characteristics (Continued)

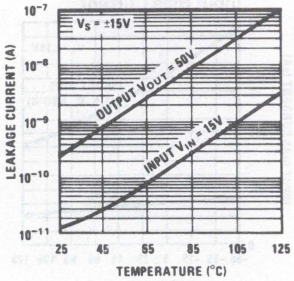
### Supply Current



### Supply Current



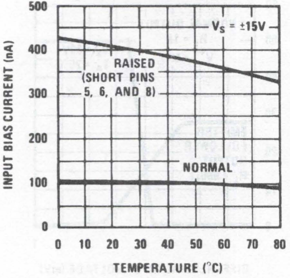
### Leakage Currents



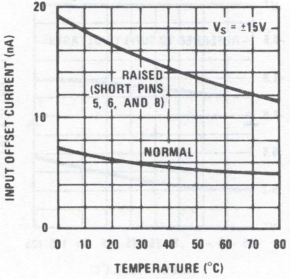
TL/H/5704-3

## LM311 Typical Performance Characteristics

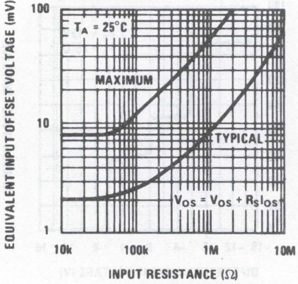
### Input Bias Current



### Input Offset Current

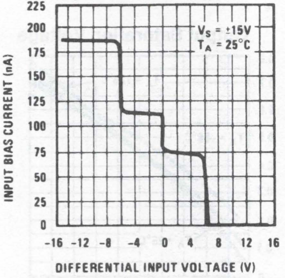


### Offset Error

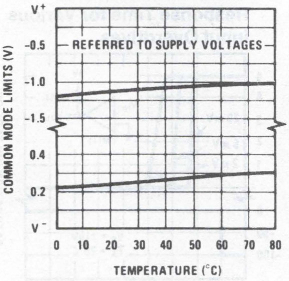


TL/H/5704-8

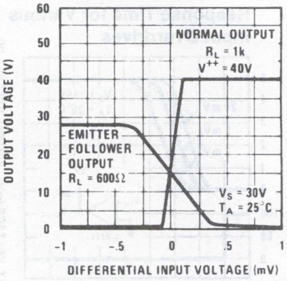
### Input Characteristics



### Common Mode Limits

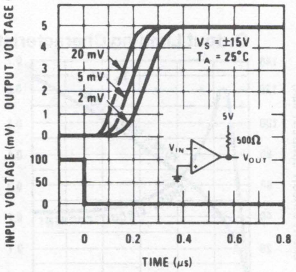


### Transfer Function

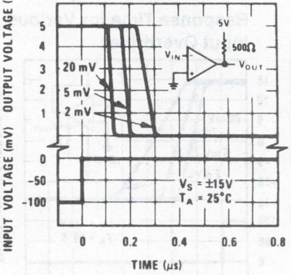


TL/H/5704-9

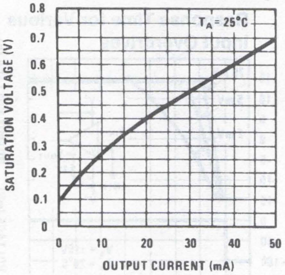
### Response Time for Various Input Overdrives



### Response Time for Various Input Overdrives

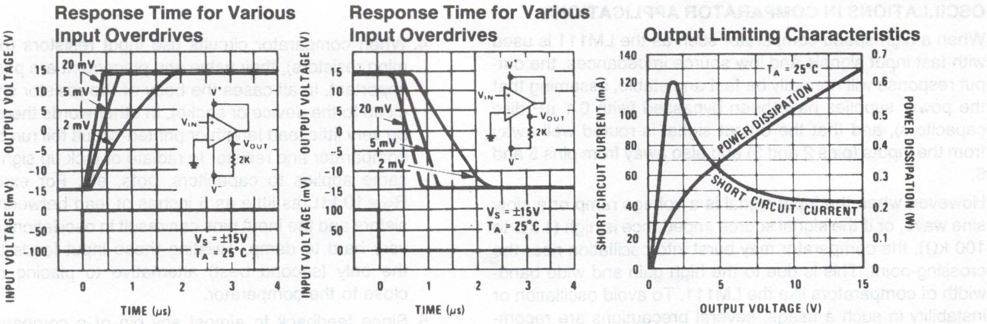


### Output Saturation Voltage



TL/H/5704-10

## LM311 Typical Performance Characteristics (Continued)

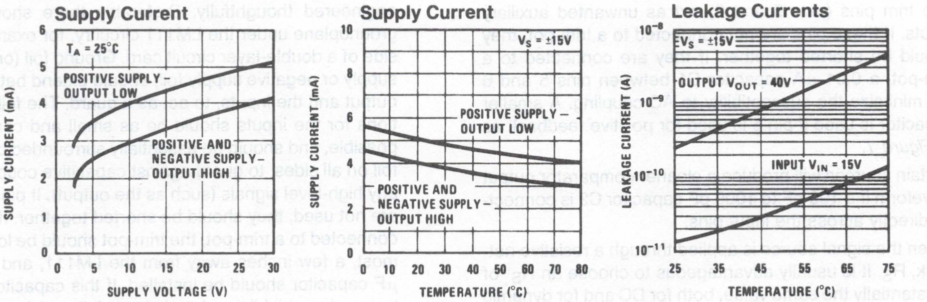


Response Time for Various Input Overdrives

Response Time for Various Input Overdrives

Output Limiting Characteristics

TL/H/5704–11



Supply Current

Supply Current

Leakage Currents

TL/H/5704–12

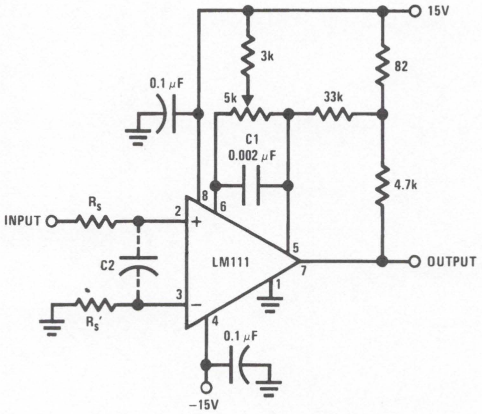
## Application Hints

### CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, $R_S$, it is usually advantageous to choose an $R_S'$ of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10$ kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



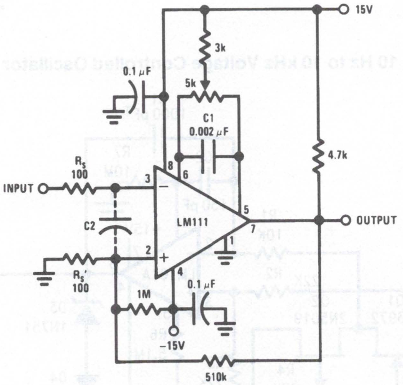
TL/H/5704–29

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

**FIGURE 1. Improved Positive Feedback**

## Application Hints (Continued)

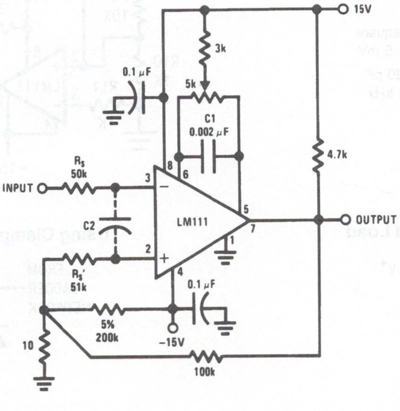
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if $R_S$ is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. the circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the $V_{OS}$ of the comparator. As much as 8 mV of $V_{OS}$ can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



TL/H/5704-30

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

**FIGURE 2. Conventional Positive Feedback**

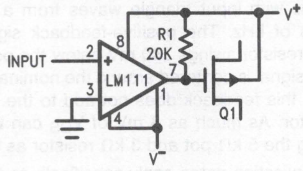


TL/H/5704-31

**FIGURE 3. Positive Feedback with High Source Resistance**

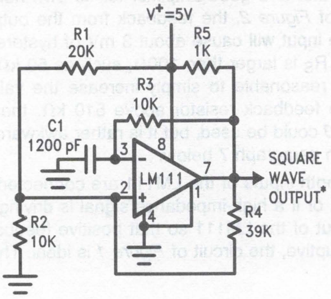
## Typical Applications (Continued) (Pin numbers refer to TO-5 package)

### Zero Crossing Detector Driving MOS Switch


V+
R1
20K
INPUT
2
3
8
7
1
4
LM111
Q1
V−

TL/H/5704–13

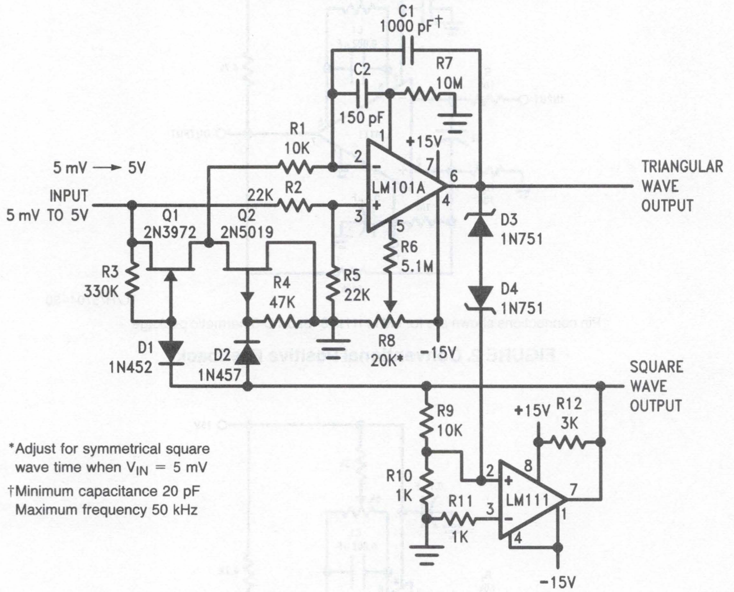
### 100 kHz Free Running Multivibrator


V+=5V
R1
20K
R5
1K
R3
10K
C1
1200 pF
3
8
LM111
7
2
1
4
SQUARE
WAVE
OUTPUT*
R4
39K
R2
10K

*TTL or DTL fanout of two

TL/H/5704–14

### 10 Hz to 10 kHz Voltage Controlled Oscillator

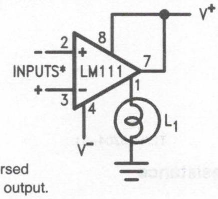

C1
1000 pF†
C2
R7
10M
150 pF
R1
10K
1
+15V
2
7
5 mV ⟶ 5V
R2
22K
LM101A
6
INPUT
5 mV TO 5V
3
4
TRIANGULAR
WAVE
OUTPUT
Q1
2N3972
Q2
2N5019
5
D3
1N751
R6
5.1M
R3
330K
R4
47K
R5
22K
D4
1N751
D1
1N452
D2
1N457
R8
20K*
−15V
SQUARE
WAVE
OUTPUT
R9
10K
+15V
R12
3K
R10
1K
2
8
LM111
7
R11
1K
3
1
4
−15V

*Adjust for symmetrical square wave time when $V_{IN} = 5$ mV

†Minimum capacitance 20 pF Maximum frequency 50 kHz

TL/H/5704–15

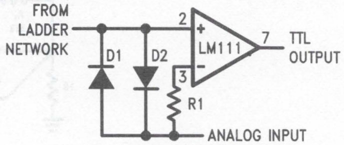
### Driving Ground-Referred Load


V+
2
8
INPUTS*
LM111
7
1
3
4
L1
V−

*Input polarity is reversed when using pin 1 as output.

TL/H/5704–16

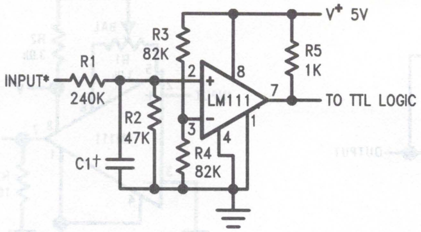
### Using Clamp Diodes to Improve Response


FROM
LADDER
NETWORK
D1
D2
2
LM111
7
TTL
OUTPUT
3
R1
ANALOG INPUT

TL/H/5704–17

## Typical Applications (Continued) (Pin numbers refer to TO-5 package)

### TTL Interface with High Level Logic

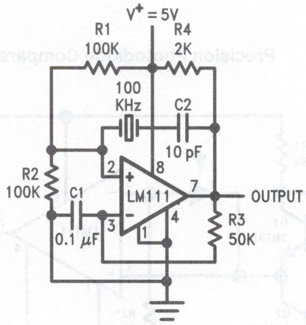

V+ 5V
R3
82K
R5
1K
R1
240K
INPUT*
2
8
LM111
7
TO TTL LOGIC
R2
47K
3
4
1
R4
82K
C1†

*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

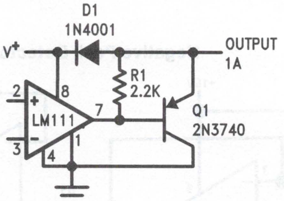
TL/H/5704–18

### Crystal Oscillator


V+ = 5V
R1
100K
R4
2K
100
KHz
C2
10 pF
R2
100K
C1
0.1 μF
2
8
LM111
7
3
1
4
OUTPUT
R3
50K

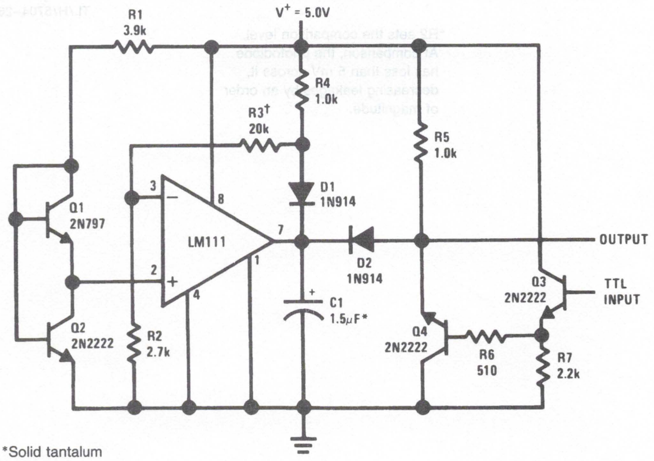
TL/H/5704–19

### Comparator and Solenoid Driver


D1
1N4001
V+
OUTPUT
1A
R1
2.2K
2
8
LM111
7
Q1
2N3740
3
1
4

TL/H/5704–20

### Precision Squarer

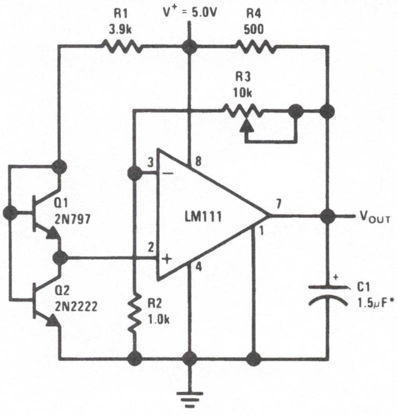

R1
3.9k
V+ = 5.0V
R4
1.0k
R3†
20k
R5
1.0k
D1
1N914
Q1
2N797
3
8
LM111
7
OUTPUT
D2
1N914
2
1
4
Q3
2N2222
TTL
INPUT
Q2
2N2222
R2
2.7k
C1
1.5μF*
Q4
2N2222
R6
510
R7
2.2k

*Solid tantalum

†Adjust to set clamp level

TL/H/5704–21

### Low Voltage Adjustable Reference Supply

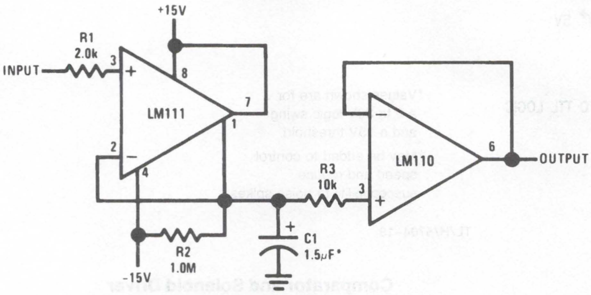

R1
3.9k
V+ = 5.0V
R4
500
R3
10k
3
8
Q1
2N797
LM111
7
V_OUT
2
1
4
Q2
2N2222
R2
1.0k
C1
1.5μF*

*Solid tantalum

TL/H/5704–22

## Typical Applications (Continued) (Pin numbers refer to TO-5 package)

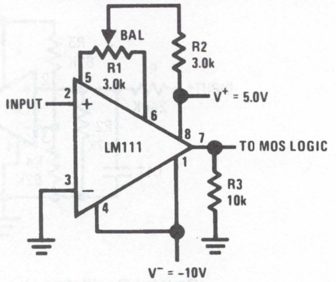
### Positive Peak Detector


+15V
R1
2.0k
INPUT
3
+
8
LM111
7
1
2
–
4
–15V
R2
1.0M
R3
10k
3
+
–
LM110
6
OUTPUT
+
C1
1.5μF*

*Solid tantalum

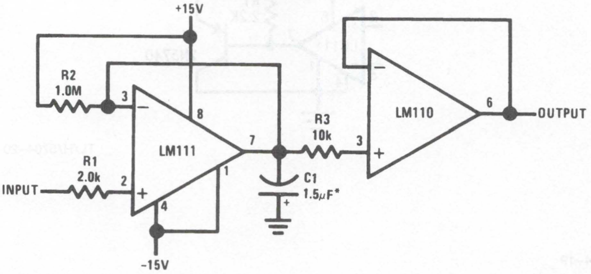
TL/H/5704-23

### Zero Crossing Detector Driving MOS Logic


BAL
R1
3.0k
5
R2
3.0k
V+ = 5.0V
INPUT
2
+
6
LM111
8
7
TO MOS LOGIC
1
R3
10k
3
–
4
V– = –10V

TL/H/5704-24

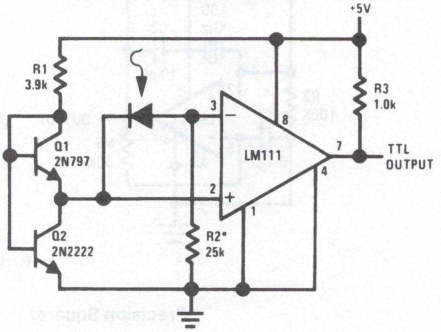
### Negative Peak Detector


+15V
R2
1.0M
3
–
8
LM111
7
1
R1
2.0k
INPUT
2
+
4
–15V
R3
10k
3
+
–
LM110
6
OUTPUT
C1
1.5μF*
+

*Solid tantalum

TL/H/5704-25

### Precision Photodiode Comparator

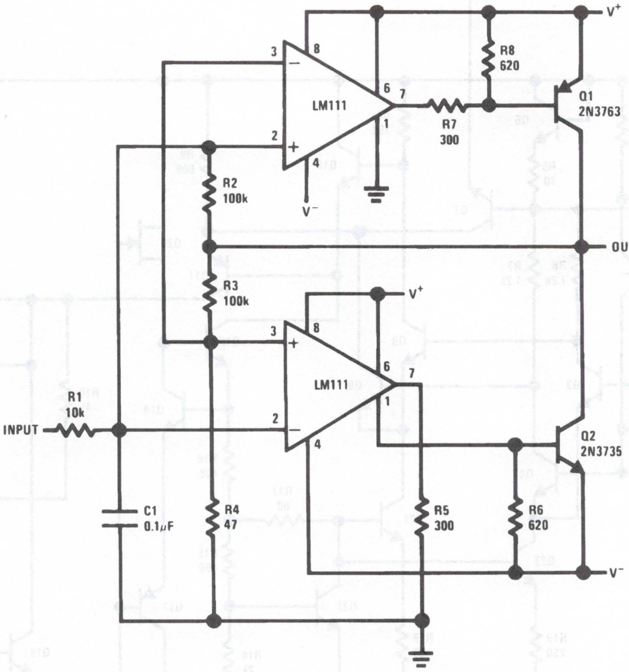

+5V
R1
3.9k
Q1
2N797
Q2
2N2222
3
–
8
LM111
7
TTL OUTPUT
2
+
1
4
R2*
25k
R3
1.0k

TL/H/5704-26

*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

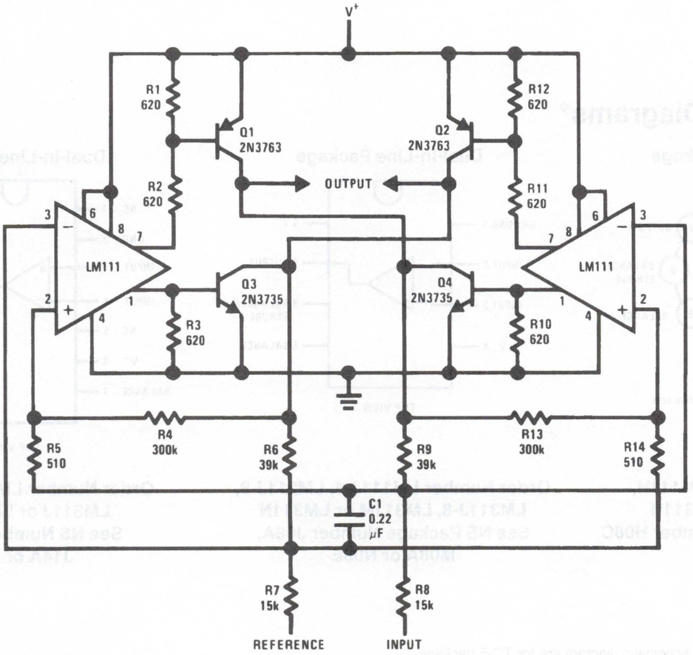
## Typical Applications (Continued) (Pin numbers refer to TO-5 package)

### Switching Power Amplifier


V+
3
8
−
LM111
6
7
1
2
+
4
V−
R8
620
Q1
2N3763
R7
300
R2
100k
OUTPUT
R3
100k
V+
3
8
+
LM111
6
7
1
2
−
4
R1
10k
INPUT
Q2
2N3735
C1
0.1μF
R4
47
R5
300
R6
620
V−

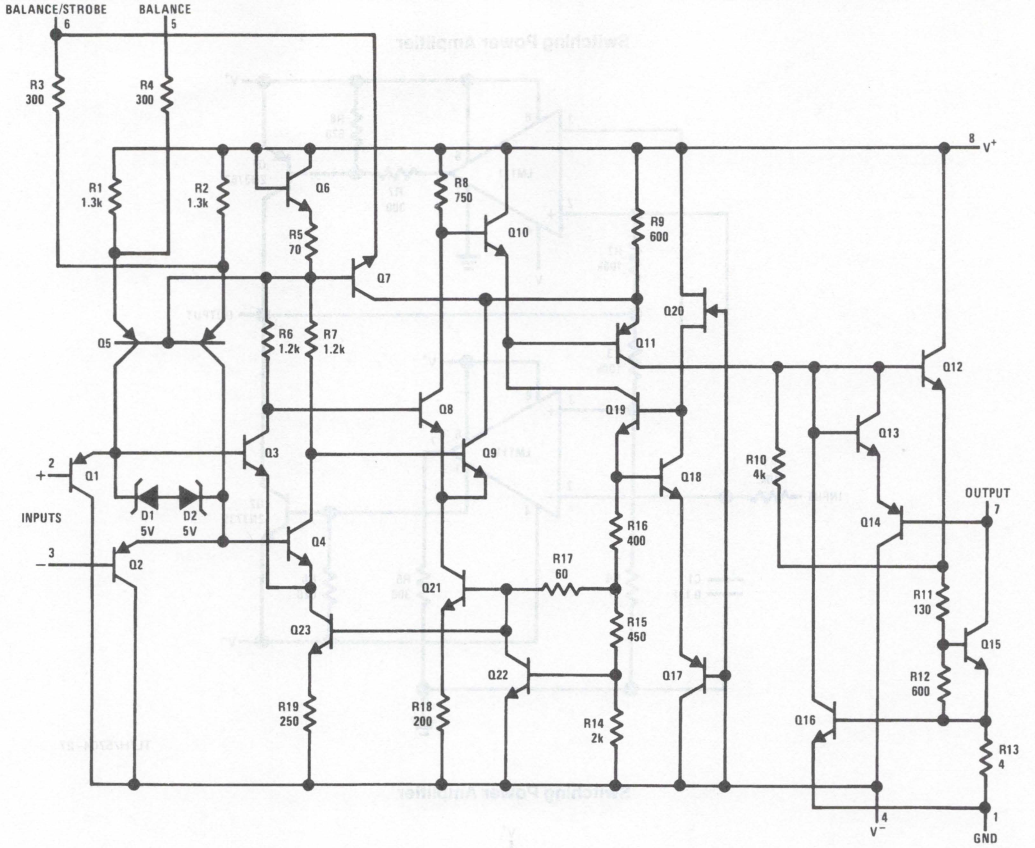
TL/H/5704–27

### Switching Power Amplifier


V+
R1
620
Q1
2N3763
Q2
2N3763
R12
620
R2
620
OUTPUT
R11
620
3
6
8
7
−
LM111
2
+
1
4
6
3
8
7
−
LM111
1
4
+
2
Q3
2N3735
Q4
2N3735
R3
620
R10
620
R4
300k
R13
300k
R5
510
R6
39k
R9
39k
R14
510
C1
0.22
μF
R7
15k
R8
15k
REFERENCE
INPUT

TL/H/5704–28

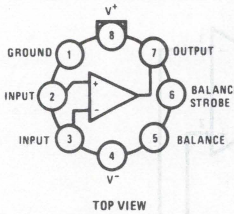
## Schematic Diagram


BALANCE/STROBE
6
BALANCE
5
R3
300
R4
300
R1
1.3k
R2
1.3k
Q6
R5
70
Q7
R8
750
Q10
R9
600
8
V+
Q5
R6
1.2k
R7
1.2k
Q20
Q11
Q12
Q8
Q19
2
+
Q1
Q3
Q9
Q13
Q18
R10
4k
INPUTS
D1
5V
D2
5V
Q14
OUTPUT
7
3
−
Q2
Q4
R16
400
R17
60
Q21
R11
130
Q23
R15
450
Q15
Q22
Q17
R12
600
R19
250
R18
200
R14
2k
Q16
R13
4
4
V−
1
GND

TL/H/5704-5

## Connection Diagrams*

### Metal Can Package

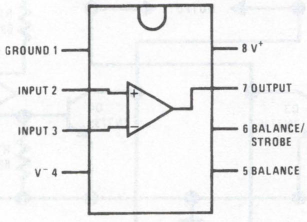

V+
8
GROUND
1
7
OUTPUT
INPUT
2
6
BALANCE/
STROBE
INPUT
3
5
BALANCE
4
V−
+
−

TOP VIEW

NOTE: Pin 4 connected to case.

**Order Number LM111H, LM211H or LM311H**
**See NS Package Number H08C**

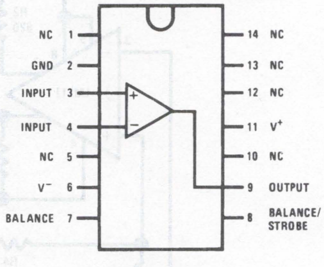
### Dual-In-Line Package


GROUND 1
INPUT 2
INPUT 3
V− 4
8 V+
7 OUTPUT
6 BALANCE/
STROBE
5 BALANCE
+
−

TOP VIEW

**Order Number LM111J-8, LM211J-8, LM311J-8, LM311M or LM311N**
**See NS Package Number J08A, M08A or N08E**

### Dual-In-Line Package


NC 1
GND 2
INPUT 3
INPUT 4
NC 5
V− 6
BALANCE 7
14 NC
13 NC
12 NC
11 V+
10 NC
9 OUTPUT
8 BALANCE/
STROBE
+
−

TOP VIEW

TL/H/5704-6

**Order Number LM111J, LM211J, LM311J or LM311N-14**
**See NS Number Package J14A or N14A**

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*Pin connections shown on schematic diagram are for TO-5 package.

**National Semiconductor Corporation**

# LM119/LM219/LM319 High Speed Dual Comparator

## General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

## Features

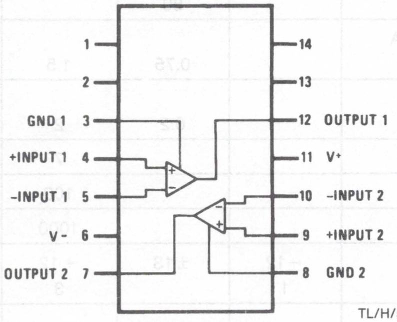
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

## Connection Diagrams

### Dual-In-Line-Package


1
2
GND 1 3
+INPUT 1 4
−INPUT 1 5
V− 6
OUTPUT 2 7
14
13
12 OUTPUT 1
11 V+
10 −INPUT 2
9 +INPUT 2
8 GND 2

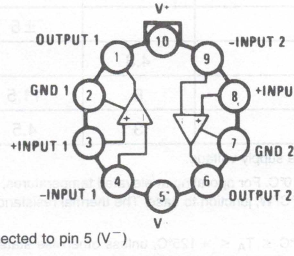
TL/H/5705-4

**Top View**

**Order Number LM119J, LM219J, LM319J, LM319M or LM319N**

**See NS Package Number J14A, M14A or N14A**

### Metal Can Package


V+
OUTPUT 1
−INPUT 2
GND 1
+INPUT 2
+INPUT 1
GND 2
−INPUT 1
OUTPUT 2
V−
1
2
3
4
5
6
7
8
9
10

Case is connected to pin 5 (V⁻)

TL/H/5705-7

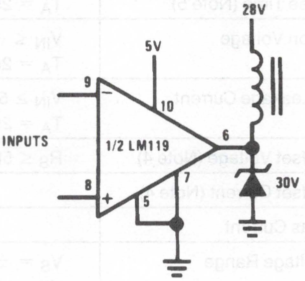
**Top View**

**Order Number LM119H or LM319H**

**See NS Package Number H10C**

## Typical Applications*

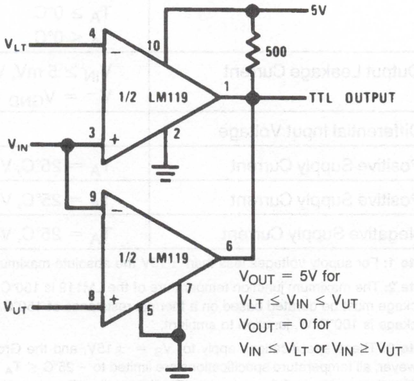
### Relay Driver


28V
5V
9
10
INPUTS
1/2 LM119
6
8
7
5
30V

TL/H/5705-5

*Pinout is for metal can package.

### Window Detector


5V
V_LT
4
10
500
1/2 LM119
1
TTL OUTPUT
V_IN
3
2
9
1/2 LM119
6
8
7
5
V_UT

$V_{OUT} = 5V$ for

$V_{LT} \le V_{IN} \le V_{UT}$

$V_{OUT} = 0$ for

$V_{IN} \le V_{LT}$ or $V_{IN} \ge V_{UT}$

TL/H/5705-6

## Absolute Maximum Ratings LM119/219

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)**

| | |
|---|---|
| Total Supply Voltage | 36V |
| Output to Negative Supply Voltage | 36V |
| Ground to Negative Supply Voltage | 25V |
| Ground to Positive Supply Voltage | 18V |
| Differential Input Voltage | ±5V |
| Input Voltage (Note 1) | ±15V |

ESD rating to be determined.

| | |
|---|---|
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range LM119 | −55°C to 125°C |
| LM219 | −25°C to 85°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 3) LM119/LM219

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25^\circ C, R_S \leq 5k$ | | 0.7 | 4.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25^\circ C$ | | 30 | 75 | nA |
| Input Bias Current | $T_A = 25^\circ C$ | | 150 | 500 | nA |
| Voltage Gain | $T_A = 25^\circ C$ (Note 6) | 10 | 40 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ C, V_S = \pm 15V$ | | 80 | | ns |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA<br>$T_A = 25^\circ C$ | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$<br>$T_A = 25^\circ C$ | | 0.2 | 2 | μA |
| Input Offset Voltage (Note 4) | $R_S \leq 5k$ | | | 7 | mV |
| Input Offset Current (Note 4) | | | | 100 | nA |
| Input Bias Current | | | | 1000 | nA |
| Input Voltage Range | $V_S = \pm 15V$<br>$V^+ = 5V, V^- = 0$ | −12<br>1 | ±13 | +12<br>3 | V<br>V |
| Saturation Voltage | $V^+ \geq 4.5V, V^- = 0$<br>$V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA<br>$T_A \geq 0^\circ C$<br>$T_A \leq 0^\circ C$ | | 0.23 | 0.4<br>0.6 | V<br>V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$,<br>$V^- = V_{GND} = 0V$ | | 1 | 10 | μA |
| Differential Input Voltage | | | | ±5 | V |
| Positive Supply Current | $T_A = 25^\circ C, V^+ = 5V, V^- = 0$ | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25^\circ C, V_S = \pm 15V$ | | 8 | 11.5 | mA |
| Negative Supply Current | $T_A = 25^\circ C, V_S = \pm 15V$ | | 3 | 4.5 | mA |

**Note 1:** For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 3:** These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to $V_S$.

**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

**Note 5:** The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

**Note 6:** Output is pulled up to 15V through a 1.4 kΩ resistor.

**Note 7:** Refer to RETS119X for LM119H/883, LM119H-MIL, LM119J/883 and LM119J-MIL specifications.

## Absolute Maximum Ratings LM319

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Total Supply Voltage | 36V |
| Output to Negative Supply Voltage | 36V |
| Ground to Negative Supply Voltage | 25V |
| Ground to Positive Supply Voltage | 18V |
| Differential Input Voltage | ±5V |
| Input Voltage (Note 1) | ±15V |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |

ESD rating to be determined.

| | |
|---|---|
| Operating Temperature Range LM319 | 0°C to 70°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 3) LM319

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C$, $R_S \le 5k$ | | 2.0 | 8.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$ | | 80 | 200 | nA |
| Input Bias Current | $T_A = 25°C$ | | 250 | 1000 | nA |
| Voltage Gain | $T_A = 25°C$ (Note 6) | 8 | 40 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$, $V_S = \pm 15V$ | | 80 | | ns |
| Saturation Voltage | $V_{IN} \le -10$ mV, $I_{OUT} = 25$ mA<br>$T_A = 25°C$ | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \ge 10$ mV, $V_{OUT} = 35V$,<br>$V^- = V_{GND} = 0V$, $T_A = 25°C$ | | 0.2 | 10 | μA |
| Input Offset Voltage (Note 4) | $R_S \le 5k$ | | | 10 | mV |
| Input Offset Current (Note 4) | | | | 300 | nA |
| Input Bias Current | | | | 1200 | nA |
| Input Voltage Range | $V_S = \pm 15V$ | | ±13 | | V |
| | $V^+ = 5V$, $V^- = 0$ | 1 | | 3 | V |
| Saturation Voltage | $V^+ \ge 4.5V$, $V^- = 0$<br>$V_{IN} \le -10$ mV, $I_{SINK} \le 3.2$ mA | | 0.3 | 0.4 | V |
| Differential Input Voltage | | | | ±5 | V |
| Positive Supply Current | $T_A = 25°C$, $V^+ = 5V$, $V^- = 0$ | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25°C$, $V_S = \pm 15V$ | | 8 | 12.5 | mA |
| Negative Supply Current | $T_A = 25°C$, $V_S = \pm 15V$ | | 3 | 5 | mA |

**Note 1:** For supply voltages less than ±15 the absolute maximum input voltage is equal to the supply voltage.

**Note 2:** The maximum junction temperature of the LM319 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 3:** These specifications apply for $V_S = \pm 15V$, and $0°C \le T_A \le 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to $V_S$.

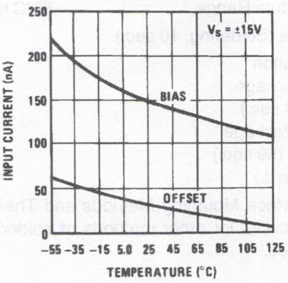
**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

**Note 5:** The response time specified is for a 100 mV input step with 5 mV overdrive.

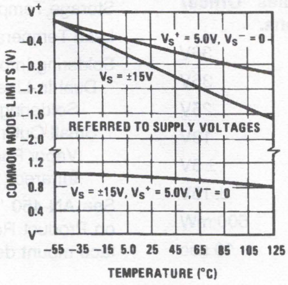
**Note 6:** Output is pulled up to 15V through a 1.4 kΩ resistor.

## Typical Performance Characteristics LM119/LM219

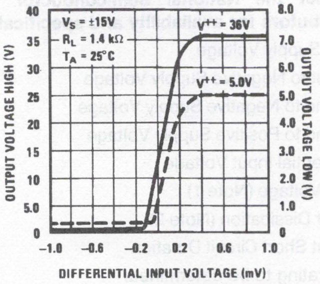
**Input Currents**



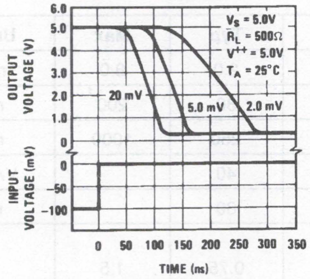
**Common Mode Limits**



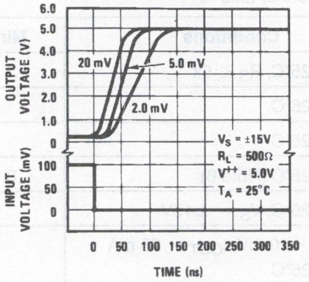
**Transfer Function**



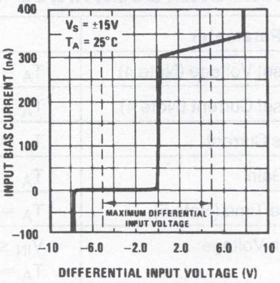
**Response Time for Various Input Overdrives**



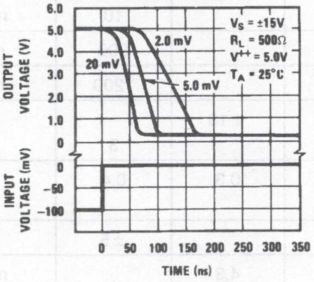
**Response Time for Various Input Overdrives**



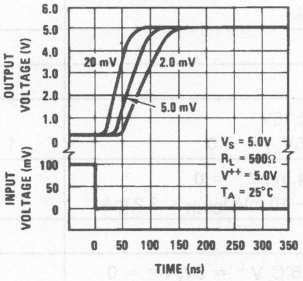
**Input Characteristics**



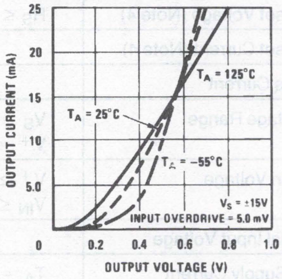
**Response Time for Various Input Overdrives**



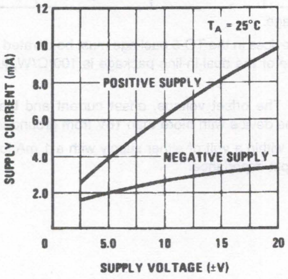
**Response Time for Various Input Overdrives**



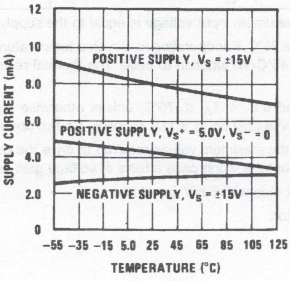
**Output Saturation Voltage**



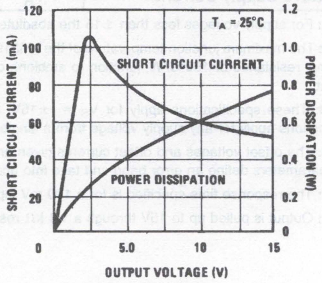
**Supply Current**



**Supply Current**



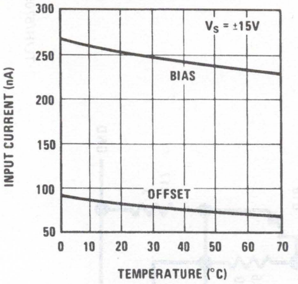
**Output Limiting Characteristics**



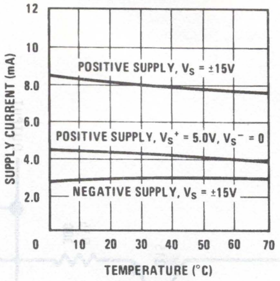
TL/H/5705–2

## Typical Performance Characteristics LM319

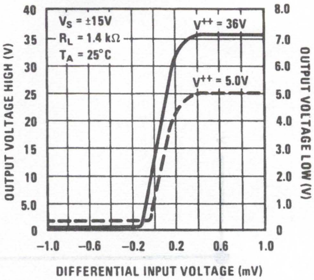
### Input Currents



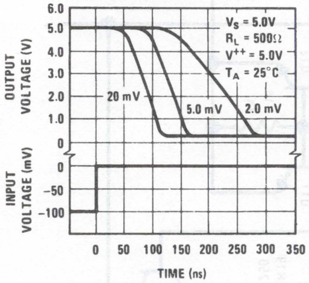
### Supply Currents



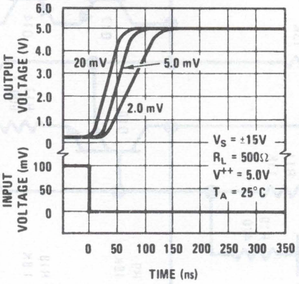
### Transfer Function



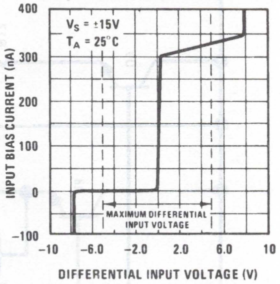
### Response Time for Various Input Overdrives



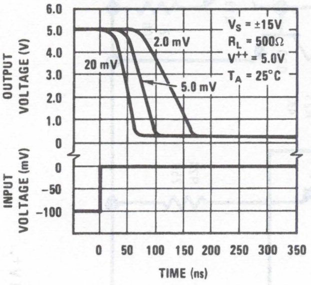
### Response Time for Various Input Overdrives



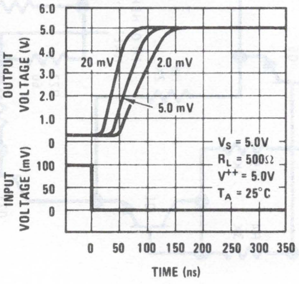
### Input Characteristics



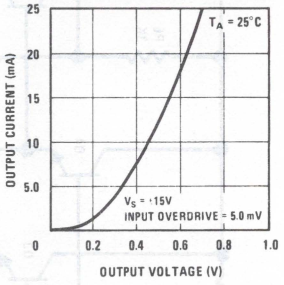
### Response Time for Various Input Overdrives



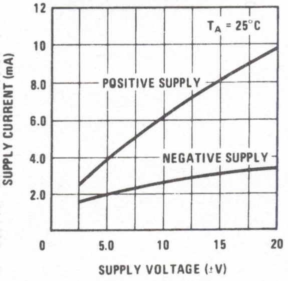
### Response Time for Various Input Overdrives



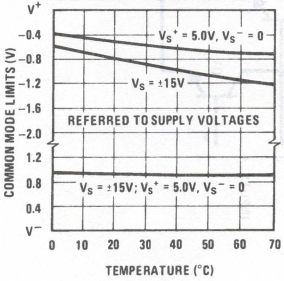
### Output Saturation Voltage



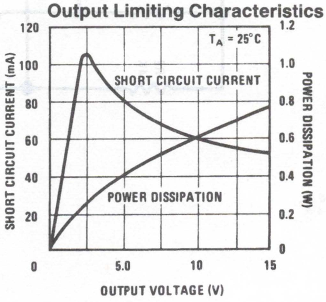
### Supply Current



### Common Mode Limits



### Output Limiting Characteristics



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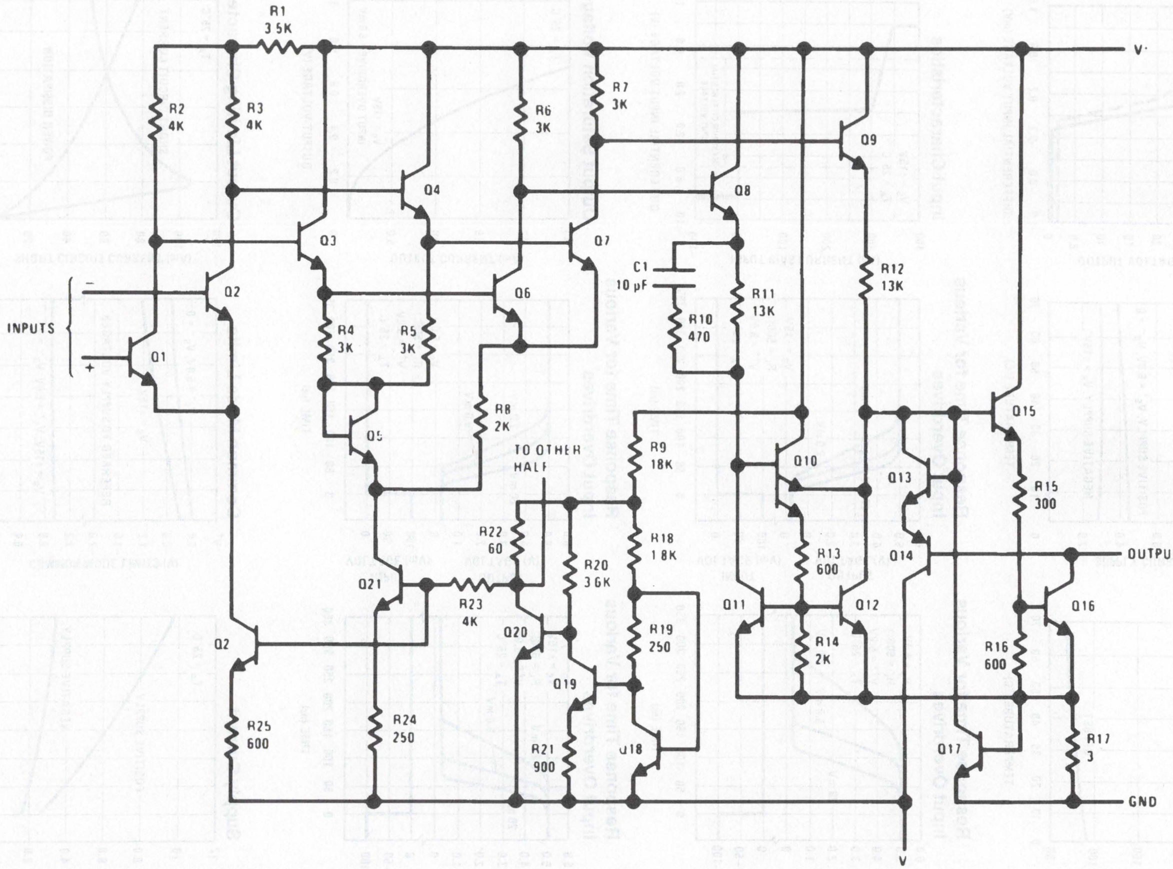
## Schematic Diagram


R1
3.5K
V+
R2
4K
R3
4K
R6
3K
R7
3K
Q9
Q4
Q8
Q3
Q7
C1
10 pF
R12
13K
Q2
Q6
R11
13K
INPUTS
−
+
R10
470
R4
3K
R5
3K
Q1
R8
2K
Q15
Q5
TO OTHER
HALF
R9
18K
Q10
Q13
R15
300
R22
60
R18
1.8K
R20
3.6K
R13
600
Q14
OUTPUT
Q21
R23
4K
Q11
Q12
Q16
Q20
R19
250
R14
2K
R16
600
Q2
Q19
R25
600
R24
250
R21
900
Q18
Q17
R17
3
GND
V−

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*Do not operate the LM119 with more than 16V between GND and V+.

**National Semiconductor Corporation**

# LM139/239/339, LM139A/239A/339A, LM2901, LM3302 Low Power Low Offset Voltage Quad Comparators

## General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

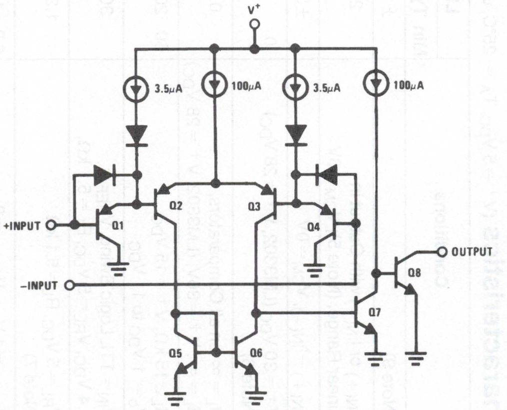
## Advantages

- High precision comparators
- Reduced $V_{OS}$ drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

## Features

- Wide single supply voltage range of dual supplies
  - LM139 series, LM139A series, LM2901: 2 $V_{DC}$ to 36 $V_{DC}$ or ±1 $V_{DC}$ to ±18 $V_{DC}$
  - LM3302: 2 $V_{DC}$ to 28 $V_{DC}$ or ±1 $V_{DC}$ to ±14 $V_{DC}$
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 $V_{DC}$)
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

## Schematic and Connection Diagrams



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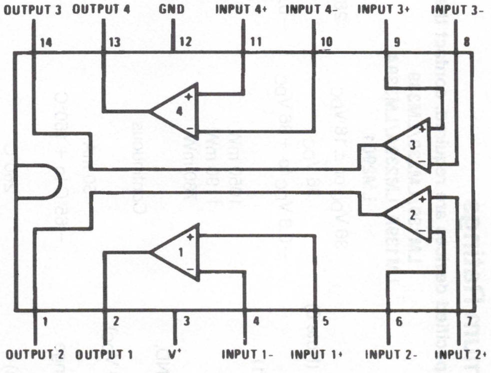
**Dual-In-Line Package**



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**Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J**
**See NS Package Number J14A**
**Order Number LM339AM, LM339M or LM2901M**
**See NS Package Number M14A**
**Order Number LM339N, LM339AN, LM2901N or LM3302N**
**See NS Package Number N14A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**(Note 10)

| | LM139/LM239/LM339<br>LM139A/LM239A/LM339A<br>LM2901 | LM3302 |
|---|---|---|
| Supply Voltage, $V^+$ | 36 $V_{DC}$ or ±18 $V_{DC}$ | 28 $V_{DC}$ or ±14 $V_{DC}$ |
| Differential Input Voltage (Note 8) | 36 $V_{DC}$ | 28 $V_{DC}$ |
| Input Voltage | −0.3 $V_{DC}$ to +36 $V_{DC}$ | −0.3 $V_{DC}$ to +28 $V_{DC}$ |
| Power Dissipation (Note 1) | | |
| Molded DIP | 1050 mW | 1050 mW |
| Cavity DIP | 1190 mW | |
| Small Outline Package | 760 mW | |
| Output Short-Circuit to GND, (Note 2) | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3\ V_{DC}$), (Note 3) | 50 mA | 50 mA |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |

| | LM139/LM239/LM339<br>LM139A/LM239A/LM339A<br>LM2901 | LM3302 |
|---|---|---|
| Operating Temperature Range | | −40°C to +85°C |
| LM339/LM339A | 0°C to +70°C | |
| LM239/LM239A | −25°C to +85°C | |
| LM2901 | −40°C to +85°C | |
| LM139/LM139A | −55°C to +125°C | |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A$ = 25°C, unless otherwise stated)

| Parameter | Conditions | LM139A | | | LM239A, LM339A | | | LM139 | | | LM239, LM339 | | | LM2901 | | | LM3302 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 9) | | ±1.0 | ±2.0 | | ±1.0 | ±2.0 | | ±2.0 | ±5.0 | | ±2.0 | ±5.0 | | ±2.0 | ±7.0 | | ±3 | ±20 | $mV_{DC}$ |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM}$=0V | | 25 | 100 | | 25 | 250 | | 25 | 100 | | 25 | 250 | | 25 | 250 | | 25 | 500 | $nA_{DC}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM}$=0V | | ±3.0 | ±25 | | ±5.0 | ±50 | | ±3.0 | ±25 | | ±5.0 | ±50 | | ±5 | ±50 | | ±3 | ±100 | $nA_{DC}$ |
| Input Common-Mode Voltage Range | $V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | $V_{DC}$ |
| Supply Current | $R_L = \infty$ on all Comparators,<br>$R_L = \infty$, $V^+$=36V, (LM3302, $V^+ = 28\ V_{DC}$) | | 0.8 | 2.0 | | 0.8<br>1.0 | 2.0<br>2.5 | | 0.8<br>1.0 | 2.0<br>2.5 | | 0.8<br>1.0 | 2.0<br>2.5 | | 0.8<br>1.0 | 2.0<br>2.5 | | 0.8<br>1.0 | 2.0<br>2.5 | $mA_{DC}$<br>$mA_{DC}$ |
| Voltage Gain | $R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$<br>$V_o$ = 1 $V_{DC}$ to 11 $V_{DC}$ | 50 | 200 | | 50 | 200 | | 50 | 200 | | 50 | 200 | | 25 | 100 | | 2 | 30 | | V/mV |
| Large Signal Response Time | $V_{IN}$ = TTL Logic Swing, $V_{REF}$ = 1.4 $V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, | | 300 | | | 300 | | | 300 | | | 300 | | | 300 | | | 300 | | ns |
| Response Time | $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, (Note 7) | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | μs |
| Output Sink Current | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$,<br>$V_O \geq 1.5\ V_{DC}$ | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | $mA_{DC}$ |

## Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated) (Continued)

| Parameter | Conditions | LM139A | | | LM239A, LM339A | | | LM139 | | | LM239, LM339 | | | LM2901 | | | LM3302 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Saturation Voltage | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA | | 250 | 400 | | 250 | 400 | | 250 | 400 | | 250 | 400 | | 250 | 400 | | 250 | 500 | $mV_{DC}$ |
| Output Leakage Current | $V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$ | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | $nA_{DC}$ |

## Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

| Parameter | Conditions | LM139A | | | LM239A, LM339A | | | LM139 | | | LM239, LM339 | | | LM2901 | | | LM3302 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 9) | | | ±4.0 | | | ±4.0 | | | ±9.0 | | | ±9.0 | | ±9 | ±15 | | | ±40 | $mV_{DC}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | | ±100 | | | ±150 | | | ±100 | | | ±150 | | ±50 | ±200 | | | ±300 | $nA_{DC}$ |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5) | | | 300 | | | 400 | | | 300 | | | 400 | | 200 | 500 | | | 1000 | $nA_{DC}$ |
| Input Common-Mode Voltage Range | $V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6) | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | $V_{DC}$ |
| Saturation Voltage | $V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA | | | 700 | | | 700 | | | 700 | | | 700 | | 400 | 700 | | | 700 | $mV_{DC}$ |
| Output Leakage Current | $V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$) | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | $\mu A_{DC}$ |
| Differential Input Voltage | Keep all $V_{IN}$'s $\geq 0\ V_{DC}$ (or $V^-$, if used), (Note 8) | | | 36 | | | 36 | | | 36 | | | 36 | | | 36 | | | 28 | $V_{DC}$ |

**Note 1:** For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of $V^+$.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a valve greater than $-0.3\ V_{DC}$ (at 25°)C.

**Note 4:** These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

**Note 5:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

**Note 6:** The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of $V^+$.

**Note 7:** The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

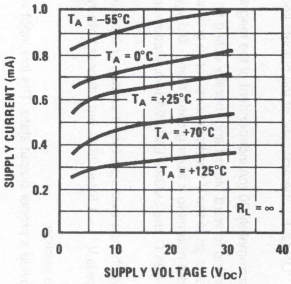
**Note 8:** Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

**Note 9:** At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with $V^+$ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, $V^+$ from $5\ V_{DC}$ to $28\ V_{DC}$.

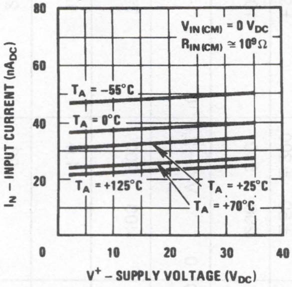
**Note 10:** Refer to RETS139AX for LM139AJ military specifications and to RETS139X for LM139J military specifications.

## Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

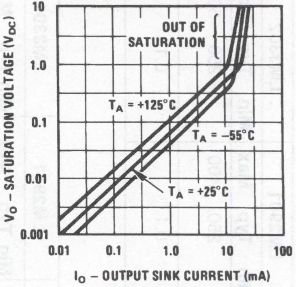
### Supply Current



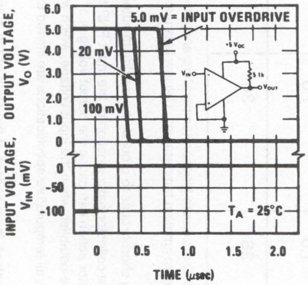
### Input Current



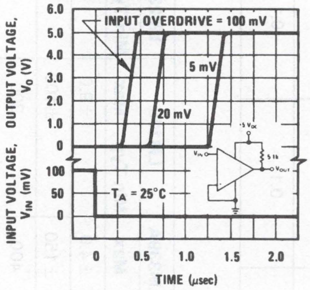
### Output Saturation Voltage



### Response Time for Various Input Overdrives—Negative Transition



### Response Time for Various Input Overdrives—Positive Transition



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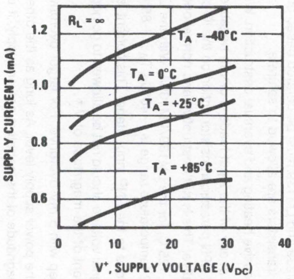
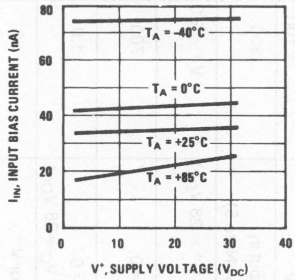
## Typical Performance Characteristics LM2901

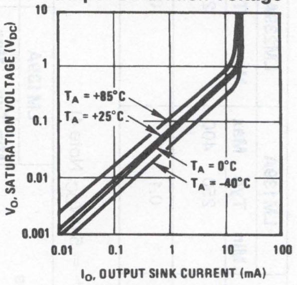
### Supply Current



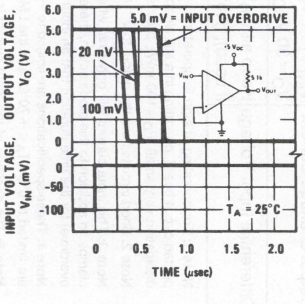
### Input Current



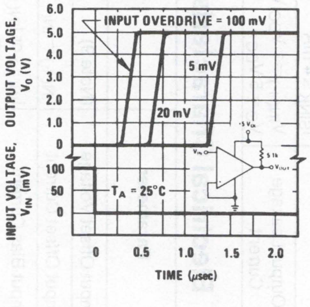
### Output Saturation Voltage



### Response Time for Various Input Overdrives-Negative Transition



### Response Time for Various Input Overdrives-Positive Transition



TL/H/5706–7

## Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10\ \text{k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 $V_{DC}$ to 30 $V_{DC}$.

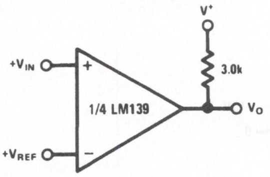
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than $V+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3$ $V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the $V+$ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of $V+$) and the $\beta$ of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\Omega$ $R_{SAT}$ of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

## Typical Applications ($V^+ = 5.0\ V_{DC}$)

### Basic Comparator



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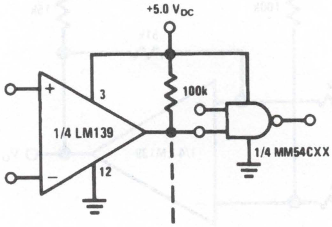
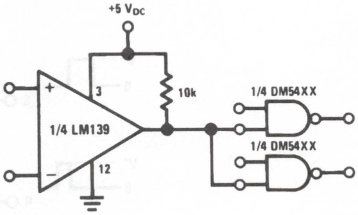
### Driving CMOS



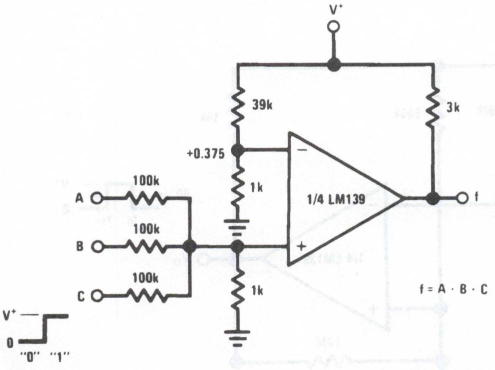
TL/H/5706-4

### Driving TTL



TL/H/5706-5

### AND Gate



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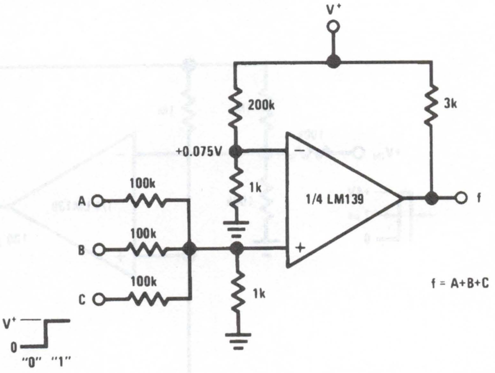
### OR Gate



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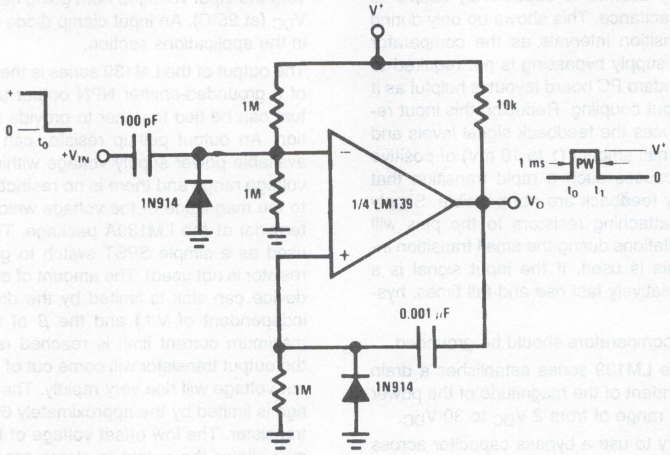
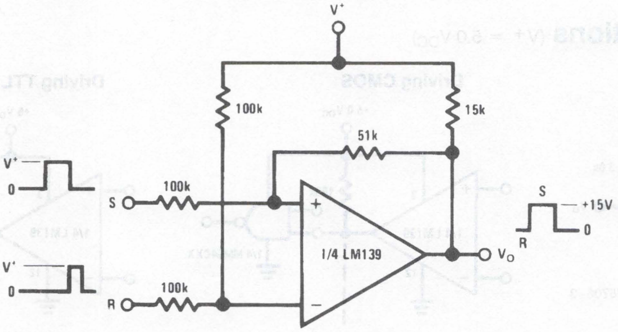
# Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### One-Shot Multivibrator


V+
10k
1M
100 pF
0
$t_0$
$+V_{IN}$
1N914
1M
1/4 LM139
1 ms
PW
V+
0
$t_0$
$t_1$
$V_O$
0.001 μF
1M
1N914

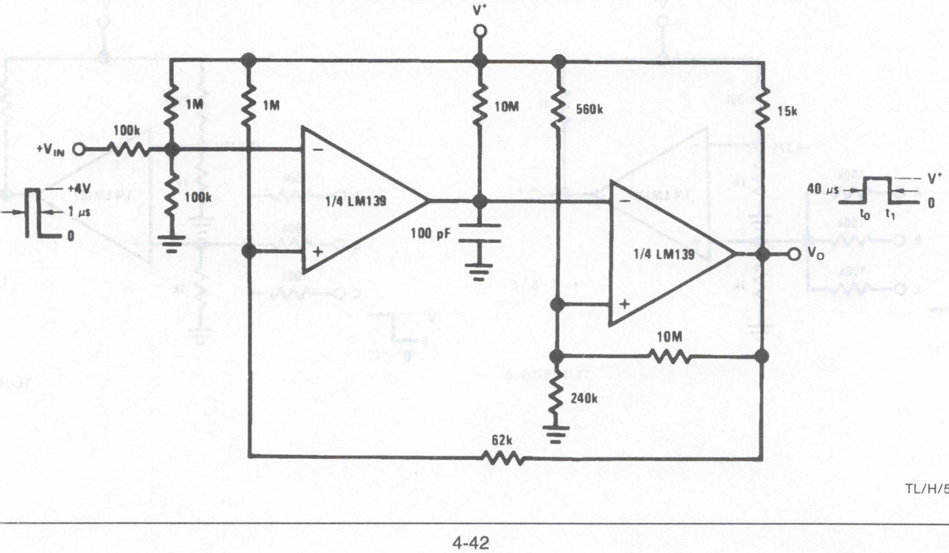
TL/H/5706–10

### Bi-Stable Multivibrator


V+
100k
15k
51k
V+
0
S
100k
V+
0
R
100k
1/4 LM139
$V_O$
S
+15V
0
R

TL/H/5706–11

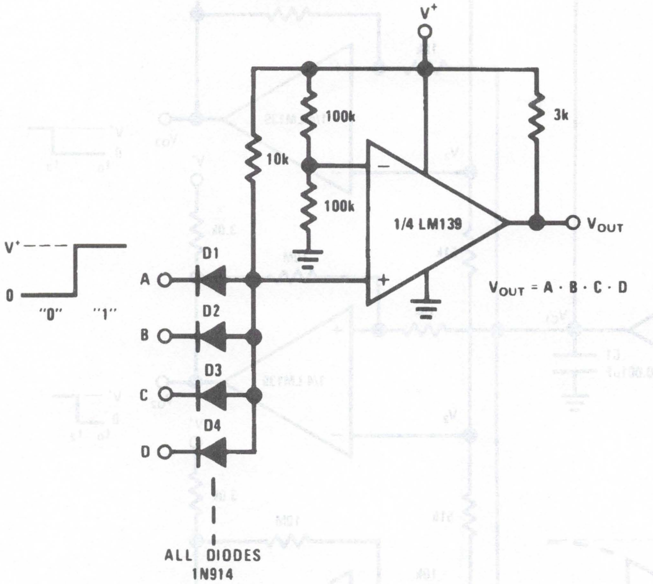
### One-Shot Multivibrator with Input Lock Out


V+
1M
1M
10M
560k
15k
$+V_{IN}$
100k
+4V
1 μs
0
100k
1/4 LM139
100 pF
1/4 LM139
40 μs
V+
0
$t_0$
$t_1$
$V_O$
10M
240k
62k

TL/H/5706–12

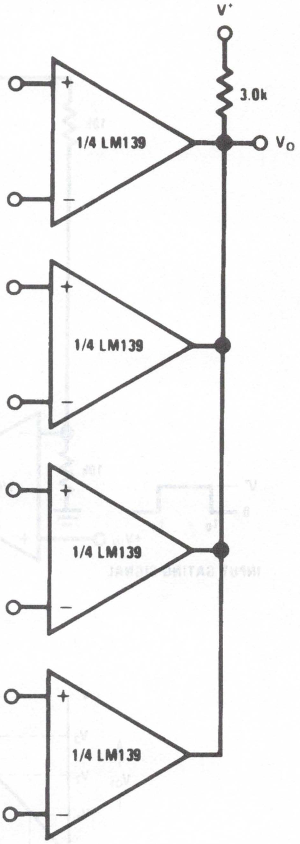
## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Large Fan-In AND Gate


V+
100k
3k
10k
100k
1/4 LM139
VOUT
V+
0
"0"
"1"
D1
A
D2
B
D3
C
D4
D
VOUT = A · B · C · D
ALL DIODES
1N914

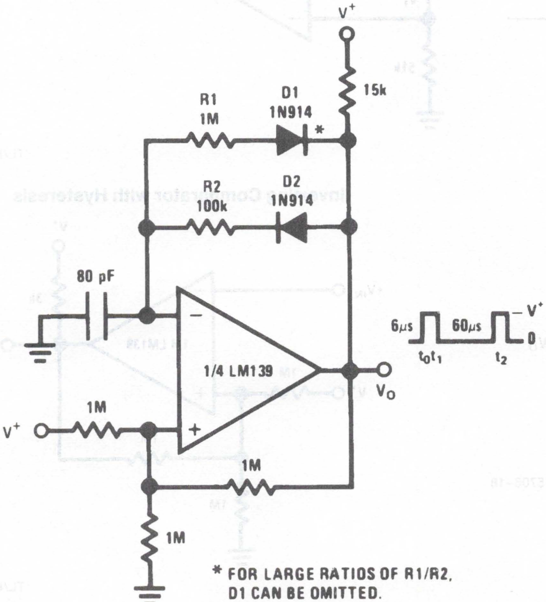
TL/H/5706–13

### ORing the Outputs


V+
3.0k
VO
1/4 LM139
1/4 LM139
1/4 LM139
1/4 LM139

TL/H/5706–15

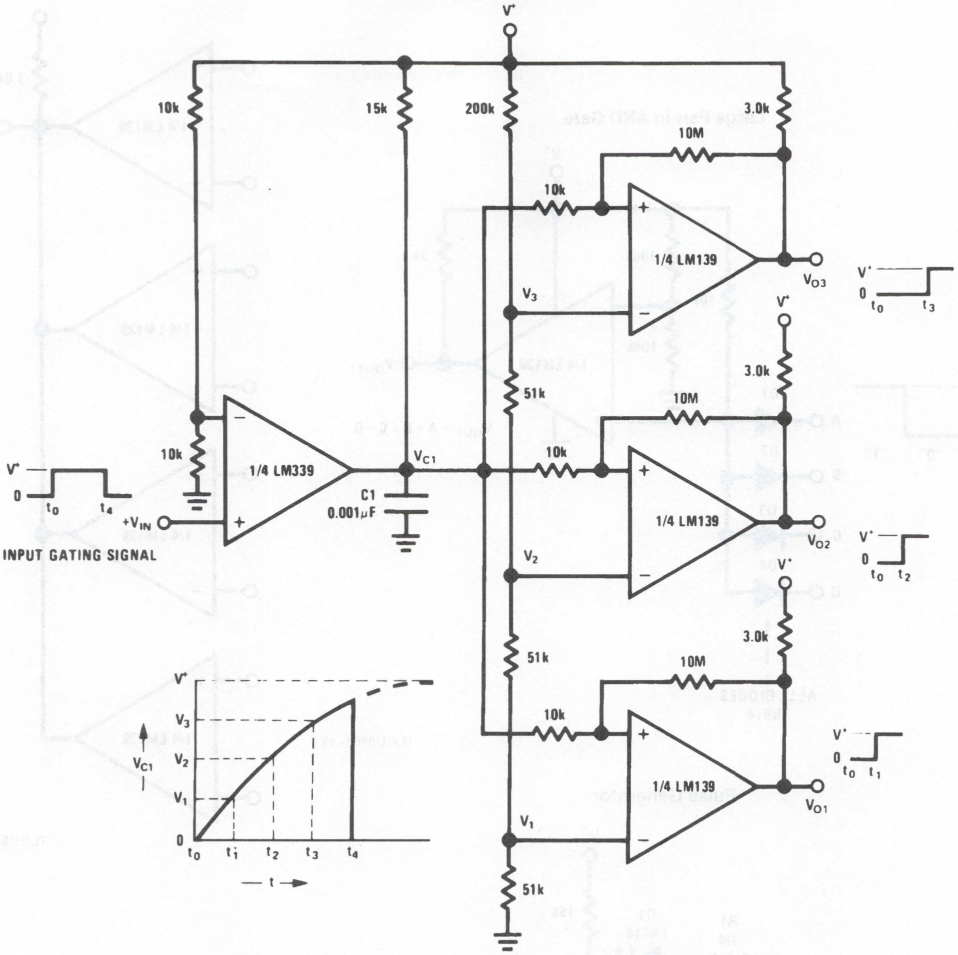
### Pulse Generator


V+
15k
R1
1M
D1
1N914
*
R2
100k
D2
1N914
80 pF
1/4 LM139
VO
6μs
60μs
V+
0
t0 t1
t2
V+
1M
1M
1M
* FOR LARGE RATIOS OF R1/R2, D1 CAN BE OMITTED.

TL/H/5706–17

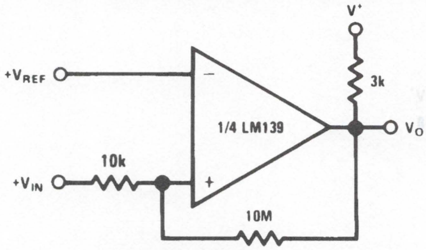
## Typical Applications (V+ = 15 $V_{DC}$) (Continued)

### Time Delay Generator


V⁺
10k
15k
200k
3.0k
10M
10k
1/4 LM139
$V_{O3}$
$V_3$
V⁺
3.0k
51k
10M
10k
10k
1/4 LM339
$V_{C1}$
C1
0.001μF
+$V_{IN}$
V⁺
0
$t_0$
$t_4$
INPUT GATING SIGNAL
1/4 LM139
$V_{O2}$
$V_2$
V⁺
3.0k
51k
10M
10k
1/4 LM139
$V_{O1}$
$V_1$
51k
V⁺
$V_3$
$V_2$
$V_1$
$V_{C1}$
0
$t_0$
$t_1$
$t_2$
$t_3$
$t_4$
t
V⁺
0
$t_0$
$t_3$
V⁺
0
$t_0$
$t_2$
V⁺
0
$t_0$
$t_1$

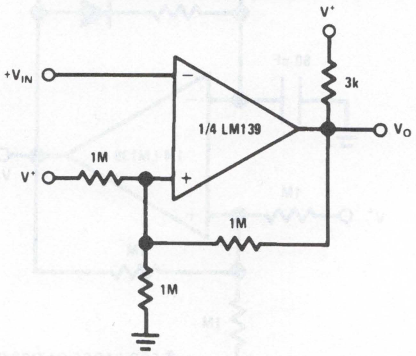
TL/H/5706-14

### Non-Inverting Comparator with Hysteresis


V⁺
+$V_{REF}$
3k
1/4 LM139
$V_O$
10k
+$V_{IN}$
10M

TL/H/5706-18

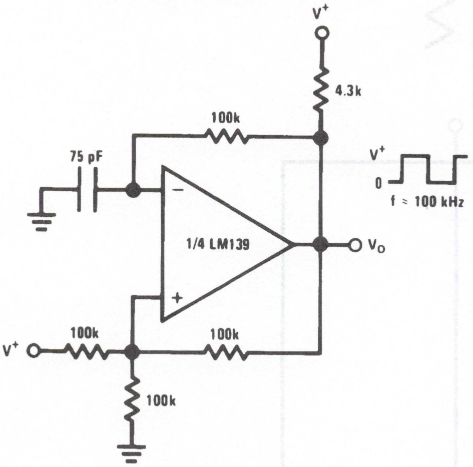
### Inverting Comparator with Hysteresis


V⁺
+$V_{IN}$
3k
1/4 LM139
$V_O$
1M
V⁺
1M
1M

TL/H/5706-19

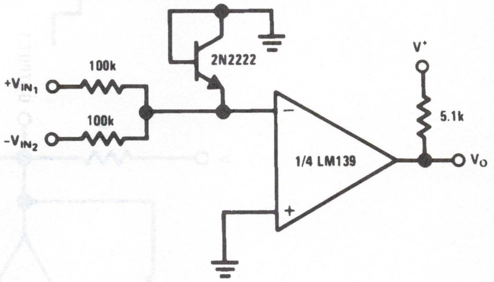
## Typical Applications ($V^{+} = 15\ V_{DC}$) (Continued)

### Squarewave Oscillator


V+
4.3k
100k
75 pF
1/4 LM139
VO
100k
100k
V+
100k
V+
0
f ≈ 100 kHz

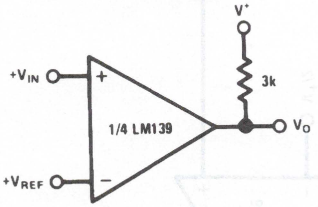
TL/H/5706-16

### Comparing Input Voltages of Opposite Polarity


2N2222
100k
+VIN1
100k
-VIN2
V+
5.1k
1/4 LM139
VO

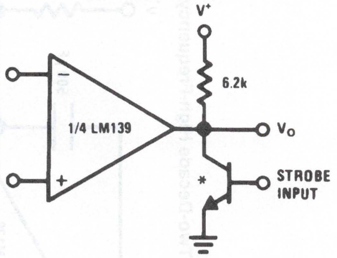
TL/H/5706-20

### Basic Comparator


V+
3k
+VIN
1/4 LM139
VO
+VREF

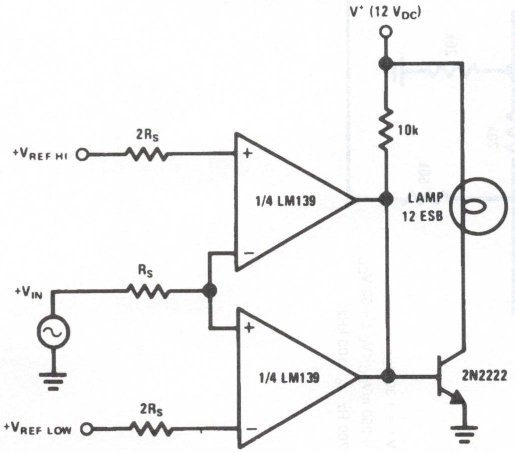
TL/H/5706-21

### Output Strobing


V+
6.2k
1/4 LM139
VO
*
STROBE INPUT

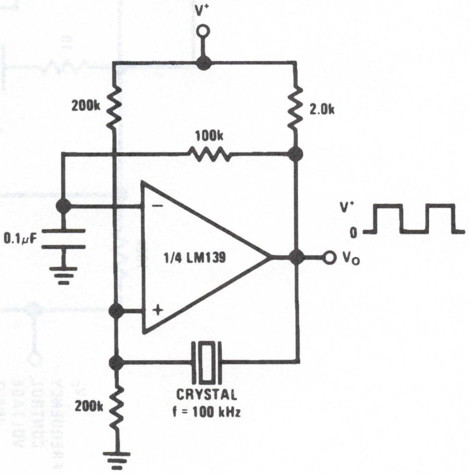
TL/H/5706-22

### Limit Comparator


V+ (12 VDC)
10k
2RS
+VREF HI
1/4 LM139
LAMP
12 ESB
RS
+VIN
1/4 LM139
2N2222
2RS
+VREF LOW

TL/H/5706-24

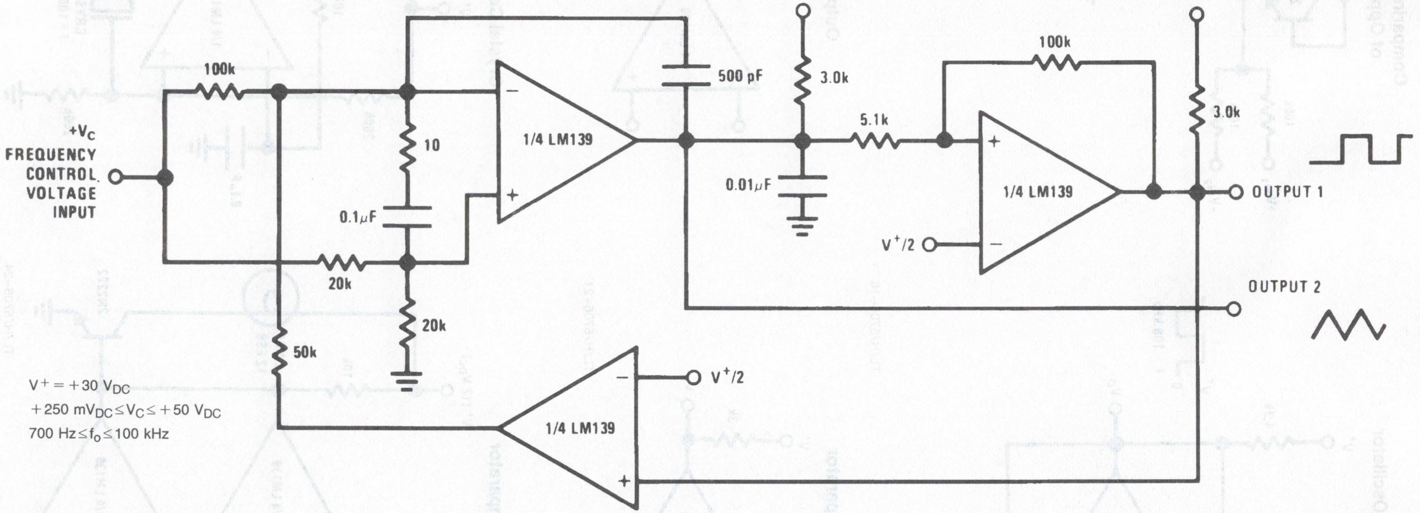
### Crystal Controlled Oscillator


V+
200k
2.0k
100k
0.1μF
1/4 LM139
V+
0
VO
CRYSTAL
f = 100 kHz
200k

TL/H/5706-25

## Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

### Two-Decade High-Frequency VCO


100k
+V_C
FREQUENCY
CONTROL
VOLTAGE
INPUT
10
0.1µF
20k
20k
50k
1/4 LM139
500 pF
V+
3.0k
0.01µF
5.1k
100k
V+
3.0k
1/4 LM139
V+/2
OUTPUT 1
OUTPUT 2
1/4 LM139
V+/2

$V^+ = +30\ V_{DC}$

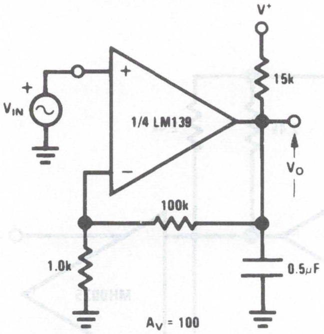
$+250\ mV_{DC} \leq V_C \leq +50\ V_{DC}$

$700\ Hz \leq f_o \leq 100\ kHz$

TL/H/5706–23

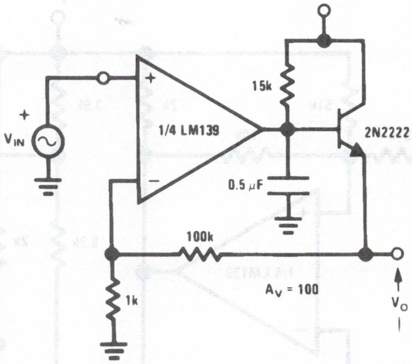
## Typical Applications $(V^+ = 5\ V_{DC})$ (Continued)

### Low Frequency Op Amp


V+
+
VIN
1/4 LM139
+
−
15k
VO
100k
1.0k
0.5µF
AV = 100

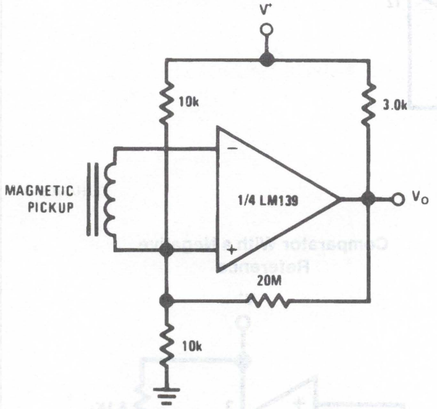
TL/H/5706-26

### Low Frequency Op Amp ($V_O$ = 0V for $V_{IN}$ = 0V)


V+
+
VIN
1/4 LM139
+
−
15k
2N2222
0.5 µF
100k
1k
AV = 100
VO

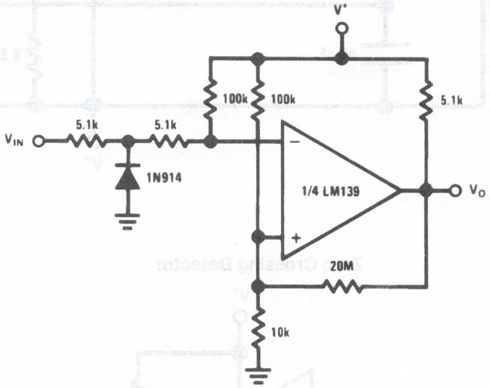
TL/H/5706-27

### Transducer Amplifier


V+
10k
3.0k
MAGNETIC PICKUP
1/4 LM139
−
+
VO
20M
10k

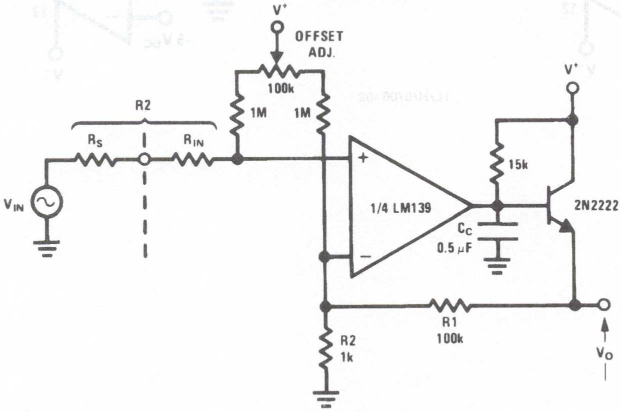
TL/H/5706-28

### Zero Crossing Detector (Single Power Supply)


V+
100k
100k
5.1k
VIN
5.1k
5.1k
1N914
1/4 LM139
−
+
VO
20M
10k

TL/H/5706-30

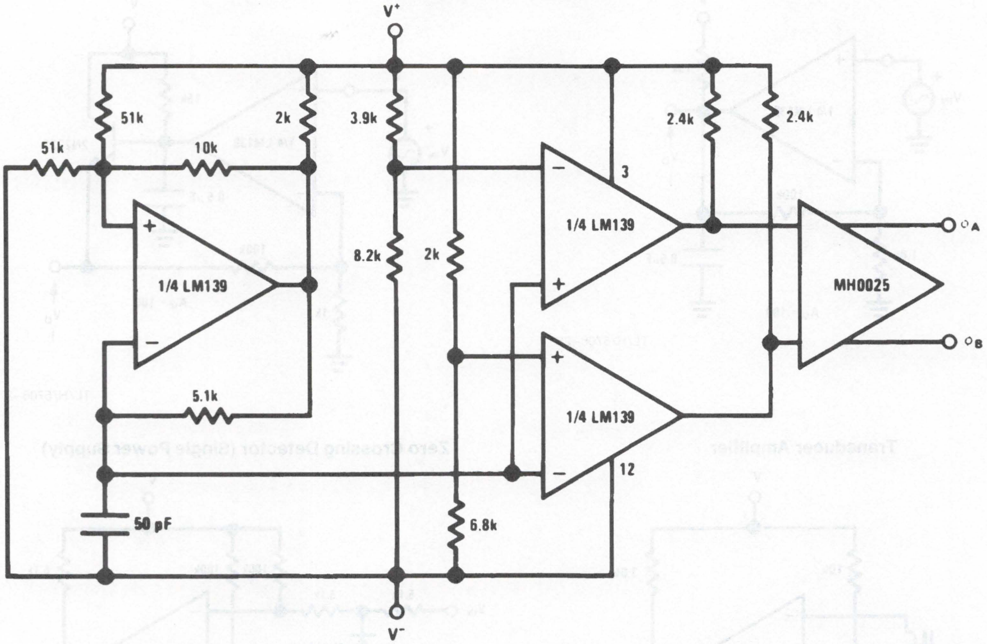
### Low Frequency Op Amp with Offset Adjust


V+
OFFSET ADJ.
100k
1M
1M
R2
RS
RIN
VIN
1/4 LM139
+
−
V+
15k
2N2222
CC
0.5 µF
R1
100k
R2
1k
VO

TL/H/5706-29

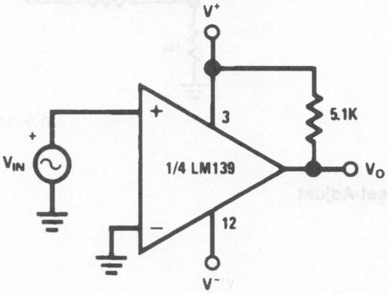
## Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

### MOS Clock Driver


V⁺
51k
2k
3.9k
2.4k
2.4k
51k
10k
3
1/4 LM139
1/4 LM139
8.2k
2k
MH0025
ϕA
ϕB
1/4 LM139
5.1k
12
50 pF
6.8k
V⁻

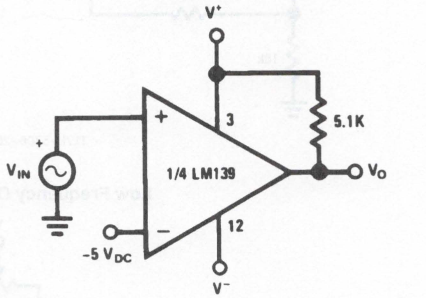
TL/H/5706-31

### Zero Crossing Detector


V⁺
3
5.1K
+
V_IN
1/4 LM139
V_O
12
V⁻

TL/H/5706-32

### Comparator With a Negative Reference


V⁺
3
5.1K
+
V_IN
1/4 LM139
V_O
-5 V_DC
12
V⁻

TL/H/5706-33

**National Semiconductor Corporation**

# LM160/LM260/LM360 High Speed Differential Comparator

## General Description

The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

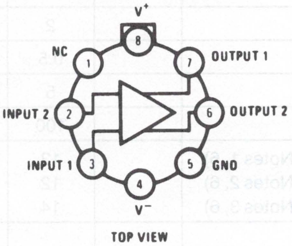
Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

## Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

## Connection Diagrams

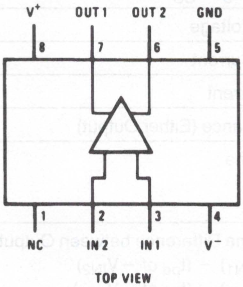
**Metal Can Package**


V⁺
8
NC
1
7
OUTPUT 1
INPUT 2
2
6
OUTPUT 2
INPUT 1
3
5
GND
4
V⁻
TOP VIEW

TL/H/5707–4

**Order Number LM160H, LM260H or LM360H**
**See NS Package Number H08C**

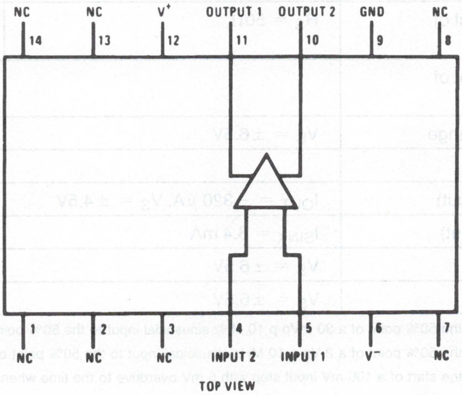
**Dual-In-Line Package**


V⁺
OUT 1
OUT 2
GND
8
7
6
5
1
2
3
4
NC
IN 2
IN 1
V⁻
TOP VIEW

TL/H/5707–5

**Order Number LM360M or LM360N**
**See NS Package Number M08A or N08E**

**Dual-In-Package**


NC
NC
V⁺
OUTPUT 1
OUTPUT 2
GND
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
NC
INPUT 2
INPUT 1
V⁻
NC
TOP VIEW

TL/H/5707–6

**Order Number LM160J-14, LM360J-14 or LM360N-14**
**See NS Package Number J14A or N14A**

## Absolute Maximum Ratings (Note 5)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

**(Note 7)**

| | |
|---|---|
| Positive Supply Voltage | +8V |
| Negative Supply Voltage | −8V |
| Peak Output Current | 20 mA |
| Differential Input Voltage | ±5V |
| Input Voltage | $V^+ \geq V_{IN} \geq V^-$ |

ESD rating is to be determined.

| | |
|---|---|
| Operating Temperature Range | |
| LM160 | −55°C to +125°C |
| LM260 | −25°C to +85°C |
| LM360 | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operating Conditions | | | | | |
| Supply Voltage $V_{CC}^+$ | | 4.5 | 5 | 6.5 | V |
| Supply Voltage $V_{CC}^-$ | | −4.5 | −5 | −6.5 | V |
| Input Offset Voltage | $R_S \leq 200\Omega$ | | 2 | 5 | mV |
| Input Offset Current | | | 0.5 | 3 | μA |
| Input Bias Current | | | 5 | 20 | μA |
| Output Resistance (Either Output) | $V_{OUT} = V_{OH}$ | | 100 | | Ω |
| Response Time | $T_A = 25°C$, $V_S = \pm 5V$ (Notes 1, 6) | | 13 | 25 | ns |
| | $T_A = 25°C$, $V_S = \pm 5V$ (Notes 2, 6) | | 12 | 20 | ns |
| | $T_A = 25°C$, $V_S = \pm 5V$ (Notes 3, 6) | | 14 | | ns |
| Response Time Difference between Outputs | | | | | |
| ($t_{pd}$ of $+V_{IN1}$) − ($t_{pd}$ of $-V_{IN2}$) | $T_A = 25°C$ (Notes 1, 6) | | 2 | | ns |
| ($t_{pd}$ of $+V_{IN2}$) − ($t_{pd}$ of $-V_{IN1}$) | $T_A = 25°C$ (Notes 1, 6) | | 2 | | ns |
| ($t_{pd}$ of $+V_{IN1}$) − ($t_{pd}$ of $+V_{IN2}$) | $T_A = 25°C$ (Notes 1, 6) | | 2 | | ns |
| ($t_{pd}$ of $-V_{IN1}$) − ($t_{pd}$ of $-V_{IN2}$) | $T_A = 25°C$ (Notes 1, 6) | | 2 | | ns |
| Input Resistance | f = 1 MHz | | 17 | | kΩ |
| Input Capacitance | f = 1 MHz | | 3 | | pF |
| Average Temperature Coefficient of Input Offset Voltage | $R_S = 50\Omega$ | | 8 | | μV/°C |
| Average Temperature Coefficient of Input Offset Current | | | 7 | | nA/°C |
| Common Mode Input Voltage Range | $V_S = \pm 6.5V$ | ±4 | ±4.5 | | V |
| Differential Input Voltage Range | | ±5 | | | V |
| Output High Voltage (Either Output) | $I_{OUT} = -320\ \mu A$, $V_S = \pm 4.5V$ | 2.4 | 3 | | V |
| Output Low Voltage (Either Output) | $I_{SINK} = 6.4$ mA | | 0.25 | 0.4 | V |
| Positive Supply Current | $V_S = \pm 6.5V$ | | 18 | 32 | mA |
| Negative Supply Current | $V_S = \pm 6.5V$ | | −9 | −16 | mA |

**Note 1:** Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

**Note 2:** Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

**Note 3:** Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

**Note 4:** Typical thermal impedances are as follows:

| | | | | | | |
|---|---|---|---|---|---|---|
| Cavity DIP (J): | $\theta_{jA}$ | 135°C/W | Header (H) | $\theta_{jA}$ | 230°C/W | (Still Air) |
| Molded DIP (N): | $\theta_{jA}$ | 130°C/W | | | 190°C/W | (400 LF/min Air Flow) |
| | | | | $\theta_{jC}$ | 25°C/W | |

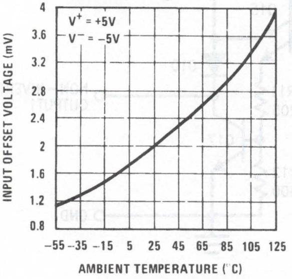
**Note 5:** The device may be damaged if used beyond the maximum ratings.

**Note 6:** Measurements are made in AC Test Circuit, Fanout = 1

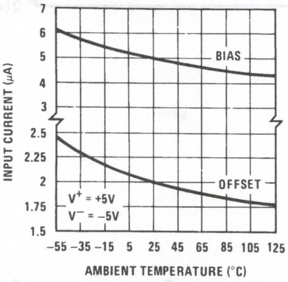
**Note 7:** Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

# Typical Performance Characteristics

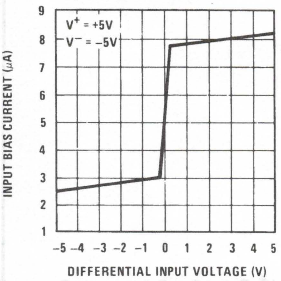
**Offset Voltage**



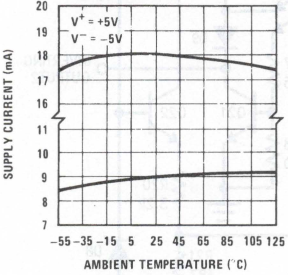
**Input Currents vs Ambient Temperature**



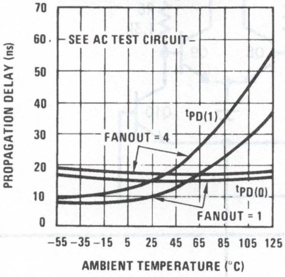
**Input Characteristics**



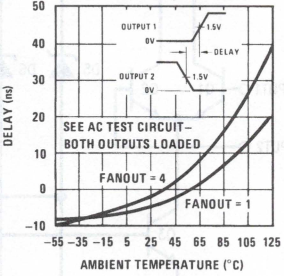
**Supply Current vs Ambient Temperature**



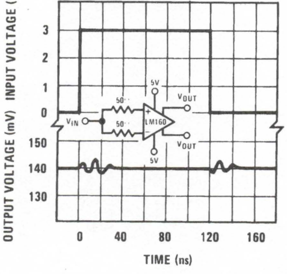
**Propagation Delay vs Ambient Temperature**



**Delay of Output 1 With Respect to Output 2 vs Ambient Temperature**

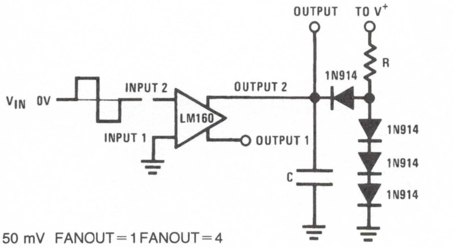


**Common-Mode Pulse Response**



TL/H/5707-2

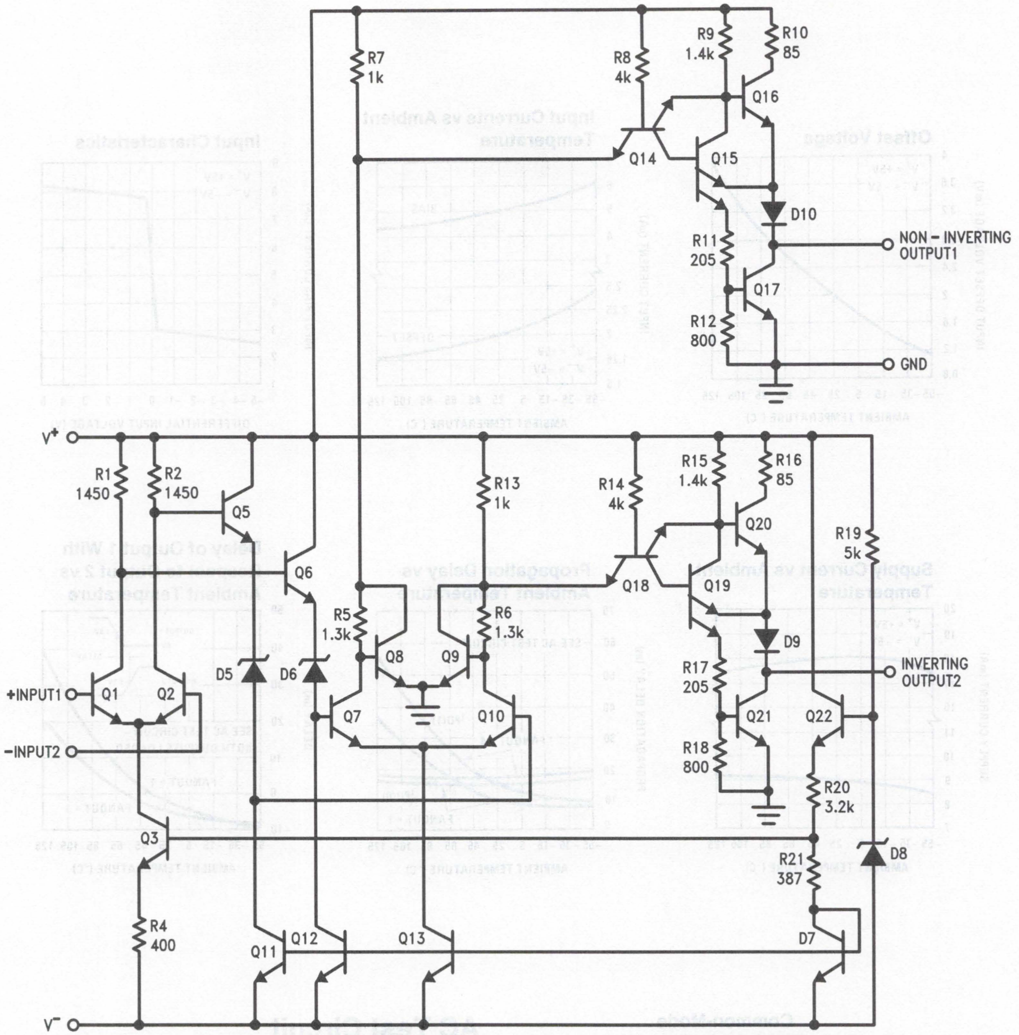
## AC Test Circuit


OUTPUT
TO V+
R
1N914
VIN 0V
INPUT 2
OUTPUT 2
LM160
INPUT 1
OUTPUT 1
1N914
1N914
1N914
C

| | | |
|---|---|---|
| $V_{IN} = \pm 50$ mV | FANOUT = 1 | FANOUT = 4 |
| $V^+ = +5V$ | R = 2.4k | R = 630Ω |
| $V^- = -5V$ | C = 15 pF | C = 30 pF |

TL/H/5707-3

## Schematic Diagram


R7
1k
R8
4k
R9
1.4k
R10
85
Q16
Q14
Q15
D10
NON – INVERTING
OUTPUT1
R11
205
Q17
R12
800
GND
V+
R1
1450
R2
1450
Q5
Q6
R13
1k
R14
4k
R15
1.4k
R16
85
Q20
R19
5k
Q18
Q19
R5
1.3k
R6
1.3k
D9
D5
D6
Q8
Q9
INVERTING
OUTPUT2
+INPUT1
Q1
Q2
Q7
Q10
R17
205
Q21
Q22
–INPUT2
R18
800
R20
3.2k
Q3
D8
R21
387
R4
400
Q11
Q12
Q13
D7
V–

TL/H/5707–1

**National Semiconductor Corporation**

# LM161/LM261/LM361 High Speed Differential Comparators

## General Description

The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

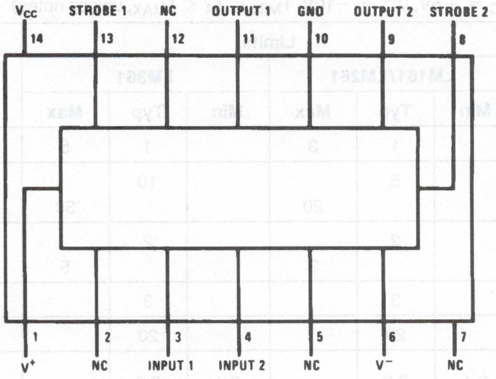
Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

## Features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

## Connection Diagrams

**Dual-In-Line Package**


$V_{CC}$
STROBE 1
NC
OUTPUT 1
GND
OUTPUT 2
STROBE 2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
$V^+$
NC
INPUT 1
INPUT 2
NC
$V^-$
NC

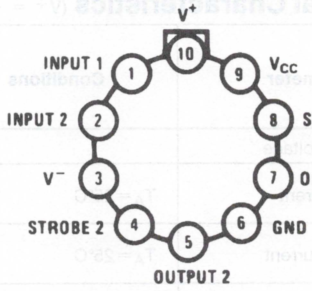
TL/H/5708–2

**Top View**

**Order Number LM161J, LM261J, LM361J, LM361M or LM361N**

**See NS Package Number J14A, M14A or N14A**

**Metal Can Package**

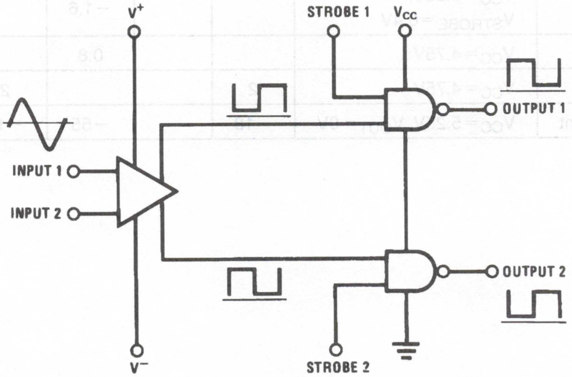

$V^+$
10
INPUT 1
1
9
$V_{CC}$
INPUT 2
2
8
STROBE 1
$V^-$
3
7
OUTPUT 1
STROBE 2
4
6
GND
5
OUTPUT 2

TL/H/5708–3

**Order Number LM161H, LM261H or LM361H**

**See NS Package H10C**

## Logic Diagram


$V^+$
STROBE 1
$V_{CC}$
OUTPUT 1
INPUT 1
INPUT 2
OUTPUT 2
$V^-$
STROBE 2

TL/H/5708–4

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | | |
|---|---|---|
| Positive Supply Voltage, $V^+$ | | +16V |
| Negative Supply Voltage, $V^-$ | | −16V |
| Gate Supply Voltage, $V_{CC}$ | | +7V |
| Output Voltage | | +7V |
| Differential Input Voltage | | ±5V |
| Input Common Mode Voltage | | ±6V |
| Power Dissipation | | 600 mW |
| Storage Temperature Range | | −65°C to +150°C |
| Operating Temperature Range | $T_{MIN}$ | $T_{MAX}$ |
| LM161 | −55°C to | +125°C |
| LM261 | −25°C to | +85°C |
| LM361 | 0°C to | +70°C |
| Lead Temp. (Soldering, 10 seconds) | | 260°C |
| For Any Device Lead Below $V^-$ | | 0.3V |

## Operating Conditions

| | Min | Typ | Max |
|---|---|---|---|
| Supply Voltage $V^+$ | | | |
| LM161/LM261 | 5V | | 15V |
| LM361 | 5V | | 15V |
| Supply Voltage $V^-$ | | | |
| LM161/LM261 | −6V | | −15V |
| LM361 | −6V | | −15V |
| Supply Voltage $V_{CC}$ | | | |
| LM161/LM261 | 4.5V | 5V | 5.5V |
| LM361 | 4.75V | 5V | 5.25V |

ESD rating to be determined.

| | |
|---|---|
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

## Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

| Parameter | Conditions | LM161/LM261 Min | LM161/LM261 Typ | LM161/LM261 Max | LM361 Min | LM361 Typ | LM361 Max | Units |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | | | 1 | 3 | | 1 | 5 | mV |
| Input Bias Current | $T_A = 25°C$ | | 5 | | | 10 | | µA |
| | | | | 20 | | | 30 | µA |
| Input Offset Current | $T_A = 25°C$ | | 2 | | | 2 | | µA |
| | | | | 3 | | | 5 | µA |
| Voltage Gain | $T_A = 25°C$ | | 3 | | | 3 | | V/mV |
| Input Resistance | $T_A = 25°C$, f = 1 kHz | | 20 | | | 20 | | kΩ |
| Logical "1" Output Voltage | $V_{CC} = 4.75V$,<br>$I_{SOURCE} = -0.5$ mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| Logical "0" Output Voltage | $V_{CC} = 4.75V$,<br>$I_{SINK} = 6.4$ mA | | | 0.4 | | | 0.4 | V |
| Strobe Input "1" Current | $V_{CC} = 5.25V$,<br>$V_{STROBE} = 2.4V$ | | | 200 | | | 200 | µA |
| Strobe Input "0" Current | $V_{CC} = 5.25V$,<br>$V_{STROBE} = 0.4V$ | | | −1.6 | | | −1.6 | mA |
| Strobe Input "0" Voltage | $V_{CC} = 4.75V$ | | | 0.8 | | | 0.8 | V |
| Strobe Input "1" Voltage | $V_{CC} = 4.75V$ | 2 | | | 2 | | | V |
| Output Short Circuit Current | $V_{CC} = 5.25V$, $V_{OUT} = 0V$ | −18 | | −55 | −18 | | −55 | mA |

## Electrical Characteristics (Continued)

($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

| Parameter | Conditions | LM161/LM261 Min | LM161/LM261 Typ | LM161/LM261 Max | LM361 Min | LM361 Typ | LM361 Max | Units |
|---|---|---|---|---|---|---|---|---|
| Supply Current $I^+$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$ | | | 4.5 | | | | mA |
| Supply Current $I^+$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$ | | | | | | 5 | mA |
| Supply Current $I^-$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$ | | | 10 | | | | mA |
| Supply Current $I^-$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$ | | | | | | 10 | mA |
| Supply Current $I_{CC}$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$ | | | 18 | | | | mA |
| Supply Current $I_{CC}$ | $V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$ | | | | | | 20 | mA |
| Transient Response | $V_{IN} = 50$ mV overdrive (Note 3) | | | | | | | |
| Propagation Delay Time ($t_{pd(0)}$) | $T_A = 25°C$ | | 14 | 20 | | 14 | 20 | ns |
| Propagation Delay Time ($t_{pd(1)}$) | $T_A = 25°C$ | | 14 | 20 | | 14 | 20 | ns |
| Delay Between Output A and B | $T_A = 25°C$ | | 2 | 5 | | 2 | 5 | ns |
| Strobe Delay Time ($t_{pd(0)}$) | $T_A = 25°C$ | | 8 | | | 8 | | ns |
| Strobe Delay Time ($t_{pd(1)}$) | $T_A = 25°C$ | | 8 | | | 8 | | ns |

**Note 1:** The device may be damaged by use beyond the maximum ratings.

**Note 2:** Typical thermal impedances are as follows:

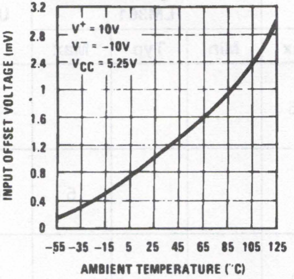
| | H Package | J Package | N Package |
|---|---|---|---|
| $\theta_{jA}$ | 230°C/W (Still Air)<br>190°C/W (400 LF/Min Air Flow) | 112°C/W | 105°C/W |
| $\theta_{jC}$ | 25°C/W | | |

**Note 3:** Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

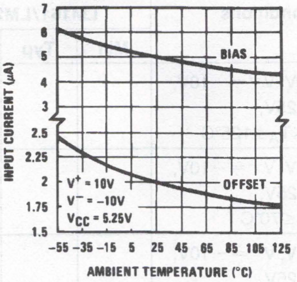
**Note 4:** Refer to RETS161X for LM161H and LM161J military specifications.

## Typical Performance Characteristics

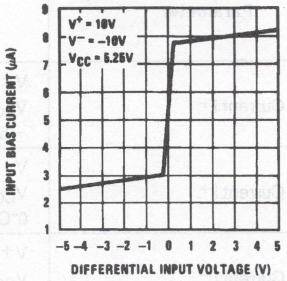
Offset Voltage



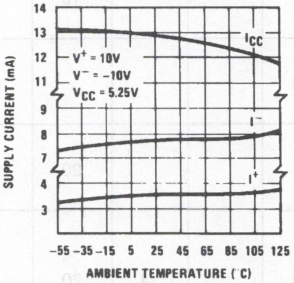
Input Currents vs Ambient Temperature



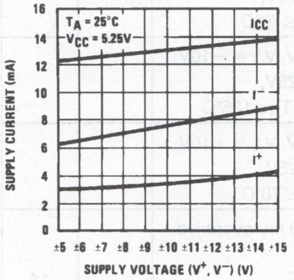
Input Characteristics



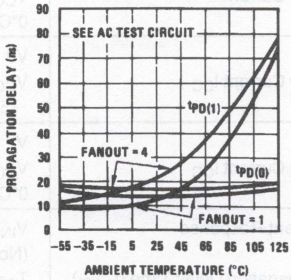
Supply Current vs Ambient Temperature



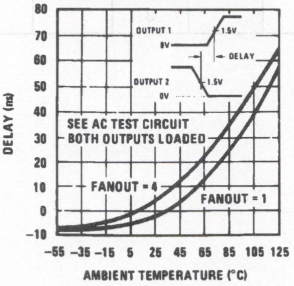
Supply Current vs Supply Voltage



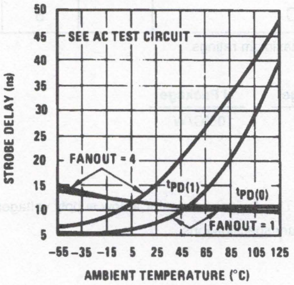
Propagation Delay vs Ambient Temperature



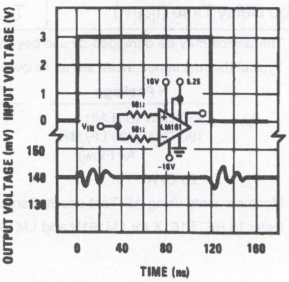
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Strobe Delay vs Ambient Temperature

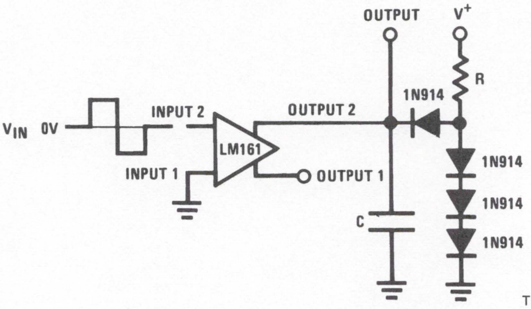


Common-Mode Pulse Response



TL/H/5708-5

## AC Test Circuit

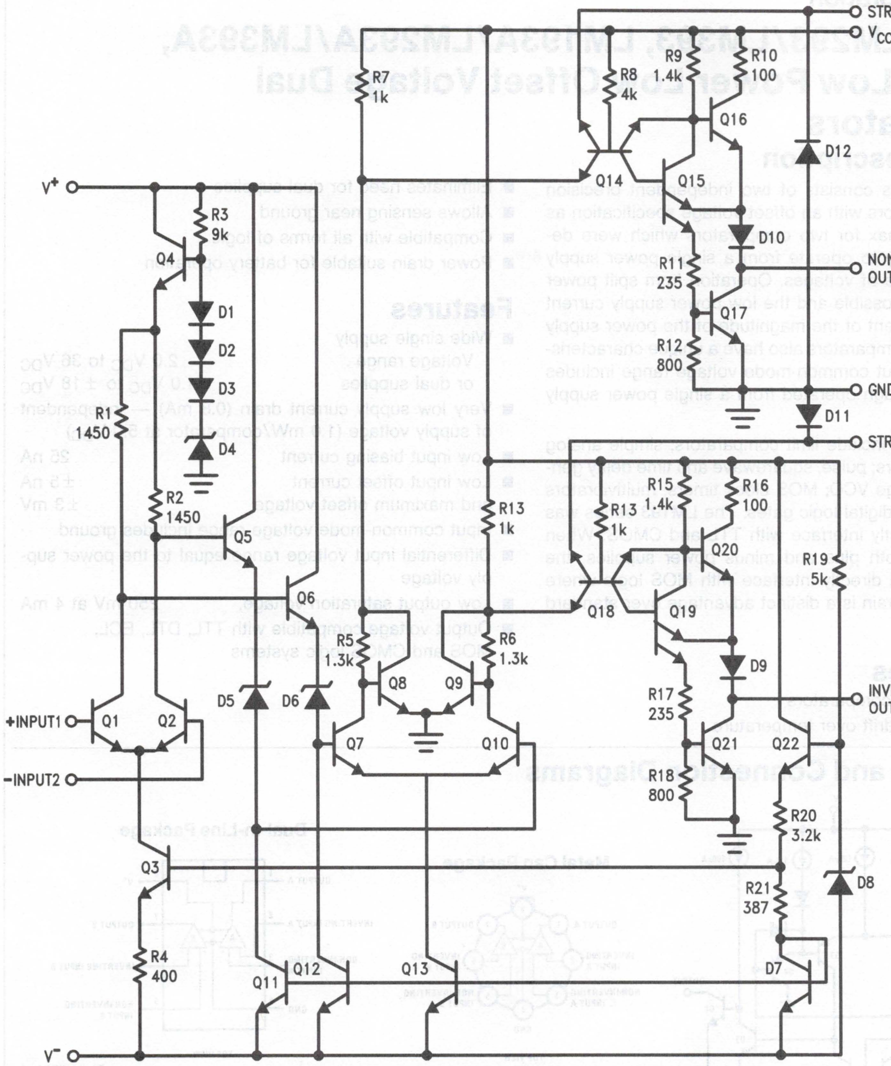

OUTPUT
V+
R
1N914
VIN
0V
INPUT 2
OUTPUT 2
LM161
INPUT 1
OUTPUT 1
1N914
1N914
1N914
C

| $V_{IN}$ = ±50 mV | FANOUT = 1 | FANOUT = 4 |
|---|---|---|
| $V^+$ = +10V | R = 2.4k | R = 680Ω |
| $V^-$ = −10V | C = 15 pF | C = 30 pF |
| $V_{CC}$ = 5.25V | | |

TL/H/5708-6

## Schematic Diagram

LM161


STROBE1
V_CC
R9
1.4k
R10
100
R7
1k
R8
4k
Q16
D12
Q14
Q15
V+
R3
9k
D10
Q4
NON-INVERTING
OUTPUT1
R11
235
D1
Q17
D2
R12
800
GND
D3
R1
1450
D11
D4
STROBE2
R15
1.4k
R16
100
R13
1.4k
R2
1450
R13
1k
Q20
R19
5k
Q5
Q6
Q18
Q19
R5
1.3k
R6
1.3k
D9
Q8
Q9
R17
235
INVERTING
OUTPUT2
D5
D6
+INPUT1
Q1
Q2
Q7
Q10
Q21
Q22
-INPUT2
R18
800
R20
3.2k
Q3
R21
387
D8
R4
400
Q12
Q13
D7
Q11
V-

TL/H/5708-1

R10, R16: 85

R11, R17: 205

**National Semiconductor Corporation**

# LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

## General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

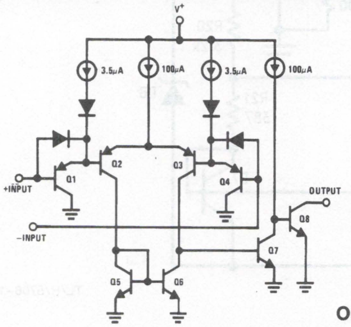
## Advantages

- High precision comparators
- Reduced $V_{OS}$ drift over temperature

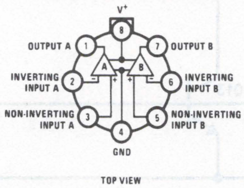
## Features

- Wide single supply
  - Voltage range 2.0 $V_{DC}$ to 36 $V_{DC}$
  - or dual supplies ±1.0 $V_{DC}$ to ±18 $V_{DC}$
- Very low supply current drain (0.8 mA) — independent of supply voltage (1.0 mW/comparator at 5.0 $V_{DC}$)
- Low input biasing current 25 nA
- Low input offset current ±5 nA and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

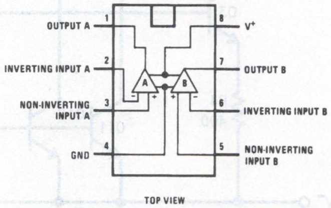
## Schematic and Connection Diagrams


V+
3.5µA
100µA
3.5µA
100µA
Q1
Q2
Q3
Q4
+INPUT
−INPUT
OUTPUT
Q8
Q7
Q5
Q6

**Metal Can Package**


V+
8
OUTPUT A 1
7 OUTPUT B
INVERTING INPUT A 2
6 INVERTING INPUT B
NON-INVERTING INPUT A 3
5 NON-INVERTING INPUT B
4
GND
A
B
TOP VIEW

**Dual-In-Line Package**


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
GND 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B
TOP VIEW

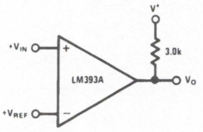
TL/H/5709–1

**Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH**
**See NS Package Number H08C**

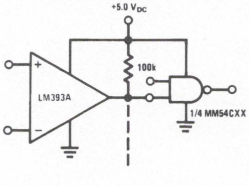
**Order Number LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM393AN or LM2903N**
**See NS Package Number J08A, M08A or N08E**

## Typical Applications ($V^+ = 5.0\ V_{DC}$)

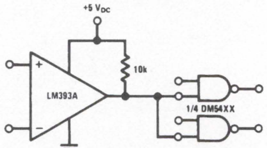
**Basic Comparator**


V+
+VIN
+VREF
LM393A
3.0k
VO

**Driving CMOS**


+5.0 VDC
LM393A
100k
1/4 MM54CXX

**Driving TTL**


+5 VDC
LM393A
10k
1/4 DM54XX

TL/H/5709–2

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.**
**(Note 10)**

| | |
|---|---|
| Supply Voltage, $V^+$ | 36 $V_{DC}$ or ±18 $V_{DC}$ |
| Differential Input Voltage (Note 8) | 36 $V_{DC}$ |
| Input Voltage | −0.3 $V_{DC}$ to +36 $V_{DC}$ |
| Power Dissipation (Note 1) | |
| Molded DIP | 780 mW |
| Metal Can | 660 mW |
| Small Outline Package | 510 mW |
| Output Short-Circuit to Ground (Note 2) | Continuous |
| Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3) | 50 mA |

| | |
|---|---|
| Operating Temperature Range | |
| LM393/LM393A | 0°C to +70°C |
| LM293/LM293A | −25°C to +85°C |
| LM193/LM193A | −55°C to +125°C |
| LM2903 | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | +260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated)

| Parameter | Conditions | LM193A | | | LM293A, LM393A | | | LM193 | | | LM293, LM393 | | | LM2903 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 9) | | ±1.0 | ±2.0 | | ±1.0 | ±2.0 | | ±1.0 | ±5.0 | | ±1.0 | ±5.0 | | ±2.0 | ±7.0 | $mV_{DC}$ |
| Input Bias Current | $I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, $V_{CM} = 0V$ (Note 5) | | 25 | 100 | | 25 | 250 | | 25 | 100 | | 25 | 250 | | 25 | 250 | $nA_{DC}$ |
| Input Offset Current | $I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$ | | ±3.0 | ±25 | | ±5.0 | ±50 | | ±3.0 | ±25 | | ±5.0 | ±50 | | ±5.0 | ±50 | $nA_{DC}$ |
| Input Common Mode Voltage Range | $V^+ = 30\ V_{DC}$ (Note 6) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | $V_{DC}$ |
| Supply Current | $R_L = \infty$ on All Comparators,<br>$R_L = \infty$ on All Amps, $V^+ = 36\ V_{DC}$ | | 0.4<br>1 | 1<br>2.5 | | 0.4<br>1 | 1<br>2.5 | | 0.4<br>1 | 1<br>2.5 | | 0.4<br>1 | 1<br>2.5 | | 0.4<br>1 | 1.0<br>2.5 | $mA_{DC}$<br>$mA_{DC}$ |
| Voltage Gain | $R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ $V_O = 1\ V_{DC}$ to 11 $V_{DC}$ | 50 | 200 | | 50 | 200 | | 50 | 200 | | 50 | 200 | | 25 | 100 | | V/mV |
| Large Signal Response Time | $V_{IN}$ = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$ | | 300 | | | 300 | | | 300 | | | 300 | | | 300 | | ns |
| Response Time | $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$ (Note 7) | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.5 | | µs |
| Output Sink Current | $V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O \geq 1.5\ V_{DC}$ | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | $mA_{DC}$ |
| Saturation Voltage | $V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA | | 250 | 400 | | 250 | 400 | | 250 | 400 | | 250 | 400 | | 250 | 400 | $mV_{DC}$ |
| Output Leakage Current | $V_{IN}(-) = 0$, $V_{IN}(+) = 1\ V_{DC}$, $V_O = 5\ V_{DC}$ | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | $nA_{DC}$ |

## Electrical Characteristics ($V^+ = 5\ V_{DC}$) (Note 4)

| Parameter | Conditions | LM193A | | | LM293A, LM393A | | | LM193 | | | LM293, LM393 | | | LM2903 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 9) | | | ±4.0 | | | ±4.0 | | | ±9 | | | ±9 | | ±9 | ±15 | $mV_{DC}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | | ±100 | | | ±150 | | | ±100 | | | ±150 | | ±50 | ±200 | $nA_{DC}$ |
| Input Bias Current | $I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5) | | | 300 | | | 400 | | | 300 | | | 400 | | 200 | 500 | $nA_{DC}$ |
| Input Common Mode Voltage Range | $V^+ = 30\ V_{DC}$ (Note 6) | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | $V_{DC}$ |
| Saturation Voltage | $V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA, | | | 700 | | | 700 | | | 700 | | | 700 | | 400 | 700 | $mV_{DC}$ |
| Output Leakage Current | $V_{IN(-)} = 0$, $V_{IN(+)} = 1\ V_{DC}$, $V_O = 30\ V_{DC}$ | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | $\mu A_{DC}$ |
| Differential Input Voltage | Keep All $V_{IN}$'s $\geq 0\ V_{DC}$ (or $V^-$, if Used), (Note 8) | | | 36 | | | 36 | | | 36 | | | 36 | | | 36 | $V_{DC}$ |

**Note 1:** For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 127°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of $V^+$.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

**Note 4:** These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

**Note 5:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

**Note 6:** The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $30\ V_{DC}$ without damage, independent of the magnitude of $V^+$.

**Note 7:** The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

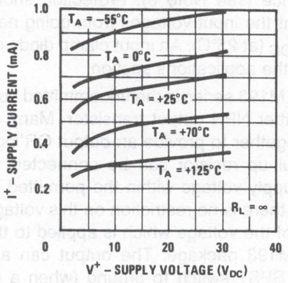
**Note 8:** Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used).

**Note 9:** At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with $V^+$ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C.

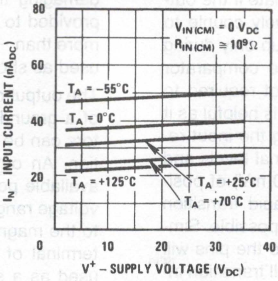
**Note 10:** Refer to RETS193AX for LM193AH/military specifications and to RETS193X for LM193H/military specifications.

## Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

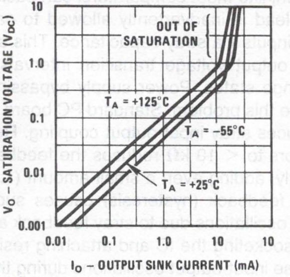
### Supply Current



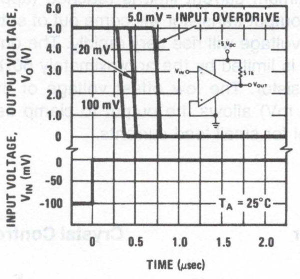
### Input Current



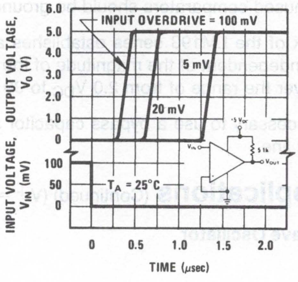
### Output Saturation Voltage



### Response Time for Various Input Overdrives—Negative Transition



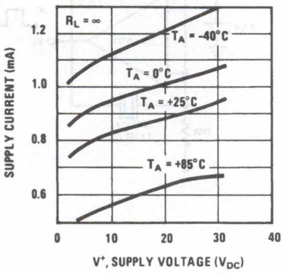
### Response Time for Various Input Overdrives—Positive Transition



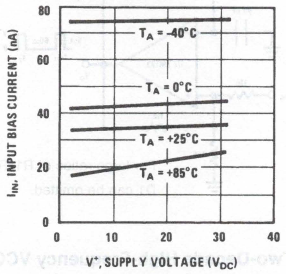
TL/H/5709–3

## Typical Performance Characteristics LM2903

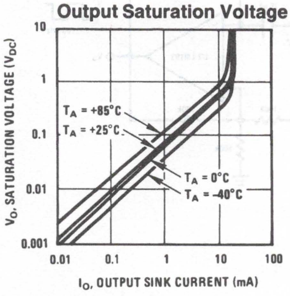
### Supply Current



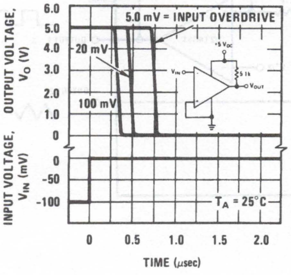
### Input Current



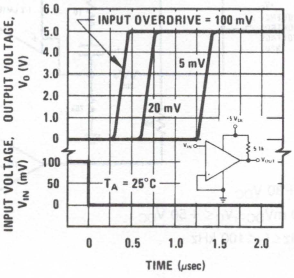
### Output Saturation Voltage



### Response Time for Various Input Overdrives—Negative Transition



### Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

## Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 $V_{DC}$ to 30 $V_{DC}$.

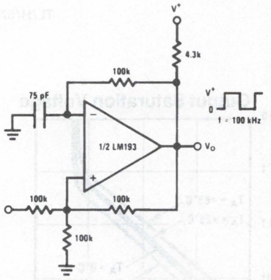
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than $V^+$ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than −0.3 $V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

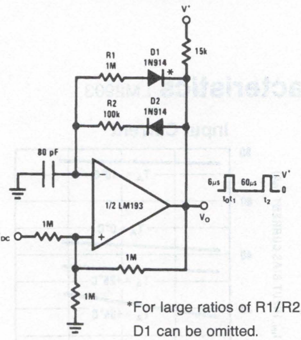
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the $V^+$ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of $V^+$) and the $\beta$ of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω $r_{SAT}$ of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

## Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

### Squarewave Oscillator

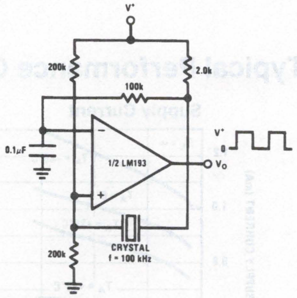


### Pulse Generator

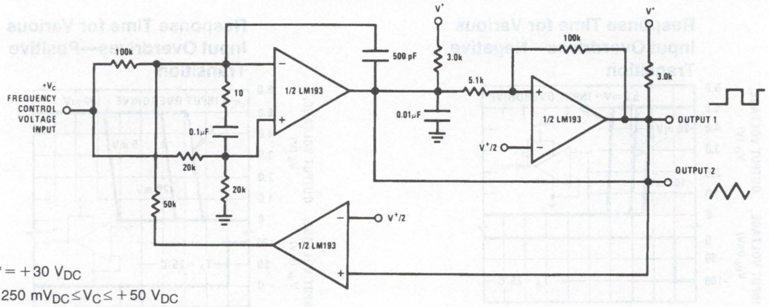


*For large ratios of R1/R2, D1 can be omitted.

### Crystal Controlled Oscillator



### Two-Decade High-Frequency VCO



$V^* = +30\ V_{DC}$

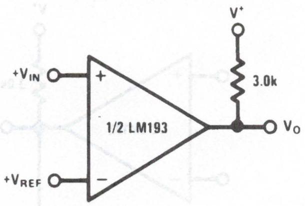
$+250\ mV_{DC} \leq V_C \leq +50\ V_{DC}$

$700\ Hz \leq f_o \leq 100\ kHz$

TL/H/5709–5

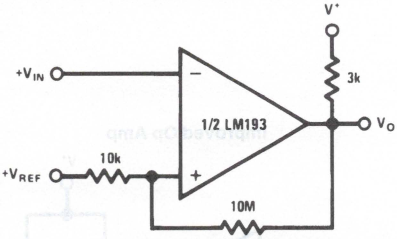
## Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

### Basic Comparator


V⁺
+V_IN
+
−
+V_REF
3.0k
1/2 LM193
V_O

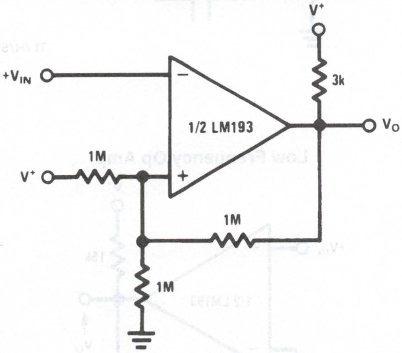
TL/H/5709-6

### Non-Inverting Comparator with Hysteresis


V⁺
+V_IN
−
+
+V_REF
10k
3k
1/2 LM193
V_O
10M

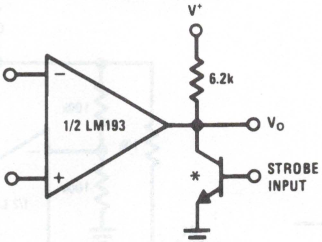
TL/H/5709-9

### Inverting Comparator with Hysteresis


V⁺
+V_IN
−
+
3k
1/2 LM193
V_O
1M
V⁺
1M
1M

TL/H/5709-10

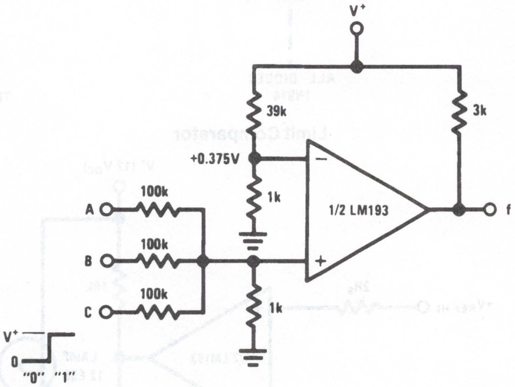
### Output Strobing


V⁺
−
+
6.2k
1/2 LM193
V_O
*
STROBE INPUT

* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

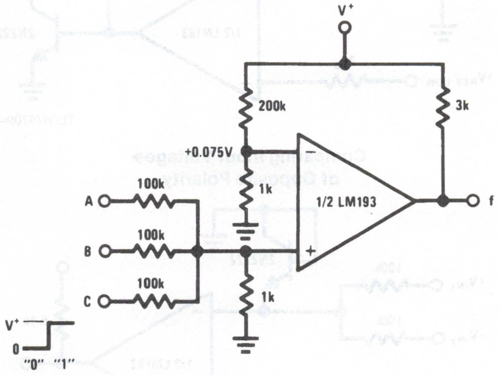
TL/H/5709-11

### AND Gate


V⁺
39k
3k
+0.375V
1k
−
+
1/2 LM193
f
A
B
C
100k
100k
100k
1k
V⁺
0
"0"
"1"

TL/H/5709-12

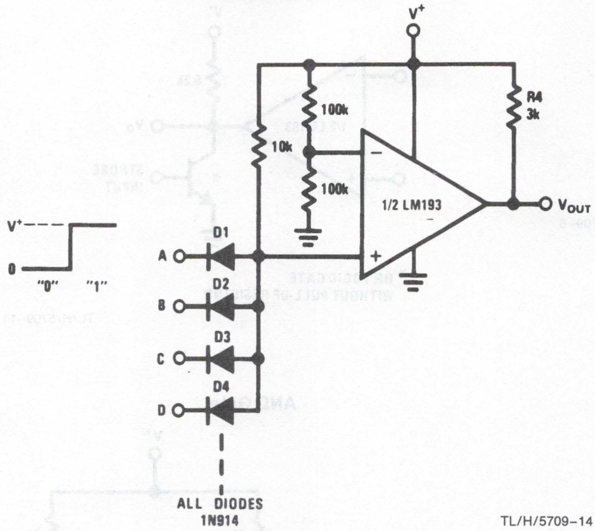
### OR Gate


V⁺
200k
3k
+0.075V
1k
−
+
1/2 LM193
f
A
B
C
100k
100k
100k
1k
V⁺
0
"0"
"1"

TL/H/5709-13

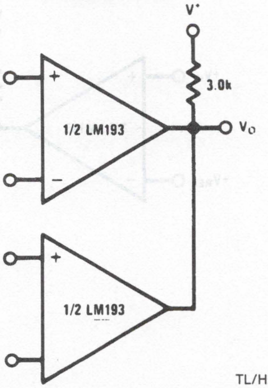
## Typical Applications (Continued) ($V^+ = V_{DC}$)

### Large Fan-in AND Gate


V+
100k
R4
3k
10k
100k
1/2 LM193
VOUT
V+
0
"0"
"1"
D1
A
D2
B
D3
C
D4
D
ALL DIODES
1N914

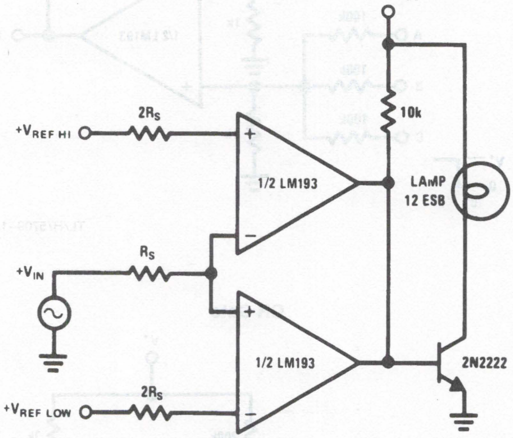
TL/H/5709-14

### ORing the Outputs


V+
3.0k
1/2 LM193
VO
1/2 LM193

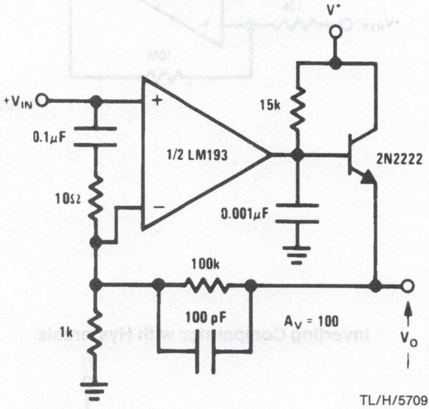
TL/H/5709-17

### Limit Comparator


V+ (12 VDC)
10k
+VREF HI
2RS
1/2 LM193
LAMP
12 ESB
RS
+VIN
1/2 LM193
2N2222
2RS
+VREF LOW

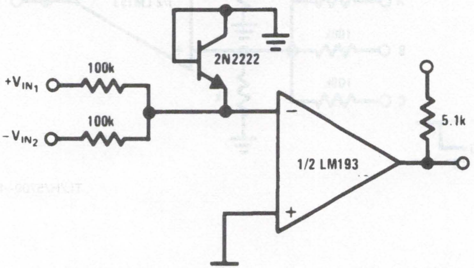
TL/H/5709-15

### Improved Op Amp


V+
+VIN
15k
0.1μF
1/2 LM193
2N2222
10Ω
0.001μF
100k
100 pF
AV = 100
1k
VO

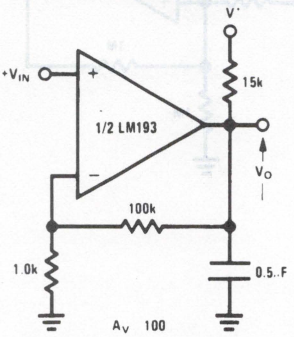
TL/H/5709-18

### Comparing Input Voltages of Opposite Polarity


2N2222
+VIN1
100k
100k
-VIN2
5.1k
1/2 LM193

TL/H/5709-16

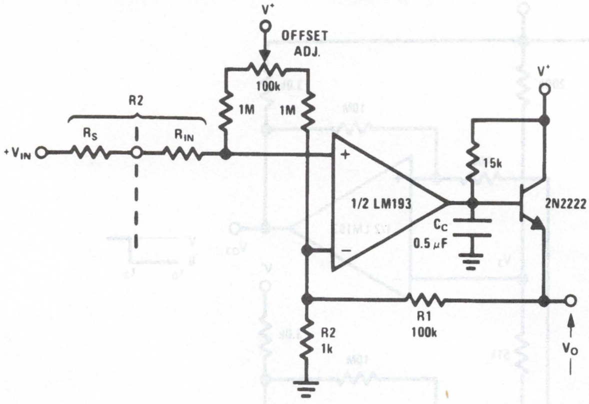
### Low Frequency Op Amp


V+
+VIN
15k
1/2 LM193
VO
100k
1.0k
0.5μF
AV 100

TL/H/5709-19

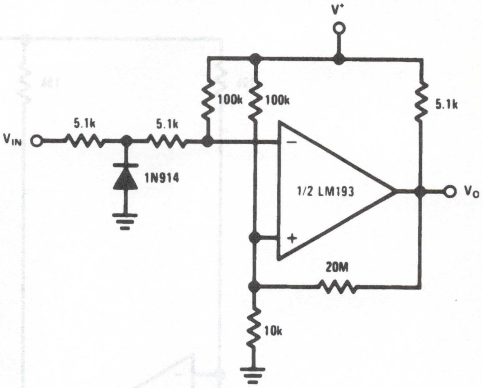
## Typical Applications (Continued) ($V^+ = V_{DC}$)

### Low Frequency Op Amp with Offset Adjust


V+
OFFSET ADJ.
100k
1M
1M
R2
RS
RIN
+VIN
+
−
1/2 LM193
V+
15k
2N2222
CC
0.5 μF
R2
1k
R1
100k
VO

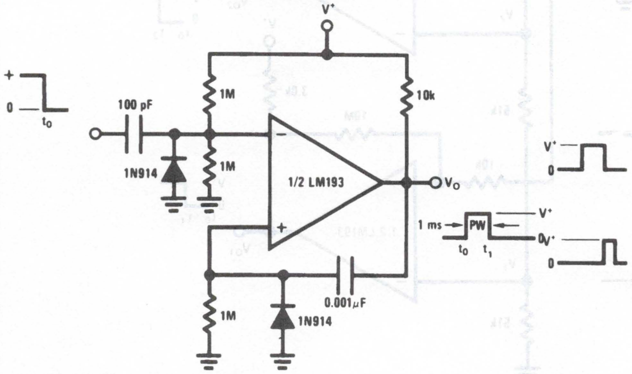
TL/H/5709-20

### Zero Crossing Detector (Single Power Supply)


V+
100k
100k
5.1k
VIN
5.1k
5.1k
1N914
−
+
1/2 LM193
VO
20M
10k

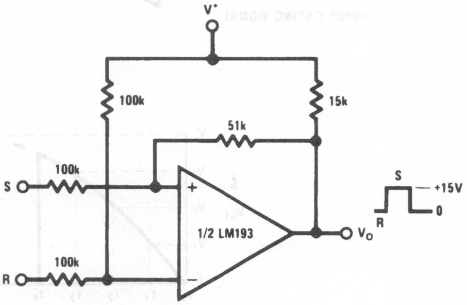
TL/H/5709-21

### One-Shot Multivibrator


+
0
t0
100 pF
1N914
V+
1M
1M
10k
−
+
1/2 LM193
VO
1 ms
PW
t0
t1
V+
0
V+
0
V+
0
1M
1N914
0.001 μF

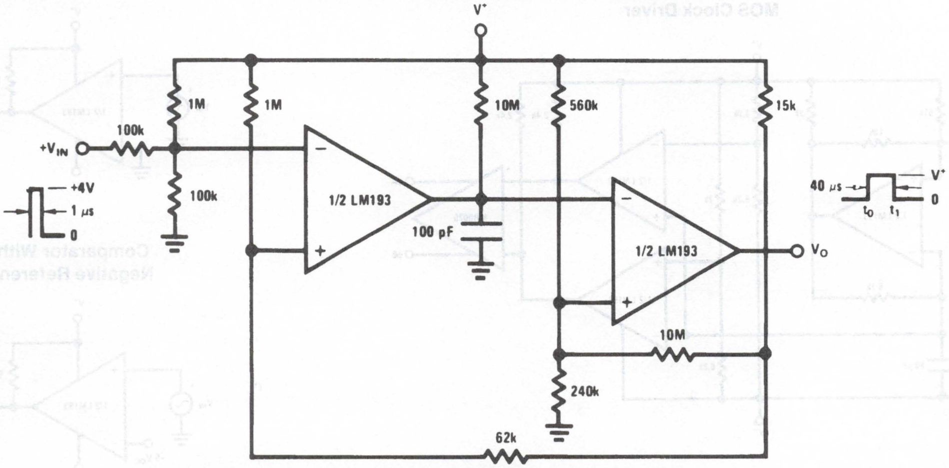
TL/H/5709-22

### Bi-Stable Multivibrator


V+
100k
15k
51k
S
100k
+
−
1/2 LM193
VO
R
100k
S
+15V
0
R

TL/H/5709-24

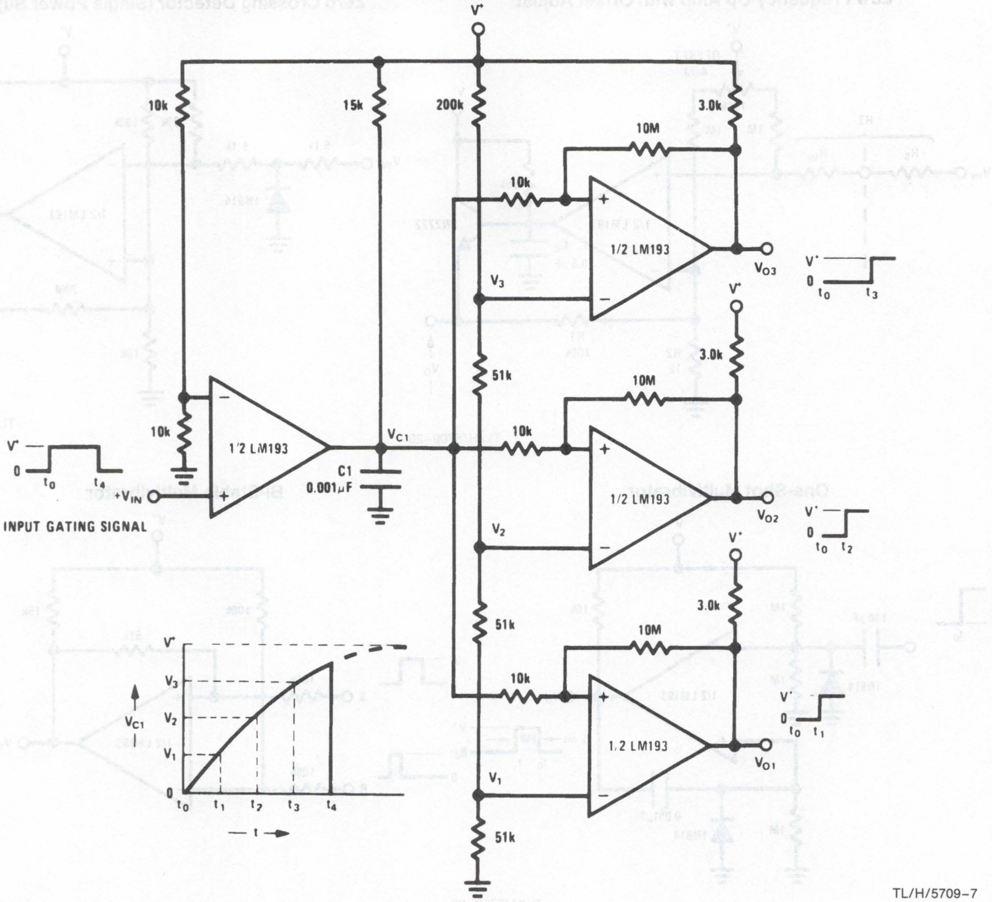
### One-Shot Multivibrator with Input Lock Out


V+
1M
1M
10M
560k
15k
+VIN
100k
100k
+4V
1 μs
0
−
+
1/2 LM193
100 pF
−
+
1/2 LM193
VO
40 μs
V+
0
t0
t1
10M
240k
62k

TL/H/5709-23

## Typical Applications (Continued) ($V^+ = V_{DC}$)

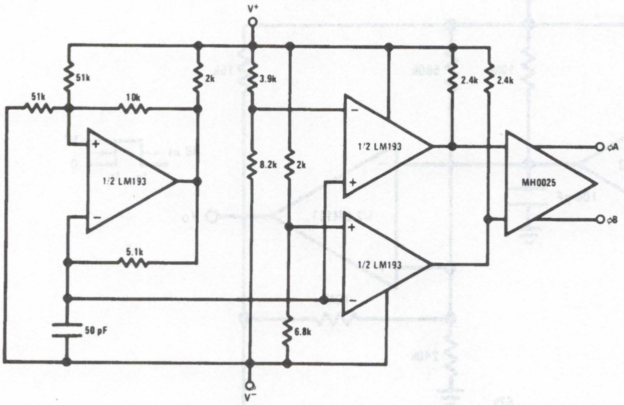
### Time Delay Generator


V+
10k
15k
200k
3.0k
10M
10k
1/2 LM193
V03
V+
0
t0
t3
V3
51k
3.0k
10M
10k
1/2 LM193
V02
V+
0
t0
t2
V2
51k
3.0k
10M
10k
1/2 LM193
V01
V+
0
t0
t1
V1
51k
10k
10k
1/2 LM193
VC1
C1
0.001μF
+VIN
V+
0
t0
t4
INPUT GATING SIGNAL
V+
V3
V2
V1
VC1
0
t0
t1
t2
t3
t4
t

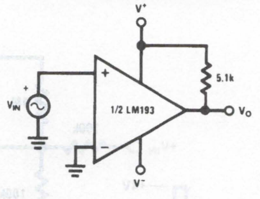
TL/H/5709–7

## Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

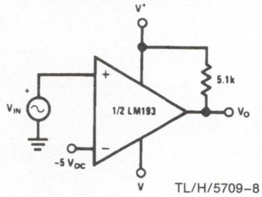
### MOS Clock Driver


V+
51k
51k
10k
2k
3.9k
2.4k
2.4k
1/2 LM193
8.2k
2k
1/2 LM193
MH0025
φA
φB
1/2 LM193
5.1k
50 pF
6.8k
V−

### Zero Crossing Detector


V+
5.1k
VIN
+
1/2 LM193
VO
V−

### Comparator With a Negative Reference


V+
5.1k
VIN
+
1/2 LM193
VO
−5 VDC
V

TL/H/5709–8

**National Semiconductor Corporation**

# LP265/LP365 Micropower Programmable Quad Comparator

## General Description

The LP365 consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the $V_{CC}$ and $I_{SET}$ pins.

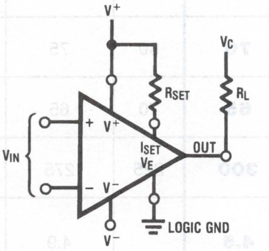
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

## Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 $V_{DC}$ to 36 $V_{DC}$ or ±2.0 $V_{DC}$ to ±18 $V_{DC}$)
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator) @ $I_{SET} = 0.5\,\mu A$ $V_{CC} = 5_{VDC}$
- Uncommitted output stage—selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

## Typical Connection



TL/H/5023–1

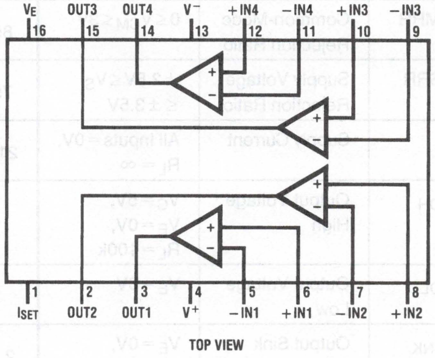
## Programming Equation

$$I_{SET} = \frac{(V^{+}) - (V^{-}) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

## Connection Diagram

**Dual-In-Line Package**



TL/H/5023–2

**Order Number LP365M, LP265N, LP365AN or LP365N**
**See NS Package Numbers M16A or N16A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 36 $V_{DC}$ or ± 18 $V_{DC}$ |
| Differential Input Voltage | ± 36 $V_{DC}$ |
| Input Voltage (Note 1) | $-0.3V$ to $+36$ $V_{DC}$ |
| Output Short Circuit to $V_E$ (Note 2) | Continuous |
| $V_{OUT}$ with Respect to $V_E$ | $V_E-7V \leq V_{OUT} \leq V_E+36V$ |

| | M Package | N Package |
|---|---|---|
| Power Dissipation (Note 3) | 500 mW | 500 mW |
| $T_j$ Max | 115°C | 115°C |
| $\theta_{jA}$ | 115°C/W | 90°C/W |
| Lead Temp. | | |
| (Soldering—10 sec.) | | 260°C |
| (Vapor Phase—60 sec.) | 215°C | |
| (Infrared—15 sec.) | 220°C | |
| Operating Temp. Range LP365: | $0°C \leq T_A \leq +70°C$ | |
| LP265: | $-40°C \leq T_A \leq +85°C$ | |
| Storage Temp. Range | $-40°C \leq T_A \leq +150°C$ | |

## Electrical Characteristics (Note 4) Low power $V_S=5V$, $I_{SET}=10\ \mu A$

| Symbol | Parameter | Conditions | LP365A<br>Typ | LP365A<br>Tested Limit (Note 5) | LP365A<br>Design Limit (Note 6) | LP265/LP365<br>Typ | LP265/LP365<br>Tested Limit (Note 5) | LP265/LP365<br>Design Limit (Note 6) | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}=0V$,<br>$R_S=100$ | 1 | 3 | **6** | 3 | 6 | **9** | mV (Max) |
| $I_{OS}$ | Input Offset Current | $V_{CM}=0V$ | 2 | 20 | **50** | 4 | 25 | **75** | nA (Max) |
| | | LP265 | | | | 4 | 25 | **150** | |
| $I_B$ | Input Bias Current | $V_{CM}=0V$ | 10 | 50 | **125** | 15 | 75 | **200** | nA (Max) |
| | | LP265 | | | | 15 | 75 | **300** | |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L=100k$ | 500 | 50 | **50** | 300 | 25 | **25** | V/mV (Min) |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | 0 | **0** | | 0 | **0** | V (Max) |
| | | | | 3 | **3** | | 3 | **3** | V (Min) |
| CMRR | Common-Mode Rejection Ratio | $0 \leq V_{CM} \leq 3V$ | 85 | 75 | **70** | 80 | 75 | **70** | dB (Min) |
| PSRR | Supply Voltage Rejection Ratio | $\pm 2.5V \leq V_S \leq \pm 3.5V$ | 75 | 65 | **65** | 70 | 65 | **65** | dB (Min) |
| $I_S$ | Supply Current | All Inputs=0V,<br>$R_L=\infty$ | 215 | 250 | **300** | 225 | 275 | **300** | μA (Max) |
| $V_{OH}$ | Output Voltage High | $V_C=5V$,<br>$V_E=0V$,<br>$R_L=100k$ | | 4.9 | **4.5** | | 4.9 | **4.5** | V (Min) |
| $V_{OL}$ | Output Voltage Low | $V_E=0V$ | | 0.4 | **0.4** | | 0.4 | **0.4** | V (Max) |
| $I_{SINK}$ | Output Sink Current | $V_E=0V$,<br>$V_O=0.4V$ | 2.4 | 1.2 | **0.6** | 2.0 | 0.8 | **0.4** | mA (Min) |
| $I_{LEAK}$ | Output Leakage Current | $V_C=5V$,<br>$V_E=0V$ | 2 | 50 | **5000** | 2 | 100 | **5000** | nA (Max) |
| $t_R$ | Response Time | $V_{CC}=5V$,<br>$V_E=0V$,<br>$R_L=5k$,<br>$C_L=10$ pF<br>(Note 7) | 4 | | | 4 | | | μs |

## Electrical Characteristics (Continued) (Note 8) High power $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$

| Symbol | Parameter | Conditions | LP365A | | | LP265/LP365 | | | Units (Limit) |
|---|---|---|---|---|---|---|---|---|---|
| | | | Typ | Tested Limit (Note 5) | Design Limit (Note 6) | Typ | Tested Limit (Note 5) | Design Limit (Note 6) | |
| $V_{OS}$ | Input Offset Voltage | $V_{CM} = 0V$, $R_S = 100$ | 1 | 3 | **6** | 3 | 6 | **9** | mV (Max) |
| $I_{OS}$ | Input Offset Current | $V_{CM} = 0V$<br>LP265 | 5 | 50 | **100** | 10 | 90 | **200** | nA (Max) |
| | | | | | | 10 | 90 | **500** | |
| $I_B$ | Input Bias Current | $V_{CM} = 0V$<br>LP265 | 60 | 200 | **500** | 80 | 300 | **500** | nA (Max) |
| | | | | | | 80 | 300 | **800** | |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L = 15k$ | 500 | 100 | **100** | 500 | 100 | **100** | V/mV (Min) |
| $V_{CM}$ | Input Common-Mode Voltage Range | | | −15 | **−15** | | −15 | **−15** | V (Max) |
| | | | | 13 | **13** | | 13 | **13** | V (Min) |
| CMRR | Common-Mode Rejection Ratio | $-15V \leq V_{CM} \leq 13V$ | 85 | 75 | **70** | 80 | 75 | **70** | dB (Min) |
| PSRR | Supply Voltage Rejection Ratio | $\pm 10V \leq V_S \leq \pm 15V$ | 80 | 70 | **70** | 75 | 70 | **70** | dB (Min) |
| $I_S$ | Supply Current | All Inputs = 0V, $R_L = \infty$, LP265 | 2.6 | 3 | **3.3** | 2.8 | 3.5 | **3.7** | mA (Max) |
| | | | | | | 2.8 | 3.5 | **4.3** | |
| $V_{OH}$ | Output Voltage High | $V_C = 5V$, $V_E = 0V$, $R_L = 100k$ | | 4.9 | **4.5** | | 4.9 | **4.5** | V (Min) |
| $V_{OL}$ | Output Voltage Low | $V_E = 0V$ | | 0.4 | **0.4** | | 0.4 | **0.4** | V (Max) |
| $I_{SINK}$ | Output Sink Current | $V_E = 0V$, $V_O = 0.4V$ | 10 | 8 | **5.5** | 7.5 | 6 | **4** | mA (Min) |
| $I_{LEAK}$ | Output Leakage Current | $V_C = 15V$, $V_E = -15V$ | 5 | 50 | **5000** | 5 | 50 | **5000** | nA (Max) |
| $t_R$ | Response Time | $V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10\ pF$ (Note 7) | 1.0 | | | 1.0 | | | µs |

**Note 1:** The input voltage is not allowed to go 0.3V above $V^+$ or −0.3V below $V^-$ as this will turn on a parasitic transistor causing large currents to flow through the device.

**Note 2:** Short circuits from the output to $V^+$ may cause excessive heating and eventual destruction. The current in the output leads and the $V_E$ lead should not be allowed to exceed 30 mA. The output should not be shorted to $V^-$ if $V_E \leq (V^-) + 7V$.

**Note 3:** For operating at elevated temperatures, these devices must be derated based on a thermal resistance of $\theta_{jA}$ and $T_j$ max. $T_j = T_A + \theta_{jA} P_D$.

**Note 4: Boldface numbers apply at temperature extremes.** All other numbers apply at $T_A = T_j = 25°C$. $V^+ = 5V$, $V^- = 0V$, $I_{SET} = 10\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

**Note 5:** Guaranteed and 100% production tested.

**Note 6:** Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate out-going quality levels.

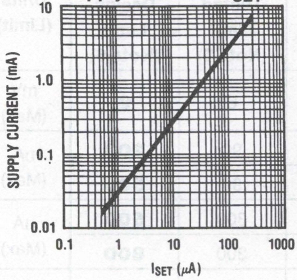
**Note 7:** The response time specified is for a 100 mV input step with 5 mV overdrive.

**Note 8: Boldface numbers apply at temperature extremes.** All other numbers apply at $T_A = T_j = 25°C$. $V^+ = +15V$, $V^- = -15V$, $I_{SET} = 100\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

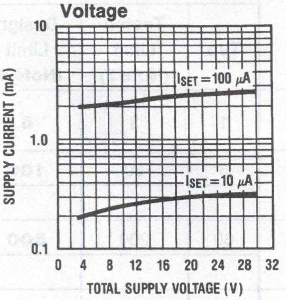
**Note 9:** See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

# Typical Performance Characteristics

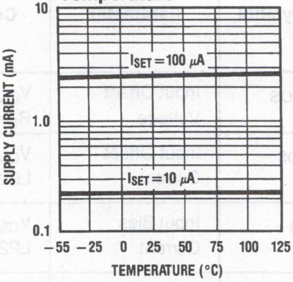
Supply Current vs $I_{SET}$



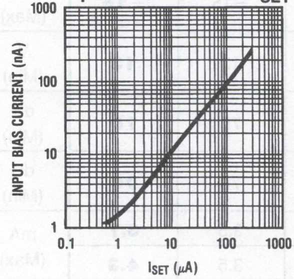
Supply Current vs Supply Voltage



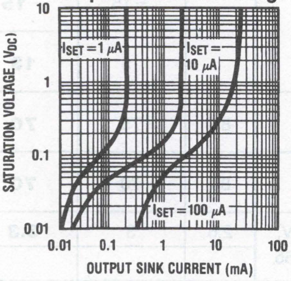
Supply Current vs Temperature



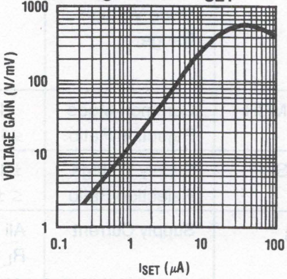
Input Bias Current vs $I_{SET}$



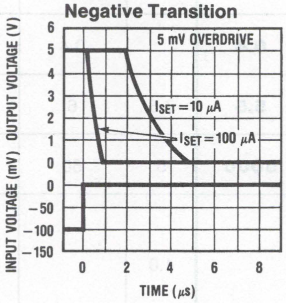
Output Saturation Voltage



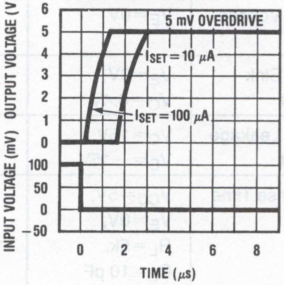
Voltage Gain vs $I_{SET}$



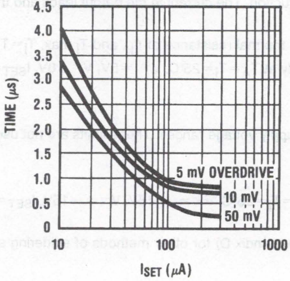
Response Time Negative Transition



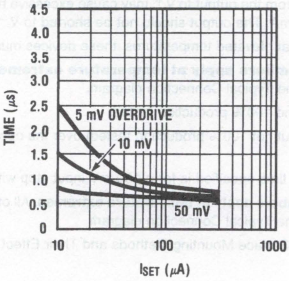
Response Time Positive Transition



Response Time Negative Transition



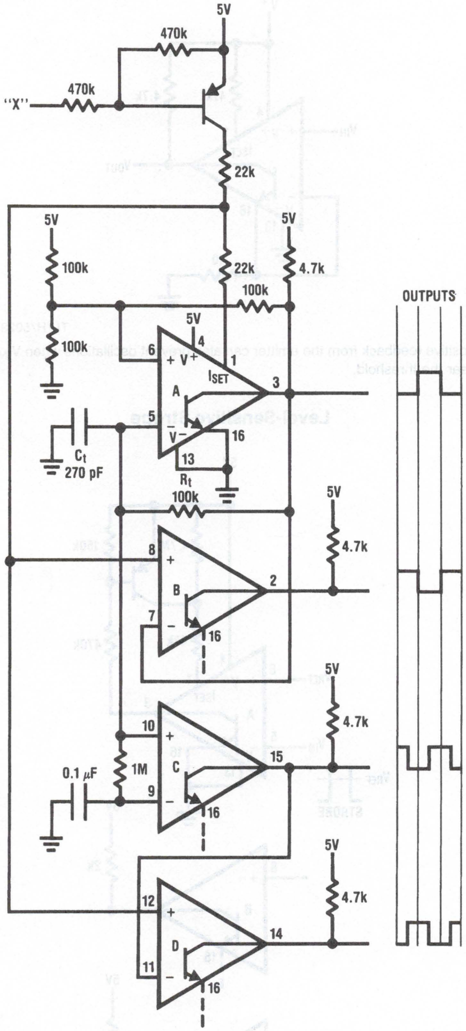
Response Time Positive Transition



TL/H/5023-3

# Typical Applications

### Gated 4-Phase Oscillator


5V
470k
"X"
470k
22k
5V
100k
5V
22k
4.7k
100k
OUTPUTS
5V
4
100k
6
+ V+
1
$I_{SET}$
3
A
5
V−
16
13
$C_t$
270 pF
$R_t$
100k
5V
8
+
4.7k
B
2
7
−
16
5V
10
+
4.7k
0.1 µF
1M
C
15
9
−
16
5V
12
+
4.7k
D
14
11
−
16

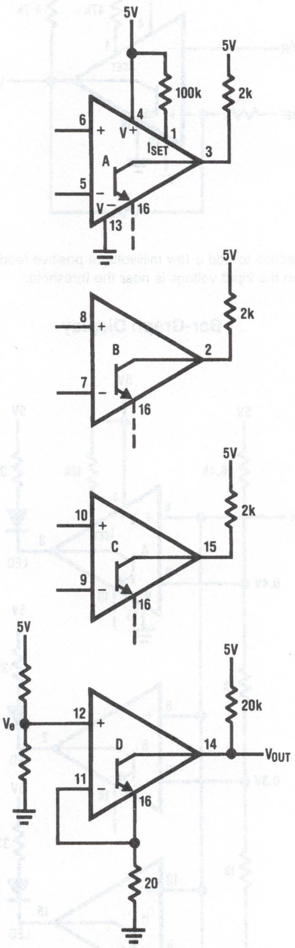
TL/H/5023-4

f = 20 kHz

$$f = \frac{1}{1.6 \bullet R_t \bullet C_t}$$

All four phases run when X is low. When X is high, oscillation stops and power drain is zero.

### Voltage Comparator

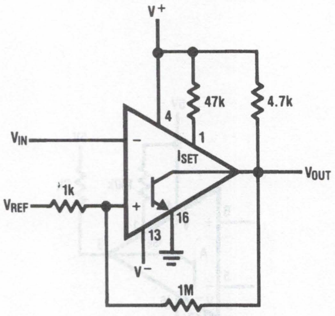

5V
5V
100k
2k
6
+
4
V+
1
$I_{SET}$
3
A
5
−
V−
16
13
5V
2k
8
+
B
2
7
−
16
5V
2k
10
+
C
15
9
−
16
5V
5V
20k
$V_e$
12
+
D
14
$V_{OUT}$
11
−
16
20

TL/H/5023-5

If you choose $V_e = 25$ mV, 75 mV, or 125 mV, then $V_{OUT}$ will fall if ⅓, ⅔ or all of the other three outputs are low.

## Typical Applications (Continued)

### Ordinary Hysteresis

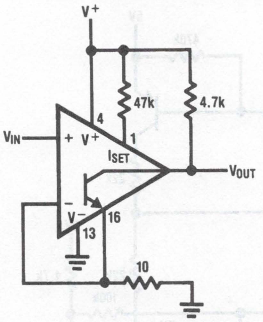


V+
47k
4.7k
4
1
VIN
ISET
VOUT
VREF
1k
16
13
V−
1M

TL/H/5023-6

It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

### Hysteresis from Emitter

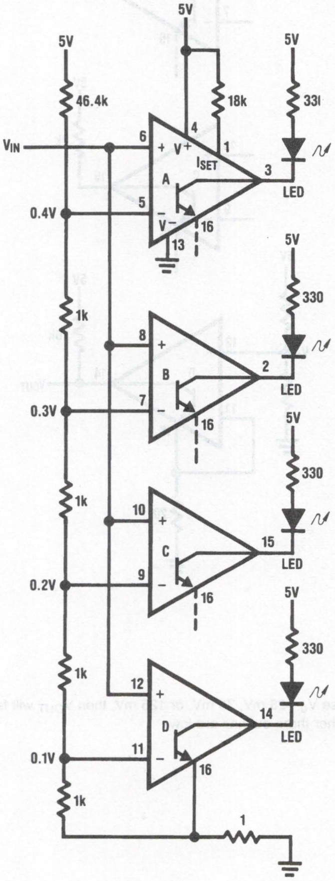


V+
47k
4.7k
4
1
VIN
+ V+
ISET
VOUT
V−
16
13
10

TL/H/5023-7

Positive feedback from the emitter can also prevent oscillations when $V_{IN}$ is near the threshold.

### Bar-Graph Display

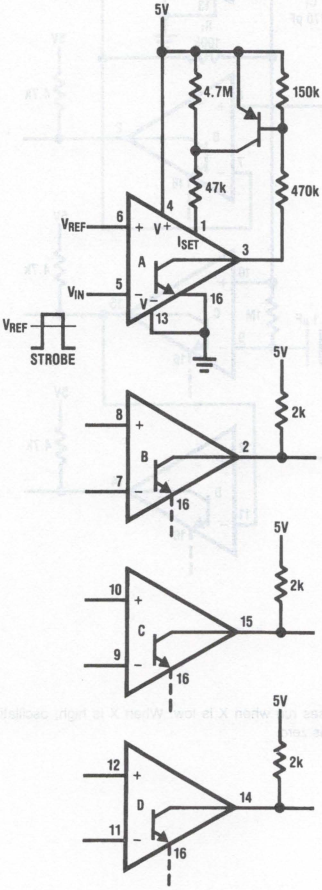


5V
5V
5V
46.4k
18k
330
VIN
6
4
1
+ V+
ISET
A
3
LED
0.4V
5
V−
16
13
1k
330
8
B
2
LED
0.3V
7
16
1k
330
10
C
15
LED
0.2V
9
16
1k
330
12
D
14
LED
0.1V
11
16
1k
1

TL/H/5023-8

The positive feedback from pin 16 provides hysteresis.

### Level-Sensitive Strobe



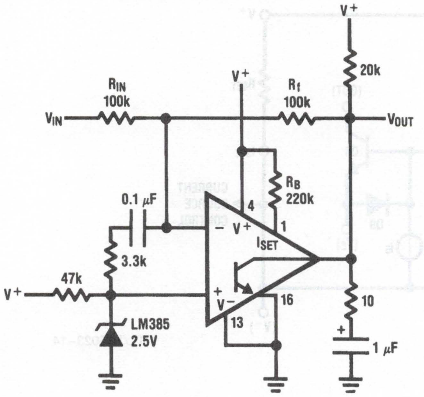
5V
4.7M
150k
47k
470k
4
VREF
6
+ V+
1
ISET
A
3
VIN
5
V−
16
13
VREF
STROBE
5V
2k
8
B
2
7
16
5V
2k
10
C
15
9
16
5V
2k
12
D
14
11
16

TL/H/5023-9

Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

## Typical Applications (Continued)

### Slow Op Amp (Inverter)

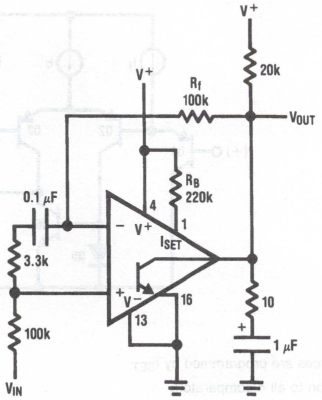

V+
20k
RIN
100k
V+
Rf
100k
VIN
VOUT
RB
220k
0.1 μF
4
− V+
1
ISET
3.3k
47k
V+
+
V−
16
10
LM385
2.5V
13
+
1 μF

TL/H/5023-10

$R_B = V^+/20\ \mu A$

Unlike most comparators, the LP365 can be used as an op amp, if suitable R-C damping networks are used.

### Slow Op Amp (Unity-Gain Follower)

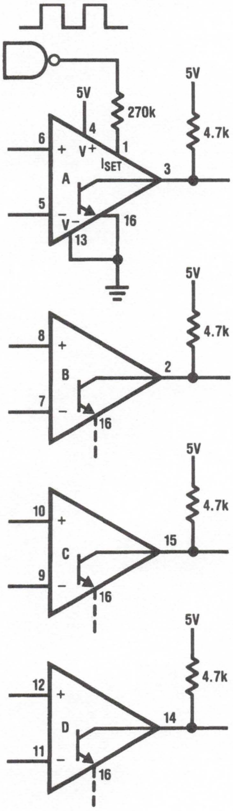

V+
20k
V+
Rf
100k
VOUT
RB
220k
0.1 μF
4
− V+
1
ISET
3.3k
+
V−
16
10
13
100k
+
1 μF
VIN

TL/H/5023-11

$R_B = V^+/20\ \mu A$

The LP365 can also be used as a high-input-impedance follower-amplifier with the damping components shown.

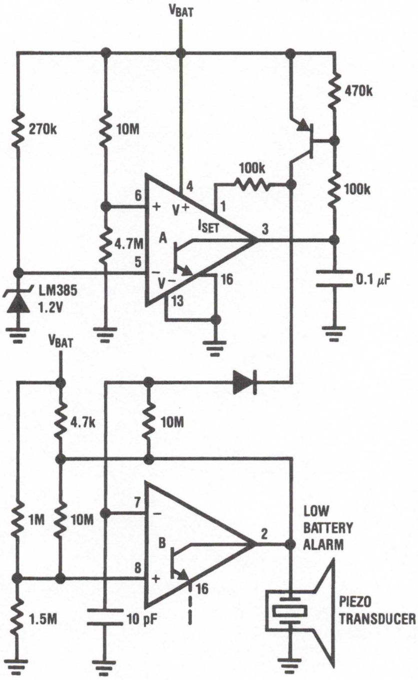
### Chopping Outputs


5V
5V
270k
4.7k
6
+ V+
4
1
ISET
A
3
5
−
V−
16
13
5V
8
+
4.7k
B
2
7
−
16
5V
10
+
4.7k
C
15
9
−
16
5V
4.7k
12
+
D
14
11
−
16

TL/H/5023-12

Chopping the outputs by modulating the $I_{SET}$ current allows data to be transmitted via opto-couplers, transformers, etc.

### Low Battery Detector


VBAT
470k
270k
10M
100k
100k
6
4
+ V+
1
ISET
A
3
4.7M
5
0.1 μF
LM385
1.2V
V−
16
13
VBAT
4.7k
10M
7
−
LOW
BATTERY
ALARM
1M
10M
B
2
8
+
16
PIEZO
TRANSDUCER
1.5M
10 pF

TL/H/5023-13

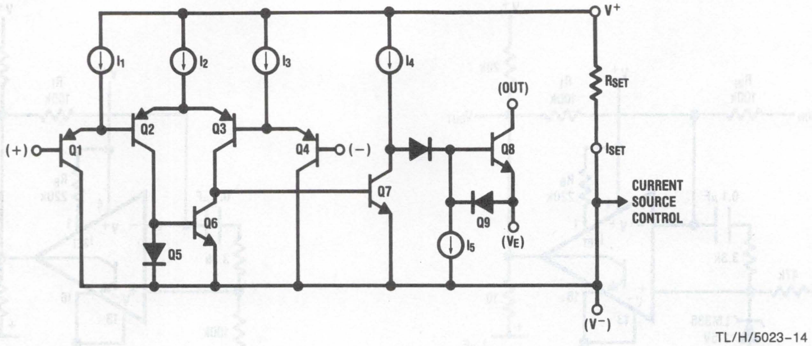
$I_S$ @ 6V = 45 μA

$I_S$ @ 3.8V = 1 μA

f = 3 kHz

Comparator A detects when the supply voltage drops to 4V and enables comparator B to drive a piezoelectric alarm.

## Simplified Schematic


V+
I1
I2
I3
I4
RSET
(OUT)
(+)
Q1
Q2
Q3
Q4
(−)
Q8
ISET
Q7
CURRENT SOURCE CONTROL
Q6
Q9
Q5
I5
(VE)
(V−)

TL/H/5023-14

Current sources are programmed by $I_{SET}$

$V_E$ is common to all 4 comparators

**National Semiconductor Corporation**

# LP311 Voltage Comparator

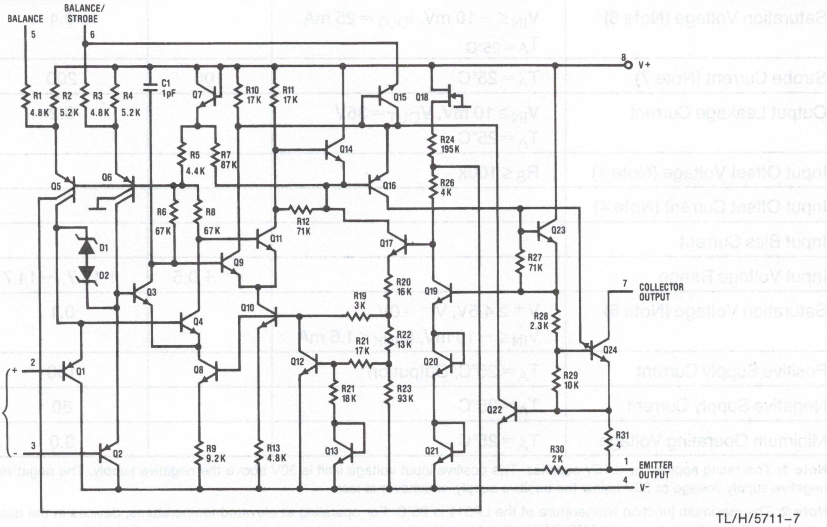
## General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. (See the LM311 section of the Linear Databook.)

## Features

- Low power drain, 900 μW on 5V supply
- Operates from ±15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: −14.6V to 13.6V with ±15V supply

## Schematic Diagram

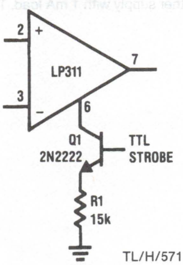


BALANCE
5
BALANCE/STROBE
6
8
V+
R1 4.8K
R2 5.2K
R3 4.8K
R4 5.2K
C1 1pF
Q7
R10 17K
R11 17K
Q15
Q18
R24 195K
Q14
R5 4.4K
R7 87K
Q5
Q6
Q16
R26 4K
R6 67K
R8 67K
R12 71K
Q11
Q23
D1
D2
Q9
Q17
R27 71K
Q3
R20 16K
Q19
7
COLLECTOR OUTPUT
R19 3K
Q10
Q4
R28 2.3K
R22 13K
R21 17K
Q24
2
Q1
Q8
Q12
Q20
R29 10K
INPUTS
R21 18K
R23 93K
Q22
R31 4
3
Q2
R9 9.2K
R13 4.8K
Q13
Q21
R30 2K
1
EMITTER OUTPUT
4
V−

TL/H/5711–7

## Auxiliary Circuits

### Strobing

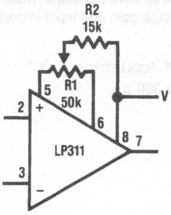


2
+
3
−
LP311
7
6
Q1
2N2222
TTL
STROBE
R1
15k

TL/H/5711–1

**Note:** Do not ground strobe pin.

### Offset Balancing

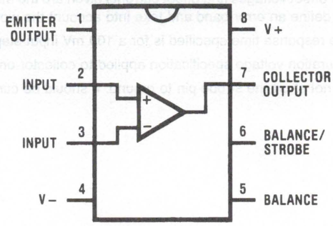


R2
15k
R1
50k
5
6
2
+
V+
8
7
LP311
3
−

TL/H/5711–2

## Connection Diagram

### Dual-In-Line Package



EMITTER OUTPUT
1
INPUT
2
INPUT
3
V−
4
8
V+
7
COLLECTOR OUTPUT
6
BALANCE/STROBE
5
BALANCE
+
−

TL/H/5711–4

**Top View**

**Order Number LP311N**
**See NS Package Number N08E**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Total Supply Voltage ($V_{8-4}$) | 36V |
| Collector Output to Negative Supply Voltage ($V_{7-4}$) | 40V |
| Collector Output to Emitter Output | 40V |
| Emitter Output to Negative Supply Voltage ($V_{1-4}$) | ±30V |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 1) | ±15V |

| | |
|---|---|
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

## Electrical Characteristics (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage (Note 4) | $T_A = 25°C$, $R_S \leq 100k$ | | 2.0 | 7.5 | mV |
| Input Offset Current (Note 4) | $T_A = 25°C$ | | 2.0 | 25 | nA |
| Input Bias Current | $T_A = 25°C$ | | 15 | 100 | nA |
| Voltage Gain | $T_A = 25°C$, $R_L = 5k$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25°C$ | | 1.2 | | μs |
| Saturation Voltage (Note 6) | $V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA<br>$T_A = 25°C$ | | 0.4 | 1.5 | V |
| Strobe Current (Note 7) | $T_A = 25°C$ | 100 | 200 | 300 | μA |
| Output Leakage Current | $V_{IN} \geq 10$ mV, $V_{OUT} = 35V$<br>$T_A = 25°C$ | | 0.2 | 100 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 100k$ | | | 10 | mV |
| Input Offset Current (Note 4) | | | | 35 | nA |
| Input Bias Current | | | | 150 | nA |
| Input Voltage Range | | $V^- + 0.5$ | $+13.7, -14.7$ | $V^+ - 1.5$ | V |
| Saturation Voltage (Note 6) | $V^+ \geq 4.5V$, $V^- = 0V$<br>$V_{IN} \leq -10$ mV, $I_{SINK} \leq 1.6$ mA | | 0.1 | 0.4 | V |
| Positive Supply Current | $T_A = 25°C$, Output on | | 150 | 300 | μA |
| Negative Supply Current | $T_A = 25°C$ | | 80 | 180 | μA |
| Minimum Operating Voltage | $T_A = 25°C$ | | 3.0 | 3.5 | V |

**Note 1:** This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

**Note 2:** The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 160°C/W, junction to ambient.

**Note 3:** These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

**Note 4:** The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

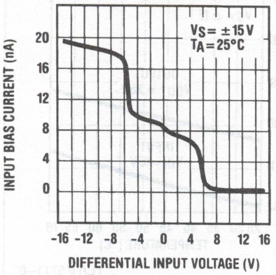
**Note 5:** The response time specified is for a 100 mV input step with 5 mV overdrive.

**Note 6:** Saturation voltage specification applied to collector-emitter voltage (V7-1) for $V_{COLLECTOR} \leq (V^+ - 3V)$.

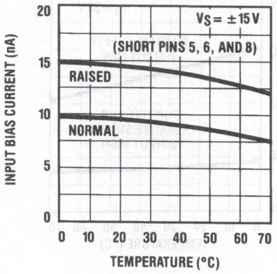
**Note 7:** Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA.

## Typical Performance Characteristics

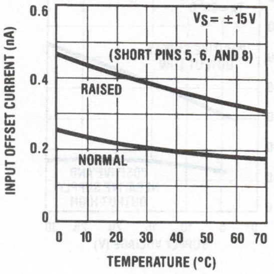
### Input Characteristics



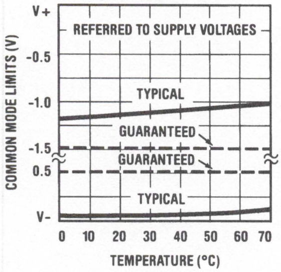
### Input Bias Current



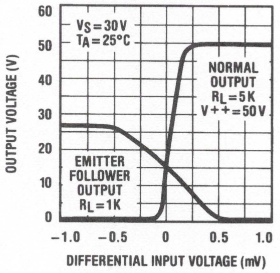
### Input Offset Current



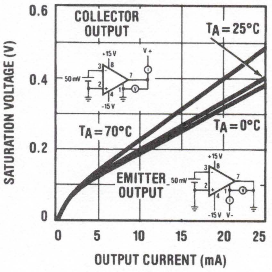
### Common Mode Limits



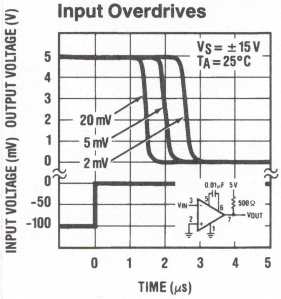
### Transfer Function



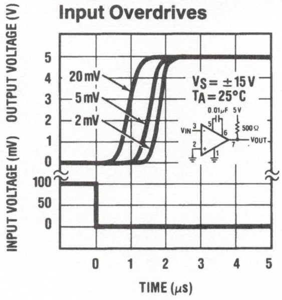
### Output Saturation Voltage



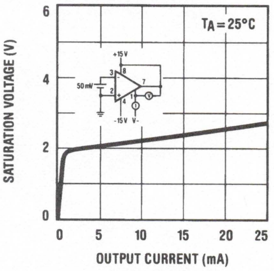
### Response Time for Various Input Overdrives



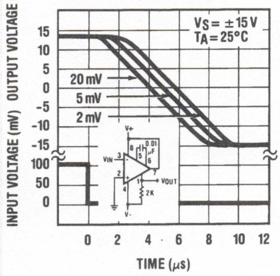
### Response Time for Various Input Overdrives



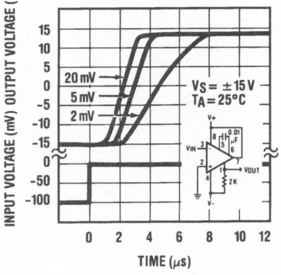
### Output Saturation Voltage (Emitter Output)



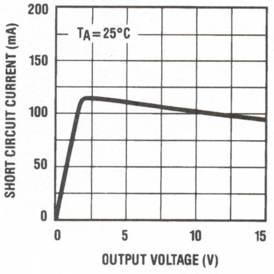
### Response Time for Various Input Overdrives



### Response Time for Various Input Overdrives



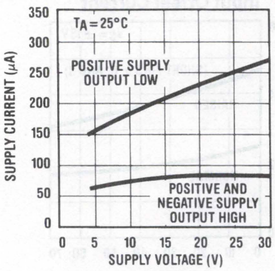
### Output Limiting Characteristics



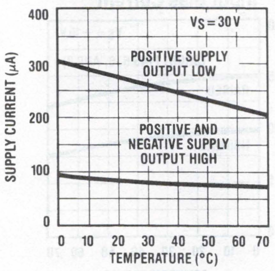
TL/H/5711-5

## Typical Performance Characteristics (Continued)

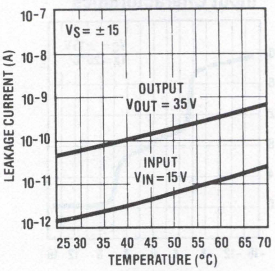
### Supply Current



### Supply Current



### Leakage Currents



TL/H/5711-6

**National Semiconductor Corporation**

**PRELIMINARY**

# LP339 Ultra-Low Power Quad Comparator

## General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 µA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

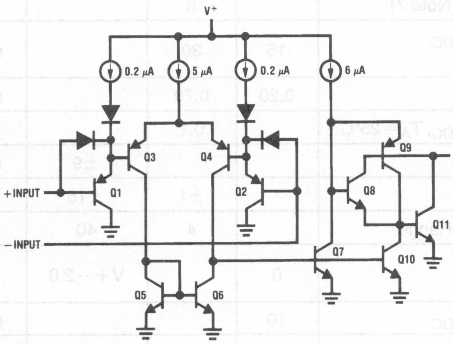
## Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

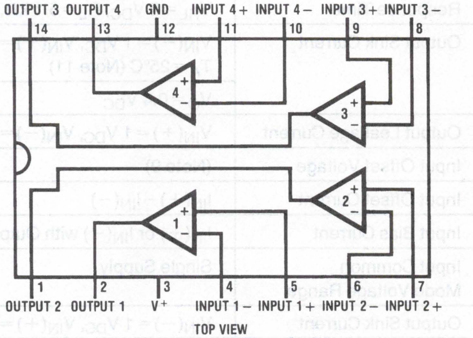
## Features

- Ultra-low power supply current drain (60 µA)—independent of the supply voltage (75 µW/comparator at $+5\ V_{DC}$)
- Low input biasing current 3 nA
- Low input offset current ±0.5 nA
- Low input offset voltage ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at $V_O = 2\ V_{DC}$)
- Supply Input protected against reverse voltages

## Schematic and Connection Diagrams


V+
0.2 µA
5 µA
0.2 µA
6 µA
Q3
Q4
Q9
OUTPUT
+INPUT
Q1
Q2
Q8
Q11
−INPUT
Q7
Q10
Q5
Q6

TL/H/5226–1


OUTPUT 3
OUTPUT 4
GND
INPUT 4+
INPUT 4−
INPUT 3+
INPUT 3−
14
13
12
11
10
9
8
4
3
1
2
1
2
3
4
5
6
7
OUTPUT 2
OUTPUT 1
V+
INPUT 1−
INPUT 1+
INPUT 2−
INPUT 2+
TOP VIEW

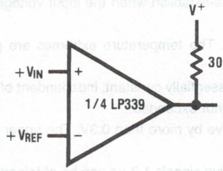
TL/H/5226–2

**Order Number LP339M for S.O. Package**
**See NS Package Number M14A**

**Order Number LP339N for Dual-In-Line Package**
**See NS Package Number N14A**

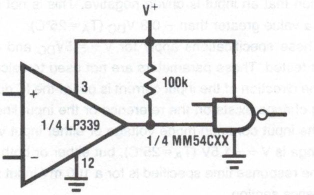
## Typical Applications ($V+ = 5.0\ V_{DC}$)

**Basic Comparator**


V+
+V_IN
+V_REF
1/4 LP339
30k

TL/H/5226–3

**Driving CMOS**


V+
3
100k
1/4 LP339
1/4 MM54CXX
12

TL/H/5226–4

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 36 $V_{DC}$ or ±18 $V_{DC}$ |
| Differential Input Voltage | ±36 $V_{DC}$ |
| Input Voltage | −0.3 $V_{DC}$ to 36 $V_{DC}$ |
| Power Dissipation (Note 1) Molded DIP | 570 mW |
| Output Short Circuit to GND (Note 2) | Continuous |
| Input Current $V_{IN} < -0.3\ V_{DC}$ (Note 3) | 50 mA |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65° to +150°C |
| Soldering Information: | |
| Dual-In-Line Package (10 sec.) | +260°C |
| S.O. Package: | |
| Vapor Phase (60 sec.) | +215°C |
| Infrared (15 sec.) | +220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

## Electrical Characteristics ($V+ = 5\ V_{DC}$, Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ (Note 9) | | ±2 | ±5 | $mV_{DC}$ |
| Input Bias Current | $I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, $T_A = 25°C$ (Note 5) | | 2.5 | 25 | $nA_{DC}$ |
| Input Offset Current | $I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$ | | ±0.5 | ±5 | $nA_{DC}$ |
| Input Common Mode Voltage Range | $T_A = 25°C$ (Note 6) | 0 | | V+ −1.5 | $V_{DC}$ |
| Supply Current | $R_L$ = Infinite on all Comparators, $T_A = 25°C$ | | 60 | 100 | $\mu A_{DC}$ |
| Voltage Gain | $V_O = 1\ V_{DC}$ to $11\ V_{DC}$, $R_L = 15\ k\Omega$, $V+ = 15\ V_{DC}$, $T_A = 25°C$ | | 500 | | V/mV |
| Large Signal Response Time | $V_{IN}$ = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$ | | 1.3 | | $\mu$Sec |
| Response Time | $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$ (Note 7) | | 8 | | $\mu$Sec |
| Output Sink Current | $V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O = 2\ V_{DC}$, $T_A = 25°C$ (Note 11) | 15 | 30 | | $mA_{DC}$ |
| | $V_O = 0.4\ V_{DC}$ | 0.20 | 0.70 | | $mA_{DC}$ |
| Output Leakage Current | $V_{IN}(+) = 1\ V_{DC}$, $V_{IN}(-) = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$ | | 0.1 | | $nA_{DC}$ |
| Input Offset Voltage | (Note 9) | | | ±9 | $mV_{DC}$ |
| Input Offset Current | $I_{IN}(+) - I_{IN}(-)$ | | ±1 | ±15 | $nA_{DC}$ |
| Input Bias Current | $I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range | | 4 | 40 | $nA_{DC}$ |
| Input Common Mode Voltage Range | Single Supply | 0 | | V+ −2.0 | $V_{DC}$ |
| Output Sink Current | $V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O = 2\ V_{DC}$ | 10 | | | $mA_{DC}$ |
| Output Leakage Current | $V_{IN}(+) = 1\ V_{DC}$, $V_{IN}(-) = 0$, $V_O = 30\ V_{DC}$ | | | 1.0 | $\mu A_{DC}$ |
| Differential Input Voltage | All $V_{IN}$'s $\geq 0\ V_{DC}$ (or V− on split supplies) (Note 8) | | | 36 | $V_{DC}$ |

**Note 1:** For elevated temperature operation, $T_j$ max is 125°C for the LP339. $\theta_{ja}$ (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

**Note 2:** Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 $V_{DC}$ ($T_A = 25°C$).

**Note 4:** These specifications apply for $V+ = 5V_{DC}$ and $0°C \leq T_A \leq 70°$ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

**Note 5:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

**Note 6:** The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V ($T_A = 25°C$), but either or both inputs can go to 30 $V_{DC}$ without damage.

**Note 7:** The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 $\mu$s can be obtained. See Typical Performance Characteristics section.

## Electrical Characteristics (V+ = 5 $V_{DC}$, Note 4) (Continued)

**Note 8:** Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 $V_{DC}$ (or 0.3 $V_{DC}$ below the magnitude of the negative power supply, if used) at $T_A = 25°C$.

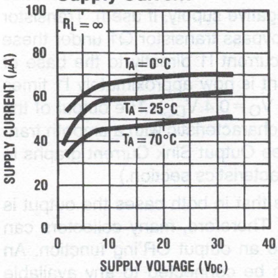
**Note 9:** At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5 $V_{DC}$; and over the full input common-mode range (0 $V_{DC}$ to V+ −1.5 $V_{DC}$).

**Note 10:** For input signals that exceed V+, only the overdriven comparator is affected. With a 5V supply, $V_{IN}$ should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

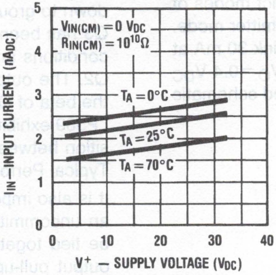
**Note 11:** The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 $V_{DC}$ and sink lower currents below this point. (See typical characteristics section and applications section).

## Typical Performance Characteristics

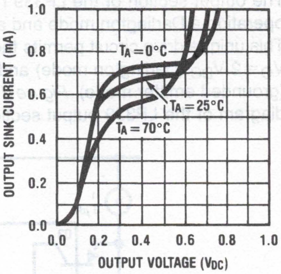
**Supply Current**



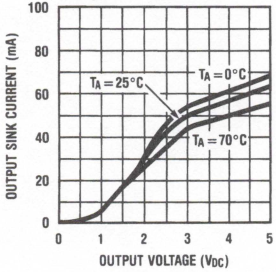
**Input Current**



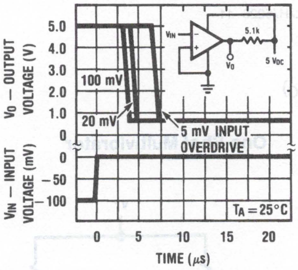
**Output Sink Current**



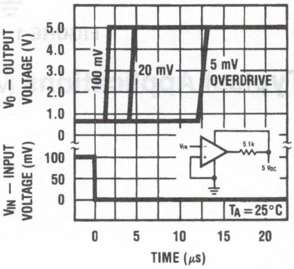
**Output Sink Current**



**Response Times for Various Input Overdrives — Negative Transition**



**Response Times for Various Input Overdrives — Positive Transition**



TL/H/5226–10

## Application Hints

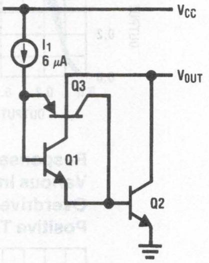
All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 $V_{DC}$ to 30 $V_{DC}$.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 $V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2\ V_{DC}$ (Darlington mode) and 700 $\mu A$ at $V_O = 0.4\ V_{DC}$ (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.



TL/H/5226-11

**FIGURE 1**

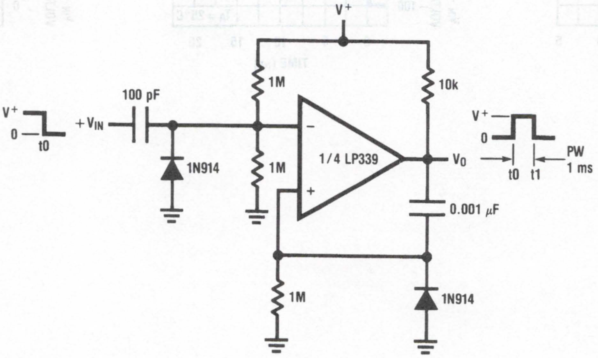
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1\ V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω $R_{SAT}$ of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 $\mu A$.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 $V_{DC}$, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 $\mu A$ at $V_O = 0.4\ V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

## Typical Applications ($V^+ = 15\ V_{DC}$)

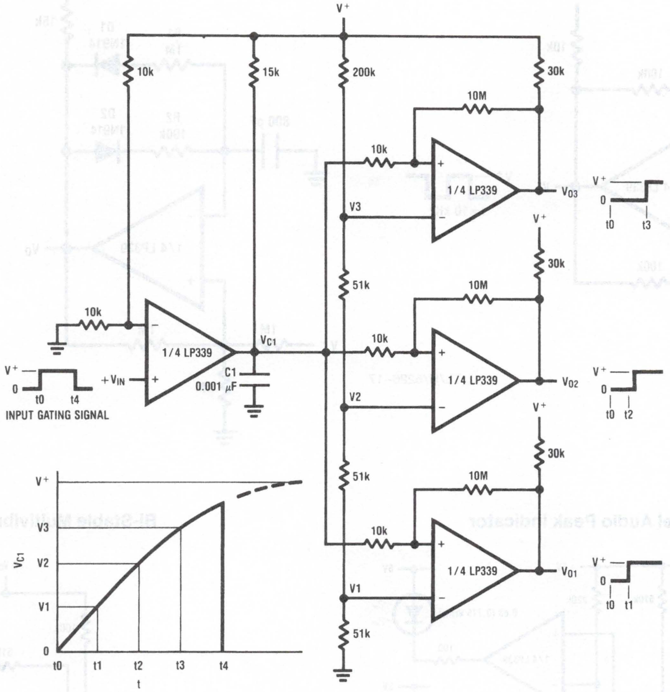
**One-Shot Multivibrator**



TL/H/5226-13

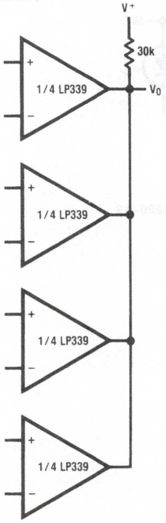
## Typical Applications (V+ = 15 $V_{DC}$)

### Time Delay Generator


V+
10k
15k
200k
30k
10M
10k
1/4 LP339
$V_{O3}$
V3
51k
30k
10M
10k
1/4 LP339
$V_{O2}$
V2
51k
30k
10M
10k
1/4 LP339
$V_{O1}$
V1
51k
10k
1/4 LP339
$V_{C1}$
C1
0.001 μF
+$V_{IN}$
INPUT GATING SIGNAL
0
t0
t1
t2
t3
t4
$V_{C1}$
t

TL/H/5226–15

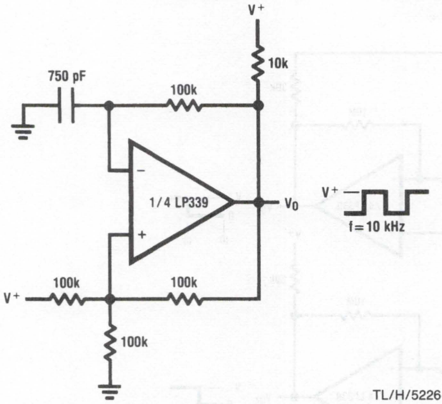
### ORing the Outputs


V+
30k
$V_O$
1/4 LP339
1/4 LP339
1/4 LP339
1/4 LP339
+
−

TL/H/5226–16

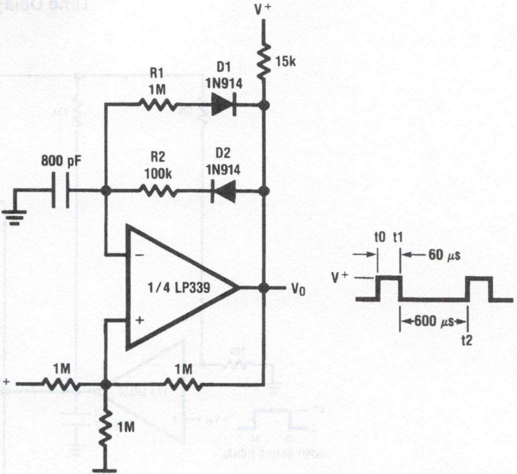
## Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

### Squarewave Oscillator


V+
10k
750 pF
100k
1/4 LP339
V0
V+
f = 10 kHz
V+
100k
100k
100k

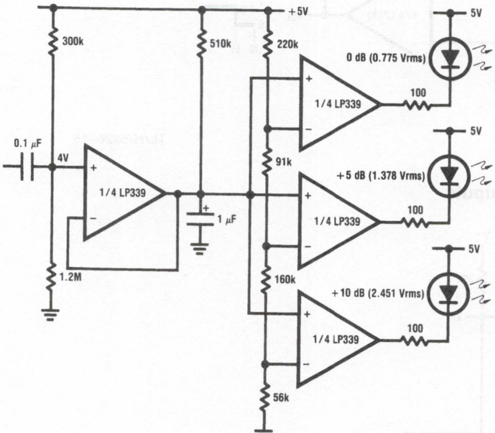
TL/H/5226-17

### Pulse Generator


V+
15k
R1
1M
D1
1N914
800 pF
R2
100k
D2
1N914
1/4 LP339
V0
V+
1M
1M
1M
t0 t1
60 μs
V+
600 μs
t2

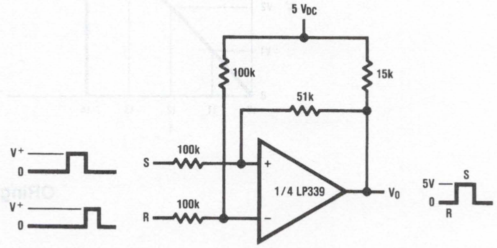
TL/H/5226-18

### Three Level Audio Peak Indicator


+5V
300k
510k
220k
5V
0 dB (0.775 Vrms)
100
1/4 LP339
0.1 μF
4V
1/4 LP339
91k
5V
+5 dB (1.378 Vrms)
100
1/4 LP339
1 μF
1.2M
160k
5V
+10 dB (2.451 Vrms)
100
1/4 LP339
56k

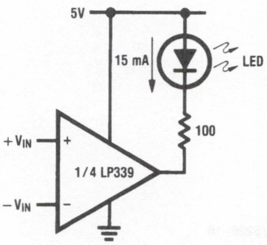
TL/H/5226-19

### Bi-Stable Multivibrator


5 VDC
100k
15k
51k
V+
0
S
100k
1/4 LP339
V0
5V
0
S
R
V+
0
R
100k

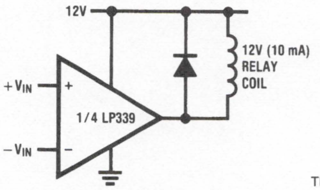
TL/H/5226-21

### LED Driver


5V
15 mA
LED
100
+VIN
1/4 LP339
−VIN

TL/H/5226-22

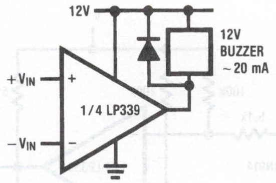
### Relay Driver


12V
12V (10 mA)
RELAY
COIL
+VIN
1/4 LP339
−VIN

TL/H/5226-23

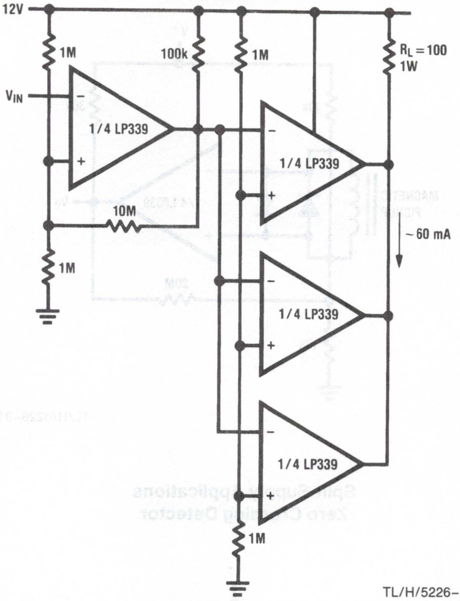
## Typical Applications (Continued) (Single Supply)

### Buzzer Driver


12V
12V
BUZZER
~20 mA
+VIN
−VIN
1/4 LP339
+
−

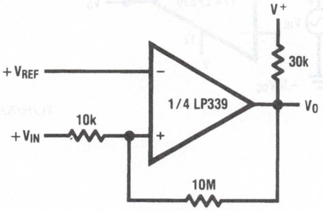
TL/H/5226-24

### Comparator With 60 mA Sink Capability


12V
1M
100k
1M
RL = 100
1W
VIN
1/4 LP339
10M
1M
1/4 LP339
~60 mA
1/4 LP339
1/4 LP339
1M

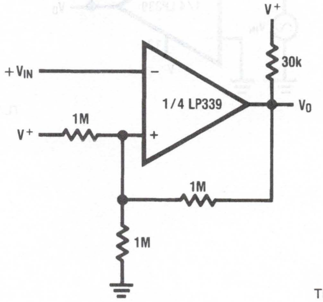
TL/H/5226-25

### Non-Inverting Comparator with Hysteresis


V+
30k
+VREF
1/4 LP339
VO
10k
+VIN
10M

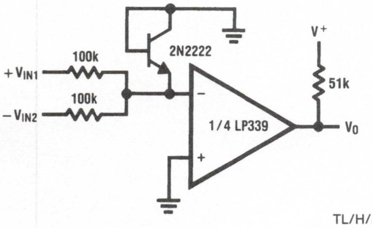
TL/H/5226-26

### Inverting Comparator with Hysteresis


V+
30k
+VIN
1/4 LP339
VO
1M
V+
1M
1M

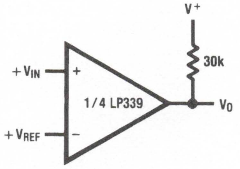
TL/H/5226-27

### Comparing Input Voltages of Opposite Polarity


2N2222
V+
100k
+VIN1
100k
−VIN2
51k
1/4 LP339
VO

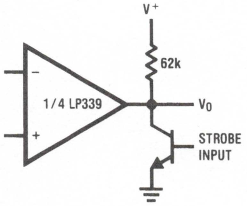
TL/H/5226-28

### Basic Comparator


V+
30k
+VIN
1/4 LP339
VO
+VREF

TL/H/5226-29

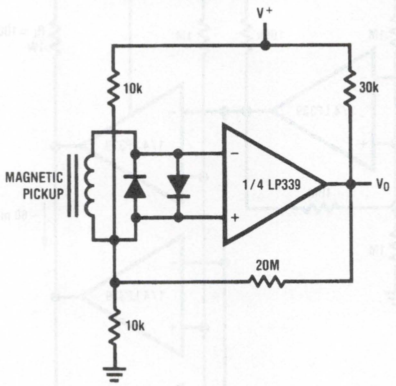
### Output Strobing


V+
62k
1/4 LP339
VO
STROBE
INPUT

TL/H/5226-30

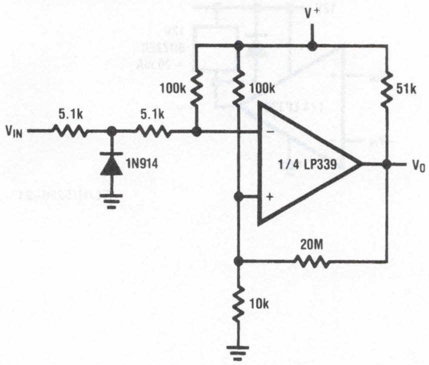
## Typical Applications (Continued) (Single Supply)

### Transducer Amplifier


V+
10k
30k
MAGNETIC PICKUP
1/4 LP339
VO
20M
10k

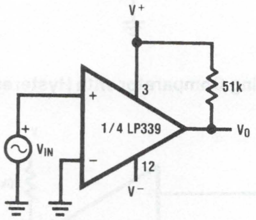
TL/H/5226-31

### Zero Crossing Detector (Single Power Supply)


V+
100k
100k
51k
VIN
5.1k
5.1k
1N914
1/4 LP339
VO
20M
10k

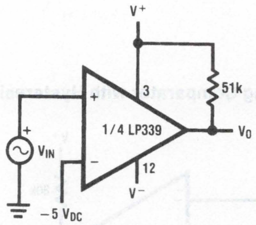
TL/H/5226-32

### Split-Supply Applications Zero Crossing Detector


V+
3
51k
1/4 LP339
VO
VIN
12
V−

TL/H/5226-33

### Comparator With a Negative Reference


V+
3
51k
1/4 LP339
VO
VIN
12
V−
−5 VDC

TL/H/5226-34

# Section 5

# Instrumentation Amplifiers

## Section 5 Contents

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Instrumentation Selection Guide . . . . . 5-4
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LH0038/LH0038C True Instrumentation Amplifier . . . . . 5-14
LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier . . . . . 5-25
LM221/LM321/LM321A Precision Preamplifiers . . . . . 5-37
LM363 Precision Instrumentation Amplifier . . . . . 5-46

**National Semiconductor Corporation**

# Instrumentation Amplifiers Definition of Terms

**Bandwidth:** That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

**Common-Mode Rejection Ratio:** The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

**Harmonic Distortion:** That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

**Input Bias Current:** The average of the two input currents.

**Input Common-Mode Voltage Range:** The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

**Input Impedance:** The ratio of input voltage to input current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Input Offset Current:** The difference in the currents into the two input terminals when the output is at zero.

**Input Offset Voltage:** That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Input Voltage Range:** The range of voltages on the input terminals for which the amplifier operates within specifications.

**Large-Signal Voltage Gain:** The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

**Output Impedance:** The ratio of output voltage to output current under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

**Output Resistance:** The small signal resistance seen at the output with the output voltage near zero.

**Output Voltage Swing:** The peak output voltage swing, referred to zero, that can be obtained without clipping.

**Offset Voltage Temperature Drift:** The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

**Power Supply Rejection:** The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Settling Time:** The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**Slew Rate:** The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

**Supply Current:** The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

**Transient Response:** The closed-loop step-function response of the amplifier under small-signal conditions.

**Unity Gain Bandwidth:** The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

**Voltage Gain:** The ratio of output voltage to input voltage under the stated conditions for source resistance ($R_S$) and load resistance ($R_L$).

National Semiconductor Corporation

# Instrumentation Amplifiers Selection Guide

| Part Number | Gain Error (Max) | Gain Linearity (Typ) | CMRR dB (Min) | $I_B$ nA (Max) |
|---|---|---|---|---|
| | | $T_A = 25°C$ | | |
| LH0036 μ Power | 3% | 0.03% | 46 | 125 |
| LH0038 | 3% | 0.0001% | 86 | 100 |
| LH0084 | 0.3% | 0.005% | 80 | 0.500 |
| LM363 | 2.5% | 0.01% | 90 | 10 |

**Note 1:** Datasheet should be referred to for test conditions and more detailed information.

**National Semiconductor Corporation**

# LH0036/LH0036C Instrumentation Amplifier

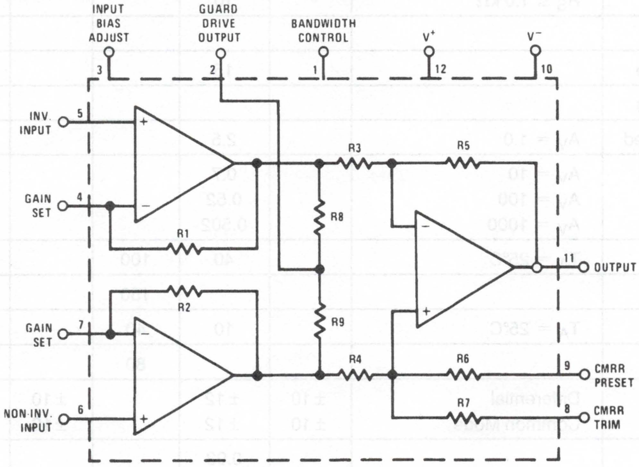
## General Description

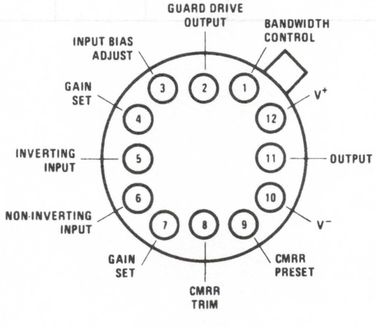
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable from 1 to 1000 with a single external resistor. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

## Features

| | |
|---|---|
| ■ High input impedance | 300 MΩ |
| ■ High CMRR | 100 dB |
| ■ Single resistor gain adjust | 1 to 1000 |
| ■ Low power | 90 μW |
| ■ Wide supply range | ±1V to ±18V |
| ■ Adjustable input bias current | |
| ■ Adjustable output bandwidth | |
| ■ Guard drive output | |

## Equivalent Circuit and Connection Diagrams


INPUT BIAS ADJUST
GUARD DRIVE OUTPUT
BANDWIDTH CONTROL
V+
V−
3
2
1
12
10
INV. INPUT
5
GAIN SET
4
R1
R2
GAIN SET
7
NON-INV. INPUT
6
R3
R5
R8
R9
R4
R6
R7
11
OUTPUT
9
CMRR PRESET
8
CMRR TRIM


GUARD DRIVE OUTPUT
BANDWIDTH CONTROL
INPUT BIAS ADJUST
GAIN SET
V+
INVERTING INPUT
OUTPUT
NON-INVERTING INPUT
V−
GAIN SET
CMRR PRESET
CMRR TRIM
1
2
3
4
5
6
7
8
9
10
11
12

TOP VIEW

TL/H/5545-1

**Order Number LH0036G or LH0036CG**
**See NS Package Number G12B**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±30V |
| Input Voltage Range | $\pm V_S$ |
| Shield Drive Voltage | $\pm V_S$ |
| CMRR Preset Voltage | $\pm V_S$ |
| CMMR Trim Voltage | $\pm V_S$ |
| Power Dissipation (Note 3) | 1.5W |
| Short Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0036 | −55°C to +125°C |
| LH0036C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

ESD rating to be determined.

## Electrical Characteristics (Notes 1 and 2)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH00336 | | | LH0036C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S = 1.0\ k\Omega$, $T_A = 25°C$ | | 0.5 | 1.0 | | 1.0 | 2.0 | mV |
| ($V_{IOS}$) | $R_S = 1.0\ k\Omega$ | | | 2.0 | | | 3.0 | mV |
| Output Offset Voltage | $R_S = 1.0\ k\Omega$, $T_A = 25°C$ | | 2.0 | 5.0 | | 5.0 | 10 | mV |
| ($V_{OOS}$) | $R_S = 1.0\ k\Omega$ | | | 6.0 | | | 12 | mV |
| Input Offset Voltage | $R_S \leq 1.0\ k\Omega$ | | 10 | | | 10 | | µV/°C |
| Tempco ($\Delta V_{IOS}/\Delta T$) | | | | | | | | |
| Output Offset Voltage | | | 15 | | | 15 | | µV/°C |
| Tempco ($\Delta V_{OOS}/\Delta T$) | | | | | | | | |
| Overall Offset Referred | $A_V = 1.0$ | | 2.5 | | | 6.0 | | mV |
| to Input ($V_{OS}$) | $A_V = 10$<br>$A_V = 100$<br>$A_V = 1000$ | | 0.7<br>0.52<br>0.502 | | | 1.5<br>1.05<br>1.005 | | mV<br>mV<br>mV |
| Input Bias Current | $T_A = 25°C$ | | 40 | 100 | | 50 | 125 | nA |
| ($I_B$) | | | | 150 | | | 200 | nA |
| Input Offset Current | $T_A = 25°C$ | | 10 | 40 | | 20 | 50 | nA |
| ($I_{OS}$) | | | | 80 | | | 100 | nA |
| Input Voltage Range | Differential<br>Common Mode | ±10<br>±10 | ±12<br>±12 | | ±10<br>±10 | ±12<br>±12 | | V<br>V |
| Gain Nonlinearity | | | 0.03 | | | 0.03 | | % |
| Deviation From Gain Equation Formula | $A_V = 1$ to 1000 (Note 4) | | ±0.3 | ±1.0 | | ±1.0 | ±3.0 | % |

## Electrical Characteristics (Notes 1 and 2) (Continued)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | LH00336 | | | LH0036C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| PSRR | $\pm5.0V \le V_S \le \pm15V$, $A_V = 1.0$ | | 1.0 | 2.5 | | 1.0 | 5.0 | mV/V |
| | $\pm5.0V \le V_S \le \pm15V$, $A_V = 100$ | | 0.05 | 0.25 | | 0.10 | 0.50 | mV/V |
| CMRR | $A_V = 1.0$ DC to | | 1.0 | 2.5 | | 2.5 | 5.0 | mV/V |
| | $A_V = 10$ 100 Hz | | 0.1 | 0.25 | | 0.25 | 0.50 | mV/V |
| | $A_V = 100$ $\Delta R_S = 1.0k$ | | 50 | 100 | | 50 | 100 | μV/V |
| Output Voltage | $V_S = \pm15V$, $R_L = 10\ k\Omega$ | ±10 | ±13.5 | | ±10 | ±13.5 | | V |
| | $V_S = \pm1.5V$, $R_L = 100\ k\Omega$ | ±0.6 | ±0.8 | | ±0.6 | ±0.8 | | V |
| Output Resistance | | | 0.5 | | | 0.5 | | Ω |
| Supply Current | | | 300 | 400 | | 400 | 600 | μA |
| Small Signal Bandwidth | $A_V = 1.0$, $R_L = 10\ k\Omega$ | | 350 | | | 350 | | kHz |
| | $A_V = 10$, $R_L = 10\ k\Omega$ | | 35 | | | 35 | | kHz |
| | $A_V = 100$, $R_L = 10\ k\Omega$ | | 3.5 | | | 3.5 | | kHz |
| | $A_V = 1000$, $R_L = 10\ k\Omega$ | | 350 | | | 350 | | Hz |
| Full Power Bandwidth | $V_{IN} = \pm10V$, $R_L = 10k$, $A_V = 1$ | | 5.0 | | | 5.0 | | kHz |
| Equivalent Input Noise Voltage | 0.1 Hz $< f <$ 10 kHz, $R_S < 50\Omega$ | | 20 | | | 20 | | μV/p-p |
| Slew Rate | $\Delta V_{IN} = \pm10V$, $R_L = 10\ k\Omega$, $A_V = 1.0$ | | 0.3 | | | 0.3 | | V/μS |
| Settling Time | To ±10 mV, $R_L = 10\ k\Omega$, $\Delta V_{OUT} = 1.0V$ | | | | | | | |
| | $A_V = 1.0$ | | 3.8 | | | 3.8 | | μS |
| | $A_V = 100$ | | 180 | | | 180 | | μS |

**Note 1:** Unless otherwise specified, all specifications apply for $V_S = \pm15V$, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

**Note 2:** All typical values are for $T_A = 25°C$.

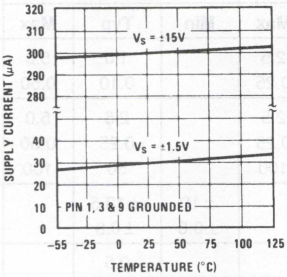
**Note 3:** The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

**Note 4:** $A_V = 1000$ guaranteed by design and testing at $A_V = 100$.

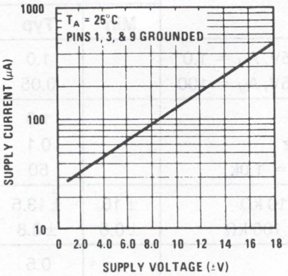
**Note 5:** Refer to RETS0036G for LH0036G military specifications.

# Typical Performance Characteristics

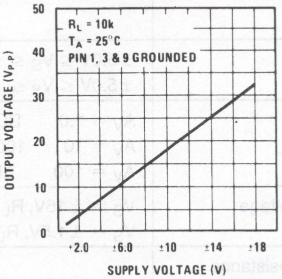
### Supply Current vs Temperature



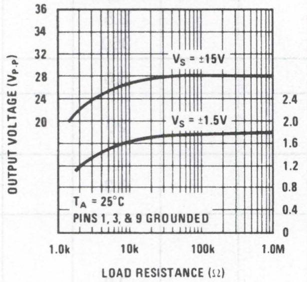
### Supply Current vs Supply Voltage



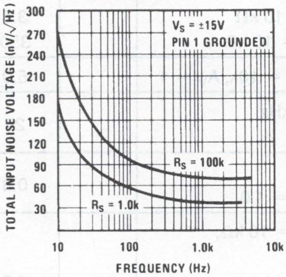
### Output Voltage Swing vs Supply Voltage



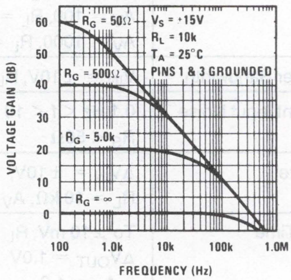
### Peak to Peak Output Voltage Swing vs $R_L$



### Total Input Noise Voltage* vs Frequency

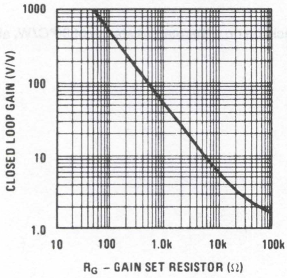


### Closed Loop Voltage Gain vs Frequency

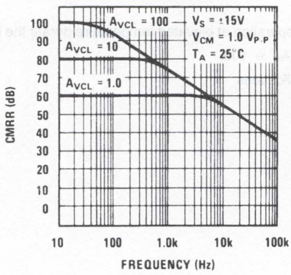


*Noise voltage includes contribution from source resistance

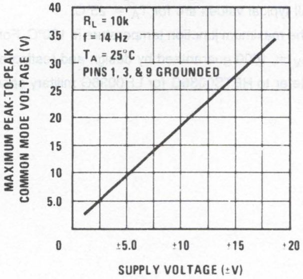
### Closed Loop Voltage Gain



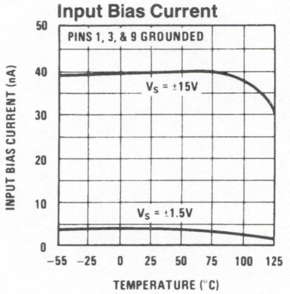
### CMRR vs Frequency



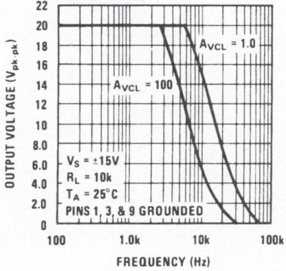
### Common Mode Voltage vs Supply Voltage



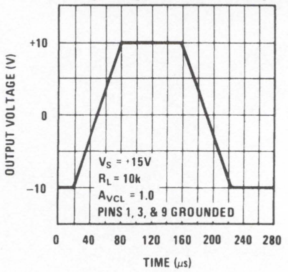
### Input Bias Current



### Output Voltage Swing vs Frequency



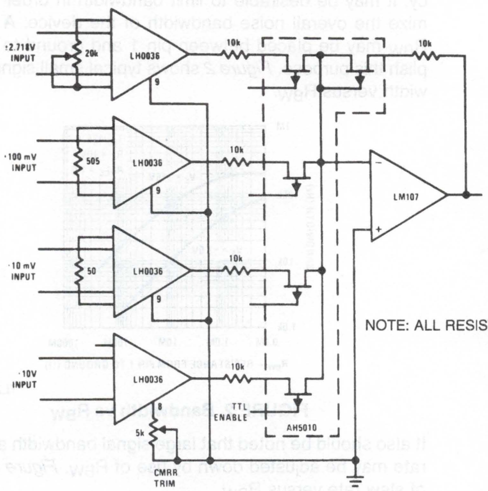
### Large Signal Pulse Response



TL/H/5545–2

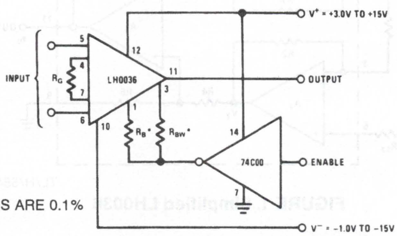
# Typical Applications

## Pre MUX Signal Conditioning


+2.718V INPUT
20k
LH0036
9
10k
10k
·100 mV INPUT
505
LH0036
9
10k
LM107
·10 mV INPUT
50
LH0036
9
10k
·10V INPUT
LH0036
10k
5k
CMRR TRIM
TTL ENABLE
AH5010

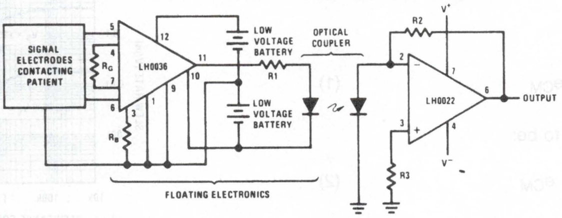
NOTE: ALL RESISTORS ARE 0.1%

## Instrumentation Amplifier with Logic Controlled Shut-Down

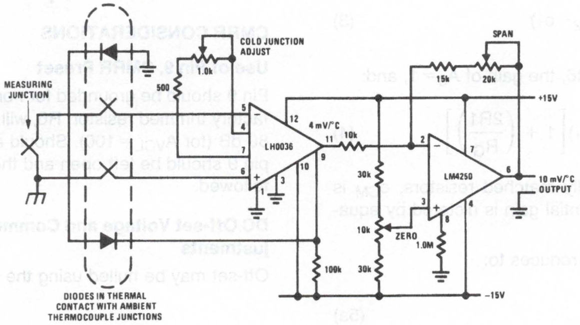

V⁺ = +3.0V TO +15V
INPUT
R_G
LH0036
OUTPUT
R_B*
R_BW*
74C00
ENABLE
V⁻ = -1.0V TO -15V

*$R_{BW}$ AND $R_B$ ARE OPTIONAL BANDWIDTH AND INPUT BIAS CURRENT CONTROLLING RESISTORS.

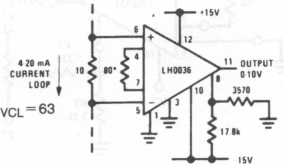
## Isolation Amplifier for Medical Telemetry


SIGNAL ELECTRODES CONTACTING PATIENT
R_G
R_B
LH0036
LOW VOLTAGE BATTERY
R1
LOW VOLTAGE BATTERY
OPTICAL COUPLER
V⁺
R2
LH0022
OUTPUT
V⁻
R3
FLOATING ELECTRONICS

## Thermocouple Amplifier with Cold Junction Compensation

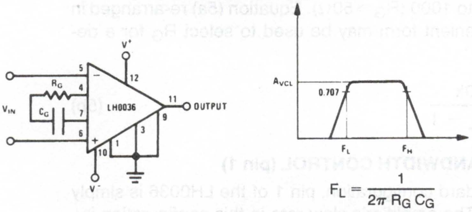

COLD JUNCTION ADJUST
1.0k
500
MEASURING JUNCTION
LH0036
4 mV/°C
10k
SPAN
15k
20k
+15V
LM4250
10 mV/°C OUTPUT
30k
10k
ZERO
1.0M
100k
30k
-15V
DIODES IN THERMAL CONTACT WITH AMBIENT THERMOCOUPLE JUNCTIONS

## Process Control Interface


+15V
4-20 mA CURRENT LOOP
80*
LH0036
OUTPUT 0-10V
3570
17.8k
-15V

*$A_{VCL} = 63$

## High Pass Filter


V⁺
R_G
C_G
V_IN
LH0036
OUTPUT
GAIN
A_VCL
0.707
F_L
F_H

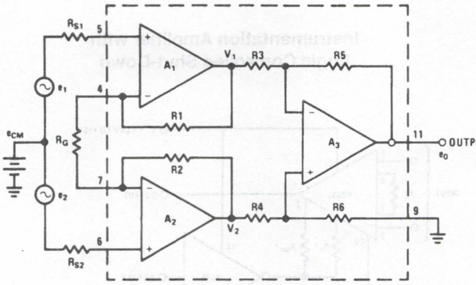
$$F_L = \frac{1}{2\pi R_G C_G}$$

TL/H/5545-3

$F_H$ = A FUNCTION OF SELECTED $A_{VCL}$, $R_S$ AND $R_{SW}$

## Applications Information

### THEORY OF OPERATION



TL/H/5545–4

**FIGURE 1. Simplified LH0036**

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of $A_1$ and $A_2$ and a differential to single-ended unity gain stage, $A_3$. Operational amplifier, $A_1$, receives differential input signal, $e_1$, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

$A_1$ also receives input $e_2$ via $A_2$ and R2. $e_2$ is seen as an inverting signal with a gain of $R1/R_G$. $A_1$ also receives the common mode signal $e_{CM}$ and processes it with a gain of $+1$.

Hence:

$$V_1 = \frac{R1+R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \qquad (1)$$

By similar analysis $V_2$ is seen to be:

$$V_2 = \frac{R2+R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \qquad (2)$$

For $R1 = R2$:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \qquad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \qquad (4)$$

As can be seen for identically matched resistors, $e_{CM}$ is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

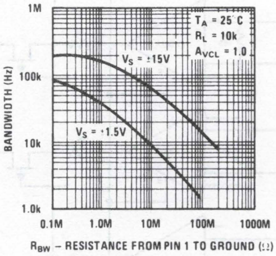
$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \qquad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select $R_G$ for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \qquad (5b)$$

### USE OF BANDWIDTH CONTROL (pin 1)

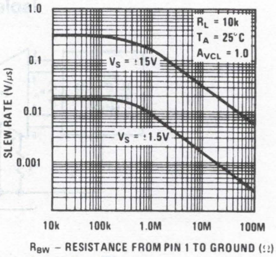
In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/µS and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor $R_{BW}$ may be placed between pin 1 and ground to accomplish this purpose. *Figure 2* shows typical small signal bandwidth versus $R_{BW}$.



TL/H/5545–5

**FIGURE 2. Bandwidth vs $R_{BW}$**

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of $R_{BW}$. *Figure 3* is plot of slew rate versus $R_{BW}$.



TL/H/5545–6

**FIGURE 3. Output Slew Rate vs $R_{BW}$**

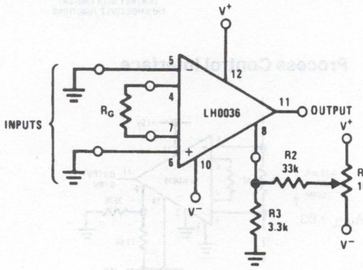
### CMRR CONSIDERATIONS

#### Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

#### DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in *Figure 4*.

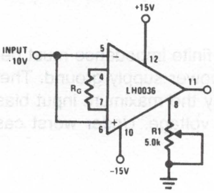


TL/H/5545–7

**FIGURE 4. $V_{OS}$ Adjustment Circuit**

## Applications Information (Continued)

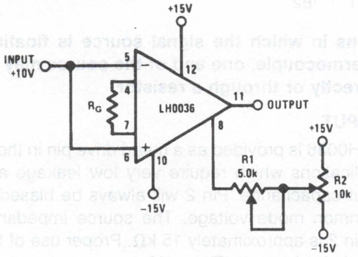
Pin 8 is also used to improve the common mode rejection ratio as shown in *Figure 5*. Null is achieved by alternately applying ±10V (for V+ & V− = 15V) to the inputs and adjusting R1 for minimum change at the output.


+15V
INPUT
±10V
5
12
4
R<sub>G</sub>
7
LH0036
11
OUTPUT
8
6
10
R1
5.0k
−15V

TL/H/5545-8

**FIGURE 5. CMRR Adjustment Circuit**

The circuits of *Figure 4* and *5* may be combined as shown in *Figure 6* to accomplish both $V_{OS}$ and CMRR null. However, the $V_{OS}$ and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

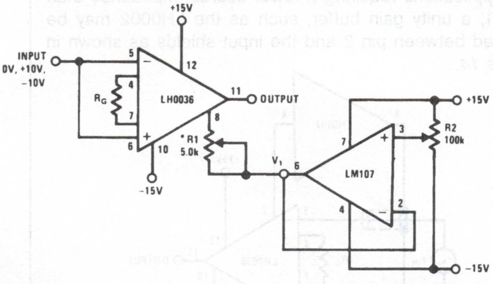

+15V
INPUT
±10V
5
12
4
R<sub>G</sub>
7
LH0036
11
OUTPUT
8
+15V
6
10
R1
5.0k
R2
10k
−15V
−15V

TL/H/5545-10

**FIGURE 6. Combined CMRR, $V_{OS}$ Adjustment Circuit**

R2 is adjusted for $V_{OS}$ null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in *Figure 7*. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.


+15V
INPUT
0V, +10V,
−10V
5
12
4
R<sub>G</sub>
7
LH0036
11
OUTPUT
8
6
10
*R1
5.0k
−15V
V<sub>1</sub>
6
7
3
2
4
LM107
+15V
R2
100k
−15V

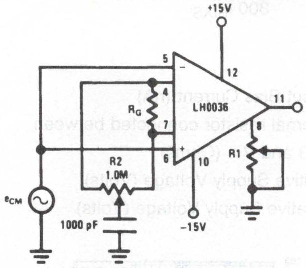
TL/H/5545-11

*Note: Nominal value R1 to Achieve Optimum CMRR is 3.0 kΩ.

**FIGURE 7. Improved $V_{OS}$, CMRR Nulling Circuit**

**AC CMRR Considerations**

The ac CMRR may be improved using the circuit of *Figure 8*.


+15V
5
12
4
R<sub>G</sub>
LH0036
11
OUTPUT
7
6
10
R1
R2
1.0M
e<sub>CM</sub>
1000 pF
−15V

TL/H/5545-9

**FIGURE 8. Improved AC CMRR Circuit**

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

### INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor ($R_B$) between 3 and ground or, alternatively, between 3 and V−. For $R_B$ returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\ R_B} \quad (6a)$$

or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (6b)$$

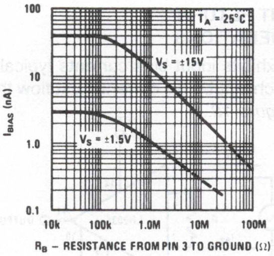
Where:

$I_{BIAS}$ = Input Bias Current (nA)

$R_B$ = External Resistor connected between pin 3 and ground (Ohms)

$V^+$ = Positive Supply Voltage (Volts)

*Figure 9* is a plot of input bias current versus $R_B$.



TL/H/5545-12

**FIGURE 9. Input Bias Current as a Function of $R_B$**

As indicated above, $R_B$ may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\ R_B}$$

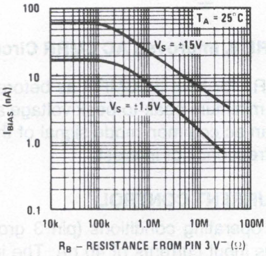
## Applications Information (Continued)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \qquad (8)$$

Where:

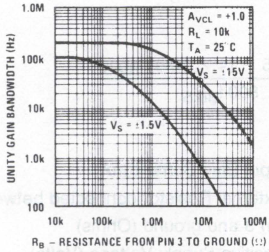
$I_{BIAS}$ = Input Bias Current (nA)
$R_B$ = External resistor connected between pin 3 and $V^-$ (Ohms)
$V^+$ = Positive Supply Voltage (Volts)
$V^-$ = Negative Supply Voltage (Volts)



TL/H/5545–13

FIGURE 10. Input Bias Current as a Function of $R_B$

*Figure 10* is a plot of input bias current versus $R_B$ returned to $V^-$ it should be noted that bandwidth is affected by changes in $R_B$. *Figure 11* is a plot of bandwidth versus $R_B$.

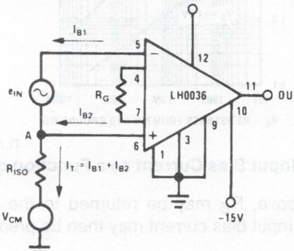


TL/H/5545–14

FIGURE 11. Unity Gain Bandwidth as a Function of $R_B$

### BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through $R_{ISO}$ as shown in *Figure 12*.



TL/H/5545–16

FIGURE 12. Bias Current Return Path

In a typical application, $V_S = \pm 15V$, $I_{B1} \cong I_{B2} \cong 40$ nA, the total current, $I_T$, would flow through $R_{ISO}$ causing a voltage rise at point A. For values of $R_{ISO} \geq 150\ M\Omega$, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \qquad (9)$$

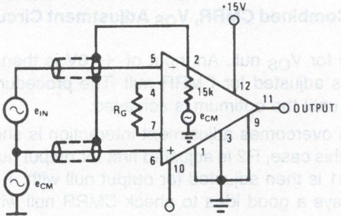
Where:

$V_{CMR}$ = Common Mode Range (10V for the LH0036)
$V_{CM}$ = Common Mode Voltage
$I_T = I_{B1} + I_{B2}$

**In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.**

### GUARD OUTPUT

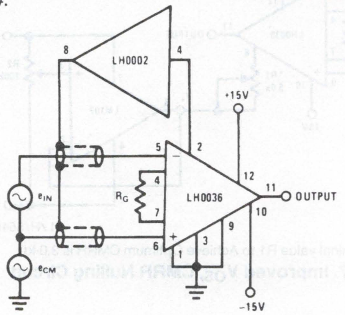
Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in *Figure 13*.



TL/H/5545–15

FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in *Figure 14*.



TL/H/5545–17

FIGURE 14. Guard Pin With Buffer

## Definition of Terms

**Bandwidth:** The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

**Closed Loop Gain, $A_{VCL}$:** The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: $R_G$ = Gain Set Resistor.

**Common Mode Rejection Ratio:** The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

**Gain Equation Accuracy:** The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

**Input Bias Current:** The current flowing at pin 5 and 6 under the specified operating conditions.

**Input Offset Current:** The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

**Input Stage Offset Voltage, $V_{IOS}$:** The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

**Output Stage Offset Voltage, $V_{OOS}$:** The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting $V_{IOS}$.

$$V_{OOS} = \left[ V_{OS} \Big|_{A_{VCL}=1} \right] - \left[ V_{OS} \Big|_{A_{VCL}=1000} \right]$$

**Overall Offset Voltage:**

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

**Power Supply Rejection Ratio:** The ratio of the change in offset voltage, $V_{OS}$, to the change in supply voltage producing it.

**Resistor, $R_B$:** An optional resistor placed between pin 3 of the LH0036 and ground (or $V^-$) to reduce the input bias current.

**Resistor, $R_{BW}$:** An optional resistor placed between pin 1 of the LH0036 and ground (or $V^-$) to reduce the bandwidth of the output stage.

**Resistor, $R_G$:** A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

**Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**National Semiconductor Corporation**

# LH0038/LH0038C True Instrumentation Amplifier

## General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain gauge outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

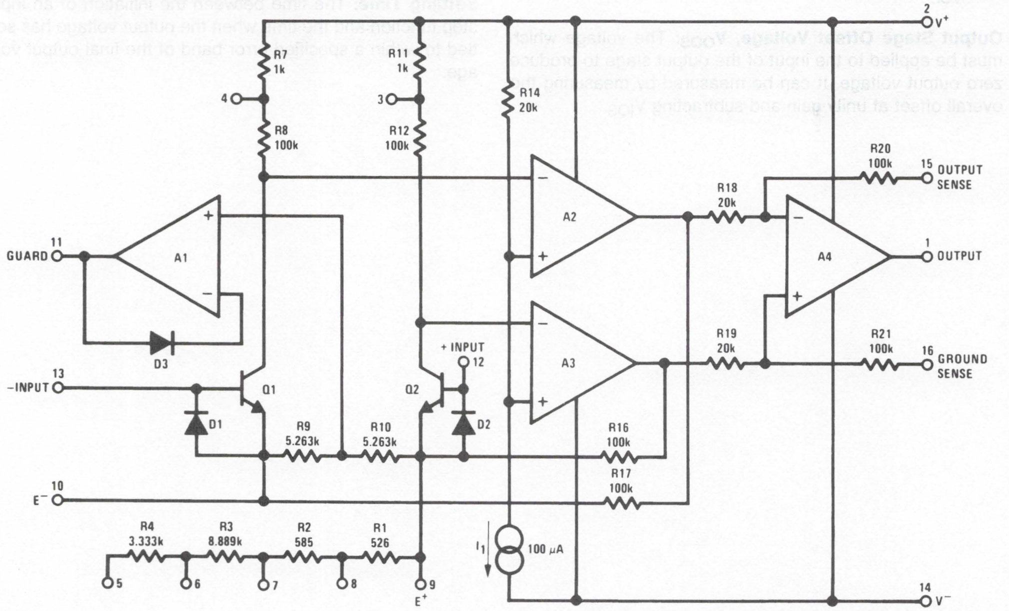
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

## Features

| | |
|---|---|
| ■ Ultra-low input offset voltage | 25 $\mu$V typ., 100 $\mu$V max |
| ■ Ultra-low input offset drift | 0.25 $\mu$V/°C max |
| ■ Ultra-low input noise | 0.2 $\mu$Vp-p |
| ■ Pin strap gain options 100, 200, 400, 500, 1k, 2k | |
| ■ Excellent PSRR and CMRR | 120 dB |

## Simplified Schematic Diagram



2
V⁺
R7
1k
R11
1k
4
3
R8
100k
R12
100k
R14
20k
R20
100k
15
OUTPUT SENSE
R18
20k
A2
A4
1
OUTPUT
11
GUARD
A1
D3
+INPUT
12
13
−INPUT
Q1
Q2
D1
D2
A3
R19
20k
R21
100k
16
GROUND SENSE
R9
5.263k
R10
5.263k
R16
100k
R17
100k
10
E⁻
R4
3.333k
R3
8.889k
R2
585
R1
526
5
6
7
8
9
E⁺
I1
100 µA
14
V⁻

TL/H/5543–1

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)**

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage (Note 1) | ±1V |
| Input Voltage | $\pm V_S$ |
| Power Dissipation (Note 3) | 500 mW |
| Short Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0038 | −55°C to +125°C |
| LH0038C | −25°C to +85°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| ESD rating to be determined. | |

## DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Conditions | | LH0038 | | | LH0038C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IOS}$ | Input Offset Voltage | $R_S = 50\Omega$<br>$V_{CM} = 0V$ | $T_A = 25°C$ | | 25 | 100 | | 30 | 150 | μV |
| | | | | | | 125 | | | 220 | |
| $\Delta V_{IOS}/\Delta T$ | Input Offset Voltage Tempco | | | | 0.1 | 0.25 | | 0.2 | 1.0 | μV/°C |
| $V_{OOS}$ | Output Offset Voltage | | $T_A = 25°C$ | | 3 | 10 | | 5 | 25 | mV |
| | | | | | | 15 | | | 30 | |
| $\Delta V_{OOS}/\Delta T$ | Output Offset Voltage Tempco | | | | 25 | | | 25 | | μV/°C |
| $I_B$ | Input Bias Current | | $T_A = 25°C$ | | 50 | 100 | | 50 | 100 | nA |
| | | | | | | 200 | | | 200 | |
| $I_{OS}$ | Input Offset Current | | $T_A = 25°C$ | | 2 | 5 | | 7 | 10 | |
| | | | | | | 8 | | | 15 | |
| $\Delta I_B/\Delta T$ | Input Bias Current Tempco | | | | 500 | | | 500 | | pA/°C |
| $A_{VCL}$ | Closed Loop Gain | Gain Pins Jumped | | | | | | | | V/V |
| | | None | | | 100 | | | 100 | | |
| | | 6-10 | | | 200 | | | 200 | | |
| | | 6-9, 10-5 | | | 400 | | | 400 | | |
| | | 6-10, 5-9 | | | 500 | | | 500 | | |
| | | 7-10 | | | 1000 | | | 1000 | | |
| | | 8-10 | | | 2000 | | | 2000 | | |
| | Closed Loop Gain Error | $A_{VCL} = 100, 200$ | | | 0.1 | 0.3 | | 0.1 | 0.4 | % |
| | | $A_{VCL} = 400, 500$ | | | 0.2 | 0.3 | | 0.2 | 0.6 | |
| | | $A_{VCL} = 1000$ | | | 0.3 | 0.5 | | 0.5 | 1.0 | |
| | | $A_{VCL} = 2000$ | | | 1.0 | 2.0 | | 1.5 | 3.0 | |
| | Gain Temperature Coefficient | $A_{VCL} = 1k$ | | | 7 | | | 7 | | ppm/°C |
| | Gain Nonlinearity | $100 \le A_{VCL} \le 2k$ | | | 1 | | | 1 | | ppm |
| $V_{INCM}$ | Common-Mode Input Voltage Range | | | ±10 | ±12 | | ±10 | ±12 | | V |
| $V_O$ | Output Voltage | $R_L \ge 10\ k\Omega$ | | ±10 | ±12 | | ±10 | ±12 | | |
| $V_S$ | Supply Voltage Range | | | ±5 | | ±18 | ±5 | | ±18 | |
| | Guard Voltage Error | $-10V < V_{CM} < +10V$ | | | ±10 | ±100 | | ±10 | ±100 | mV |
| CMRR | Common-Mode Rejection Ratio | $V_{IN} = \pm 10V$ | $A_{VCL} = 100$ | 94 | 110 | | 86 | 110 | | dB |
| | | | $A_{VCL} = 1000$ | 114 | 120 | | 106 | 110 | | |
| PSRR | Power Supply Rejection Ratio | $\pm 5V \le \Delta V_S \le \pm 15V$ | $A_{VCL} = 100$ | 94 | 110 | | 94 | 110 | | |
| | | | $A_{VCL} = 1000$ | 110 | 120 | | 100 | 110 | | |

## DC Electrical Characteristics (Note 2) (Continued)

| Symbol | Parameter | Conditions | LH0038 Min | LH0038 Typ | LH0038 Max | LH0038C Min | LH0038C Typ | LH0038C Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $I_{OSC}$ | Output Short Circuit Current | $T_A = 25°C$ | ±2 | ±5 | ±10 | ±2 | ±5 | ±10 | mA |
| $I_S$ | Supply Current | $T_A = 25°C$ | | 1.6 | 2.0 | | 1.6 | 3.0 | |
| $R_{IN}$ DIFF | Input Resistance | $A_{VCL} = 1000, T_A = 25°C$ | | 5 | | | 5 | | MΩ |
| $R_{IN}{}^{CM}$ | Common-Mode Input Resistance | | | 1 | | | 1 | | GΩ |
| $R_{OUT}$ | Output Resistance | | | 1 | | | 1 | | mΩ |

## AC Electrical Characteristics $V_S = \pm 15V, T_A = 25°C$

| Symbol | Parameter | Comment | Conditions | | Typ | Units |
|---|---|---|---|---|---|---|
| $e_n$ | Equivalent Input Noise Voltage | *Figure 1* | $R_S = 0$, f = 0.1 to 10Hz | | 0.2 | μVp-p |
| $\overline{e_n}$ | Equivalent Input Spot Noise Voltage | *Figure 1* | $R_S = 100\Omega$ | f = 10 Hz | 6.5 | nV/$\sqrt{Hz}$ |
| | | | | f = 100 Hz | 6.0 | |
| | | | | f = 1 kHz | 6.0 | |
| | | | | f = 10 kHz | 6.0 | |
| BW | Large Signal Bandwidth | | $V_{OUT} = \pm 10V$ | | 1.6 | kHz |
| $S_r$ | Slew Rate | | $V_{OUT} = \pm 10V$ | | 0.3 | V/μs |
| $t_s$ | Settling Time to 0.01% | *Figure 13* | | 20V Step | 120 | μs |
| | | | | −10V Step | 80 | |
| | | | | +10V Step | 60 | |
| $t_r$ | Rise Time | | $\Delta V_{OUT}$ | $A_{VCL} = 100$ | 6 | μs |
| | | | | $A_{VCL} = 1000$ | 13 | |
| $\overline{i_n}$ | Equivalent Input Spot Noise Current | | $R_S = 100\ M\Omega$ | f = 10 Hz | 0.1 | pA/$\sqrt{Hz}$ |

**Note 1:** The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

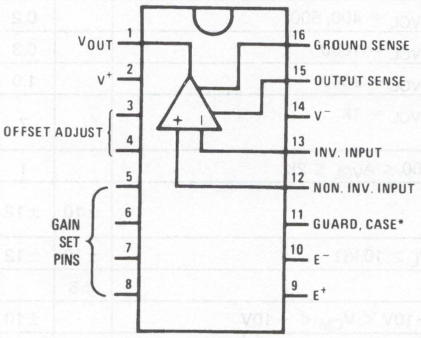
**Note 2:** Unless otherwise noted these specifications apply for $V_S = \pm 15.0V$, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C. $T_A = T_j$ unless otherwise specified.

**Note 3:** See Typical Performance Characteristics for Thermal Resistance Information.

**Note 4:** Refer to RETS0038D for LH0038D military specifications.

## Connection Diagram

**Dual-In-Line Package**



TL/H/5543-2

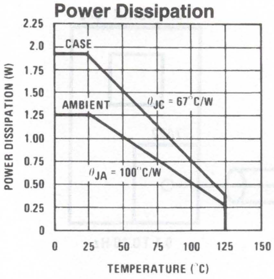
**Top View**

*Guard output is connected to the case.

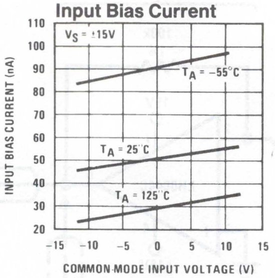
**Order Number LH0038 or LH0038CD**
**See NS Package Number D16D**

## Typical Performance Characteristics

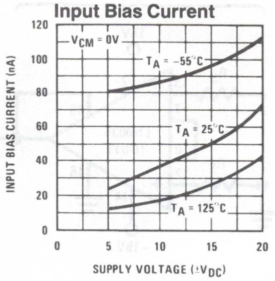
### Power Dissipation



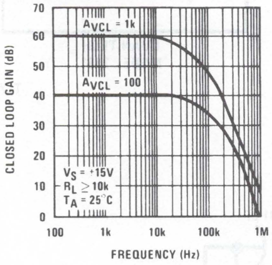
### Input Bias Current



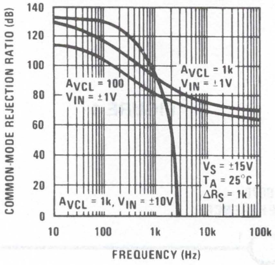
### Input Bias Current



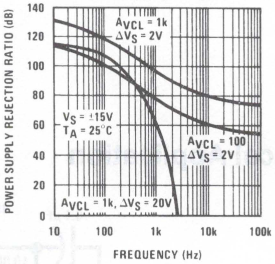
### Closed Loop Frequency Response



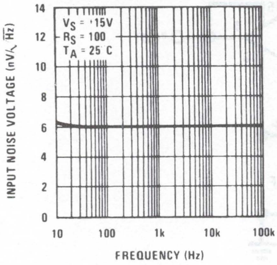
### Common-Mode Rejection



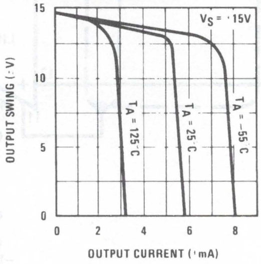
### Power Supply Rejection



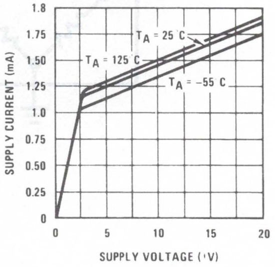
### Input Noise Voltage (Includes Source Impedance)



### Output Swing

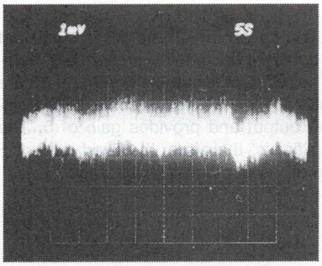


### Supply Current



TL/H/5543-3

### Wide Band Noise



TL/H/5543-4

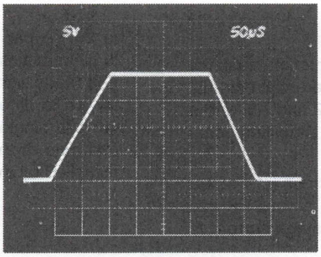
$V_S$ = ±15V, $R_S$ = 1 kΩ, $A_V$ = 10k, DUT = 1k

Vertical sensitivity: 0.1 μV/CM

Horizontal sensitivity: 5 s/CM

Bandwidth: 0.1 Hz to 10 Hz

### Pulse Response



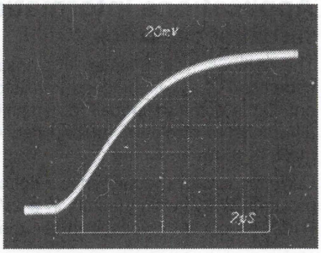
TL/H/5543-5

$V_S$ = ±15V

$R_L$ ≥ 10 kΩ

$A_{VCL}$ = 1k

### Rise Time



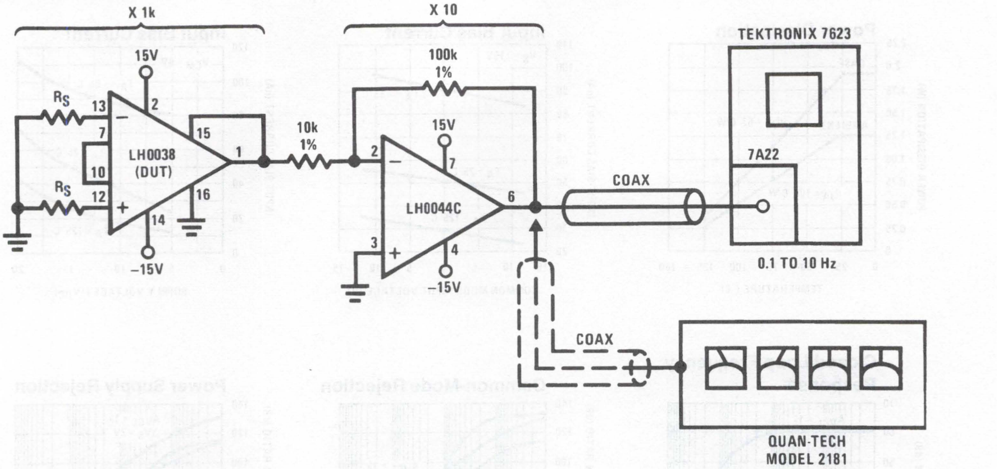
TL/H/5543-6

$V_S$ = ±15V

$R_L$ ≥ 10kΩ

$A_{VCL}$ = 1k

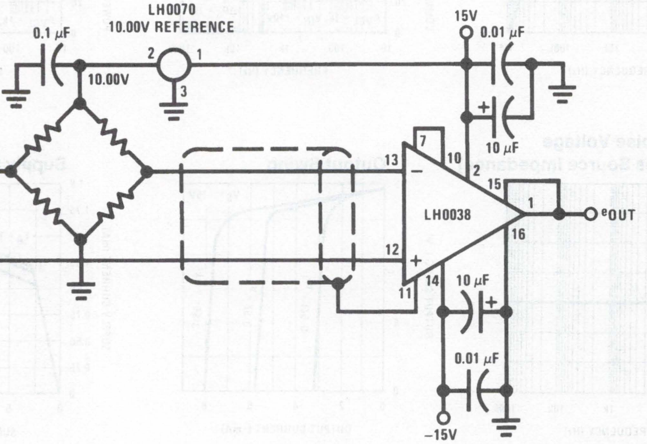
## Noise Test Circuit


X 1k
15V
RS
13
7
2
RS
10
12
LH0038
(DUT)
15
1
16
14
−15V
X 10
100k
1%
10k
1%
15V
2
7
LH0044C
6
3
4
−15V
COAX
TEKTRONIX 7623
7A22
0.1 TO 10 Hz
COAX
QUAN-TECH
MODEL 2181

TL/H/5543-7

FIGURE 1

## Typical Application


LH0070
10.00V REFERENCE
0.1 μF
2
1
3
10.00V
15V
0.01 μF
10 μF
7
10
2
13
15
1
LH0038
eOUT
16
12
11
14
10 μF
0.01 μF
−15V

TL/H/5543-8

FIGURE 2. X1000 Bridge Amplifier

## Applications Information

### THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3*.

Current source, $I_A$, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

## Applications Information (Continued)

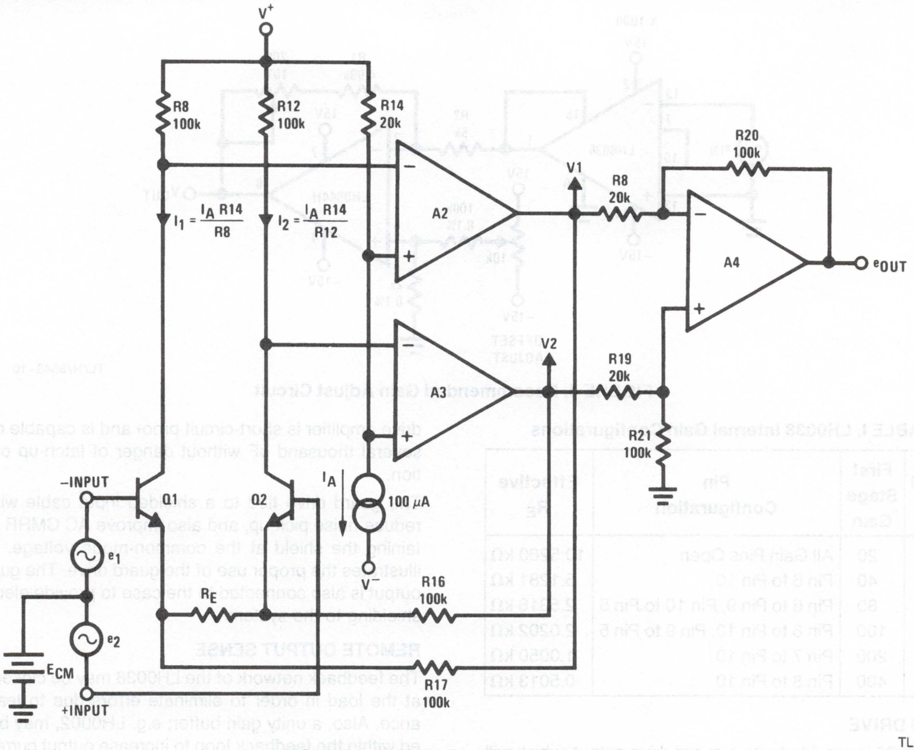


**FIGURE 3. LH0038 Simplified Schematic**

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3.* The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1 \left(\frac{R17 + R_E}{R_E}\right) - e2 \left(\frac{R17}{R_E}\right) + E_{CM} - V_{BE1} - I_1 R17 \quad (1)$$

By similar analysis:

$$v2 = e2 \left(\frac{R16 + R_E}{R_E}\right) - e1 \left(\frac{R16}{R_E}\right) + E_{CM} - V_{BE2} - I_2 R16 \quad (2)$$

For $I_1 \equiv I_2$, $R17 \equiv R16$, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1) \left(\frac{R16 + R_E}{R_E}\right) + (e2 - e1) \left(\frac{R16}{R_E}\right) \quad (3)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \quad (4)$$

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})\,(e2 - e1) \quad (5)$$

where:

$$A_{VCL4} = \frac{R20}{R8} = 5.00$$

$$\boxed{A_{VCL} = 5 \left(\frac{2R16}{R_E} + 1\right)} \quad (6)$$

As an example, with all gain pins open, $R_E = 10.525\ k\Omega$, and;

$$A_{VCL} = 5 \left(\frac{(2)\,(100k)}{R_E} + 1\right) = 100.0 \quad (7)$$

All other closed loop gain configurations place a precision resistor in parallel with $R_E(R9 + R10)$. For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

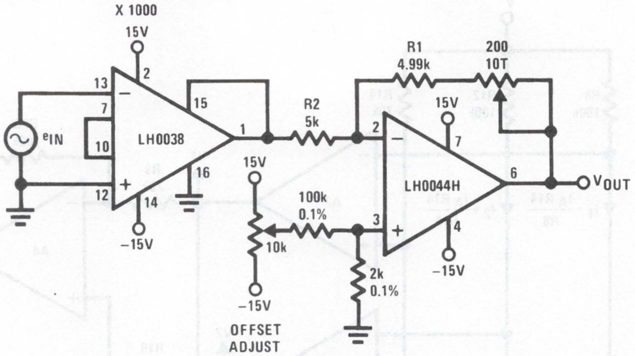
$$A_{VCL} = 5.00 \left[\frac{(2)\,(100k)}{(10.526)\,\|\,(10.000k)} + 1\right] = (5.00)\,(40) = 200 \quad (8)$$

### CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table 1 summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and $R_E$ all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4.*

## Applications Information (Continued)


X 1000
15V
2
13
7
10
12
14
−15V
LH0038
15
16
1
$e_{IN}$
R2
5k
15V
100k
0.1%
10k
−15V
OFFSET
ADJUST
R1
4.99k
200
10T
15V
2
7
3
4
6
LH0044H
−15V
2k
0.1%
$V_{OUT}$

TL/H/5543-10

**FIGURE 4. Recommended Gain Adjust Circuit**

**TABLE I. LH0038 Internal Gain Configurations**

| Overall Gain | First Stage Gain | Pin Configuration | Effective $R_E$ |
|---|---|---|---|
| 100 | 20 | All Gain Pins Open | 10.5260 kΩ |
| 200 | 40 | Pin 6 to Pin 10 | 5.1281 kΩ |
| 400 | 80 | Pin 6 to Pin 9, Pin 10 to Pin 5 | 2.5316 kΩ |
| 500 | 100 | Pin 6 to Pin 10, Pin 9 to Pin 5 | 2.0202 kΩ |
| 1000 | 200 | Pin 7 to Pin 10 | 1.0050 kΩ |
| 2000 | 400 | Pin 8 to Pin 10 | 0.5013 kΩ |

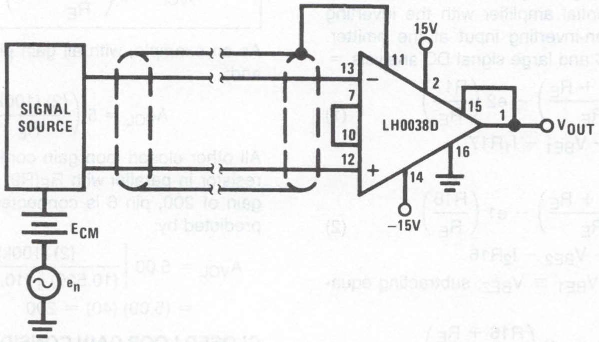
### GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive. The guard drive output is also connected to the case to provide electrostatic shielding to the system.

### REMOTE OUTPUT SENSE

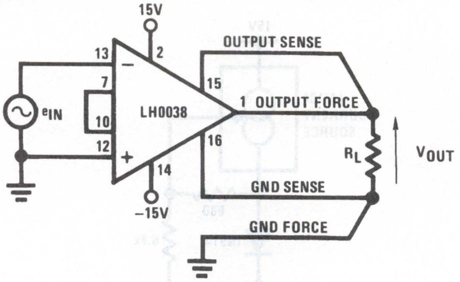
The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7.*


SIGNAL
SOURCE
$E_{CM}$
$e_n$
15V
11
13
7
10
12
2
15
1
16
14
LH0038D
−15V
$V_{OUT}$

TL/H/5543-11

**FIGURE 5. Guard Drive Application**

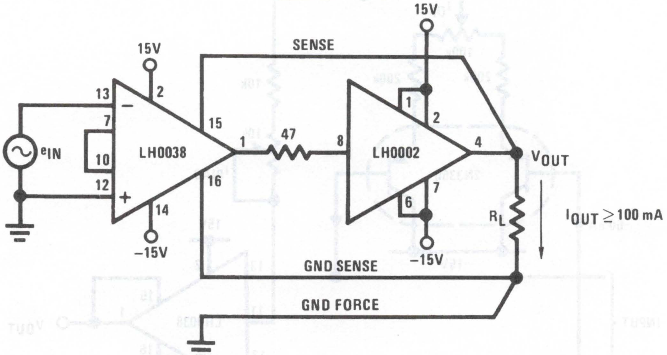
## Applications Information (Continued)



15V
13
2
7
10
12
14
15
16
1
LH0038
eIN
OUTPUT SENSE
OUTPUT FORCE
$R_L$
$V_{OUT}$
GND SENSE
GND FORCE
−15V

TL/H/5543–12

FIGURE 6. Remote Sense Connection



15V
SENSE
15V
13
2
7
10
12
14
15
16
1
47
8
LH0038
LH0002
1
2
4
7
6
eIN
$V_{OUT}$
$R_L$
$I_{OUT} \geq 100$ mA
−15V
−15V
GND SENSE
GND FORCE

TL/H/5543–13

FIGURE 7. Output Buffer Connection

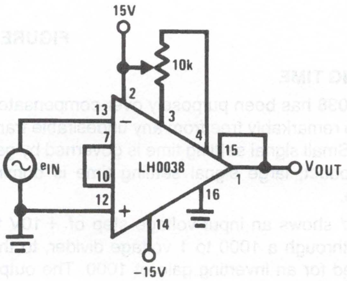
### OFFSET NULL

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8*. However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

### BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance between the inputs and ground is dictated by negative common-mode range as shown in *Figure 9*. For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

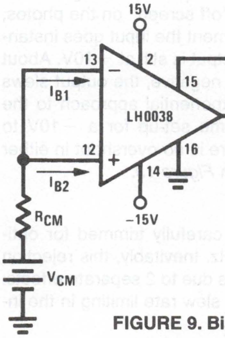
The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10*. The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.



15V
10k
2
3
4
7
13
10
12
14
15
16
1
LH0038
eIN
$V_{OUT}$
−15V

TL/H/5543–14

FIGURE 8. Offset Adjust Circuit (See also *Figure 4*)



15V
13
2
15
1
12
16
14
$I_{B1}$
$I_{B2}$
LH0038
$V_{OUT}$
$R_{CM}$
$V_{CM}$
−15V

$$R_{CM} \leq \frac{|V_{CMR}| - V_{CM}}{I_{B1} + I_{B2}}$$

where:

$V_{CMR}$ = Common-Mode Range = ±12V

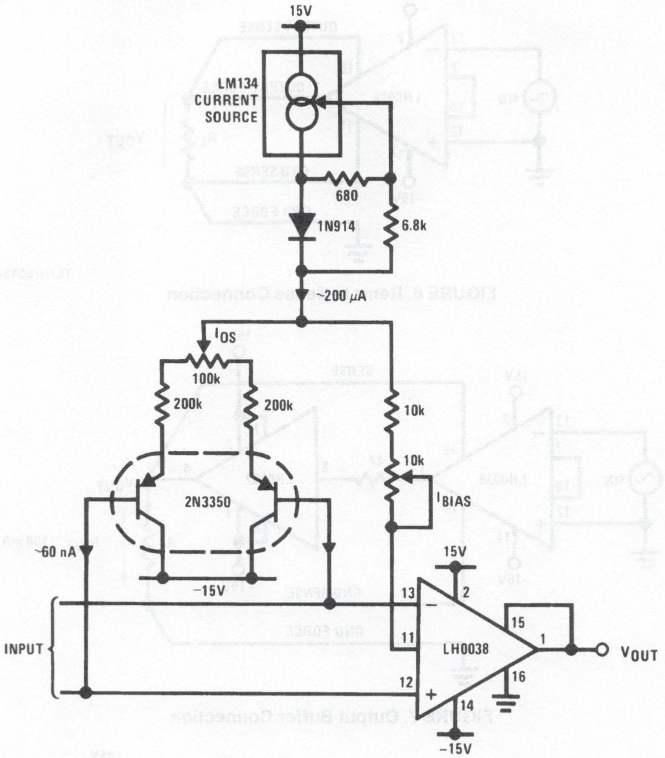
$V_{CM}$ = Common-Mode Input Voltage

$I_{B1} + I_{B2}$ = Bias Current = 100 nA

FIGURE 9. Bias Current Return

TL/H/5543–15

## Applications Information (Continued)



TL/H/5543–16

**FIGURE 10. Bias Current Compensation**

### SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

*Figure 11* shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 µs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13.*

### HIGH FREQUENCY CMRR

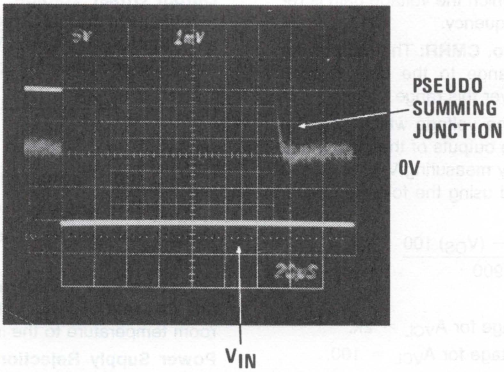
The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/µs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/µs corresponds to about 2 kHz (20 Vp-p).

### POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V+ and V− leads be by-passed with 1 µF electrolytic in shunt with 0.01 µF ceramic disc no further than 1 inch from the device.

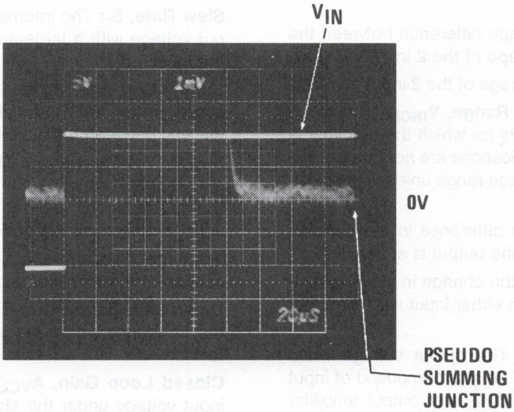
## Applications Information (Continued)


PSEUDO
SUMMING
JUNCTION
0V
$V_{IN}$
5V
2mV
20µS

TL/H/5543-17

$t_s$, $A_V = 100$, $V_{IN} = -20V$

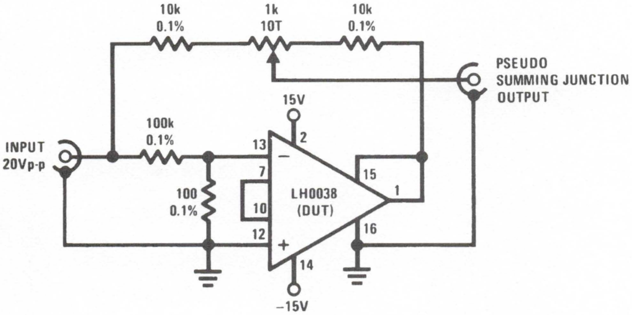
**FIGURE 11. Settling Time**


$V_{IN}$
0V
PSEUDO
SUMMING
JUNCTION
5V
2mV
20µS

TL/H/5543-18

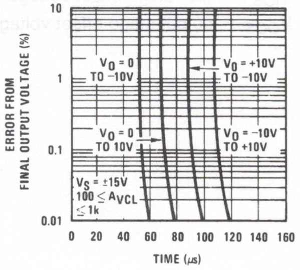
$t_s$, $A_V = 100$, $V_{IN} = -20V$

**FIGURE 12. Settling Time**


10k
0.1%
1k
10T
10k
0.1%
PSEUDO
SUMMING JUNCTION
OUTPUT
15V
100k
0.1%
INPUT
20Vp-p
13
2
7
15
1
100
0.1%
10
LH0038
(DUT)
12
16
14
−15V

TL/H/5543-19

**FIGURE 13. Settling Time Test Circuit**



TL/H/5543-20

**FIGURE 14. Settling Time**

## Definition of Terms

**Bandwidth:** That frequency at which the voltage gain is reduced to 3 dB below the low frequency.

**Common-Mode Rejection Ratio, CMRR:** The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

**Input Offset Voltage, $V_{IOS}$:** The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. $V_{IOS}$ can be calculated by measuring $V_{OS}$ at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\,2k - (V_{OS})\,100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for $A_{VCL} = 2k$.

$(V_{OS})100$ = overall offset voltage for $A_{VCL} = 100$.

**Gain Non-Linearity:** The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

**Guard Voltage Error:** The voltage difference between the guard drive output and the average of the 2 input voltages.

**Input Bias Current, $I_B$:** The average of the 2 input currents.

**Input Common-Mode Voltage Range, $V_{INCM}$:** The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

**Input Offset Current, $I_{OS}$:** The difference in the currents into the 2 input terminals when the output is at zero.

**Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

**Overall Offset Voltage, $V_{OS}$:** The output voltage when both inputs are connected to 0V. $V_{OS}$ is composed of input amplifier offset voltage effects, $V_{IOS}$, and output amplifier effects, $V_{OOS}$. It is given by:

$$V_{OS} = (A_{VCL})\,(V_{IOS}) - V_{OOS}$$

Where:

$A_{VCL}$ = closed loop gain = 100 to 2k

$V_{IOS}$ = input stage offset voltage

$V_{OOS}$ = output stage offset voltage

**Output Offset Voltage, $V_{OOS}$:** The output voltage when theoutputs of the input stage are forced to 0V. $V_{OOS}$ may be calculated by measuring $V_{OS}$ at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\,(V_{OS})\,100 - (V_{OS})\,2k}{19}$$

Where:

$(V_{OS})$ 100 = overall offset voltage for $A_{VCL} = 100$

$(V_{OS})$ 2k = overall offset voltage for $A_{VCL}$

**Output Voltage, $V_O$:** The peak output voltage swing, referred to zero.

**Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$:** The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

**Power Supply Rejection Ratio, PSRR:** The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**Settling times, $t_s$:** The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**Slew Rate, $S_r$:** The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

**Supply Current, $\pm I_s$:** The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

**Supply Voltage Range:** The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

**Transient Response, $t_r$:** The closed-loop step-function response of the amplifier under small-signal conditions.

**Unity Gain Bandwidth:** The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

**Closed Loop Gain, $A_{VCL}$:** The ratio of output voltage to input voltage under the stated conditions of source resistance ($R_S$) and load resistance ($R_L$).

**Voltage Gain Error:** The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

**National Semiconductor Corporation**

# LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

## General Description

The LH0084/LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

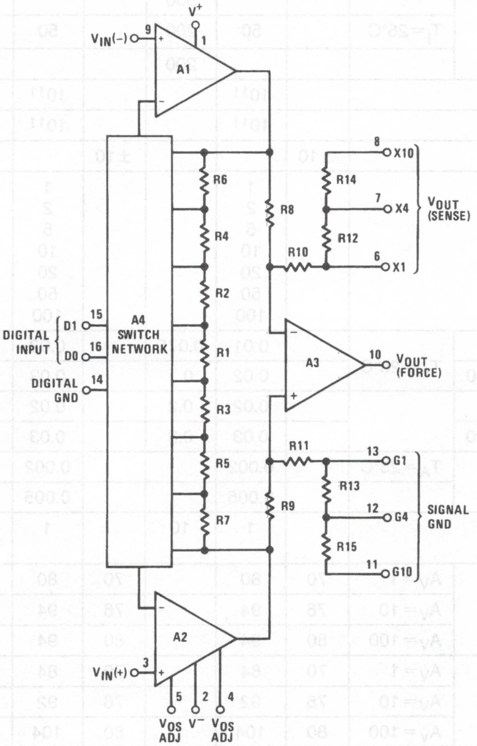
The device exhibits high input impedance, low offset voltage, high PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084 is guaranteed from −55°C to +125°C. The LH0084C is guaranteed from −25°C to +85°C. Both devices are provided in a hermetically sealed 16-lead dual-in-line metal package.

## Features

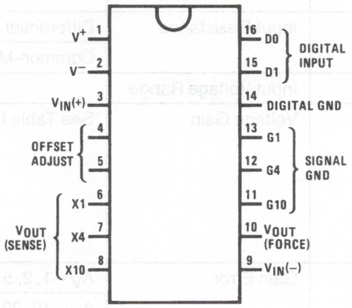
| | |
|---|---|
| ■ Excellent gain accuracy | 0.075% max |
| and low gain non-linearity | 0.01% typ |
| ■ Extremely low gain drift | 1 ppm/°C typ |
| | 10 ppm/°C max |
| ■ High input impedance | $10^{11}\Omega$ typ |
| ■ High PSRR | 70 dB min |
| ■ TTL compatible digital inputs | |
| ■ High speed, settling to 0.1% | 4 µs max |

## Simplified Schematic and Connection Diagrams



V+
VIN(−) 9
1
A1
8 X10
R6
R14
7 X4
VOUT (SENSE)
R8
R4
R12
R10
6 X1
R2
DIGITAL INPUT
D1 15
D0 16
A4 SWITCH NETWORK
R1
A3
10 VOUT (FORCE)
DIGITAL GND 14
R3
R11
13 G1
R5
R13
R9
12 G4
SIGNAL GND
R7
R15
11 G10
A2
VIN(+) 3
5 2 4
VOS ADJ V− VOS ADJ

**Dual-In-Line Package**



V+ 1
V− 2
VIN(+) 3
OFFSET ADJUST 4 5
X1 6
X4 7
X10 8
VOUT (SENSE)
16 D0
15 D1
DIGITAL INPUT
14 DIGITAL GND
13 G1
12 G4
11 G10
SIGNAL GND
10 VOUT (FORCE)
9 VIN(−)

TOP VIEW

Case is electrically isolated

**Order Number LH0084D or LH0084CD**
**See NS Package D16D**

TL/H/5651–1

5

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)**

| | |
|---|---|
| Supply Voltage (Note 1) | ±18V |
| Analog Input Voltage (Note 2) | ±15V |
| Differential Input Voltage (Note 2) | ±30V |
| Digital Input Voltage | −4V, +18V |
| Power Dissipation (Note 5) | 2.5W |
| Output Short Circuit Duration | Continuous |
| Operating Temperature Range | |
| LH0084 | −55°C to +125°C |
| LH0084C | −25°C to +85°C |
| Lead Temp. (Soldering, 10 seconds) | +260°C |

ESD rating to be determined.

## DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless noted

| Symbol | Parameter | Conditions | | LH0084 | | | LH0084C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IOS}$ | Input Offset Voltage | $R_S = 100\Omega$<br>$V_{CM} = 0$<br>(Note 3) | $T_j = 25°C$ | | 0.3 | 5 | | 0.3 | 10 | mV |
| | | | | | | 7 | | | 13 | |
| $\Delta V_{IOS}/\Delta T$ | Input Offset Voltage Change with Temperature | | | | 10 | | | 10 | | μV/°C |
| $V_{OOS}$ | Output Offset Voltage | | $T_j = 25°C$ | | 0.6 | 5 | | 0.6 | 10 | mV |
| | | | | | | 7 | | | 13 | |
| $\Delta V_{OOS}/\Delta T$ | Output Offset Voltage Change with Temperature | | | | 20 | | | 20 | | μV/°C |
| $I_B$ | Input Bias Current | | $T_j = 25°C$ | | 150 | 500 | | 150 | 500 | pA |
| | (Note 4) | | | | | 500 | | | 100 | nA |
| $I_{OS}$ | Input Offset Current | | $T_j = 25°C$ | | 50 | 200 | | 50 | 200 | pA |
| | | | | | | 200 | | | 50 | nA |
| $R_{IN}$ | Input Resistance | Differential | | | $10^{11}$ | | | $10^{11}$ | | Ω |
| | | Common-Mode | | | $10^{11}$ | | | $10^{11}$ | | |
| $V_{IN}$ | Input Voltage Range | | | ±10 | | | ±10 | | | V |
| $A_V$ | Voltage Gain | See Table I | | | 1<br>2<br>5<br>10<br>20<br>50<br>100 | | | 1<br>2<br>5<br>10<br>20<br>50<br>100 | | V/V |
| | Gain Error | $A_V = 1, 2, 5$ | $T_A = 25°C$ | | 0.01 | 0.075 | | 0.02 | 0.15 | % |
| | | $A_V = 10, 20, 50, 100$ | | | 0.02 | 0.1 | | 0.03 | 0.2 | |
| | | $A_V = 1, 2, 5$ | | | 0.02 | 0.2 | | 0.02 | 0.2 | |
| | | $A_V = 10, 20, 50, 100$ | | | 0.03 | 0.3 | | 0.03 | 0.3 | |
| | Gain Nonlinearity | | $T_A = 25°C$ | | 0.002 | | | 0.002 | | |
| | | | | | 0.005 | | | 0.005 | | |
| $\Delta A_V/\Delta T$ | Gain Temperature Coefficient | | | | 1 | 10 | | 1 | 10 | ppm/°C |
| CMRR | Common-Mode Rejection Ratio | $V_{IN} = \pm 10V$ | $A_V = 1$ | 70 | 80 | | 70 | 80 | | dB |
| | | | $A_V = 10$ | 76 | 94 | | 76 | 94 | | |
| | | | $A_V = 100$ | 80 | 94 | | 80 | 94 | | |
| PSRR | Power Supply Rejection Ratio | $\pm 8V \leq V_S \leq +18V$ | $A_V = 1$ | 70 | 84 | | 70 | 84 | | dB |
| | | | $A_V = 10$ | 76 | 92 | | 76 | 92 | | |
| | | | $A_V = 100$ | 80 | 104 | | 80 | 104 | | |
| $V_O$ | Output Voltage Swing | $II_L \geq 10\ k\Omega$ | | ±10 | ±12 | | ±10 | ±12 | | V |
| $I_O$ | Output Short Circuit Current | | $T_A = 25°C$ | ±5 | ±18 | ±40 | ±5 | ±18 | ±40 | mA |
| | | | | ±2 | | ±40 | ±2 | | ±40 | |

## DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

| Symbol | Parameter | Conditions | LH0084 | | | LH0084C | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $R_O$ | Output Resistance | | | 0.05 | | | 0.05 | | Ω |
| $V_{IL}$ | Digital "0" Input Voltage | | | | 0.7 | | | 0.7 | V |
| $V_{IH}$ | Digital "1" Input Voltage | | 2.0 | | | 2.0 | | | |
| $I_{IL}$ | Digital "0" Input Current | $V_{IN} = 0.4V$ | | 1.5 | 40 | | 1.5 | 40 | μA |
| $I_{IH}$ | Digital "1" Input Current | $V_{IN} = 2.4V$ | | 0.01 | | | 0.01 | | |
| $V_S$ | Supply Voltage Range | | ±8 | | ±18 | ±8 | | ±18 | V |
| $I_S(+)$ | Positive Supply Current | $V_S \le \pm 18V$ | | 12 | 18 | | 12 | 26 | mA |
| $I_S(-)$ | Negative Supply Current | | | 8 | 12 | | 8 | 14 | |
| $P_D$ | Power Dissipation | $V_S = \pm 15V$ | | 315 | 450 | | 315 | 600 | mW |

## AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| BW | Bandwidth (*Figure 1*) | Small Signal, −3 dB | $A_V = 1$ | | 3250 | | kHz |
| | | | $A_V = 10$ | | 500 | | |
| | | | $A_V = 100$ | | 350 | | |
| | | Small Signal, −1% | $A_V = 1$ | | 300 | | |
| | | | $A_V = 10$ | | 75 | | |
| | | | $A_V = 100$ | | 55 | | |
| PBW | Power Bandwidth | $V_O = \pm 10V$ | | | 200 | | |
| SR | Slew Rate | | | 10 | 13 | | V/μs |
| $t_s$ | Settling Time (*Figure 2*) ±0.1% | $\Delta V_o = \pm 20V$ | $A_V = 1$ | | 2.3 | 3.0 | μs |
| | | | $A_V = 10$ | | 2.7 | 3.5 | |
| | | | $A_V = 100$ | | 3.1 | 4.0 | |
| | Gain Switching Time | | | | 3.5 | | |
| $E_N$ | Equivalent Input Noise Voltage (*Figure 3*) | BW = 0.1 Hz − 10 Hz | $A_V = 100$ | | 7 | | μVp-p |
| | | BW = 10 Hz − 10 kHz | | | 1.4 | | μVrms |
| $I_N$ | Equivalent Input Noise Current (*Figure 3*) | BW = 10 Hz − 10 kHz | | | 30 | | pArms |

**Note 1:** Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

**Note 2:** For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

**Note 3:** These parameters are specified at junction temperature, $T_J$. In normal operation the junction temperature rises above the ambient temperature, $T_A$, as a result of internal power dissipation, $P_D$. $T_J = T_A + \theta_{JA} P_D$ where $\theta_{JA}$ is the thermal resistance from junction to ambient.

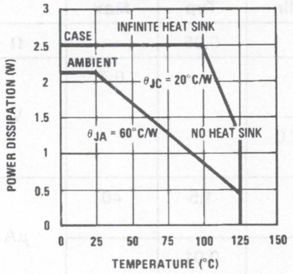
**Note 4:** The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

**Note 5:** See Typical Performance Characteristics for Thermal Resistance Information.

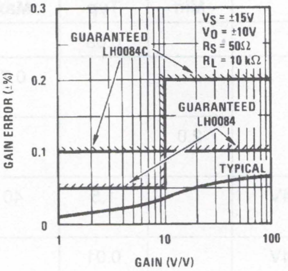
**Note 6:** Refer to RETS0084D for LH0084D military specifications.

## Typical Performance Characteristics

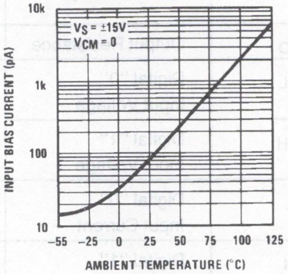
### Power Dissipation



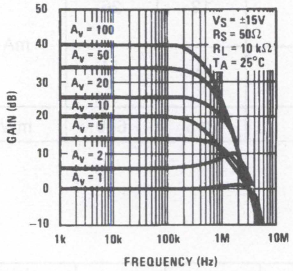
### Gain Accuracy



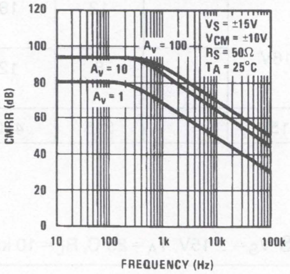
### Input Bias Current



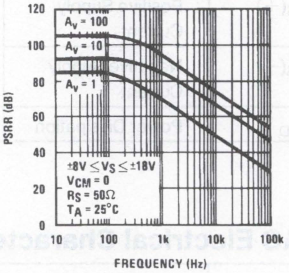
### Small Signal Frequency Response



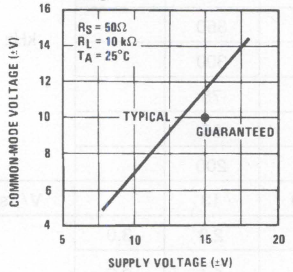
### Common-Mode Rejection



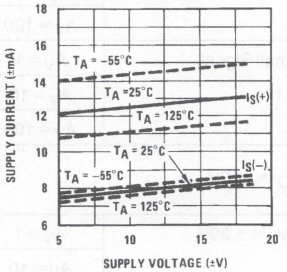
### Power Supply Rejection



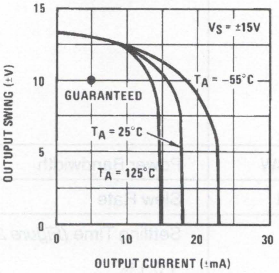
### Input Common-Mode Range



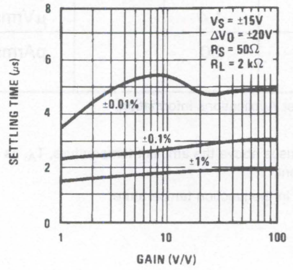
### Supply Current



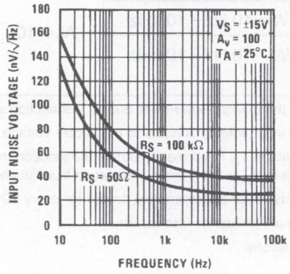
### Output Swing



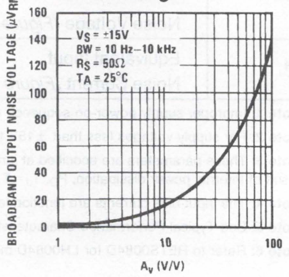
### Settling Time



### Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



### Broadband Output Noise Voltage



TL/H/5651–2

## AC Test Circuits

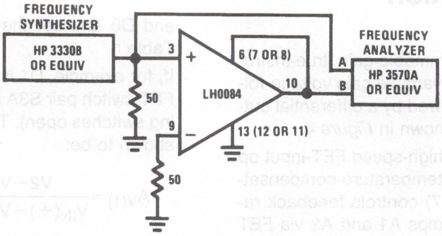

FREQUENCY SYNTHESIZER
HP 3330B OR EQUIV
3
+
50
LH0084
9
−
50
6 (7 OR 8)
10
13 (12 OR 11)
A
B
FREQUENCY ANALYZER
HP 3570A OR EQUIV

**FIGURE 1. Frequency Response Measurement Circuit**

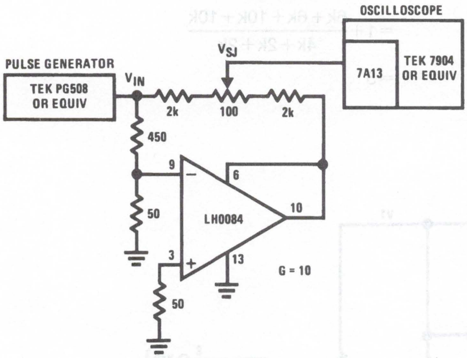
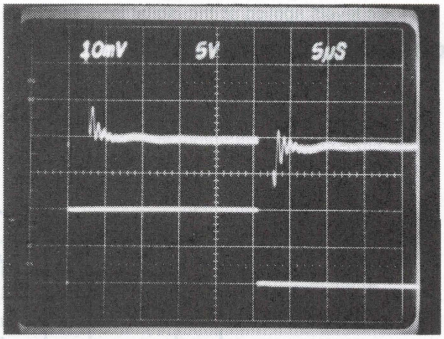

PULSE GENERATOR
TEK PG508 OR EQUIV
$V_{IN}$
2k
100
2k
$V_{SJ}$
OSCILLOSCOPE
7A13
TEK 7904 OR EQUIV
450
9
−
6
50
LH0084
10
3
+
13
G = 10
50

**FIGURE 2. Settling Time Measurement Circuit**

**Settling Time**



$A_V = 10$ Input Stage

TL/H/5651-4

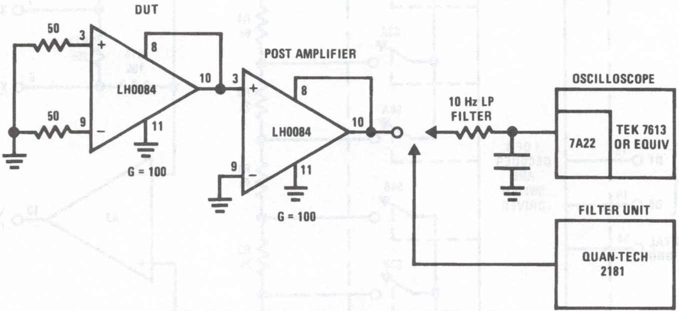
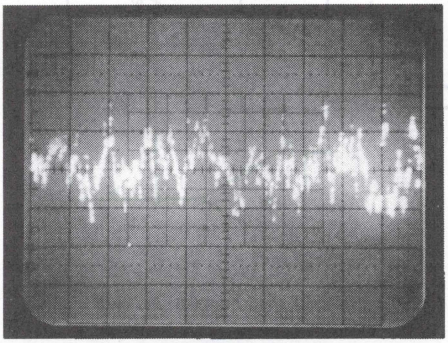

DUT
50
3
+
8
LH0084
10
50
9
−
11
G = 100
POST AMPLIFIER
3
+
8
LH0084
10
9
−
11
G = 100
10 Hz LP FILTER
OSCILLOSCOPE
7A22
TEK 7613 OR EQUIV
FILTER UNIT
QUAN-TECH 2181

**FIGURE 3. Noise Measurement Circuit**

TL/H/5651-3

**Wideband Noise**



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz

1μV/Division Vertical 5 Seconds/Division Horizontal

TL/H/5651-5

## Applications Information

### THEORY OF OPERATION

The LH0084 is a digitally-programmable-gain true-instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4*.

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A–S4A and S1B–S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

If, for example, D1 is High (≥2.0V) and D0 is Low (≤0.7V), FET switch pair S3A and S3B will be closed (and all remaining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

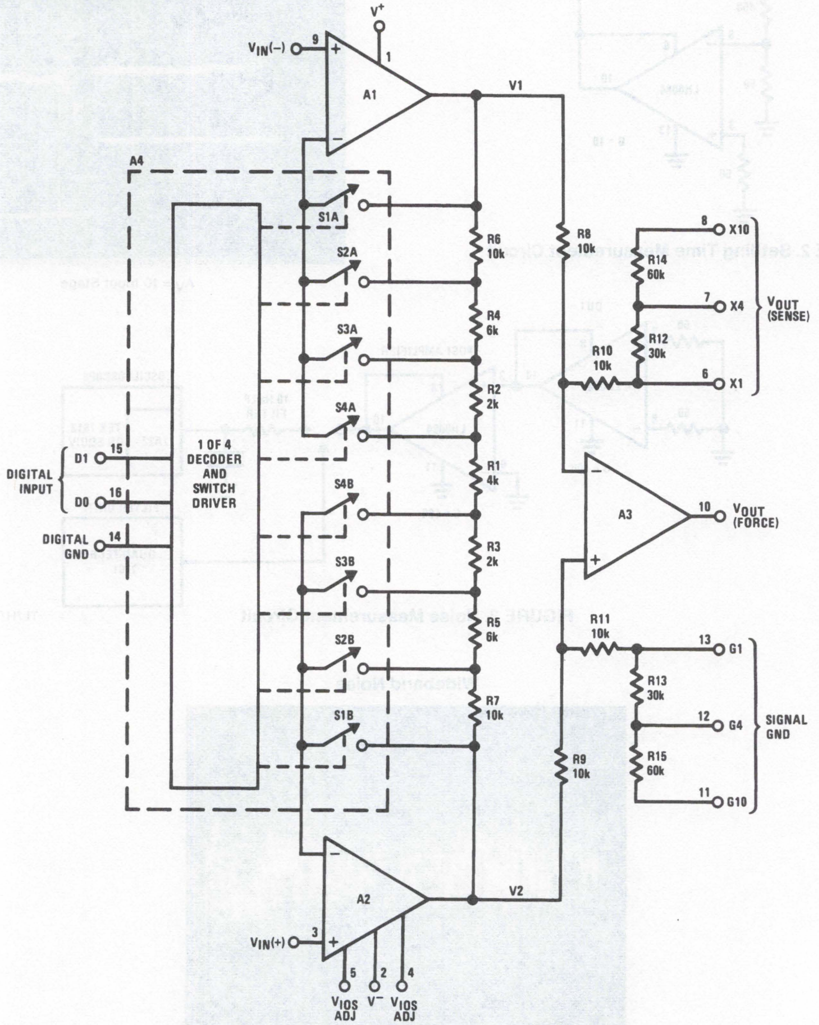
$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3}$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

## Schematic Diagram



V+
1
V_IN(−)
9
A1
V1
A4
S1A
S2A
S3A
S4A
S4B
S3B
S2B
S1B
R6 10k
R4 6k
R2 2k
R1 4k
R3 2k
R5 6k
R7 10k
R8 10k
R14 60k
R12 30k
R10 10k
8
X10
7
X4
6
X1
V_OUT (SENSE)
A3
10
V_OUT (FORCE)
R11 10k
R13 30k
R15 60k
R9 10k
13
G1
12
G4
11
G10
SIGNAL GND
1 OF 4 DECODER AND SWITCH DRIVER
DIGITAL INPUT
D1
15
D0
16
DIGITAL GND
14
A2
V2
V_IN(+)
3
5
2
4
V_IOS ADJ
V−
V_IOS ADJ

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FIGURE 4

## Applications Information (Continued)

**TABLE I. Gain Truth Table and Connection Table**

| Digital Inputs | | 1st Stage Gain $A_{V(1)}$ | Pin Connections | 2nd Stage Gain $A_{V(2)}$ | Overall Gain $A_V$ |
|---|---|---|---|---|---|
| D1 | D0 | | | | |
| 0 | 0 | 1 | 6-10, 13-GND | 1 | 1 |
| 0 | 1 | 2 | | | 2 |
| 1 | 0 | 5 | | | 5 |
| 1 | 1 | 10 | | | 10 |
| 0 | 0 | 1 | 7–10, 12-GND | 4 | 4 |
| 0 | 1 | 2 | | | 8 |
| 1 | 0 | 5 | | | 20 |
| 1 | 1 | 10 | | | 40 |
| 0 | 0 | 1 | 8–10, 11-GND | 10 | 10 |
| 0 | 1 | 2 | | | 20 |
| 1 | 0 | 5 | | | 50 |
| 1 | 1 | 10 | | | 100 |

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10+R12, or R10+R12+R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)}=\frac{V_{OUT}}{V2-V1}$$

$$=\frac{R10+R12}{R8} \tag{2}$$

$$=\frac{10K+30K}{10k}$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11+R13 or R11+R13+R15, must match the feedback resistor used. The overall gain of the LH0084 is therefore:

$$A_V=\frac{V_{OUT}}{V_{IN}(+)-V_{IN}(-)}$$

$$=\frac{V2-V1}{V_{IN}(+)-V_{IN}(-)}\bullet\frac{V_{OUT}}{V2-V1} \tag{3}$$

$$=A_{V(1)}\bullet A_{V(2)}$$

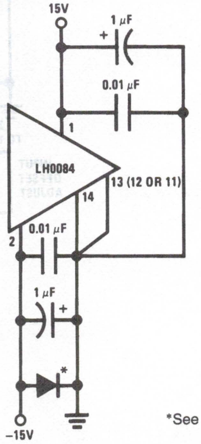
The different gains available are in the range of 1 through 100 and are summarized in Table I.

### POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5.* The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance $V^+$ and $V^-$ should be decoupled with a 0.01 µF ceramic disc in parallel with a 1 µF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together off-board. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the $V^+$ supply is applied prior to the powering on the $V^-$ supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the $V^-$ pin as shown in *Figure 5.*



*See text

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FIGURE 5. Power Supply Connections

## Applications Information (Continued)

### SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6*. To minimize errors, $R_S(+)$, $R_S(-)$ and $R_{CM}$ should be kept as small as possible.

The output connections are also shown in *Figure 6*. The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

### OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset ($V_{IOS}$) be adjusted with a potentiometer as shown in *Figure 7*. The output stage offset ($V_{OOS}$) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7*.

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, $V_{OUT1}$.

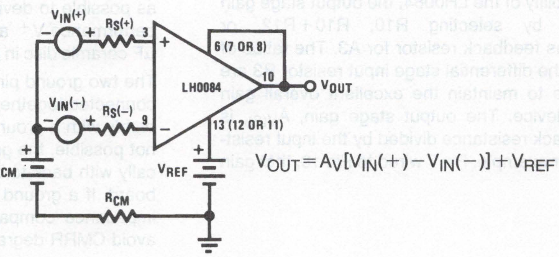
b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, $V_{OUT2}$.

c) Calculate the portion of $V_{OUT2}$ contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \bullet V_{OUT1} - V_{OUT2}) \qquad (4)$$

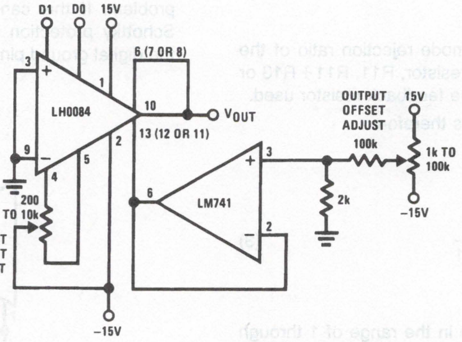
d) While maintaining an input stage gain of 10, adjust the input offset voltage ($V_{IOS}$) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage ($V_{OOS}$) potentiometer until the output voltage is zero.



VIN(+)
RS(+)
3
+
6 (7 OR 8)
10
VOUT
LH0084
VIN(−)
RS(−)
9
−
13 (12 OR 11)
VCM
VREF
RCM
VOUT = AV[VIN(+) − VIN(−)] + VREF

FIGURE 6. Signal Connections



D1
D0
15V
3
+
6 (7 OR 8)
1
LH0084
10
VOUT
13 (12 OR 11)
2
9
−
5
4
200 TO 10k
INPUT OFFSET ADJUST
−15V
6
LM741
3
+
2
−
2k
100k
OUTPUT OFFSET ADJUST
15V
1k TO 100k
−15V

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FIGURE 7. Offset Adjust Circuit

## Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

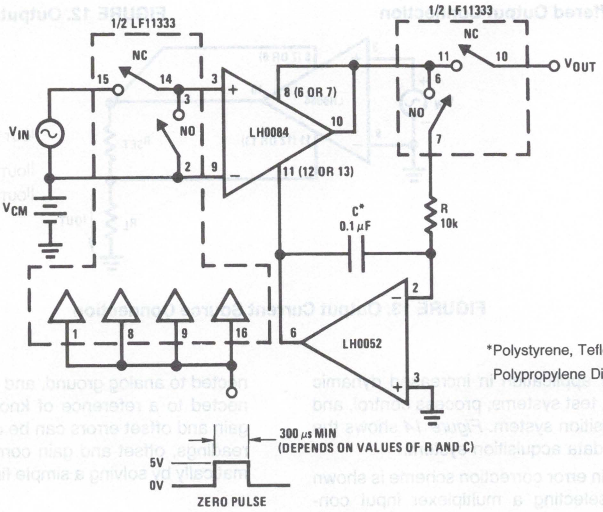
### LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

### REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance *(Figure 10)*.


1/2 LF11333
NC
15
14
3
3
NO
2
9
+
−
LH0084
8 (6 OR 7)
10
11 (12 OR 13)
$V_{IN}$
$V_{CM}$
1
8
9
16
1/2 LF11333
NC
11
10
$V_{OUT}$
6
NO
7
R
10k
C*
0.1 µF
2
6
LH0052
3
+
300 µs MIN
(DEPENDS ON VALUES OF R AND C)
5V
0V
ZERO PULSE

*Polystyrene, Teflon or Polypropylene Dielectric

**FIGURE 8. Auto Zero Circuit**

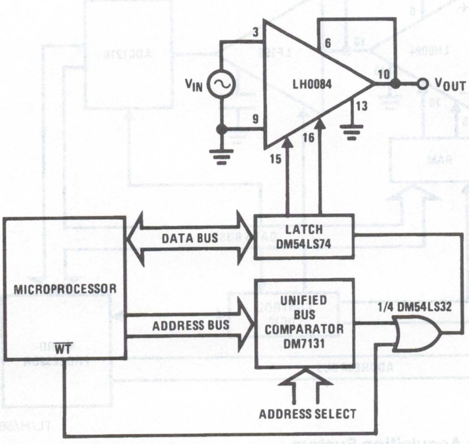
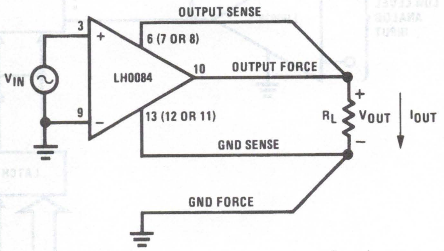

3
6
$V_{IN}$
LH0084
10
$V_{OUT}$
9
13
16
15
LATCH
DM54LS74
DATA BUS
MICROPROCESSOR
WT
ADDRESS BUS
UNIFIED
BUS
COMPARATOR
DM7131
1/4 DM54LS32
ADDRESS SELECT

**FIGURE 9. Typical Microprocessor Interface**


OUTPUT SENSE
3
+
6 (7 OR 8)
LH0084
10
OUTPUT FORCE
$V_{IN}$
9
−
13 (12 OR 11)
+
$R_L$
$V_{OUT}$
$I_{OUT}$
−
GND SENSE
GND FORCE

$|I_{OUT}| \leq 5$ mA

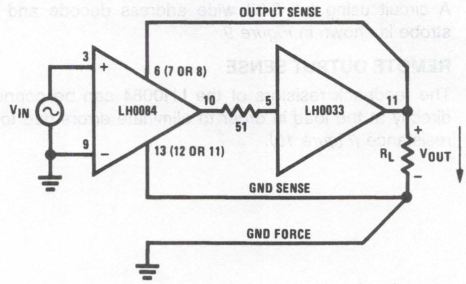
TL/H/5651–9

**FIGURE 10. Remote Sense Connection**

## Applications Information (Continued)

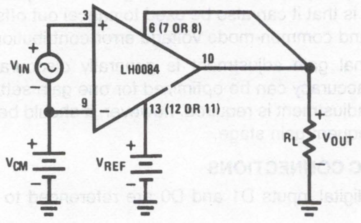
Also, a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11*.

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13*.


OUTPUT SENSE
3
+
6 (7 OR 8)
V_IN
LH0084
10
5
51
LH0033
11
9
−
13 (12 OR 11)
+
R_L
V_OUT
I_OUT
−
GND SENSE
GND FORCE

$|I_{OUT}| \leq 90$ mA

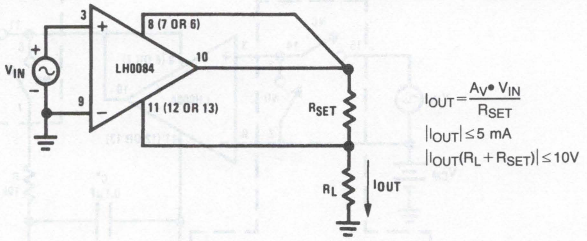
FIGURE 11. Buffered Output Connection


3
+
6 (7 OR 8)
+
V_IN
LH0084
10
9
13 (12 OR 11)
+
V_CM
V_REF
R_L
V_OUT

$V_{OUT} A_V \bullet V_{IN} + V_{REF}$

$|V_{OUT}| \leq 10V$

FIGURE 12. Output Offset Connection


3
+
8 (7 OR 6)
+
V_IN
−
LH0084
10
9
−
11 (12 OR 13)
R_SET
R_L
I_OUT

$$I_{OUT} = \frac{A_V \bullet V_{IN}}{R_{SET}}$$

$|I_{OUT}| \leq 5$ mA

$|I_{OUT}(R_L + R_{SET})| \leq 10V$

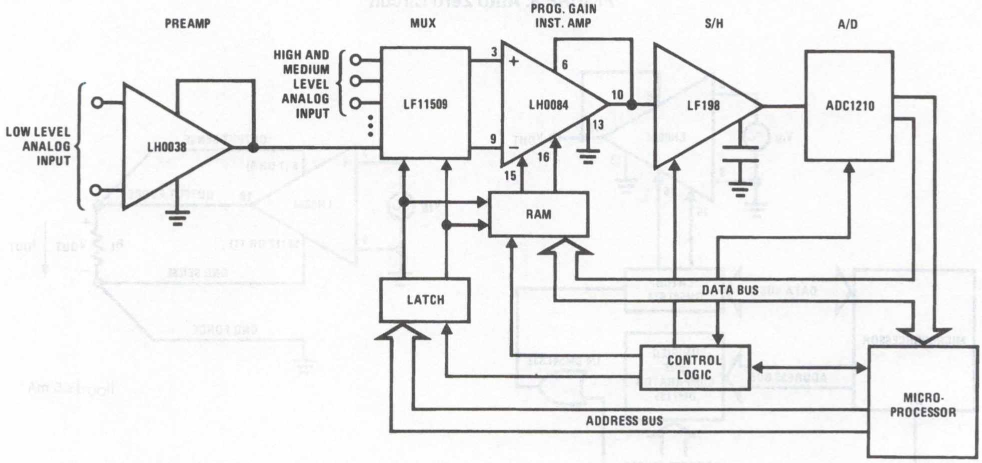
TL/H/5651-10

FIGURE 13. Output Current Source Connection

## Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition system. *Figure 14* shows the device used in a typical data acquisition system.

A software offset and gain error correction scheme is shown in *Figure 15*. By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.


PREAMP
MUX
PROG. GAIN INST. AMP
S/H
A/D
LOW LEVEL ANALOG INPUT
LH0038
HIGH AND MEDIUM LEVEL ANALOG INPUT
LF11509
3
+
9
−
LH0084
6
10
13
16
15
LF198
ADC1210
RAM
LATCH
DATA BUS
CONTROL LOGIC
MICRO-PROCESSOR
ADDRESS BUS

TL/H/5651-11

FIGURE 14. Typical Data Acquisition System

## Applications (Continued)

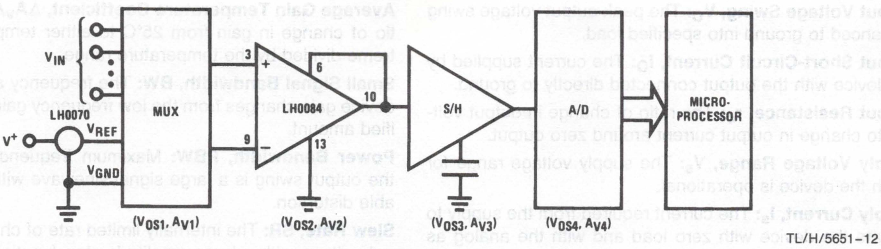


**FIGURE 15. Software System Offset and Gain Calibration Circuit**

## Definition of Terms

**Input Offset Voltage, $V_{IOS}$:** The voltage which must be applied to the inputs to force the output of the input stage to 0V. $V_{IOS}$ can be calculated by measuring $V_{OS}$ (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS} = \frac{1}{9}\left(V_{OS}|_{A_V=10} - V_{OS}|_{A_V=1}\right)$$

where:

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

**Input Offset Current, $I_{OS}$:** The difference in the currents into the 2 analog input terminals at 0V.

**Input Bias Current, $I_B$:** The average of the currents into the 2 analog input terminals at 0V.

**Input Resistance, $R_{IN}$:** Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

**Input Voltage Range, $V_{IN}$:** The voltage range for which the device is operational.

**Common-Mode Rejection Ratio, CMRR:** The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

**Power Supply Rejection Ratio, PSRR:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

**Voltage Gain, $A_V$:** The ratio of output voltage change to the input voltage change producing it.

**Gain Error:** The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

**Gain Non-Linearity:** The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

**Output Stage Offset Voltage, $V_{OOS}$:** The voltage which must be applied to the input of the output stage for the output to be forced to 0V. $V_{OOS}$ can be calculated by measuring $V_{OS}$ (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS} = \frac{1}{9}\left(10 \bullet V_{OS}|_{A_V=1} - V_{OS}|_{A_V=10}\right)$$

where:

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V = 1$

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V = 10$

**Offset Voltage (Referred to Output), $V_{OS(RTO)}$:** The output voltage when both inputs are connected to 0V. $V_{OS}$ is composed of input offset voltage, $V_{IOS}$, and output offset voltage, $V_{OOS}$, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)} = A_{V(2)}(A_{V(1)}\ V_{IOS} + V_{OOS})$$

where:

$V_{IOS}$ = Input offset voltage

$V_{OOS}$ = Output stage offset voltage

$A_{V(1)}$ = Input state gain

$A_{V(2)}$ = Output stage gain

## Definition of Terms (Continued)

**Output Voltage Swing, $V_O$:** The peak output voltage swing referenced to ground into specified load.

**Output Short-Circuit Current, $I_O$:** The current supplied by the device with the output connected directly to ground.

**Output Resistance, $r_O$:** The ratio of change in output voltage to change in output current around zero output.

**Supply Voltage Range, $V_S$:** The supply voltage range for which the device is operational.

**Supply Current, $I_S$:** The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

**Power Dissipation, $P_D$:** The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

**Digital "1" Input Voltage, $V_{IH}$:** Minimum voltage required at the digital input to guarantee a high logic state.

**Digital "0" Input Voltage, $V_{IL}$:** Maximum voltage required at the digital input to guarantee a low logic state.

**Digital "1" Input Current, $I_{IH}$:** The current into a digital input at specified logic level.

**Digital "0" Input Current, $I_{IL}$:** The current into a digital input at specified logic level.

**Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

**Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$:** The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

**Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$:** The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

**Small Signal Bandwidth, BW:** The frequency at which the device gain changes from the low frequency gain by a specified amount.

**Power Bandwidth, PBW:** Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

**Slew Rate, SR:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

**Settling Time, $t_s$:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

**Gain Switching Time:** The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

**Equivalent Input Noise Voltage, $E_N$:** The rms of peak noise voltage referred to the input (RTI) over a specified frequency band.

**Equivalent Input Noise Current, $I_N$:** The rms of peak noise current referred to the input (RTI) over a specified frequency band.

National
Semiconductor
Corporation

# LM221/LM321/LM321A Precision Preamplifiers

## General Description

The LM121 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM121 decreases the closed loop gain error.

The LM121 series operates with supply voltages from ±3V to ±20V and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from 5 μA to 200 μA so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

The extremely low drift of the LM121 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with the LM121. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM121 allows tailoring the input characteristics to match those of specialized op amps.

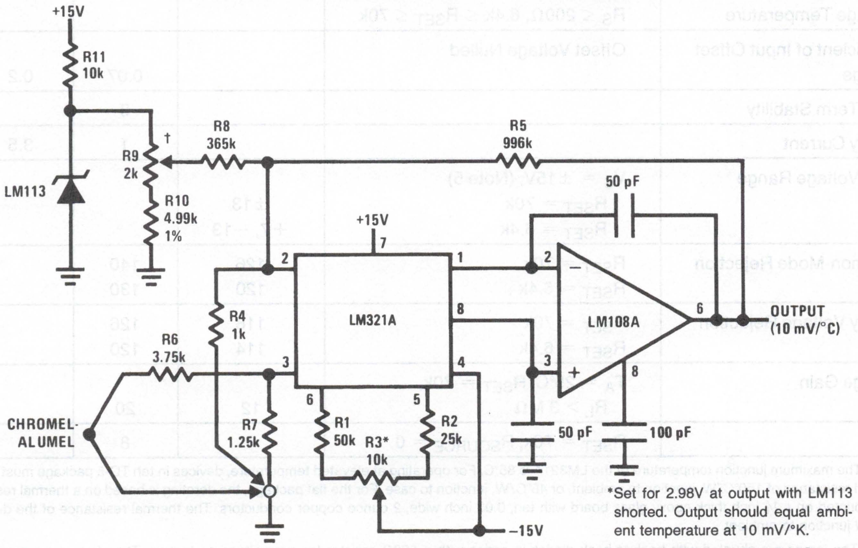
The LM221 is specified over a −25°C to +85°C range and the LM321 over a 0°C to +70°C temperature range.

## Features

- Guaranteed drift of LM321A—0.2 μV/°C
- Guaranteed drift of LM221 series—1 μV/°C
- Offset voltage less than 0.4 mV
- Bias current less than 10 nA at 10 μA operating current
- CMRR 126 dB minimum
- 120 dB supply rejection
- Easily nulled offset voltage

## Typical Applications

**Thermocouple Amplifier with Cold Junction Compensation**



*Set for 2.98V at output with LM113 shorted. Output should equal ambient temperature at 10 mV/°K.

†Adjust for output reading in °C.

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## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Voltage (Notes 2 and 3) | ±15V |
| Input Voltage (Note 3) | ±15V |
| Operating Temperature Range | |
| LM321A | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## Electrical Characteristics (Note 4) LM321A

| Parameter | Conditions | LM321A Min | LM321A Typ | LM321A Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$, $6.4k \le R_{SET} \le 70k$ | | 0.2 | 0.4 | mV |
| Input Offset Current | $T_A = 25°C$, | | | | |
| | $R_{SET} = 70k$ | | 0.3 | 0.5 | nA |
| | $R_{SET} = 6.4k$ | | | 5 | nA |
| Input Bias Current | $T_A = 25°C$, | | | | |
| | $R_{SET} = 70k$ | | 5 | 15 | nA |
| | $R_{SET} = 6.4k$ | | 50 | 150 | nA |
| Input Resistance | $T_A = 25°C$, | | | | |
| | $R_{SET} = 70k$ | 2 | 8 | | MΩ |
| | $R_{SET} = 6.4k$ | 0.2 | | | MΩ |
| Supply Current | $T_A = 25°C$, $R_{SET} = 70k$ | | 0.8 | 2.2 | mA |
| Input Offset Voltage | $6.4k \le R_{SET} \le 70k$ | | 0.5 | 0.65 | mV |
| Input Bias Current | $R_{SET} = 70k$ | | 15 | 25 | nA |
| | $R_{SET} = 6.4k$ | | 150 | 250 | nA |
| Input Offset Current | $R_{SET} = 70k$ | | 0.5 | 1 | nA |
| | $R_{SET} = 6.4k$ | | 5 | 10 | nA |
| Input Offset Current Drift | $R_{SET} = 70k$ | | 3 | | pA/°C |
| Average Temperature | $R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$ | | | | |
| Coefficient of Input Offset Voltage | Offset Voltage Nulled | | 0.07 | 0.2 | μV/°C |
| Long Term Stability | | | 3 | | μV/yr |
| Supply Current | | | 1 | 3.5 | mA |
| Input Voltage Range | $V_S = \pm 15V$, (Note 5) | | | | |
| | $R_{SET} = 70k$ | ±13 | | | V |
| | $R_{SET} = 6.4k$ | +7, −13 | | | V |
| Common-Mode Rejection Ratio | $R_{SET} = 70k$ | 126 | 140 | | dB |
| | $R_{SET} = 6.4k$ | 120 | 130 | | dB |
| Supply Voltage Rejection Ratio | $R_{SET} = 70k$ | 118 | 126 | | dB |
| | $R_{SET} = 6.4k$ | 114 | 120 | | dB |
| Voltage Gain | $T_A = 25°C$, $R_{SET} = 70k$, $R_L > 3\ M\Omega$ | 12 | 20 | | V/V |
| Noise | $R_{SET} = 70k$, $R_{SOURCE} = 0$ | | 8 | | $nV/\sqrt{Hz}$ |

**Note 1:** The maximum junction temperature of the LM321A is 85°C. For operating at elevated temperature, devices in teh TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185° C/W when mounted on a ⅙ inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

**Note 2:** The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221A, however all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321A the specifications apply over a 0°C to +70°C temperature range.

**Note 5:** External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Voltage (Notes 2 and 3) | ±15V |
| Input Voltage (Note 3) | ±15V |
| Operating Temperature Range | |
| LM221 | −25°C to +85°C |
| LM321, LM321A | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| ESD rating to be determined. | |

## Electrical Characteristics (Note 4) LM221, LM321

| Parameter | Conditions | LM221 | | | LM321 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25°C$, $6.4k \le R_{SET} \le 70k$ | | | 0.7 | | | 1.5 | mV |
| Input Offset Current | $T_A = 25°C$,<br>$R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | | | <br>1<br>10 | | | <br>2<br>20 | <br>nA<br>nA |
| Input Bias Current | $T_A = 25°C$,<br>$R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | | | <br>10<br>100 | | | <br>18<br>180 | <br>nA<br>nA |
| Input Resistance | $T_A = 25°C$,<br>$R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | <br>4<br>0.4 | | | <br>2<br>0.2 | | | <br>MΩ<br>MΩ |
| Supply Current | $T_A = 25°C$, $R_{SET} = 70k$ | | | 1.5 | | | 2.2 | mA |
| Input Offset Voltage | $6.4k \le R_{SET} \le 70k$ | | | 1.0 | | | 2.5 | mV |
| Input Bias Current | $R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | | | 30<br>300 | | | 28<br>280 | nA<br>nA |
| Input Offset Current | $R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | | | 3<br>30 | | | 4<br>40 | nA<br>nA |
| Input Offset Current Drift | $R_{SET} = 70k$ | | 3 | | | 3 | | pA/°C |
| Average Temperature Coefficient of Input Offset Voltage | $R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$<br>Offset Voltage Nulled | | | 1 | | | 1 | μV/°C |
| Long Term Stability | | | 5 | | | 5 | | μV/yr |
| Supply Current | | | | 2.5 | | | 3.5 | mA |
| Input Voltage Range | $V_S = \pm 15V$, (Note 5)<br>$R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | <br>±13<br>+7, −13 | | | <br>±13<br>+7, −13 | | | <br>V<br>V |
| Common-Mode Rejection Ratio | $R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | 120<br>114 | | | 114<br>114 | | | dB<br>dB |
| Supply Voltage Rejection Ratio | $R_{SET} = 70k$<br>$R_{SET} = 6.4k$ | 120<br>114 | | | 114<br>114 | | | dB<br>dB |
| Voltage Gain | $T_A = 25°C$, $R_{SET} = 70k$,<br>$R_L > 3 M\Omega$ | 16 | | | 12 | | | V/V |
| Noise | $R_{SET} = 70k$, $R_{SOURCE} = 0$ | | 8 | | | 8 | | $nV/\sqrt{Hz}$ |

**Note 1:** The maximum junction temperature of the LM221 is 100°C. The maximum junction temperature of the LM321 is 85°C. For operating at elevated temperature, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185° C/W when mounted on a ⅛ inch thick epoxy glass board with ten, 0.03 inch wide, 2 ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

**Note 2:** The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221, however all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321 the specifications apply over a 0°C to +70°C temperature range.

**Note 5:** External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

## Frequency Compensation

### UNIVERSAL COMPENSATION

The additional gain of the LM321 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM321 is less than the gain of the LM321 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM321 is high. When high closed loop gains are used—for example $A_V = 1000$—and only an addition gain of 200 is inserted by the LM321, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. *Figure 1* shows the basic configuration of frequency stabilizing network. In operation the output of the LM321 is rendered single ended by a 0.01 μF bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

$$C = \frac{4}{10^6\, A_{CL}\, R_{SET}}$$

### ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capscitor is:

$$C = \frac{8}{10^6\, A_{CL}\, R_{SET}}$$

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

**TABLE I**

| Closed Loop Gain | Current Set Resistor | | | | |
|---|---|---|---|---|---|
| | 120 kΩ | 60 kΩ | 30 kΩ | 12 kΩ | 6 kΩ |
| $A_V = 1$ | 68 | 130 | 270 | 680 | 1300 |
| $A_V = 5$ | 15 | 27 | 56 | 130 | 270 |
| $A_V = 10$ | 10 | 15 | 27 | 68 | 130 |
| $A_V = 50$ | 1 | 3 | 5 | 15 | 27 |
| $A_V = 100$ | – | 1 | 3 | 5 | 10 |
| $A_V = 500$ | – | – | 1 | 1 | 3 |
| $A_V = 1000$ | – | – | – | – | – |

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

### DESIGN EQUATIONS FOR THE LM321 SERIES

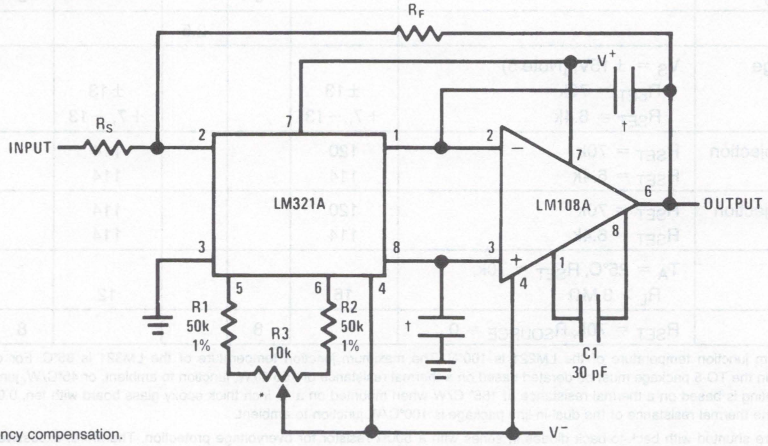
$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{SET}}$$

Null Pot Value should be 10% of $R_{SET}$

$$\text{Operating Current} \approx \frac{2 \times 0.65\text{V}}{R_{SET}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65\text{V} \times 50\text{k}}{R_{SET}}\right]$$

## Typical Applications



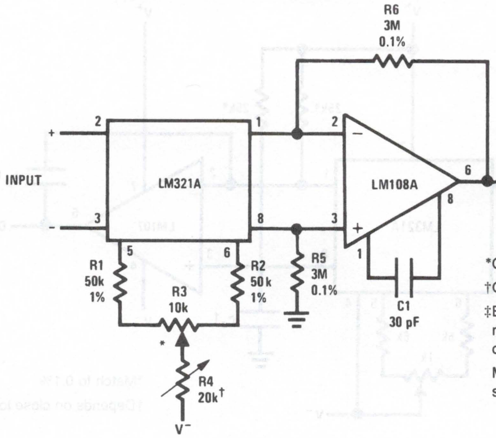
*Offset adjust.

†See table for frequency compensation.

FIGURE 1. Low Drift Op Amp Using the LM321A as a Preamp

## Typical Applications (Continued)

### Gain of 1000 Instrumentation Amplifier‡


R6
3M
0.1%
+
INPUT
−
2
3
LM321A
1
8
5
6
R1
50k
1%
R2
50 k
1%
R3
10k
*
R4
20k†
V−
2
3
−
+
LM108A
6
8
1
OUTPUT
R5
3M
0.1%
C1
30 pF

*Offset adjust

†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical +2% from −55 to +125°C.

Match of R5 and R6 effect power supply rejection

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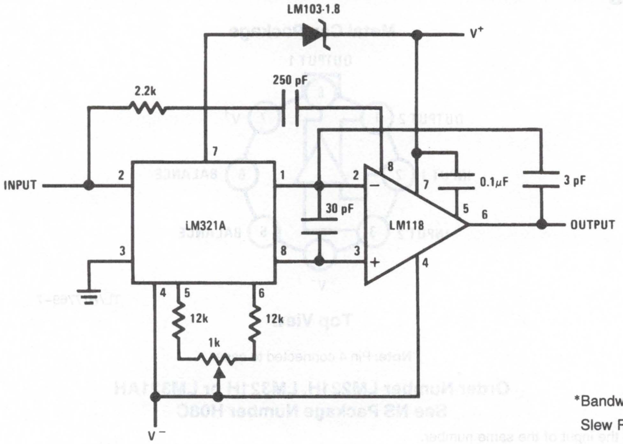
### High Speed* Inverting Amplifier with Low Drift


LM103-1.8
V+
250 pF
2.2k
INPUT
2
3
7
LM321A
1
8
4
5
6
12k
12k
1k
V−
30 pF
2
3
8
7
5
6
4
−
+
LM118
0.1μF
3 pF
OUTPUT

*Bandwidth = 10 MHz

Slew Rate = 40 V/μs

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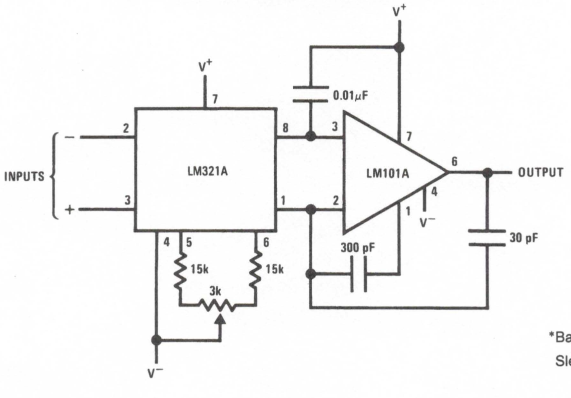
### Medium Speed* General Purpose Amplifier


V+
V+
7
0.01μF
INPUTS
−
+
2
3
LM321A
8
1
4
5
6
15k
15k
3k
V−
3
2
7
6
4
1
LM101A
V−
OUTPUT
300 pF
30 pF

*Bandwidth = 3.5 MHz

Slew Rate = 1.1 V/μs

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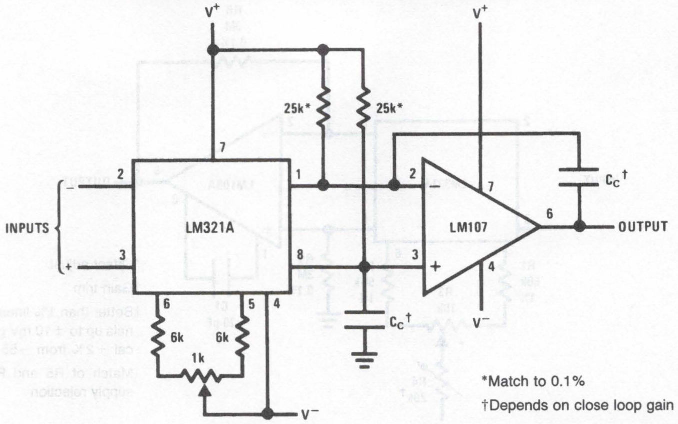
## Typical Applications (Continued)

### Increased Common-Mode Range at High Operating Currents


V+
V+
25k*
25k*
7
2
1
2
7
Cc†
INPUTS
−
+
LM321A
LM107
6
OUTPUT
3
8
3
4
6
5
4
6k
6k
1k
Cc†
V−
V−

*Match to 0.1%

†Depends on close loop gain

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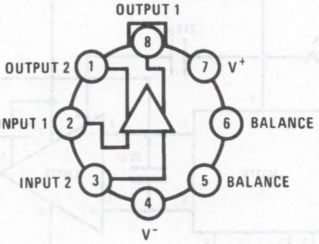
## Connection Diagram

### Metal Can Package


OUTPUT 1
8
OUTPUT 2
1
7
V+
INPUT 1
2
6
BALANCE
INPUT 2
3
5
BALANCE
4
V−

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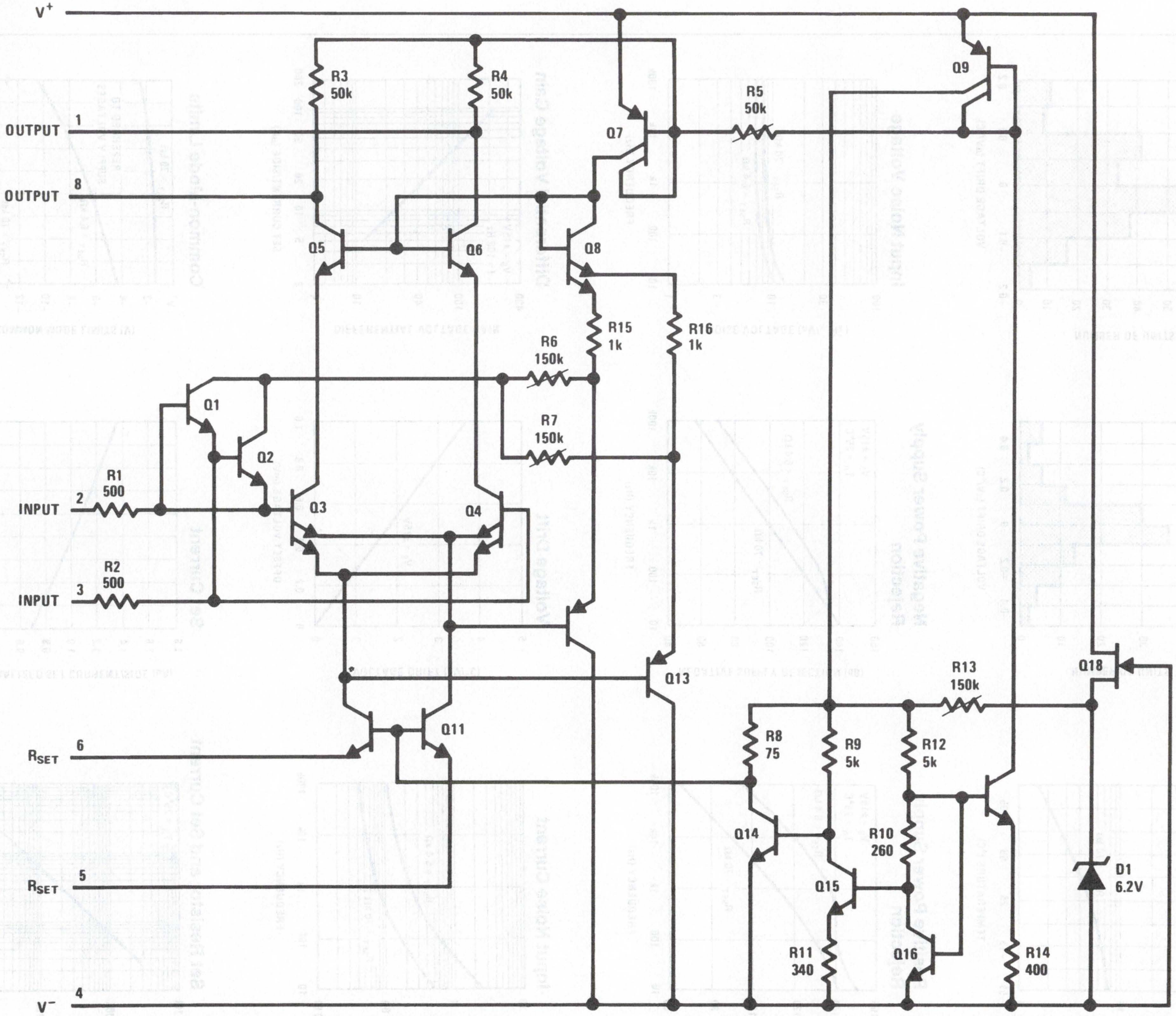
**Top View**

**Note:** Pin 4 connected to case.

**Order Number LM221H, LM321H or LM321AH**
**See NS Package Number H08C**

**Note:** Outputs are inverting from the input of the same number.

## Schematic Diagram*


V+
OUTPUT 1
OUTPUT 8
INPUT 2
INPUT 3
R_SET 6
R_SET 5
V− 4
R1 500
R2 500
R3 50k
R4 50k
R5 50k
R6 150k
R7 150k
R8 75
R9 5k
R10 260
R11 340
R12 5k
R13 150k
R14 400
R15 1k
R16 1k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q11
Q13
Q14
Q15
Q16
Q18
D1 6.2V

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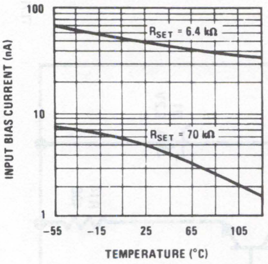
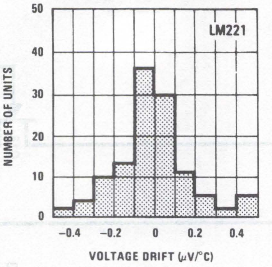
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

# Typical Performance Characteristics

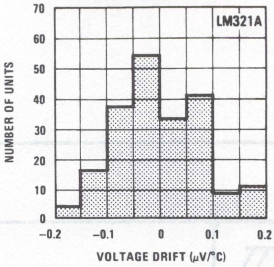
### Input Bias Current



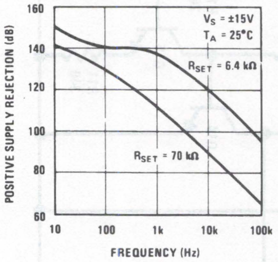
### Distribution of Offset Voltage Drift (Nulled)



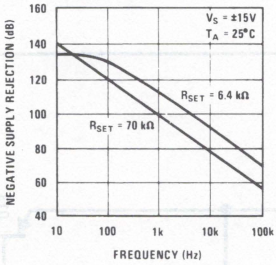
### Distribution of Offset Voltage Drift (Nulled)



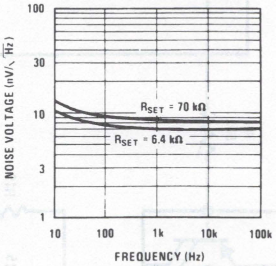
### Positive Power Supply Rejection



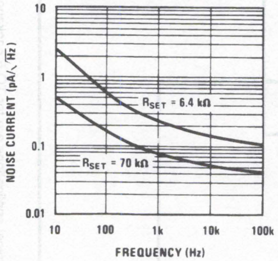
### Negative Power Supply Rejection



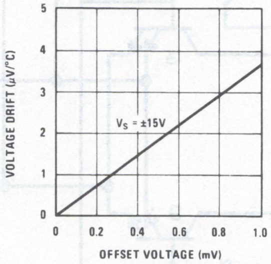
### Input Noise Voltage



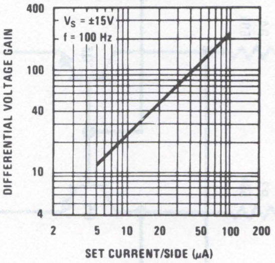
### Input Noise Current



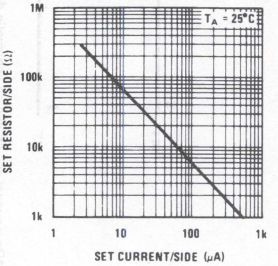
### Voltage Drift



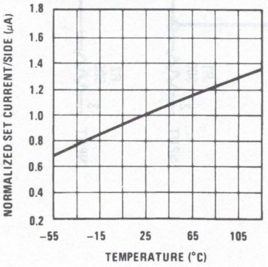
### Differential Voltage Gain



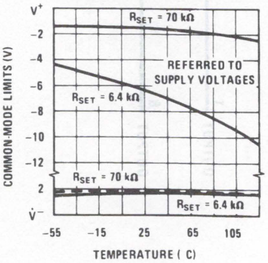
### Set Resistor and Set Current



### Set Current



### Common-Mode Limits



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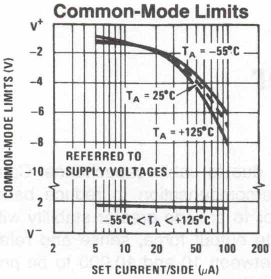
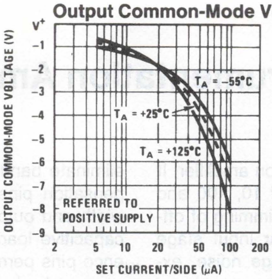
## Typical Performance Characteristics (Continued)

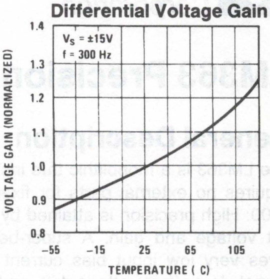
### Common-Mode Limits



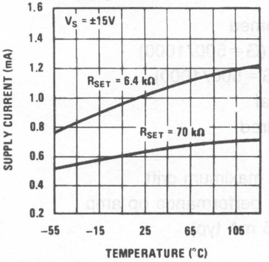
### Output Common-Mode Voltage



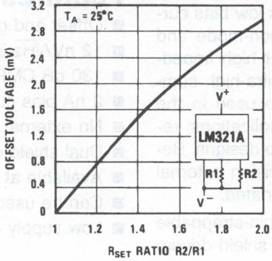
### Differential Voltage Gain



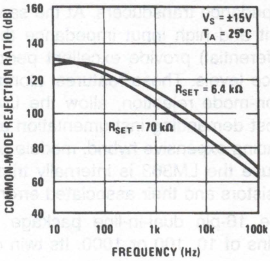
### Supply Current



### Offset Voltage Adjustment



### Common-Mode Rejection Ratio



TL/H/7769-10

National
Semiconductor
Corporation

# LM363 Precision Instrumentation Amplifier

## General Description

The LM363 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1000. High precision is attained by on-chip trimming of offset voltage and gain. A super-beta biopolar input stage gives very low input bias current and voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains. The LM363 operates with supply voltages from ±5V to ±18V with only 1.5 mA current drain.

The LM363's low voltage noise, low offset voltage and offset voltage drift make it ideal for amplifying low-level, low-impedance transducers. At the same time, its low bias current and high input impedance (both common-mode and differential) provide excellent performance at high impedance levels. These features, along with its ultra-high common-mode rejection, allow the LM363 to be used in the most demanding instrumentation amplifier applications, replacing expensive hybrid, module or multi-chip designs. Because the LM363 is internally trimmed, precision external resistors and their associated errors are eliminated.

The 16-pin dual-in-line package provides pin-strappable gains of 10, 100 or 1000. Its twin differential shield drivers eliminate bandwidth loss due to cable capacitance. Compensation pins allow overcompensation to reduce bandwidth and output noise, or to provide greater stability with capacitive loads. Separate output force, sense and reference pins permit gains between 10 and 10,000 to be programmed using external resistors.

On the 8-pin TO-5 package, gain is internally set at 10, 100 or 500 but may be increased with external resistors. The shield driver and offset adjust pins are omitted on the 8-pin versions.

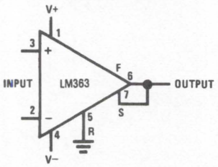
The LM363 is rated for 0°C to 70°C.

## Features

- Offset and gain pretrimmed
- 12 nV/$\sqrt{\text{Hz}}$ input noise (G = 500/1000)
- 130 dB CMRR tyical (G = 500/1000)
- 2 nA bias current typical
- No external parts required
- Dual shield drivers
- Available at 0.5 μV/°C maximum drift
- Can be used as a high performance op amp
- Low supply current (1.5 mA typ)

## Typical Connections

**8-Pin Package**



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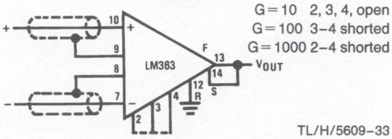
**16-Pin Package**



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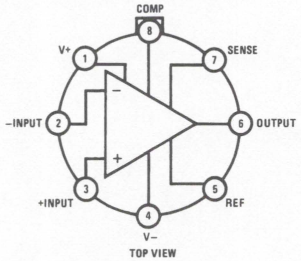
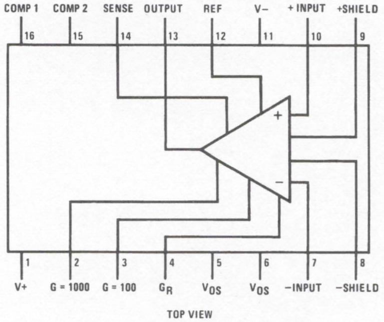
## Connection Diagrams

**Metal Can Package**



**Order Number LM363H-10, LM363H-100 or LM363H-500**
**See NS Package Number H08C**

**16-Pin Dual-In-Line Package**



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**Order Number 363D**
**See NS Package Number D16C**

## Absolute Maximum Ratings (Notes 3 and 9)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±10V |
| Input Current | ±20 mA |
| Input Voltage | Equal to Supply Voltage |
| Reference and Sense Voltage | ±25V |
| Lead Temp. (Soldering, 10 sec.) | 300°C |

ESD rating to be determined.

## LM363 Electrical Characteristics (Notes 5 and 6)

| Parameter | Conditions | LM363 | | | Units |
|---|---|---|---|---|---|
| | | Typ | Tested Limit (Note 7) | Design Limit (Note 8) | |
| **FIXED GAIN (8-PIN)** | | | | | |
| Input Offset Voltage | G=500 | 30 | 100 | **300** | μV |
| | G=100 | 50 | 200 | **600** | μV |
| | G=10 | 0.5 | 2.0 | **5** | mV |
| Input Offset Voltage Drift | G=500 | 1 | | **4** | μV/°C |
| | G=100 | 2 | | **8** | μV/°C |
| | G=10 | 20 | | **75** | μV/°C |
| Gain Error (±10V Swing, 2 kΩ Load) | G=500 | 0.1 | 0.5 | **0.8** | % |
| | G=100 | 0.05 | 0.5 | **0.7** | % |
| | G=10 | 0.05 | 0.5 | **0.6** | % |
| **PROGRAMMABLE GAIN (16-PIN)** | | | | | |
| Input Offset Voltage | G=1000 | 50 | 200 | **400** | μV |
| | G=100 | 100 | 400 | **800** | μV |
| | G=10 | 1 | 3 | **7** | mV |
| Input Offset Voltage Drift | G=1000 | 1 | | **5** | μV/°C |
| | G=100 | 2 | | **10** | μV/°C |
| | G=10 | 10 | | **100** | μV/°C |
| Gain Error (±10V Swing, 2 kΩ Load) | G=1000 | 2.0 | 2.5 | **3.0** | % |
| | G=100 | 0.1 | 0.5 | **0.7** | % |
| | G=10 | 0.6 | 1.5 | **1.7** | % |
| **FIXED GAIN AND PROGRAMMABLE** | | | | | |
| Gain Temperature Coefficient | G=1000 | 40 | | | ppm/°C |
| | G=500 | 20 | | | ppm/°C |
| | G=100, 10 | 10 | | | ppm/°C |
| Gain Non-Linearity (±10V Swing, 2 kΩ Load) | G=10, 100 | 0.01 | 0.03 | **0.04** | % |
| | G=500, 1000 | 0.01 | 0.05 | **0.06** | % |

## LM363 Electrical Characteristics (Continued) (Notes 5 and 6)

| Parameter | Conditions | LM363 | | | Units |
|---|---|---|---|---|---|
| | | Typ | Tested Limit (Note 7) | Design Limit (Note 8) | |
| Common-Mode Rejection Ratio ($-11V \leq V_{CM} \leq 13V$) | G = 1000, 500 | 130 | 114 | **104** | dB |
| | G = 100 | 120 | 94 | **84** | dB |
| | G = 10 | 105 | 90 | **80** | dB |
| Positive Supply Rejection Ratio (5V to 15V) | G = 1000, 500 | 130 | 110 | **100** | dB |
| | G = 100 | 120 | 100 | **95** | dB |
| | G = 10 | 100 | 85 | **78** | dB |
| Negative Supply Rejection Ratio (−5V to −15V) | G = 1000, 500 | 120 | 100 | **90** | dB |
| | G = 100 | 106 | 85 | **75** | dB |
| | G = 10 | 86 | 70 | **60** | dB |
| Input Bias Current | | 2 | 10 | **20** | nA |
| Input Offset Current | | 1 | 3 | **5** | nA |
| Common-Mode Input Resistance | | 100 | 8 | | GΩ |
| Differential Mode Input Resistance | G = 1000, 500 | 0.2 | | | GΩ |
| | G = 100 | 2 | | | GΩ |
| | G = 10 | 20 | | | GΩ |
| Input Offset Current Change | $-11V \leq V_{CM} \leq 13V$ | 20 | 100 | **300** | pa/V |
| Reference and Sense Resistance | | 50 | | | kΩ |
| | Min | | 30 | **27** | kΩ |
| | Max | | 80 | **83** | kΩ |
| Open Loop Gain | $G_{CL}$ = 1000, 500 | 10 | 1 | | V/μV |
| Supply Current | Positive | 1.2 | 2.4 | **3.0** | mA |
| | | | | 2.8 | mA |
| | Negative | 1.6 | 2.8 | **3.4** | mA |

**Note 1:** These conditions apply unless otherwise noted; $V^+ = V^- = 15V$, $V_{CM} = 0V$, $R_L = 2$ kΩ, reference pin grounded, sense pin connected to output and $T_j = 25°C$.

**Note 2: Boldface limits are guaranteed over full temperature range.** Operating ambient temperature range is 0°C to 70°C for the LM363.

**Note 3:** Guaranteed and 100% production tested.

**Note 4:** Guaranteed but not 100% tested. These limits are not used in determining outgoing quality levels.

**Note 5:** Maximum rated junction temperature is 100°C for the LM363. Thermal resistance, junction to ambient, is 150°C/W for the TO-99(H) package and 100°C/W for the ceramic DIP (D).

## Typical Performance Characteristics $T_A = 25^\circ C$

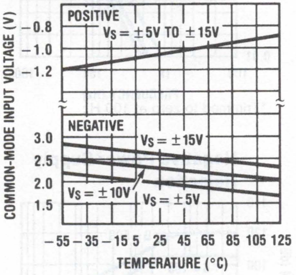
| Parameter | Fixed Gain and Programmable | | | Units |
|---|---|---|---|---|
| | 1000/500 | 100 | 10 | |
| Input Voltage Noise, rms, 1 kHz | 12 | 18 | 90 | nV/√Hz |
| Input Voltage Noise (Note 6) | 0.4 | 1.5 | 10 | μVp-p |
| Input Current Noise, rms, 1 kHz | 0.2 | 0.2 | 0.2 | pA/√Hz |
| Input Current Noise (Note 6) | 40 | 40 | 40 | pAp-p |
| Bandwidth | 30 | 100 | 200 | kHz |
| Slew Rate | 1 | 0.36 | 0.24 | V/μS |
| Settling Time, 0.1% of 10V | 70 | 25 | 20 | μS |
| Offset Voltage Warm-Up Drift (Note 7) | 5 | 15 | 50 | μV |
| Offset Voltage Stability (Note 8) | 5 | 10 | 100 | μV |
| Gain Stability (Note 8) | 0.01 | 0.005 | 0.05 | % |

**Note 6:** Measured for 100 seconds in a 0.01 Hz to 10 Hz bandwidth.

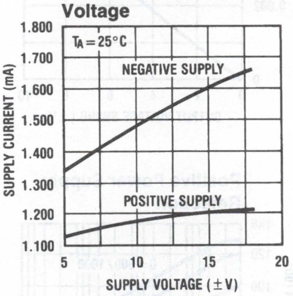
**Note 7:** Measured for 5 minutes in still air, $V^+ = V^- = -15V$. Warm-up drift is proportionally reduced at lower supply voltages.

**Note 8:** Change in 1000 hours of operation at 125°C ambient.

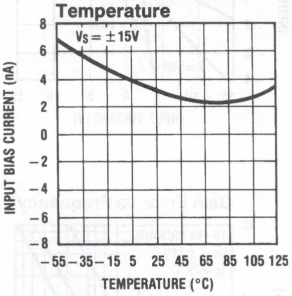
**Common-Mode Input Voltage Limit**



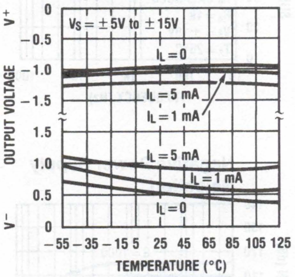
**Supply Current vs Supply Voltage**



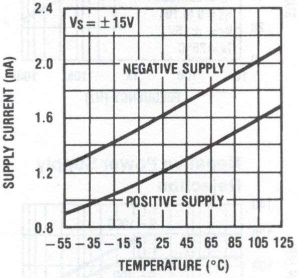
**Input Bias Current vs Temperature**



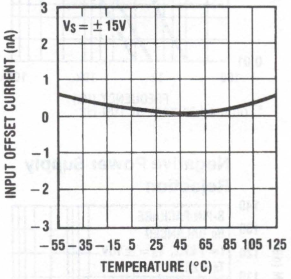
**Output Swing Referred to Supplies**



**Supply Current vs Temperature**



**Input Offset Current vs Temperature**



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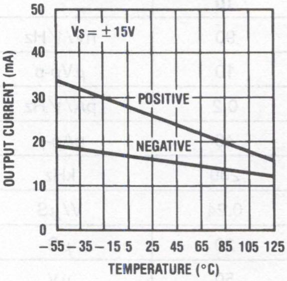
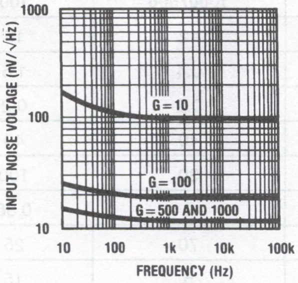
## Typical Performance Characteristics (Continued)

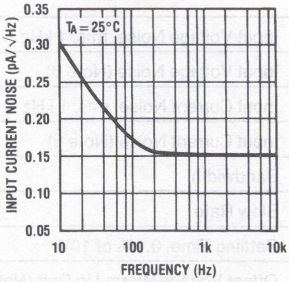
**Output Current Limit**



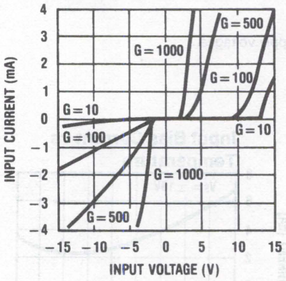
**Input Noise Voltage**



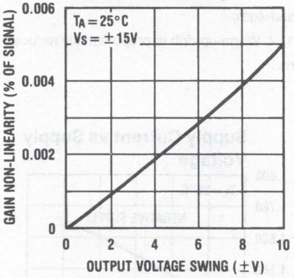
**Input Current Noise**



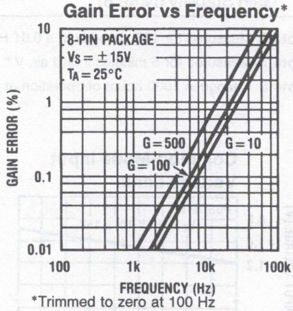
**Input Current vs Voltage Overdrive**



**Gain Non-Linearity**

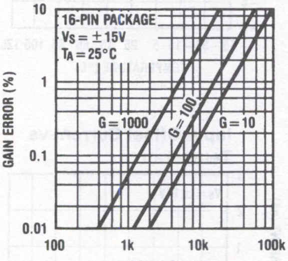


**Gain Error vs Frequency***



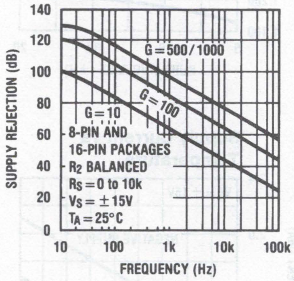
*Trimmed to zero at 100 Hz

**Gain Error vs Frequency***

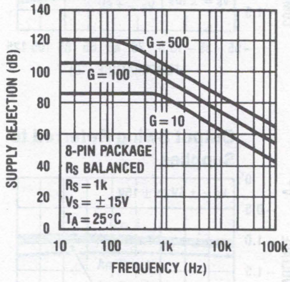


*Trimmed to zero at 100 Hz

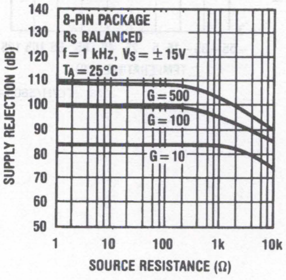
**Positive Power Supply Rejection**



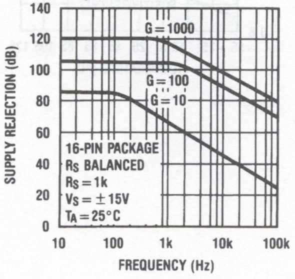
**Negative Power Supply Rejection**



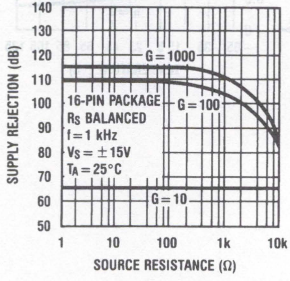
**Negative Power Supply Rejection**



**Negative Power Supply Rejection**



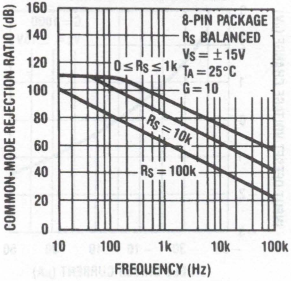
**Negative Power Supply Rejection**



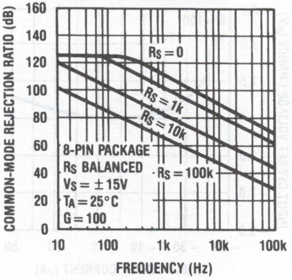
TL/H/5609-4

## Typical Performance Characteristics (Continued)

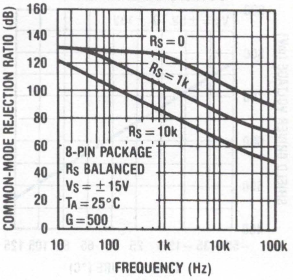
CMRR with Balanced Source Resistance



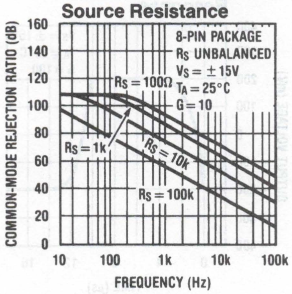
CMRR with Balanced Source Resistance



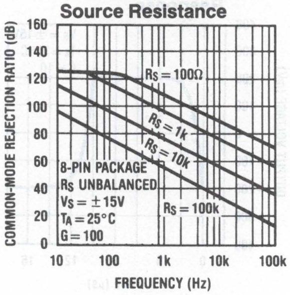
CMRR with Balanced Source Resistance



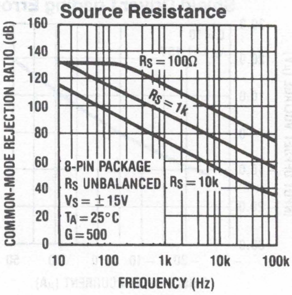
CMRR with Unbalanced Source Resistance



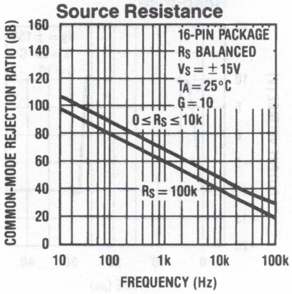
CMRR with Unbalanced Source Resistance



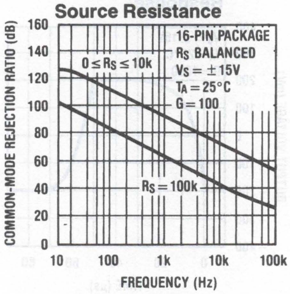
CMRR with Unbalanced Source Resistance



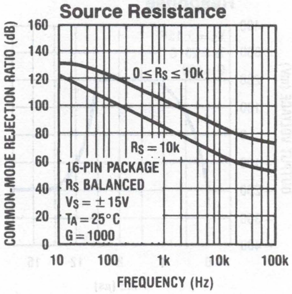
CMRR with Balanced Source Resistance



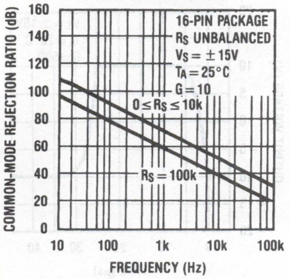
CMRR with Balanced Source Resistance



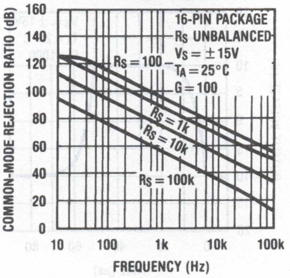
CMRR with Balanced Source Resistance



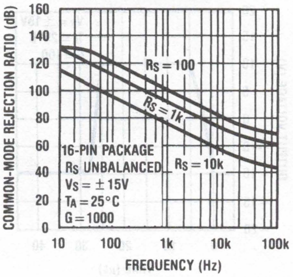
CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



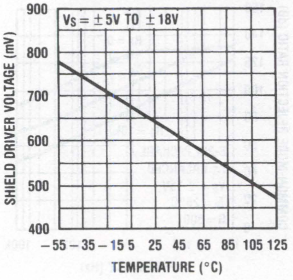
CMRR with Unbalanced Source Resistance



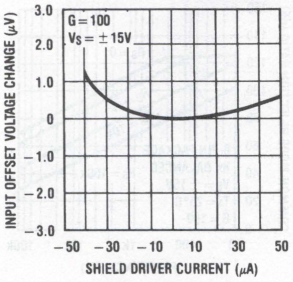
TL/H/5609–5

# Typical Performance Characteristics

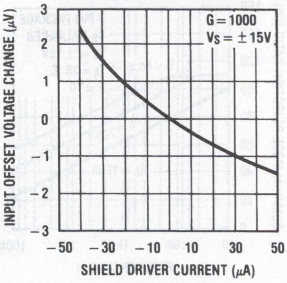
**Shield Driver Bias Voltage***



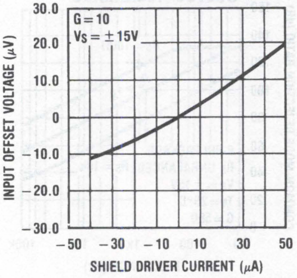
**Shield Driver Loading Error**



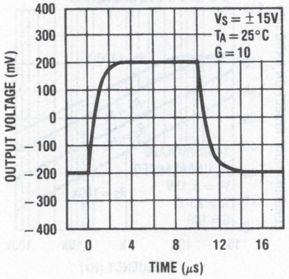
**Shield Driver Loading Error**



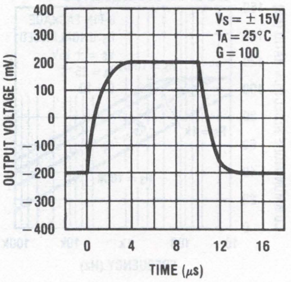
**Shield Driver Loading Error**



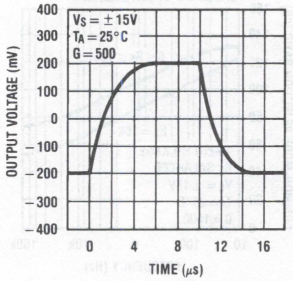
**Small Signal Transient Response**



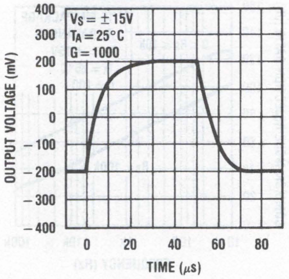
**Small Signal Transient Response**



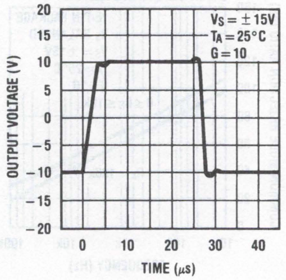
**Small Signal Transient Response**



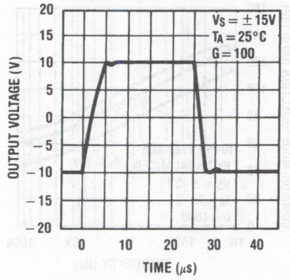
**Small Signal Transient Response**



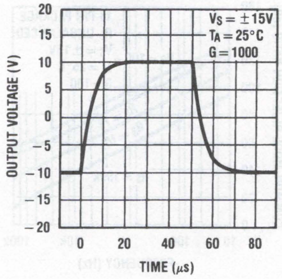
**Large Signal Transient Response**



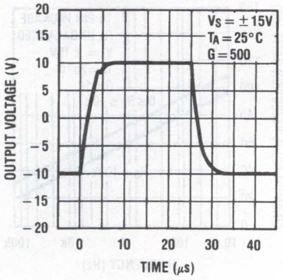
**Large Signal Transient Response**



**Large Signal Transient Response**

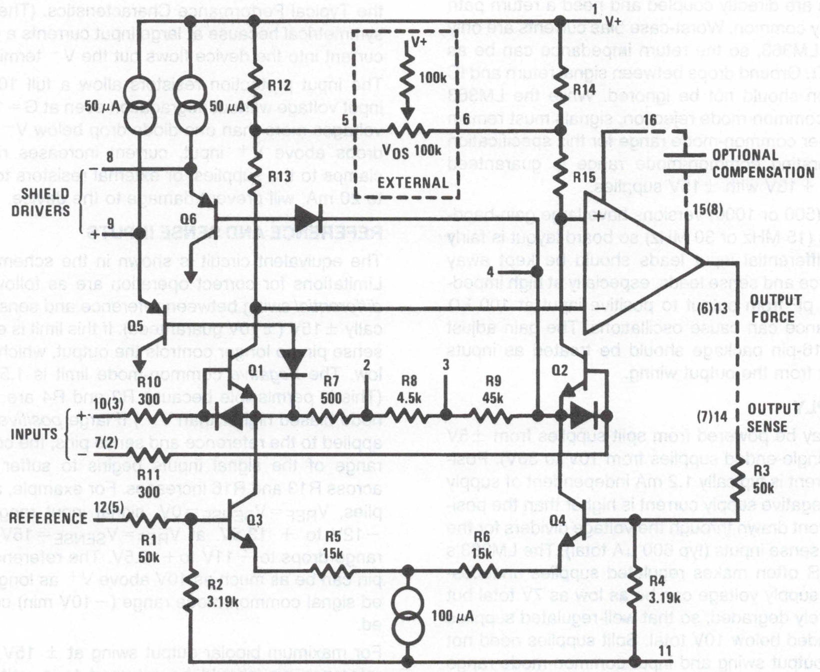


**Large Signal Transient Response**



TL/H/5609-6

## Simplified Schematic (pin numbers in parentheses are for 8-pin package)


V+
50 μA
50 μA
R12
R13
8
SHIELD DRIVERS
9
Q6
V+
100k
5
6
V$_{OS}$ 100k
EXTERNAL
R14
16
OPTIONAL COMPENSATION
R15
15(8)
4
+
−
(6)13
OUTPUT FORCE
Q5
Q1
2
3
Q2
R10
300
R7
500
R8
4.5k
R9
45k
10(3)
INPUTS
7(2)
R11
300
(7)14
OUTPUT SENSE
R3
50k
12(5)
REFERENCE
R1
50k
Q3
R5
15k
R6
15k
Q4
R2
3.19k
R4
3.19k
100 μA
11

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## Theory of Operation

Referring to the Simplified Schematic, it can be seen that the input voltage is applied across the bases of Q1 and Q2 and appears between their emitters. If $R_{E1\text{-}2}$ is the resistance across these emitters, a differential current equal to $V_{IN}/R_{E1\text{-}2}$ flows from Q1's emitter to Q2's. The second stage amplifier shown maintains Q1 and Q2 at equal collector currents by negative feedback to Q4. The emitter currents of Q3 and Q4 must therefore be unbalanced by an amount equal to the current flow across $R_{E1\text{-}2}$. Defining $R_{E3\text{-}4} = R5 + R6$, the differential voltage across the emitters of Q4 to Q3 is equal to

$$\frac{V_{IN}}{R_{E\,1\text{-}2}} \times R_{E3\text{-}4}.$$

This voltage divided by the attenuation factor

$$\frac{R4}{R3+R4} = \frac{R2}{R1+R2}$$

is equal to the output-to-reference voltage. Hence, the overall gain is given by

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{R3+R4}{R4} \times \frac{R_{E3\text{-}4}}{R_{E1\text{-}2}}.$$

## Application Hints

The LM363 was designed to be as simple to use as possible, but several general precautions must be taken. The differential inputs are directly coupled and need a return path to power supply common. Worst-case bias currents are only 10 nA for the LM363, so the return impedance can be as high as 100 MΩ. Ground drops between signal return and IC supply common should not be ignored. While the LM363 has excellent common-mode rejection, signals must remain within the proper common-mode range for this specification to apply. Operating common-mode range is guaranteed from −11V to +13V with ±15V supplies.

The high-gain (500 or 1000) versions have large gain-bandwidth products (15 MHz or 30 MHz) so board layout is fairly critical. The differential input leads should be kept away from output force and sense leads, especially at high impedances. Only 1 pF from output to positive input at 100 kΩ source impedance can cause oscillations. The gain adjust leads on the 16-pin package should be treated as inputs and kept away from the output wiring.

### POWER SUPPLY

The LM363 may be powered from split supplies from ±5V to ±18V (or single-ended supplies from 10V to 36V). Positive supply current is typically 1.2 mA independent of supply voltage. The negative supply current is higher than the positive by the current drawn through the voltage dividers for the reference and sense inputs (typ 600 µA total). The LM363's excellent PSRR often makes regulated supplies unnecessary. Actually, supply voltage can be as low as 7V total but PSRR is severely degraded, so that well-regulated supplies are recommended below 10V total. Split supplies need not be balanced; output swing and input common-mode range will simply not be symmetrical with unbalanced supplies. For example, at +12V and −5V supplies, input common-mode range is typically +10.5V to −2V and output swing is +11V to −4V.

When using ultra-low offset versions, best results are obtained at ±15V supplies. For example, the LM363-500's offset voltage is guaranteed within 100 µV at ±15V at 25°C. Running at ±5V results in a worst-case negative PSRR error of 10V (−15V to −5V) multiplied by $3.2 \times 10^{-6}$ (110 dB) or 32 µV, increasing the worst-case offset. Positive PSRR results in another 10 µV worst-case change.

### INPUTS

The LM363 input circuitry is depicted in the Simplified Schematic. The input stage is run relatively rich (50 µA) for low voltage noise and wide bandwidth; super-beta transistors and bias-current cancellation (not shown) keep bias currents low. Due to the bias-current cancellation circuitry, bias current may be either polarity at either input. While input current noise is high relative to bias current, it is not significant until source resistance approaches 100 kΩ.

Input common-mode range is typically from 3V above $V^-$ to 1.5V below $V^+$, so that a large potential drop between the input signal and output reference can be accommodated. However, a return path for the input bias current must be provided; the differential input stage is not isolated from the supplies. Differential input swing in the linear region is equal to output swing divided by gain, and typically ranges from 1.3V at G=10 to 13 mV at G=1000.

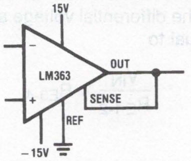
Clamp diodes are provided to prevent zener breakdown and resulting degradation of the input transistors. At large input overdrives these diodes conduct, greatly increasing input currents. This behavior is illustrated in the $I_{IN}$ VS $V_{IN}$ plot in the Typical Performance Characteristics. (The graph is not symmetrical because at large input currents a portion of the current into the device flows out the $V^-$ terminal.)

The input protection resistors allow a full 10V differential input voltage without degradation even at G=1000. At input voltages more than one diode drop below $V^-$ or two diode drops above $V^+$ input, current increases rapidly. Diode clamps to the supplies, or external resistors to limit current to 20 mA, will prevent damage to the device.

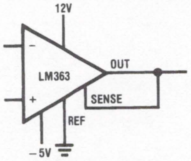
### REFERENCE AND SENSE INPUTS

The equivalent circuit is shown in the schematic diagram. Limitations for correct operation are as follows. Maximum *differential* swing between reference and sense pins is typically ±15V (±10V guaranteed). If this limit is exceeded, the sense pin no longer controls the output, which pegs high or low. The *negative* common-mode limit is 1.5V below $V^-$. (This is permissible because R2 and R4 are returned to a node biased higher than $V^-$.) If large *positive* voltages are applied to the reference and sense pins, the common-mode range of the signal inputs begins to suffer as the drop across R13 and R16 increases. For example, at ±15V supplies, $V_{REF} = V_{SENSE} = 0V$, signal input range is typically −12V to + 13.5V. at $V_{REF} = V_{SENSE} = 15V$, signal input range drops to −11V to +13.5V. The reference and sense pin can be as much as 10V above $V^+$ as long as a restricted signal common-mode range (−10V min) can be tolerated.

For maximum bipolar output swing at ± 15V supplies, the reference pin should be returned to a voltage close to ground. At lower supply voltages, the reference pin need not be halfway between the supplies for maximum output swing. For example, at $V^+ = +12V$ and $V^- = -5V$, grounding the reference pin still allows a +11V to −4V swing. For single-supply systems, the reference pin can be tied to either supply if a single output polarity is all that is required. For a bipolar input and output, create a low impedance reference with an op amp and voltage divider or a regulator (e.g., LM336, LM385, LM317L). This forms the reference for all succeeding signal-processing stages. (Don't connect the reference terminal directly to a voltage divider; this degrades gain error.) See *Figure 1*.



**a. Usual configuration maximizes bipolar output swing.**



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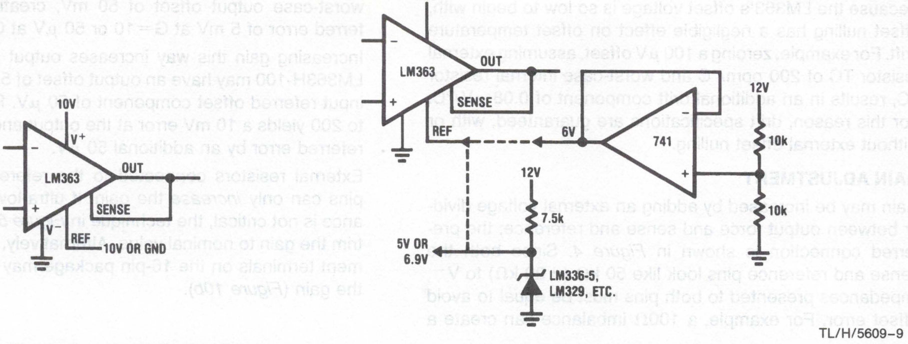
**b. Unequal supplies, output ground referred. Full output swing preserved referred to supplies.**

**FIGURE 1. Reference Connections**

## Application Hints (Continued)



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c. Single Supply, Unipolar Output

d. Single Supply, Bipolar Output

**FIGURE 1. Reference Connections** (Continued)

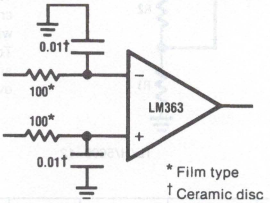
### OUTPUTS

The LM363's output can typically swing within 1V of the supplies at light loads. While specified to drive a 2 kΩ load to ±10V, current limit is typically 15 mA at room temperature. The output can stably drive capacitive loads up to 400 pF. For higher load capacitance, the amplifier may be overcompensated. The output may be continuously shorted to ground without damaging the device.

### OFFSET VOLTAGE

The LM363's offset voltage is internally trimmed to a very low value. Note that data sheet values are given at $T_j = 25°C$, $V_{CM} = 0V$ and $V^+ = V^- = 15V$. For other conditions, warm-up drift, temperature drift, common-mode rejection and power supply rejection must be taken into account. Warm-up drift, due to chip and package thermal gradients, is an effect separate from temperature drift. Typical warm-up drift is tabulated in the Electrical Characteristics; settling time is approximately 5 minutes in still air. At load currents up to 5 mA, thermal feedback effects are negligible ($\Delta V_{OS} \leq 2\mu V$ at $G = 1000$).

Care must be taken in measuring the extremely low offset voltages of the high gain amplifiers. Input leads must be held isothermal to eliminate thermocouple effects. Oscillations, due to either heavy capacitive loading or stray capacitance from input to output, can cause erroneous readings. In either case, overcompensation will help. High frequency noise fed into the inputs may be rectified internally, and produce an offset shift. A simple low-pass RC filter will usually cure this problem (*Figure 2*). Use film type resistors for their low thermal EMF. In highly noisy environments, LC filters can be substituted for increased RF attenuation.



* Film type

† Ceramic disc

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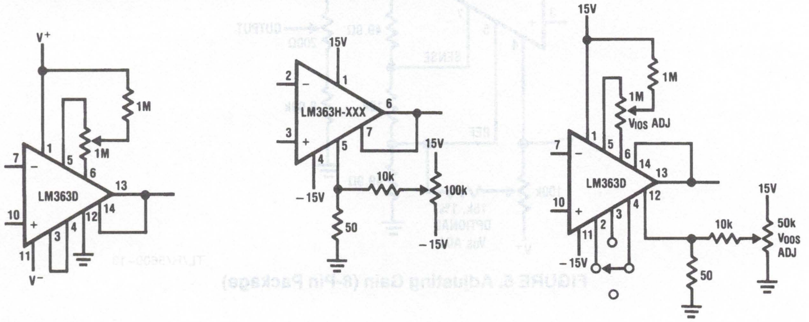
**FIGURE 2. Low Pass Filter Prevents RF Rectification**

Instrumentation amplifiers have both an input offset voltage ($V_{IOS}$) and an output offset voltage ($V_{OOS}$). The total input-referred offset voltage ($V_{OSRTI}$) is related to the instrumentation amplifier gain (G) as follows: $V_{OSRTI} = V_{IOS} + V_{OOS}/G$. The offset voltage given in the LM363 specifications is the total input-referred offset. As long as only one gain is used, offset voltage can be nulled at either input or output as shown in *Figures 3a* and *3b*. When the 16-pin device is used at multiple gain settings, both $V_{IOS}$ and $V_{OOS}$ should be nulled to get minimum offset at all gains, as shown in *Figure 3c*. The correct procedure is to trim $V_{OOS}$ for zero output at $G = 10$, then trim $V_{IOS}$ at $G = 1000$.



a. Input Offset Adj. for 16-Pin Package

b. Output Offset Adj. for 8-Pin Package

c. Input and Output Offset Adjustment for 16-Pin Package

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**FIGURE 3. Offset Voltage Trimming**

## Application Hints (Continued)

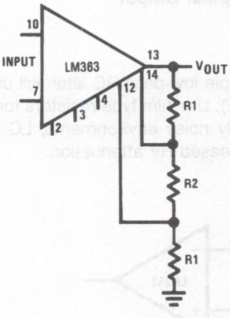
Because the LM363's offset voltage is so low to begin with, offset nulling has a negligible effect on offset temperature drift. For example, zeroing a 100 μV offset, assuming external resistor TC of 200 ppm/°C and worst-case internal resistor TC, results in an additional drift component of 0.08 μV/°C. For this reason, drift specifications are guaranteed, with or without external offset nulling.

### GAIN ADJUSTMENT

Gain may be increased by adding an external voltage divider between output force and sense and reference; the preferred connection is shown in *Figure 4*. Since both the sense and reference pins look like 50 kΩ (±20 kΩ) to V−, impedances presented to both pins must be equal to avoid offset error. For example, a 100Ω imbalance can create a worst-case output offset of 50 mV, creating an input-referred error of 5 mV at G = 10 or 50 μV at G = 1000.

Increasing gain this way increases output offset error. An LM363H-100 may have an output offset of 5 mV, resulting in input referred offset component of 50 μV. Raising the gain to 200 yields a 10 mV error at the output and changes input referred error by an additional 50 μV.

External resistors connected to the reference and sense pins can only *increase* the gain. If ultra-low output impedance is not critical, the technique in *Figure 5* can be used to trim the gain to nominal value. Alternatively, the $V_{OS}$ adjustment terminals on the 16-pin package may be used to trim the gain (*Figure 10b*).



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R1 and R2 should be as low as possible to avoid errors due to 50 kΩ input impedance of reference and sense pins. Total resistance (R2 + 2R1) should be above 4 kΩ, however, to prevent excessive load on the LM363 output. The exact formula for calculating gain (G) is:

$$G = G_O\left(1 + \frac{2R1}{R2} + \frac{R1}{50k}\right)$$

$G_O$ = preset gain

The last term may be ignored in applications where gain accuracy is not critical. The table below gives suggested values for R1 and R2 along with the calculated error due to "closest value" standard 1% resistors. Total gain error tolerance includes contributions from LM363 $G_O$ error and resistor tolerance (±1%) and works out to approximately 2.5% in every case.

| **Gain Increase** | 1.5 | 2 | 2.5 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **R1** | 1.21k | 1.21k | 2k | 2k | 1.78k | 2k | 2.49k | 2.94k | 3.48k | 3.92k | 4.42k |
| **R2** | 5k | 2.49k | 2.74k | 2.05k | 1.21k | 1k | 1k | 1k | 1k | 1k | 1k |
| **Error (typ)** | +0.6% | −0.2% | 0 | −0.3% | −0.6% | +0.8% | +0.5% | −0.9% | +0.4% | −0.9% | −0.7% |

**FIGURE 4. Increasing Gain**

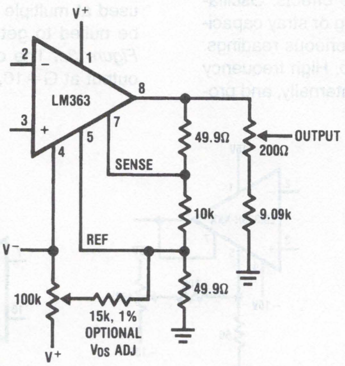

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**FIGURE 5. Adjusting Gain (8-Pin Package)**

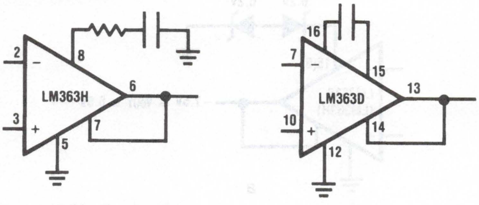
## Application Hints (Continued)

### COMPENSATION AND OUTPUT CLAMPING

The LM363 is internally compensated for unity feedback from output to sense. Increasing gain with external dividers will decrease the bandwidth and increase stability margin. Without external compensation, the amplifier can stably drive capacitive loads up to 400 pF. When used as an op amp (sense and reference pins grounded, feedback to inverting input), the LM363 is stable for gains of 100 or more. For greater stability, the device may be over-compensated as in *Figure 6*. Tables I and II depict suggested compensation components along with the resulting changes in large and small signal bandwidth for the 8-pin and 16-pin packages, respectively.

Note that the RC network from pin 8 of the 8-pin device to ground has a large effect on power bandwidth, especially at low gains. The Miller capacitance utilized for the 16-pin device permits higher slew rate and larger load capacitance for the same bandwidth, and is preferred when bandwidth must be greatly reduced (e.g., to reduce output noise).

Heavy Miller overcompensation on the 16-pin package can degrade AC PSRR. A large capacitor between pins 15 and 16 couples transients on the positive supply to the output buffer. Since the amplifier bandwidth is severely rolled off it cannot keep the output at the correct state at moderate frequencies. Hence, for good PSRR, either keep the Miller capacitance under 1000 pF or use the pin 15-to-ground compensation.



a. 8-Pin Package

b. 16-Pin Package

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**FIGURE 6. Overcompensation**

**TABLE I. Overcompensation on 8-Pin Package**

| Gain | Compensation Network (Pin 8 to Ground)† | Small Signal 3 dB Bandwidth (kHz) | Power Bandwidth (±10V Swing) (Hz) | Maximum Capacitive Load (pF) |
|---|---|---|---|---|
| 500 | — | 125 | 100k | 400 |
| | 100 pF, 15k | 95 | 15k | 600 |
| | 1000 pF, 5k | 45 | 1.8k | 800 |
| | 0.01 µF, 500Ω | 10 | 200 | 1000* |
| | 0.1 µF | 1 | 20 | 1000* |
| 100 | — | 240 | 100k | 400 |
| | 100 pF, 15k | 170 | 15k | 900 |
| | 1000 pF, 5k | 80 | 1.8k | 1200 |
| | 0.01 µF, 500Ω | 20 | 200 | 1600* |
| | 0.1 µF | 2 | 20 | 2000* |
| 10 | — | 240 | 100k | 400 |
| | 100 pF, 15k | 170 | 15k | 900 |
| | 1000 pF, 5k | 90 | 1.8k | 1200 |
| | 0.01 µF, 500Ω | 20 | 200 | 1600* |
| | 0.1 µF | 2 | 20 | 2000* |

*Also stable for $C_L \geq 0.05\ \mu F$ †Pin 15 to round on 16-pin package

**TABLE II. Overcompensation on 16-Pin Package**

| Gain | Compensation Capacitor (Pin 15 to 16) | Small Signal 3 dB Bandwidth (Hz) | Power Bandwidth (±10V Swing) (Hz) | Maximum Capacitive Load (pF) |
|---|---|---|---|---|
| 1000 | 0 | 45k | 45k | 1000* |
| | 10 pF | 16k | 16k | 2000* |
| | 100 pF | 2.5k | 2.5k | 2500* |
| | 1000 pF | 250 | 250 | 3000* |
| | 0.01 µF | 25 | 25 | 3000* |
| 100 | 0 | 140k | 100k | 900 |
| | 10 pF | 50k | 50k | 1600 |
| | 100 pF | 7.5k | 7.5k | 2000* |
| | 1000 pF | 750 | 750 | 2000* |
| | 0.01 µF | 76 | 75 | 2000* |
| 10 | 0 | 180k | 90k | 600 |
| | 10 pF | 60k | 50k | 1100 |
| | 100 pF | 9k | 9k | 1600 |
| | 1000 pF | 900 | 900 | 2000* |
| | 0.01 µF | 90 | 90 | 2000* |

*Also stable for $C_L \geq 0.05\ \mu F$

## Application Hints (Continued)

Because the LM363's output voltage is approximately one diode drop below the voltage at pin 15 (pin 8 for the 8-pin device), this point may be used to limit output swing as seen in *Figure 7a*. Current available from this pin is only 50 μA, so that zeners must have a sharp breakdown to clamp accurately. Alternatively, a diode tied to a voltage source could be used as in *Figure 7b*.

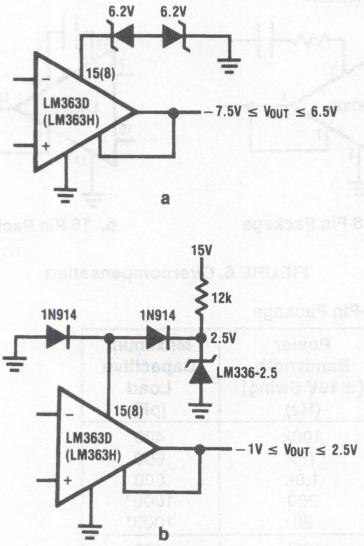

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**FIGURE 7. Output Clamp**

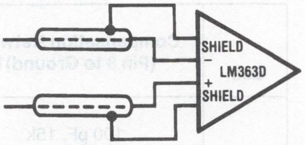
### SHIELD DRIVERS

When differential signals are sent through long cables, three problems occur. First, noise, both common-mode and differential, is picked up. Second, signal bandwidth is reduced by the RC low-pass filter formed by the source impedance and the cable capacitance. Finally, when these RC time constants are not identical (unbalanced source impedance and/or unbalanced capacitance), AC common-mode rejection is degraded, amplifying both induced noise and "ground" noise. Either filtering at the amplifier inputs or slowing down the amplifier by overcompensating will indeed reduce the noise, but the price is slower response. The LM363's dual shield drivers can actually increase bandwidth while reducing noise.

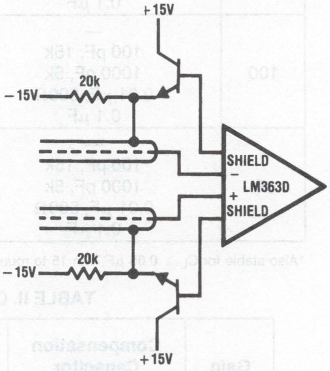
The way this is done is by bootstrapping out shield capacitance. The shield drivers follow the input signal. Since both sides of the shield capacitance swing the same amount, it is effectively out of the circuit at frequencies of interest. Hence, the input signal is not rolled off and AC CMRR is not degraded (*Figure 8*). The LM363's shield drivers can handle capacitances (shield to center conductor) as high as 1000 pF with source resistances up to 100 kΩ.

For best results, identical shielded cables should be used for both signal inputs, although small mismatches in shield driver to ground capacitance (≤500 pF) do not cause problems. At certain low values of cable capacitance (50 pF–200 pF), high frequency oscillations can occur at high source resistance (≥ 10 kΩ). This is alleviated by adding 50 pF to ground at both shield driver outputs. Do not use only one shield driver for a single-ended signal as oscillations can result; shield driver to input capacitance must be roughly balanced (±30%). To further reduce noise pickup, the shielded signal lines may be enclosed together in a grounded shield. If a large amount of RF noise is the problem, the only sure cure is a filter capacitor at both inputs; otherwise the RFI may be internally rectified, producing an offset.

DC loading on the shield drivers should be minimized. The drivers can only source approximately 40 μA; above this value the input stage bias voltages change, degrading $V_{OS}$ and CMRR. While the shield drivers can sink several mA, $V_{OS}$ may degrade severely at loads above 100 μA (see Shield Driver Loading Error curve in Typical Performance Characteristics). Because the shield drivers are one diode drop above the input levels, unbalanced leakage paths from shield to input can produce an input offset at high source impedances. Buffering with emitter-followers (*Figure 8b*) reduces this leakage current by reducing the voltage differential and eliminates any loading on the amplifier.



**a. Standard Configuration**



**b. NPN Followers to Reduce Offsets**

TL/H/5609-16

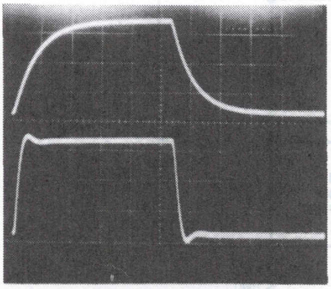
**FIGURE 8. Driving Shielded Cables**

### MISCELLANEOUS TRIMMING

The $V_{OS}$ adjust and shield driver pins available on the 16-pin package may be used to trim the other parameters besides offset voltage, as illustrated in *Figure 10*. The bias-current trim relies on the fact that the voltage on the shield driver and gain setting pins is one diode drop respectively above and below the input voltage. Input bias current can be held to within 100 pA over the entire common-mode range, and input offset current always stays under 30 pA. The CMRR trims use the shield driver pins to drive the $V_{OS}$ adjust pins, thus maintaining the LM363's ultra-high input impedance.

## Application Hints (Continued)

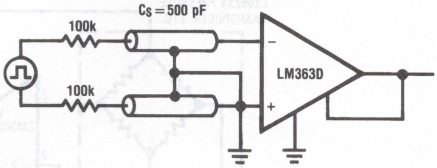
If power supply rejection is critical, frequently only the negative PSRR need be adjusted, since the positive PSRR is more tightly specified. Any or all of the trim schemes of *Figure 10* can be combined as desired. As long as the center tap of the 100k trimpot is returned to a voltage 200 mV below V+, the trim schemes shown will not greatly affect $V_{OS}$. Both the gain and DC CMRR trims can degrade positive PSRR; the positive PSRR can then be nulled out if desired. The correct order of trimming from first to last is bias current, gain, CMRR, negative PSRR, positive PSRR and $V_{OS}$.



**LM363 OUTPUT 1V/DIV**
**100 µs/DIV**

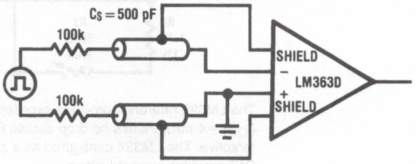
TL/H/5609-17

**Top Trace: Cable Shield Grounded**



C$_S$ = 500 pF
100k
100k
LM363D
−
+

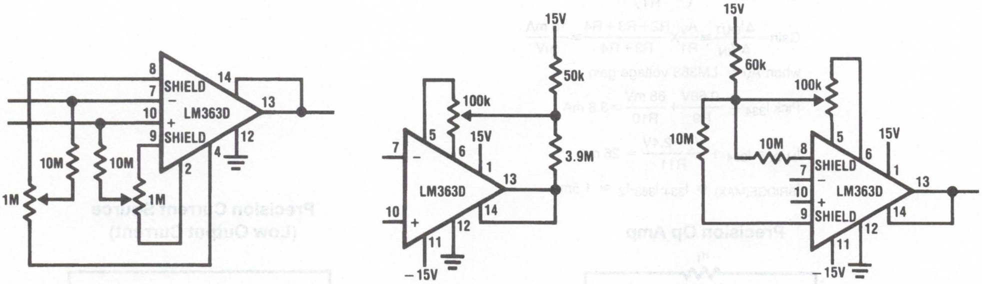
**Bottom Trace: Cable Shield Bootstrapped**



C$_S$ = 500 pF
100k
100k
SHIELD
−
LM363D
+
SHIELD

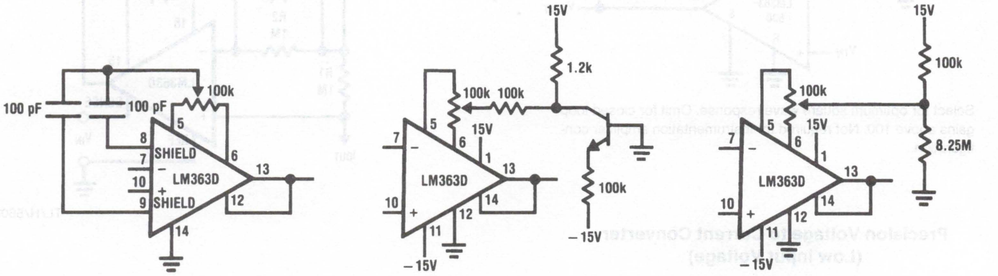
TL/H/5609-18

**FIGURE 9. Improved Response using Shield Drivers**



8
7 SHIELD
−
10
+
9 SHIELD
LM363D
14
13
12
4
2
10M
10M
1M
1M
15V
50k
100k
5
6
15V
1
7
−
LM363D
13
3.9M
10
+
14
12
11
−15V
15V
60k
100k
10M
10M
8
7 SHIELD
10
−
+
9 SHIELD
5
6
15V
1
LM363D
13
14
12
11
−15V

**a. Bias Current** **b. Gain** **c. DC CMRR**



100 pF
100 pF
100k
5
8
7 SHIELD
−
10
+
9 SHIELD
LM363D
6
13
12
14
15V
1.2k
100k
100k
5
15V
6
1
7
−
LM363D
13
10
+
14
12
11
−15V
100k
−15V
15V
100k
100k
5
15V
6
1
7
−
LM363D
13
10
+
14
12
11
−15V
8.25M

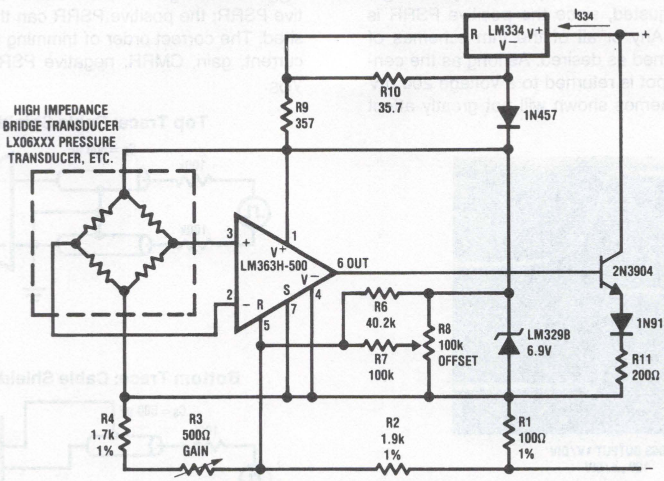
**d. AC CMRR** **e. Negative PSRR** **f. Positive PSRR**

TL/H/5609-19

**FIGURE 10. Other Trims for 16-Pin Package**

# Typical Applications

## 4 mA-20 mA Two Wire Current Transmitter


R LM334 V+ V−
I334
+
R10
35.7
R9
357
1N457
HIGH IMPEDANCE
BRIDGE TRANSDUCER
LX06XXX PRESSURE
TRANSDUCER, ETC.
3
+
1
V+
LM363H-500
6 OUT
V−
S
4
2
− R
7
5
2N3904
1N914
R6
40.2k
R8
100k
OFFSET
R7
100k
LM329B
6.9V
R11
200Ω
R4
1.7k
1%
R3
500Ω
GAIN
R2
1.9k
1%
R1
100Ω
1%
−

TL/H/5609-20

The LM329 reference provides excellent line regulation and gain stability. When bridge is balanced ($I_{OUT} = 4$ mA), there's no drop across R3 and R4, so that gain and offset adjustments are non-interactive. The LM334 configured as a zero-TC current source supplies quiescent current to circuit. R11 provides current limiting.

**Design Equations**

$$I_{OS} = (I_{R6} + I_{R7})\left(1 + \frac{R2}{R1}\right) = 4\text{ mA}$$

$$\text{Gain} = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \cong \frac{A_V}{R1} \times \frac{R2 + R3 + R4}{R3 + R4} \cong \frac{10\text{ mA}}{\text{mV}}$$

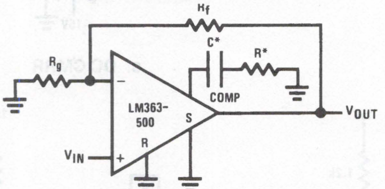
when $A_V$ = LM363 voltage gain

$$\text{Pick } I_{334} = \frac{0.68\text{V}}{R9} + \frac{68\text{ mV}}{R10} \cong 3.8\text{ mA}$$

$$I_{MAX} = I_{334} + \frac{V_Z - 2.4\text{V}}{R11} = 26\text{ mA}$$

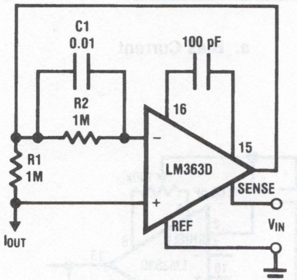
$$I_{BRIDGE(MAX)} \cong I_{334} - I_{363} - I_Z \cong 1.5\text{mA}$$

## Precision Op Amp


Rf
C*
R*
Rg
−
COMP
LM363-
500
S
VOUT
R
VIN
+

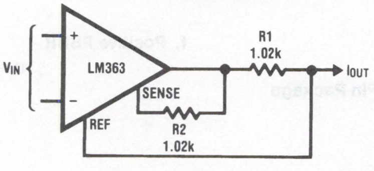
Select for optimum square wave response. Omit for closed loop gains above 100. Not required for instrumentation amplifier configuration.

## Precision Current Source (Low Output Current)


C1
0.01
100 pF
R2
1M
16
−
15
R1
1M
LM363D
SENSE
+
IOUT
REF
VIN

TL/H/5609-21

## Precision Voltage to Current Converter (Low Input Voltage)


+
VIN
LM363
−
R1
1.02k
IOUT
SENSE
REF
R2
1.02k

R1 = R2

$$\text{Req} = R1 \| 50\text{ k}\Omega$$

$$I_{OUT} = \frac{G\,V_{IN}}{\text{Req}} = \frac{G\,V_{IN}}{1\text{ k}\Omega}$$

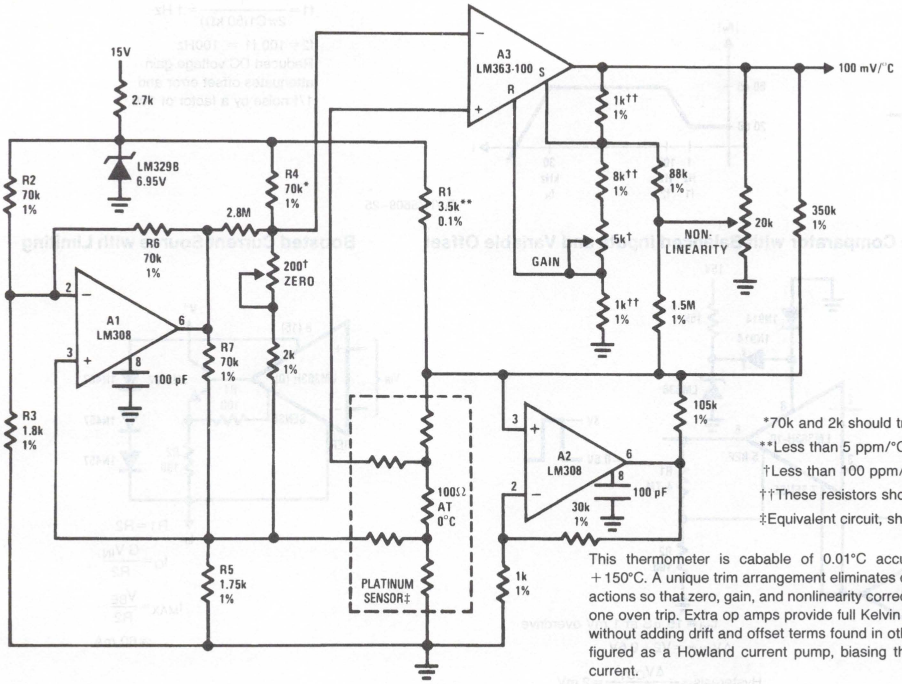
R1 = R2

$$I_{OUT} = \frac{V_{IN}}{GR1}$$

TL/H/5609-22

## Typical Applications (Continued)

### Curvature Corrected Platinum RTD Thermometer


15V
2.7k
LM329B
6.95V
R2
70k
1%
R4
70k*
1%
2.8M
R6
70k
1%
200†
ZERO
A1
LM308
2
3
6
8
100 pF
R7
70k
1%
2k
1%
R3
1.8k
1%
R5
1.75k
1%
R1
3.5k**
0.1%
100Ω
AT
0°C
PLATINUM
SENSOR‡
A3
LM363-100
S
R
100 mV/°C
1k††
1%
8k††
1%
88k
1%
5k†
GAIN
NON-
LINEARITY
20k
350k
1%
1k††
1%
1.5M
1%
105k
1%
A2
LM308
3
2
6
8
100 pF
30k
1%
1k
1%

TL/H/5609-23

*70k and 2k should track to 5 ppm/°C

**Less than 5 ppm/°C drift

†Less than 100 ppm/°C drift

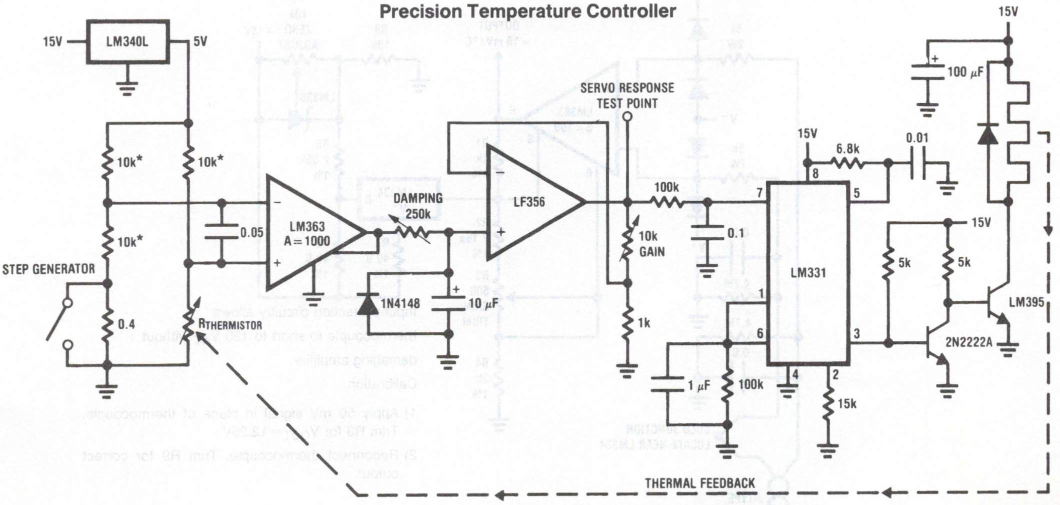
††These resistors should track to 20 ppm/°C

‡Equivalent circuit, showing lead resistance

This thermometer is cabable of 0.01°C accuracy over −50°C to +150°C. A unique trim arrangement eliminates cumbersome trim interactions so that zero, gain, and nonlinearity correction can be trimmed in one oven trip. Extra op amps provide full Kelvin sensing on the sensor without adding drift and offset terms found in other designs. A2 is configured as a Howland current pump, biasing the sensor with a fixed current.

Resistors R2, R3, R4 and R5 from a bridge driven into balance by A1. In balance, both inputs of A1 are at the same voltage. Since R6 = R7, A1 draws equal currents from both legs of the bridge. Any loading of the R4/R5 leg by the sensor would unbalance the bridge; therefore, both bridge taps are given to the sensor open circuit voltage and no current is drawn.

### Precision Temperature Controller


15V
LM340L
5V
10k*
10k*
10k*
0.4
STEP GENERATOR
RTHERMISTOR
0.05
LM363
A = 1000
DAMPING
250k
1N4148
10 μF
SERVO RESPONSE
TEST POINT
LF356
100k
10k
GAIN
1k
0.1
15V
6.8k
0.01
8
7
5
1
6
3
4
2
LM331
1 μF
100k
15k
15V
100 μF
15V
5k
5k
LM395
2N2222A
THERMAL FEEDBACK

TL/H/5609-24

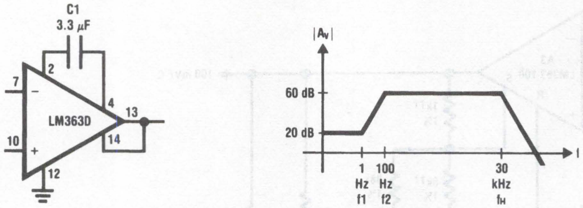
*Ultronix 105A wirewound

Thermistor = Yellow Springs #44032

Setpoint stability = 2.5X10−4°C/Hr

# Typical Applications (Continued)

## Low Frequency Rolloff (AC Coupling)


C1
3.3 µF
7
2
−
LM363D
4
13
14
10
+
12
|Av|
60 dB
20 dB
1 Hz f1
100 Hz f2
30 kHz fH
f

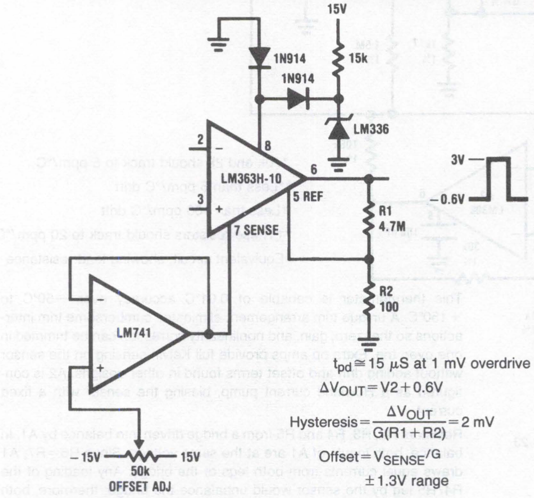
$$f1 = \frac{1}{2\pi C1(50\ k\Omega)} = 1\ Hz$$

$f2 = 100\ f1 = 100Hz$

Reduced DC voltage gain attenuates offset error and 1/f noise by a factor of 100.

TL/H/5609-25

## Precision Comparator with Balanced Inputs and Variable Offset


15V
1N914
15k
1N914
LM336
2
−
8
LM363H-10
6
3
+
5 REF
7 SENSE
3V
−0.6V
R1
4.7M
R2
100
LM741
−
+
−15V
15V
50k
OFFSET ADJ

$t_{pd} \cong 15\ \mu S$ at 1 mV overdrive

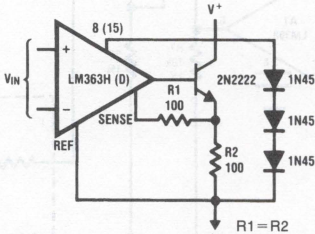
$\Delta V_{OUT} = V2 + 0.6V$

$$\text{Hysteresis} = \frac{\Delta V_{OUT}}{G(R1 + R2)} = 2\ mV$$

$\text{Offset} = V_{SENSE}/G$

$\pm 1.3V$ range

## Boosted Current Source with Limiting


V+
8 (15)
+
VIN
LM363H (D)
−
2N2222
1N457
R1
100
SENSE
1N457
REF
R2
100
1N457
IO

$R1 = R2$

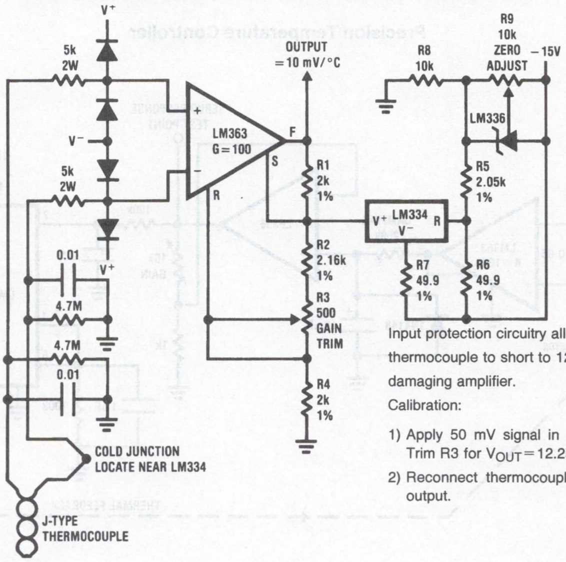
$$I_O = \frac{G\ V_{IN}}{R2}$$

$$I_{MAX} = \frac{V_{BE}}{R2}$$

$\cong 60$ mA

TL/H/5609-26

## Thermocouple Amplifier with Cold Junction Compensation


V+
5k
2W
OUTPUT
= 10 mV/°C
R8
10k
R9
10k
ZERO ADJUST
−15V
+
LM363
G = 100
F
LM336
V−
−
S
R
5k
2W
R1
2k
1%
R5
2.05k
1%
V+ LM334 R
V−
0.01
V+
R2
2.16k
1%
R7
49.9
1%
R6
49.9
1%
4.7M
R3
500
GAIN TRIM
4.7M
0.01
R4
2k
1%
COLD JUNCTION
LOCATE NEAR LM334
J-TYPE
THERMOCOUPLE

Input protection circuitry allows thermocouple to short to 120 $V_{AC}$ without damaging amplifier.

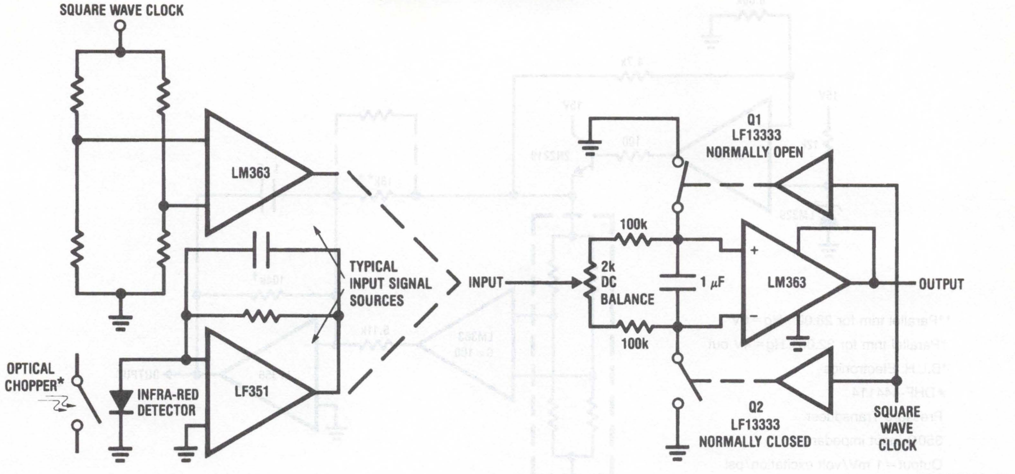
Calibration:

1) Apply 50 mV signal in place of thermocouple. Trim R3 for $V_{OUT} = 12.25V$.
2) Reconnect thermocouple. Trim R9 for correct output.

TL/H/5609-27

## Typical Applications (Continued)

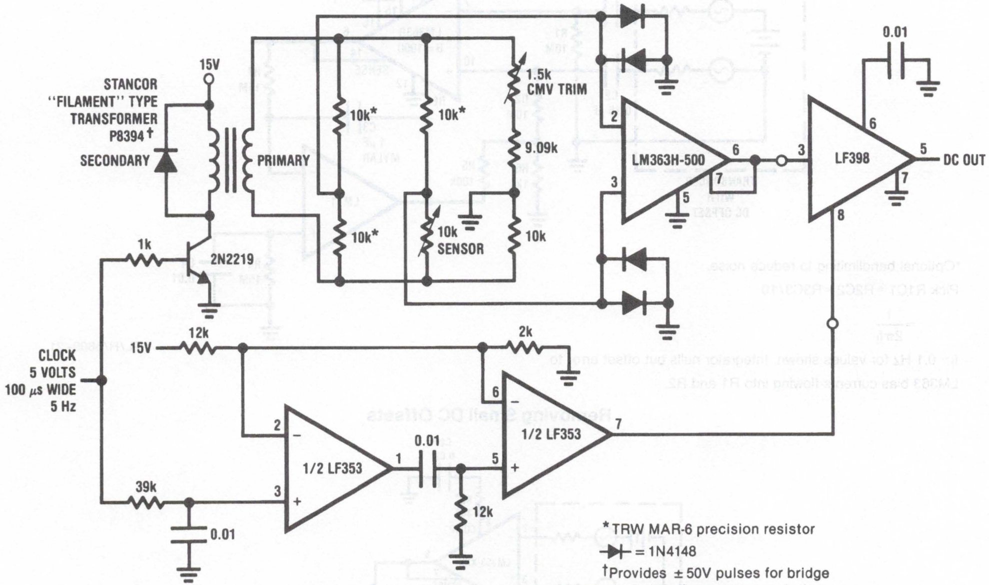
### Synchronous Demodulator


SQUARE WAVE CLOCK
LM363
TYPICAL
INPUT SIGNAL
SOURCES
INPUT
OPTICAL
CHOPPER*
INFRA-RED
DETECTOR
LF351
Q1
LF13333
NORMALLY OPEN
100k
2k
DC
BALANCE
1 μF
+
−
LM363
OUTPUT
100k
Q2
LF13333
NORMALLY CLOSED
SQUARE
WAVE
CLOCK

TL/H/5609-28

*Use square wave drive produced by optical chopper to run LF13333 switch inputs.

### Pulsed Bridge Driver/Amplifier


STANCOR
"FILAMENT" TYPE
TRANSFORMER
P8394†
SECONDARY
PRIMARY
15V
1k
2N2219
10k*
10k*
10k*
1.5k
CMV TRIM
9.09k
10k
SENSOR
10k
2
3
LM363H-500
6
7
5
3
LF398
5
7
8
DC OUT
0.01
CLOCK
5 VOLTS
100 μs WIDE
5 Hz
15V
12k
2k
6
−
1/2 LF353
7
+
5
2
−
1/2 LF353
1
0.01
3
+
39k
0.01
12k

*TRW MAR-6 precision resistor

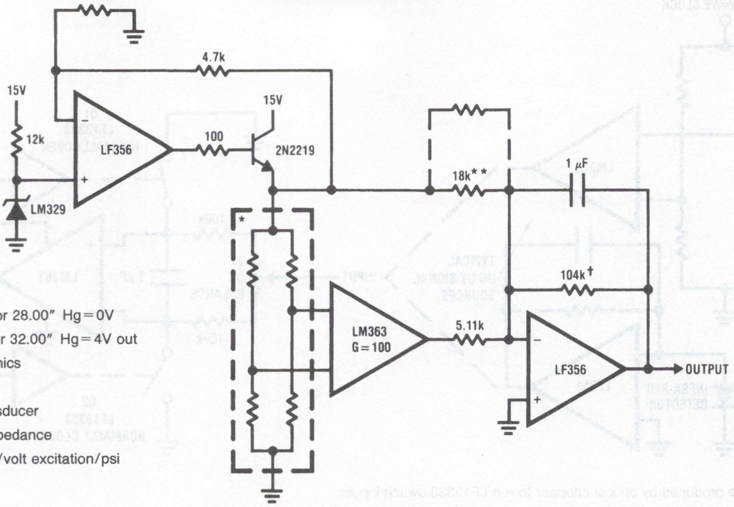
▶| = 1N4148

†Provides ±50V pulses for bridge excitation for greater resolution without overdissipation

TL/H/5609-29

## Typical Applications (Continued)

### Precision Barometer



8.06k
4.7k
15V
12k
LF356
LM329
15V
100
2N2219
*
18k**
1 μF
104k†
LM363
G=100
5.11k
LF356
OUTPUT

**Parallel trim for 28.00″ Hg=0V

†Parallel trim for 32.00″ Hg=4V out

*B.L.H. Electronics

#DHF-444114

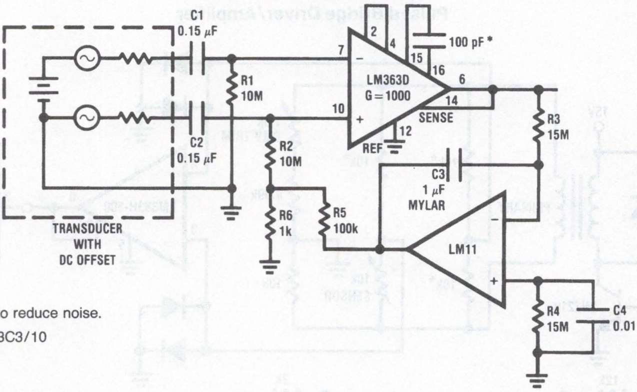
Pressure Transducer

350Ω input impedance

Output=1 mV/volt excitation/psi

TL/H/5609-30

### Removing Large DC Offsets



C1
0.15 μF
C2
0.15 μF
R1
10M
R2
10M
R6
1k
R5
100k
2
4
15
16
7
10
6
14
12
LM363D
G=1000
SENSE
REF
100 pF*
R3
15M
C3
1 μF
MYLAR
LM11
R4
15M
C4
0.01
TRANSDUCER
WITH
DC OFFSET

*Optional bandlimiting to reduce noise.

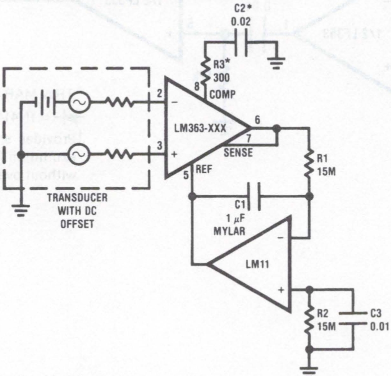
Pick R1C1=R2C2=R3C3/10

$$=\frac{1}{2\pi f_l}$$

$f_l$=0.1 Hz for values shown. Integrator nulls out offset error to LM363 bias currents flowing into R1 and R2.

TL/H/5609-31

### Removing Small DC Offsets



C2*
0.02
R3*
300
8
COMP
2
3
LM363-XXX
6
7
SENSE
5
REF
R1
15M
C1
1 μF
MYLAR
LM11
R2
15M
C3
0.01
TRANSDUCER
WITH DC
OFFSET

*Optional bandlimiting to reduce noise.

Low frequency break

$$\text{frequency } f_l=\frac{1}{2\pi R1C1}=0.01\text{ Hz}$$

Accommodates out referred offset of several volts. Limit is set by max differential between reference and sense terminals.

TL/H/5609-32

## Section 6

## Surface Mount

# Section 6 Contents

Surface Mount . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-3

**National Semiconductor Corporation**

# Surface Mount

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

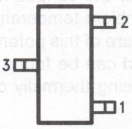
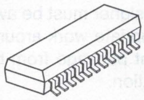
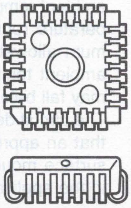
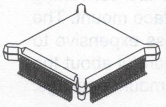
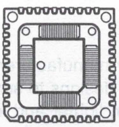
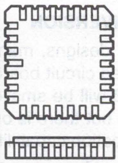
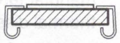
Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

## SURFACE MOUNT PACKAGING AT NATIONAL

To help our customers take advantage of this new technology, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK™) will have a lead center spacing of only 12–20 mils.

**TABLE I. Surface Mount Packages from National**

| Package Type | Small Outline Transistor (SOT) | Small Outline IC (SOIC) | Plastic Chip Carrier (PCC) | Plastic Quad Flat Pack (PQFP) | TAPEPAK™ (TP) | Leadless Chip Carrier (LCC) (LDCC) | Leaded Chip Carrier |
|---|---|---|---|---|---|---|---|
| |  |  |  |  |  |  |  |
| Package Material | Plastic | Plastic | Plastic | Plastic | Plastic | Ceramic | Ceramic |
| Lead Bend | Gull Wing | Gull Wing | J-Bend | Gull Wing | Gull Wing | | Gull Wing |
| Lead Center Spacing | 50 Mils | 50 Mils | 50 Mils | 25 Mils | 20, 15, 12 Mils | 50 Mils | 50 Mils |
| Tape & Reel Option | Yes | Yes | Yes | tbd | tbd | No | No |
| Lead Counts | SOT-23 High Profile<br>SOT-23 Low Profile | SO-8(*)<br>SO-14(*)<br>SO-14 Wide(*)<br>SO-16(*)<br>SO-16 Wide(*)<br>SO-20(*)<br>SO-24(*) | PCC-20(*)<br>PCC-28(*)<br>PCC-44(*)<br>PCC-68<br>PCC-84<br>PCC-124 | PQFP-84<br>PQFP-100<br>PQFP-132<br>PQFP-196(*)<br>PQFP-244 | TP-40(*)<br>TP-68<br>TP-84<br>TP-132<br>TP-172<br>TP-220<br>TP-284<br>TP-360 | LCC-18<br>LCC-20(*)<br>LCC-28<br>LCC-32<br>LCC-44 (*)<br>LCC-48<br>LCC-52<br>LCC-68<br>LCC-84<br>LCC-124 | LDCC-44<br>LDCC-68<br>LDCC-84<br>LDCC-124 |

*In production (or planned) for linear products.

## LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A complete list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

## BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

**TABLE II: Surface Mount Package Thermal Resistance Range***

| Package | Thermal Resistance** ($\theta_{jA}$, °C/W) |
|---|---|
| SO-8 | 120–175 |
| SO-14 | 100–140 |
| SO-14 Wide | 70–110 |
| SO-16 | 90–130 |
| SO-16 Wide | 70–100 |
| SO-20 | 60–90 |
| SO-24 | 55–85 |
| PCC-20 | 70–100 |
| PCC-28 | 60–90 |
| PCC-44 | 40–60 |

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual $\theta_{jA}$ value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

## SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

## TABLE III. Linear Surface Mount Current Device Listing

### Amplifiers and Comparators

| Part Number | Part Number |
|---|---|
| LF347WM | LM392M |
| LF351M | LM393M |
| LF451CM | LM741CM |
| LF353M | LM1458M |
| | LM2901M |
| LF355M | LM2902M |
| LF356M | LM2903M |
| LF357M | LM2904M |
| LF444CWM | LM2924M |
| LM10CWM | LM3403M |
| LM10CLWM | LM4250M |
| LM308M | LM324M |
| LM308AM | LM339M |
| LM310M | LM365WM |
| LM311M | LM607CM |
| LM318M | LMC669BCWM |
| LM319M | LMC669CCWM |
| LM324M | LF441CM |
| LM339M | |
| LM346M | |
| LM348M | |
| LM358M | |
| LM359M | |

### Regulators and References

| Part Number | Part Number |
|---|---|
| LM317LM | LM2931M-5.0 |
| LF3334M | LM3524M |
| LM336M-2.5 | LM78L05ACM |
| LF336BM-2.5 | LM78L12ACM |
| LM336M-5.0 | LM78L15ACM |
| LM336BM-5.0 | LM79L05ACM |
| LM337LM | LM79L12ACM |
| LM385M | LM79L15ACM |
| LM385M-1.2 | LP2951ACM |
| LM385BM-1.2 | LP2951CM |
| LM385M-2.5 | |
| LM385BM-2.5 | |
| LM723CM | |
| LM2931CM | |

### Data Acquisition Circuits

| Part Number | Part Number |
|---|---|
| ADC0802LCV | ADC1025BCV |
| ADC0802LCWM | ADC1025CCV |
| ADC0804LCV | DAC0800LCM |
| ADC0804LCWM | DAC0801LCM |
| ADC0808CCV | DAC0802LCM |
| ADC0809CCV | DAC0806LCM |
| ADC0811BCV | DAC0807LCM |
| ADC0811CCV | DAC0808LCM |
| ADC0819BCV | DAC0830LCWM |
| ADC0819CCV | DAC0830LCV |
| ADC0820BCV | DAC0832LCWM |
| ADC0820CCV | DAC0832LCV |
| ADC0838BCV | |
| ADC0838CCV | |
| ADC0841BCV | |
| ADC0841CCV | |
| ADC0848BCV | |
| ADC0848CCV | |
| ADC1005BCV | |
| ADC1005CCV | |

### Industrial Functions

| Part Number | Part Number |
|---|---|
| AH5012CM | LM13600M |
| LF13331M | LM13700M |
| LF13509M | LMC555CM |
| LF13333M | LM567CM |
| LM555CM | MF4CWM-50 |
| LM556CM | MF4CWM-100 |
| LM567CM | MF6CWM-50 |
| LM1496M | MF10CCWM |
| LM2917M | MF6CWM-100 |
| LM3046M | MF5CWM |
| LM3086M | |
| LM3146M | |

### Commercial and Automotive

| Part Number | Part Number |
|---|---|
| LM386M-1 | LM1837M |
| LM592M | LM1851M |
| LM831M | LM1863M |
| LM832M | LM1865M |
| LM833M | LM1870M |
| LM837M | LM1894M |
| LM838M | LM1964V |
| LM1131CM | LM2893M |
| | LM3361AM |
| | LM1881M |

## Hybrids

| Part Number | Part Number |
|---|---|
| LH0002E<br>LH4002E | LH0032E<br>LH0033E |

**A FINAL WORD**

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

## Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

| Package | Package Designator | Max/Rail | Per Reel* |
|---|---|---|---|
| SO-8 | M | 100 | 2500 |
| SO-14 | M | 50 | 2500 |
| SO-14 Wide | WM | 50 | 1000 |
| SO-16 | M | 50 | 2500 |
| SO-16 Wide | WM | 50 | 1000 |
| SO-20 | M | 40 | 1000 |
| SO-24 | M | 30 | 1000 |
| PCL-20 | V | 50 | 1000 |
| PCL-28 | V | 40 | 1000 |
| PCL-44 | V | 25 | 500 |
| PQFP-196 | VF | TBD | — |
| TP-40 | TP | 100 | TBD |
| LCC-20 | E | 50 | — |
| LCC-44 | E | 25 | — |

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324M ICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324M ICs with date code A
    Pack #2 has 500 LM324M ICs with date code A
    Pack #3 has 2,000 LM324M ICs with date code B

## Short-Form Procurement Specification

**TAPE FORMAT**

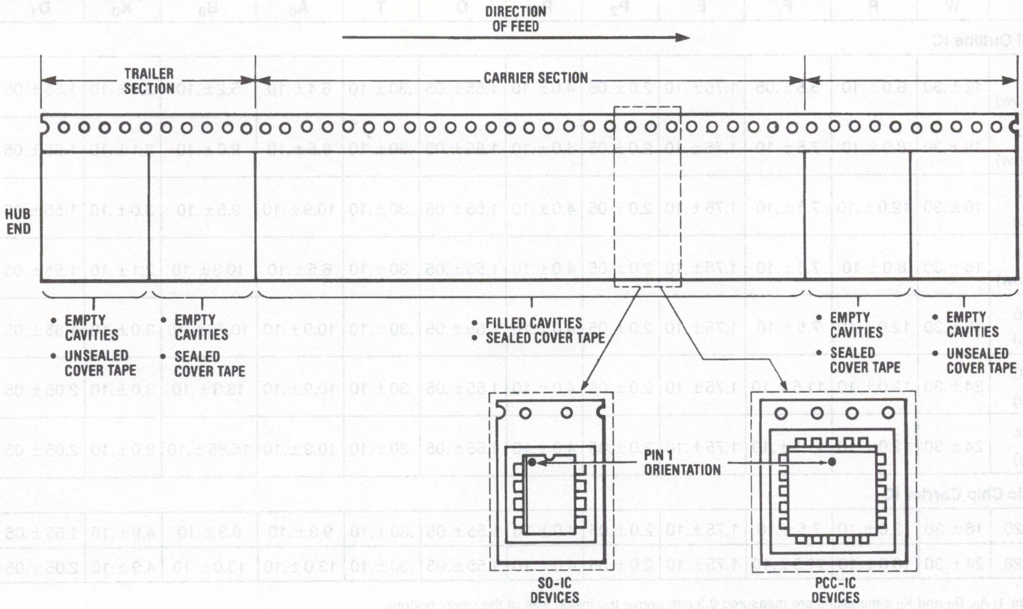
→ Direction of Feed

| | Trailer (Hub End)* | | Carrier* | Leader (Start End)* | |
|---|---|---|---|---|---|
| | Empty Cavities, min (Unsealed Cover Tape) | Empty Cavities, min (Sealed Cover Tape) | Filled Cavities (Sealed Cover Tape) | Empty Cavities, min (Sealed Cover Tape) | Empty Cavities, min (Unsealed Cover Tape) |
| **Small Outline IC** | | | | | |
| SO-8 (Narrow) | 2 | 2 | 2500 | 5 | 5 |
| SO-14 (Narrow) | 2 | 2 | 2500 | 5 | 5 |
| SO-14 (Wide) | 2 | 2 | 1000 | 5 | 5 |
| SO-16 (Narrow) | 2 | 2 | 2500 | 5 | 5 |
| SO-16 (Wide) | 2 | 2 | 1000 | 5 | 5 |
| SO-20 (Wide) | 2 | 2 | 1000 | 5 | 5 |
| SO-24 (Wide) | 2 | 2 | 1000 | 5 | 5 |
| **Plastic Chip Carrier IC** | | | | | |
| PCC-20 | 2 | 2 | 1000 | 5 | 5 |
| PCC-28 | 2 | 2 | 750 | 5 | 5 |
| PCC-44 | 2 | 2 | 500 | 5 | 5 |

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

# Short-Form Procurement Specification (Continued)

## DEVICE ORIENTATION

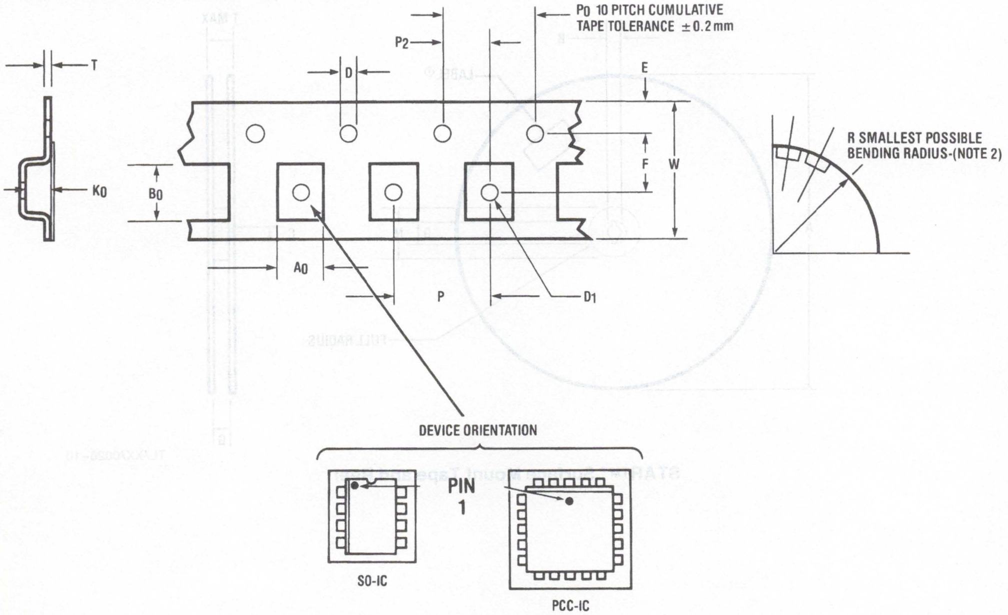

DIRECTION OF FEED
TRAILER SECTION
CARRIER SECTION
HUB END
• EMPTY CAVITIES
• UNSEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• FILLED CAVITIES
• SEALED COVER TAPE
• EMPTY CAVITIES
• SEALED COVER TAPE
• EMPTY CAVITIES
• UNSEALED COVER TAPE
PIN 1 ORIENTATION
SO-IC DEVICES
PCC-IC DEVICES

TL/XX/0026-8

## MATERIALS

- Cavity Tape: Conductive PVC (less than $10^5$ Ohms/Sq)
- Cover Tape: Polyester
  (1) Conductive cover available
- Reel:
  (1) Solid 80 pt fibreboard (standard)
  (2) Conductive fibreboard available
  (3) Conductive plastic (PVC) available

## TAPE DIMENSIONS (24 Millimeter Tape or Less)


T
K0
B0
P2
D
P0 10 PITCH CUMULATIVE TAPE TOLERANCE ±0.2 mm
E
F
W
A0
P
D1
R SMALLEST POSSIBLE BENDING RADIUS-(NOTE 2)
DEVICE ORIENTATION
PIN 1
SO-IC
PCC-IC

TL/XX/0026-9

## Short-Form Procurement Specification (Continued)

| | W | P | F | E | $P_2$ | $P_0$ | D | T | $A_0$ | $B_0$ | $K_0$ | $D_1$ | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Small Outline IC** | | | | | | | | | | | | | |
| SO-8 (Narrow) | 12 ± .30 | 8.0 ± .10 | 5.5 ± .05 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 6.4 ± .10 | 5.2 ± .10 | 2.1 ± .10 | 1.55 ± .05 | 30 |
| SO-14 (Narrow) | 16 ± .30 | 8.0 ± .10 | 7.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 6.5 ± .10 | 9.0 ± .10 | 2.1 ± .10 | 1.55 ± .05 | 40 |
| SO-14 (Wide) | 16 ± .30 | 12.0 ± .10 | 7.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 10.9 ± .10 | 9.5 ± .10 | 3.0 ± .10 | 1.55 ± .05 | 40 |
| SO-16 (Narrow) | 16 ± .30 | 8.0 ± .10 | 7.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 6.5 ± .10 | 10.3 ± .10 | 2.1 ± .10 | 1.55 ± .05 | 40 |
| SO-16 (Wide) | 16 ± .30 | 12.0 ± .10 | 7.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 10.9 ± .10 | 10.76 ± .10 | 3.0 ± .10 | 1.55 ± .05 | 40 |
| SO-20 (Wide) | 24 ± .30 | 12.0 ± .10 | 11.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 10.9 ± .10 | 13.3 ± .10 | 3.0 ± .10 | 2.05 ± .05 | 50 |
| SO-24 (Wide) | 24 ± .30 | 12.0 ± .10 | 11.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 10.9 ± .10 | 15.85 ± .10 | 3.0 ± .10 | 2.05 ± .05 | 50 |
| **Plastic Chip Carrier IC** | | | | | | | | | | | | | |
| PCC-20 | 16 ± .30 | 12.0 ± .10 | 7.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 9.3 ± .10 | 9.3 ± .10 | 4.9 ± .10 | 1.55 ± .05 | 40 |
| PCC-28 | 24 ± .30 | 16.0 ± .10 | 11.5 ± .10 | 1.75 ± .10 | 2.0 ± .05 | 4.0 ± .10 | 1.55 ± .05 | .30 ± .10 | 13.0 ± .10 | 13.0 ± .10 | 4.9 ± .10 | 2.05 ± .05 | 50 |

**Note 1:** $A_0$, $B_0$ and $K_0$ dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

**Note 2:** Tape with components shall pass around a mandril radius R without damage.

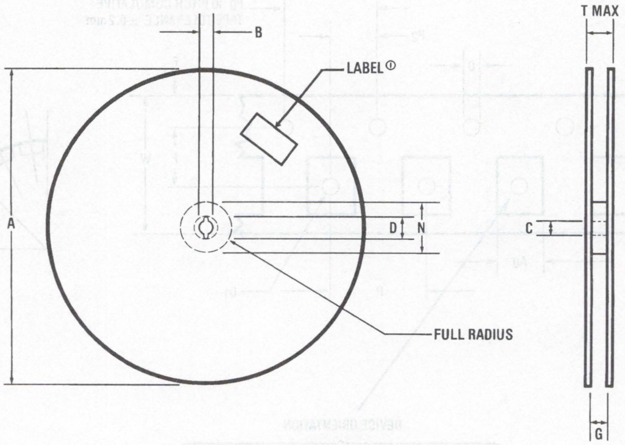
**Note 3:** Cavity tape material shall be PVC conductive (less than $10^5$ Ohms/Sq).

**Note 4:** Cover tape material shall be polyester (30–65 grams peel-back force).

**Note 5:** $D_1$ Dimension is centered within cavity.

**Note 6:** All dimensions are in millimeters.

### REEL DIMENSIONS



STAR™* Surface Mount Tape and Reel

## Short-Form Procurement Specifications (Continued)

| | | A (Max) | B (Min) | C | D (Min) | N (Min) | G | T (Max) |
|---|---|---|---|---|---|---|---|---|
| 12 mm Tape | SO-8 (Narrow) | (13.00)<br>(330) | .059<br>1.5 | .512 ± .002<br>13 ± 0.05 | .795<br>20.2 | 1.969<br>50 | $0.488^{+.078}_{-.000}$<br>$12.4^{+2}_{-0}$ | .724<br>18.4 |
| 16 mm Tape | SO-14 (Narrow)<br>SO-14 (Wide)<br>SO-16 (Narrow)<br>SO-16 (Wide)<br>PCC-20 | (13.00)<br>(330) | .059<br>1.5 | .512 ± .002<br>13 ± 0.05 | .795<br>20.2 | 1.969<br>50 | $0.646^{+.078}_{-.000}$<br>$16.4^{+2}_{-0}$ | .882<br>22.4 |
| 24 mm Tape | SO-20 (Wide)<br>SO-24 (Wide)<br>PCC-28 | (13.00)<br>(330) | .059<br>1.5 | .512 ± .002<br>13 ± 0.05 | .795<br>20.2 | 1.969<br>50 | $0.960^{+.078}_{-.000}$<br>$24.4^{+2}_{-0}$ | 1.197<br>30.4 |
| 32 mm Tape | PCC-44 | (13.00)<br>(330) | .059<br>1.5 | .512 ± .002<br>13 ± 0.05 | .795<br>20.2 | 1.969<br>50 | $1.276^{+.078}_{-.000}$<br>$32.4^{+2}_{-0}$ | 1.512<br>38.4 |

**Units:** $\frac{\text{Inches}}{\text{Millimeters}}$

**Material: Paperboard (Non-Flaking)**

**LABEL**

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

**FIELD**

Lot Number

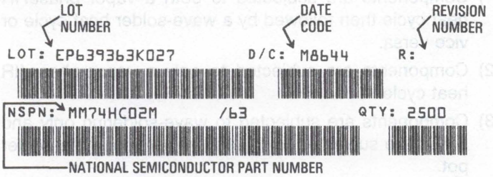
Date Code

Revision Level

National Part No. I.D.

Qty.

**EXAMPLE**



TL/XX/0026-11

Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.) National Semiconductor will also offer additional labels containing information per your specific specification.

## Wave Soldering of Surface Mount Components

### ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

### ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

## Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

### PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.

b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.

1. Components on the same side of PW Board.

   Lead insert standard DIPS onto PW Board Wave solder (conventional)

   Wash and lead trim

   Dispense solder paste on SMD pads

   Pick and place SMDs onto PW Board

   Bake

   Vapor phase/IR reflow

   Clean

2. Components on opposite side of PW Board.

   Lead insert standard DIPs onto PW Board

   Wave Solder (conventional)

   Clean and lead trim

   Invert PW Board

   Dispense solder paste on SMD pads

   Dispense drop of adhesive on SMD sites (optional for smaller components)

   Pick and place SMDs onto board

   Bake/Cure

   Invert board to rest on raised fixture

   Vapor/IR reflow soldering

   Clean

B) Vapor/IR reflow solder then Wave Solder.

1. Components on the same side of PW Board.

   Solder paste screened on SMD side of Printed Wire Board

   Pick and place SMDs

   Bake

   Vapor/IR reflow

   Lead insert on same side as SMDs

   Wave solder

   Clean and trim underside of PCB

C) Vapor/IR reflow only.

1. Components on the same side of PW Board.

   Trim and form standard DIPs in "gull wing" configuration

   Solder paste screened on PW Board

   Pick and place SMDs and DIPs

   Bake

   Vapor/IR reflow

   Clean

2. Components on opposite sides of PW Board.

   Solder paste screened on SMD-side of Printed Wire Board

   Adhesive dispensed at central location of each component

   Pick and place SMDs

   Bake

   Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads

   Lead insert DIPs

   Vapor/IR reflow

   Clean and lead trim

D) Wave Soldering Only

1. Components on opposite sides of PW Board.

   Adhesive dispense on SMD side of PW Board

   Pick and place SMDs

   Cure adhesive

   Lead insert top side with DIPs

   Wave solder with SMDs down and into solder bath

   Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

# Wave Soldering of Surface Mount Components (Continued)

## THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. Howerver, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

## CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.

2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

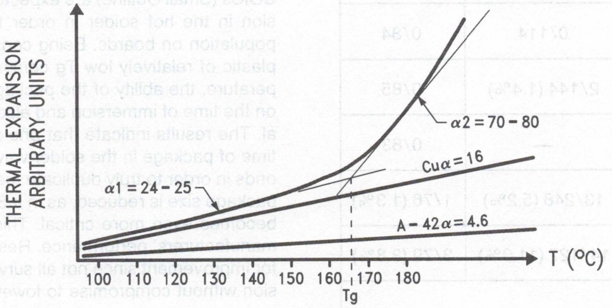


FIGURE 1. Thermal Expansion and Glass Transition Temperature

## EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

## VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

## BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

# Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

## TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

**TABLE IV. Vapor Phase vs. Wave Solder**

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

**TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)**

| | Unmounted | Mounted |
|---|---|---|
| Control/Vapor Phase 15 sec @ 215°C | 0/114 | 0/84 |
| Solder Dip 2 sec @ 260°C | 2/144 (1.4%) | 0/85 |
| Solder Dip 4 sec @ 260°C | — | 0/83 |
| Solder Dip 6 sec @ 260°C | 13/248 (5.2%) | 1/76 (1.3%) |
| Solder Dip 10 sec @ 260°C | 14/127 (11.0%) | 3/79 (3.8%) |

Package: SO-14 lead
Device: LM324M

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

**TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)**

| Package SO-8 | Vapor Phase 30 sec | Wave Solder 2 sec | Wave Solder 4 sec | Wave Solder 6 sec | Wave Solder 10 sec |
|---|---|---|---|---|---|
| Manuf A | 8/30* | 1/30* | 0.30 | 12/30* | 16/30* |
| Manuf B | 2/30* | 8/30* | 2/30* | 22/30* | 20/30* |
| Manuf C | 0/30 | 0/29 | 0/29 | 0/30 | 0/30 |
| Manuf D | 1/30* | 0/30 | 12/30* | 14/30* | 2/30* |
| Manuf E | 1/30** | 0/30 | 0/30 | 0/30 | 0/30 |
| Manuf F | 0/30 | 0/30 | 0/30 | 0/30 | 0/30 |
| Manuf G | 0/30 | 0/30 | 0/30 | 0/30 | 0/30 |

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

## SUMMARY

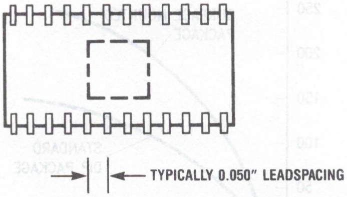
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

# Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

### COMPONENT SIZE COMPARISON

**S.O. Package**



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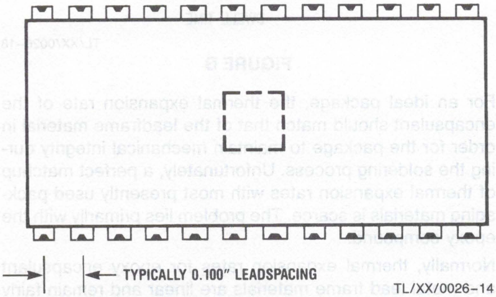
**Standard DIP Package**



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

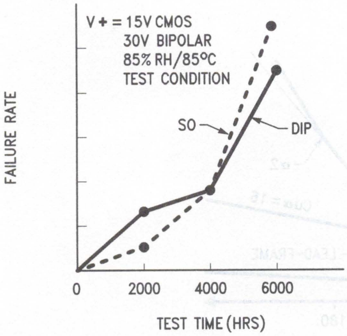

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**FIGURE A**

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

### SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

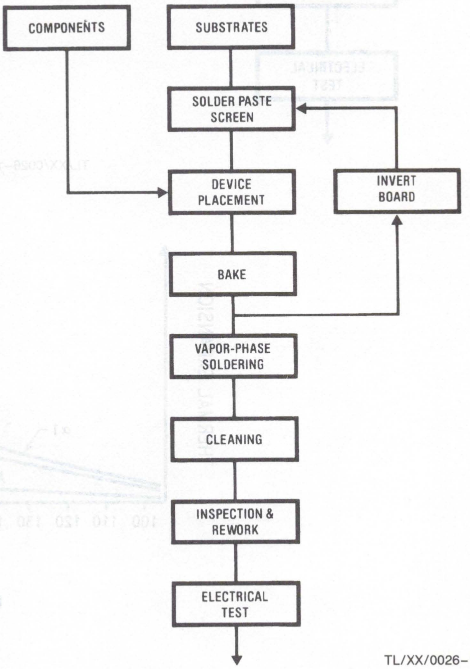
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

### PRODUCTION FLOW

**Basic Surface-Mount Production Flow**



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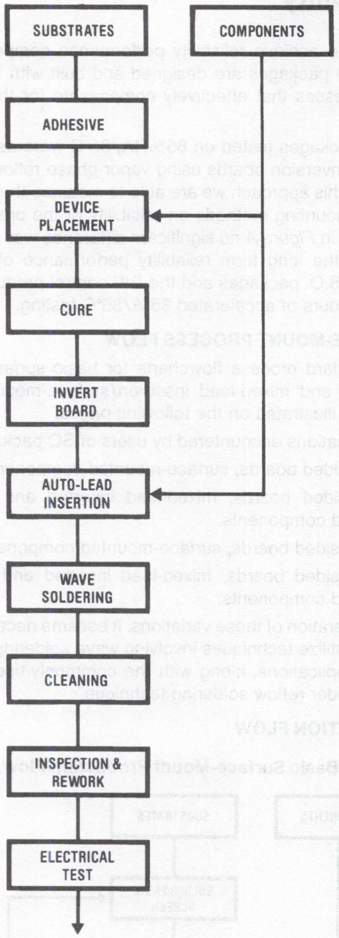
**Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow**



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

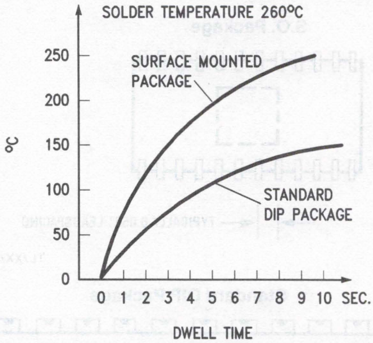

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**FIGURE B**

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature ($T_g$) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

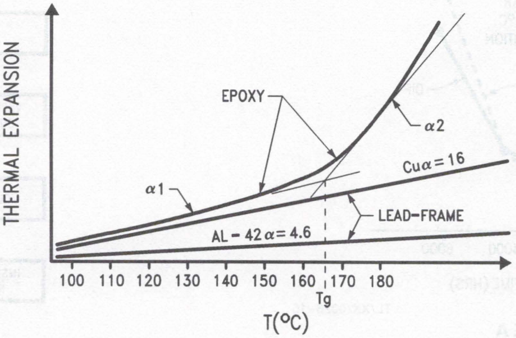

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**FIGURE C**

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

*Figure D* is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package
Group 2 — SO packages vapor-phase reflow soldered on PC boards
Group 3–6 SO packages wave soldered on PC boards
Group 3 — dwell time 2 seconds
4 — dwell time 4 seconds
5 — dwell time 6 seconds
6 — dwell time 10 seconds

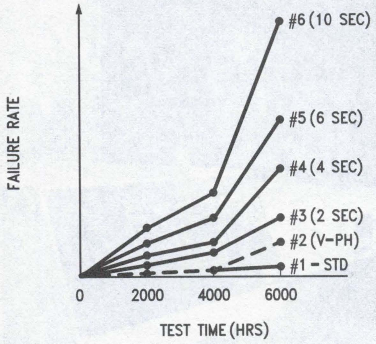

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**FIGURE D**

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

## PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement
  - Fixed placement stations
  - Boards indexed under head and respective components placed

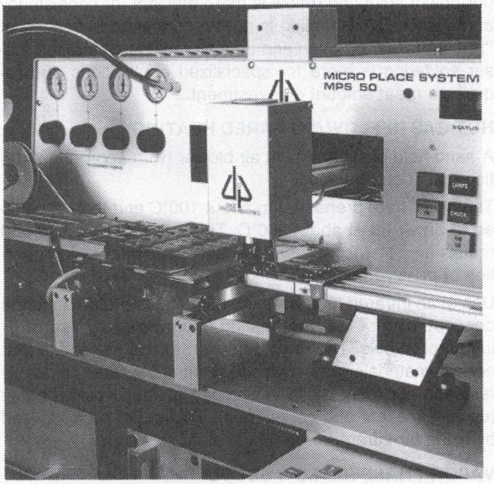
(b) Sequential placement
  - Either a X-Y moving table system or a $\theta$, X-Y moving pickup system used
  - Individual components picked and placed onto boards

(c) Simultaneous placement
  - Multiple pickup heads
  - Whole array of components placed onto the PCB at the same time

(d) Sequential/simultaneous placement
  - X–Y moving table, multiple pickup heads system
  - Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

**Pick and Place Action**



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## BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

## REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

## HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

## VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

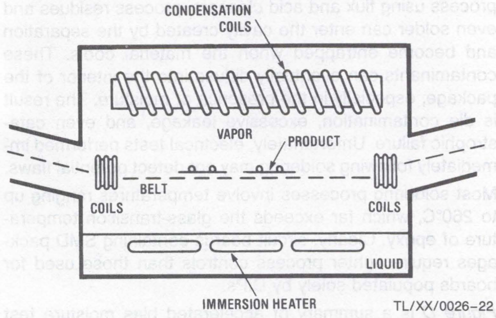
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

**In-Line Conveyorized Vapor-Phase Soldering**



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The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

**Vapor-Phase Furnace**

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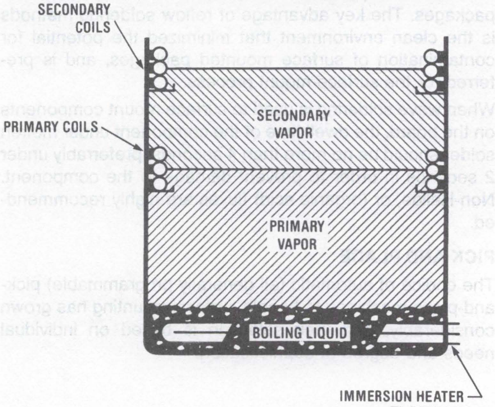
**Batch-Fed Production Vapor-Phase Soldering Unit**



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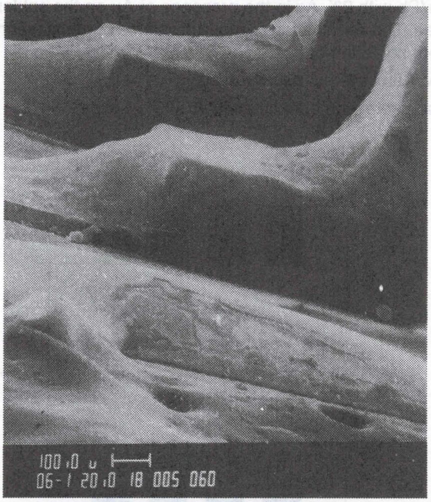
Solder Joints on a SO-14 Package on PCB



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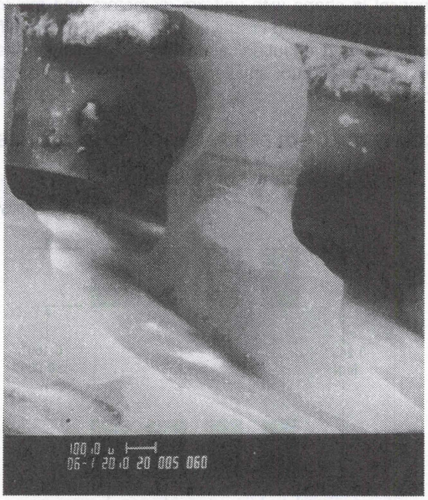
Solder Joints on a SO-14 Package on PCB



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## PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

## SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed ⅛″, to avoid damage to screens and minimize distortion.

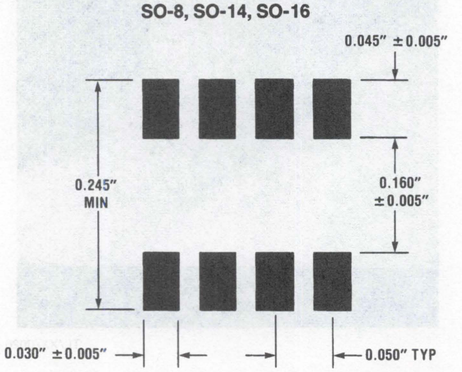
## SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.

## RECOMMENDED SOLDER PADS FOR SO PACKAGES


SO-8, SO-14, SO-16
0.045″ ±0.005″
0.245″ MIN
0.160″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

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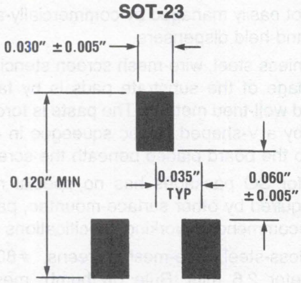
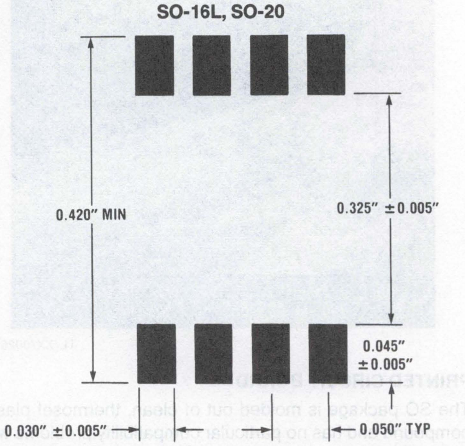

SOT-23
0.030″ ±0.005″
0.120″ MIN
0.035″ TYP
0.060″ ±0.005″

TL/XX/0026-29

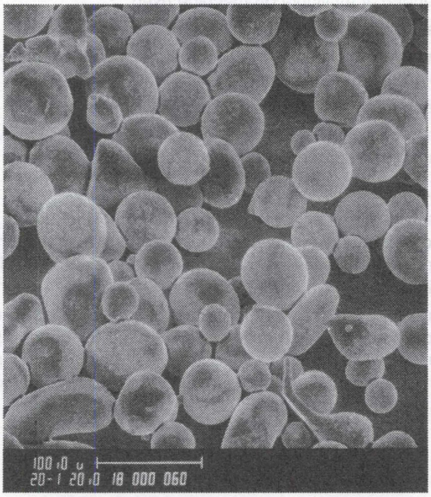
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.


SO-16L, SO-20
0.420″ MIN
0.325″ ±0.005″
0.045″ ±0.005″
0.030″ ±0.005″
0.050″ TYP

TL/XX/0026-28

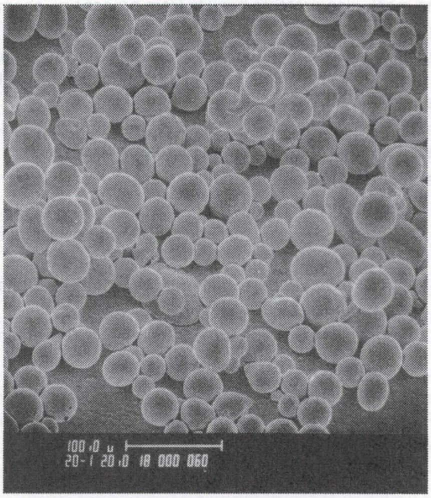
### Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)


100.0 u
20-1 20.0 18 000 060

TL/XX/0026-30

200 × Kester (63/37)


100.0 u
20-1 20.0 18 000 060

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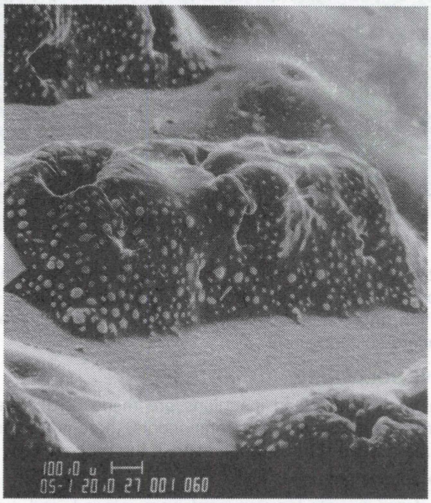
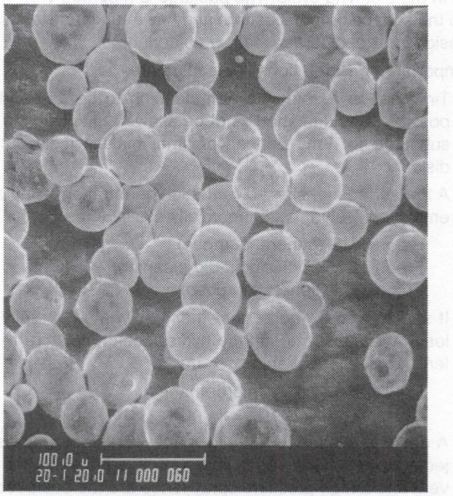
## Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

**Solder Paste Screen on Pads**


100.0 u
05-1 20.0 27 001 060

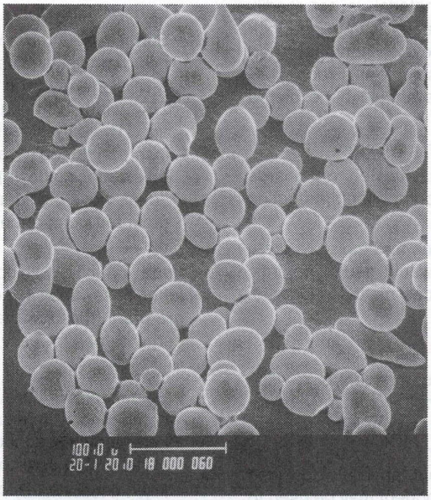
TL/XX/0026-32

**200 × Fry Metal (63/37)**


100.0 u
20-1 20.0 11 000 060

TL/XX/0026-33

**200 ESL (63/37)**


100.0 u
20-1 20.0 18 000 060

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## CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

    Freon TMS (general purpose)
    Freon TE35/TP35 (cold-dip cleaning)
    Freon TES (general purpose)

    It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

    Prelete or 1,1,1-Trichloroethane
    Kester 5120/5121

- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

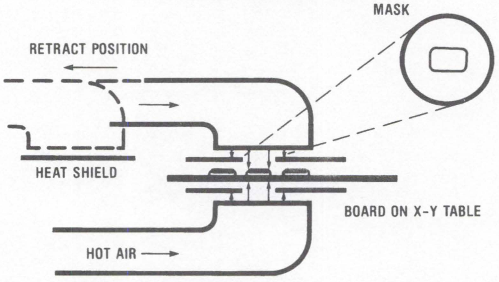
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

## REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

**Hot-Air Solder Rework Station**



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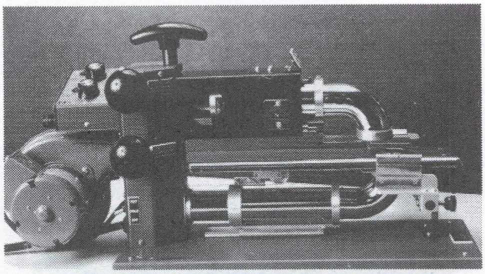
**Hot-Air Rework Machine**



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## WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

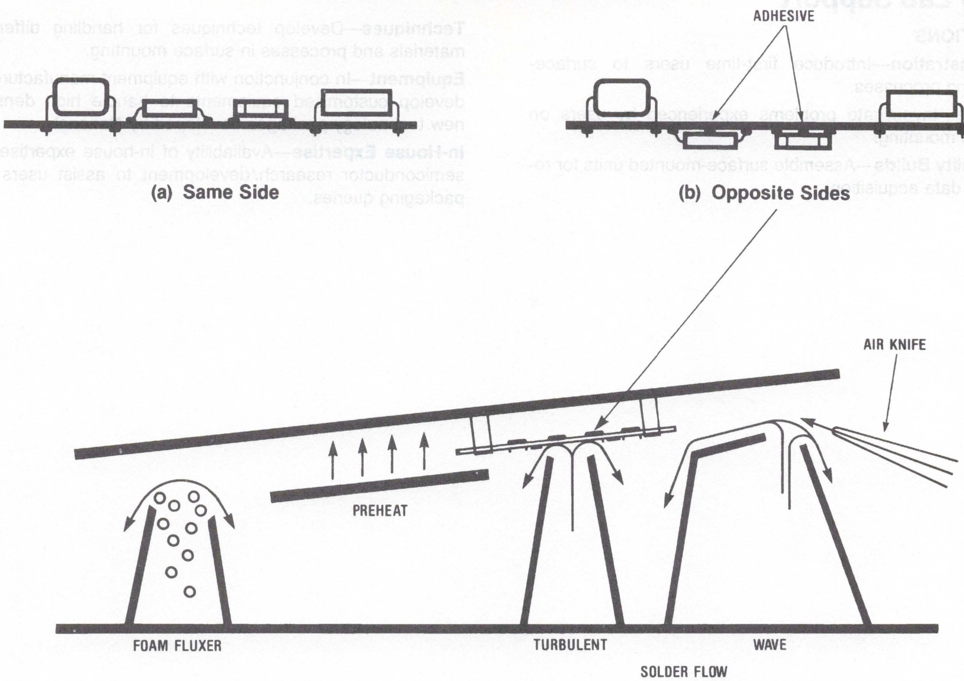
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

**Mixed Surface Mount and Lead Insertion**



(a) Same Side

(b) Opposite Sides

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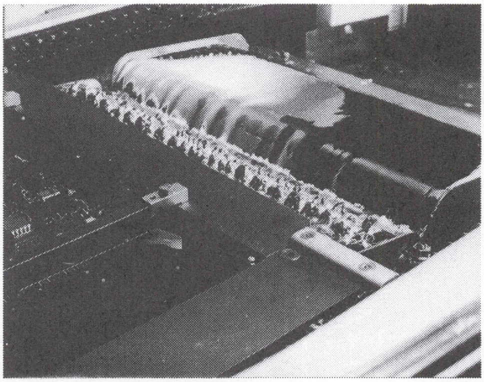
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

## AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

**Dual Wave**



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## CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

## SMD Lab Support

### FUNCTIONS

**Demonstration**—Introduce first-time users to surface-mounting processes.

**Service**—Investigate problems experienced by users on surface mounting.

**Reliability Builds**—Assemble surface-mounted units for reliability data acquisition.

**Techniques**—Develop techniques for handling different materials and processes in surface mounting.

**Equipment**—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

**In-House Expertise**—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

## Section 7

# Appendices/ Physical Dimensions

## Section 7 Contents

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Data Bookshelf
Distributors

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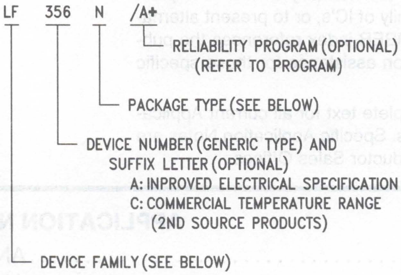
# Appendix A
# General Product Marking & Code Explanation


LF
356
N
/A+
RELIABILITY PROGRAM (OPTIONAL)
(REFER TO PROGRAM)
PACKAGE TYPE (SEE BELOW)
DEVICE NUMBER (GENERIC TYPE) AND
SUFFIX LETTER (OPTIONAL)
A: IMPROVED ELECTRICAL SPECIFICATION
C: COMMERCIAL TEMPERATURE RANGE
(2ND SOURCE PRODUCTS)
DEVICE FAMILY (SEE BELOW)

TL/XX/0027–1

## Device Family

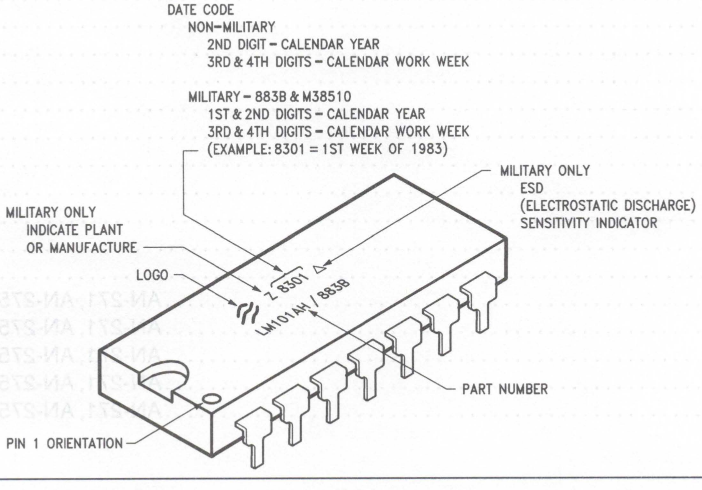
**Integrated Circuits (IC's)**

| | |
|---|---|
| ADC | Data Conversion |
| AF | Active Filter |
| AH | Analog Switch (Hybrid) |
| AM | Analog Switch (Monolithic) |
| DAC | Data Conversion |
| DM | Digital (Monolithic) |
| HS | Hybrid |
| LF | Linear (Bifet) |
| LH | Linear (Hybrid) |
| LM | Linear (Monolithic) |
| LMC | Linear CMOS |
| LP | Linear (Low Power) |
| MF | Linear (Monolithic Filter) |
| SL | Special Linear |
| LMF | Linear Monolithic Filter |

## Package Type*

**IC's Only**

| | | |
|---|---|---|
| D | Glass/Metal DIP | |
| E | Ceramic Leadless Chip Carrier (LCC) | |
| F | Glass/Metal Flat Pak (¼″ x ¼″) | |
| G | 12 Lead TO-8 M/C | |
| H | Multi-Lead M/C | |
| H-05 | 4 Lead M/C (TO-5) | Shipped with Thermal Shield |
| H-46 | 4 Lead M/C (TO-46) | |
| J | Lo-Temp Ceramic DIP (Sometimes referred to as the "Fit-Seal" Package). | |
| J-8 | 8 Lead Ceramic DIP ("MiniDIP") | |
| J-14 | 14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg). | |
| K | TO-3 M/C in Steel, except LM309K which is shipped in Aluminum | |
| KC | TO-3 M/C (Aluminum) | |
| K Steel | TO-3 M/C (Steel) | |
| M | Small Outline Package | |
| N | Molded DIP (EPOXY B) | |
| N-01 | Molded DIP (Epoxy B) with Staggered Leads | |
| N-8 | 8 Lead Molded DIP (Epoxy B) ("Mini-DIP") | |
| N-14 | 14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg). | |
| P | 3 Lead TO-202 PWR Pkg | |
| Q | Cerdip with UV Window | |
| T | 3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B) | |
| V | Multi-lead Plastic Chip Carrier (PCC) | |
| W | Lo-Temp Ceramic Flat Pak | |
| WM | Wide Body Small Outline Package | |


DATE CODE
NON-MILITARY
2ND DIGIT – CALENDAR YEAR
3RD & 4TH DIGITS – CALENDAR WORK WEEK
MILITARY – 883B & M38510
1ST & 2ND DIGITS – CALENDAR YEAR
3RD & 4TH DIGITS – CALENDAR WORK WEEK
(EXAMPLE: 8301 = 1ST WEEK OF 1983)
MILITARY ONLY
ESD
(ELECTROSTATIC DISCHARGE)
SENSITIVITY INDICATOR
MILITARY ONLY
INDICATE PLANT
OR MANUFACTURE
LOGO
Z 8301 △
LM101AH / 883B
PART NUMBER
PIN 1 ORIENTATION

TL/XX/0027–2

**National Semiconductor Corporation**

# Appendix B

## APPLICATION NOTE REFERENCED BY PART NUMBER

National Semiconductor Linear Application notes are normally written to explain the operation and use of a particular device or family of IC's, or to present alternative technical solutions. The following PART NUMBER index references the published application notes that would offer application assistance for those specific IC's.

The 1986 Linear Applications Handbook is a complete text for all current Application Notes for both Monolithic and Hybrid products. Specific Application Notes are available upon request through National Semiconductor Sales Offices.

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| ADCXXXX | AN-156 |
| ADC80 | AN-360 |
| ADC0801 | AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53 |
| ADC0802 | AN-233, AN-274, AN-280, AN-281, LB-53 |
| ADC0803 | AN-233, AN–274, AN-280, AN-281, LB-53 |
| ADC0804 | AN-233, AN-274, AN-276, AN-280, AN-281, LB-53 |
| ADC0805 | AN-233, AN-274, AN-280, AN-281, LB-53 |
| ADC0808 | AN-247, AN-280, AN-281 |
| ADC0809 | AN-247, AN-280 |
| ADC0816 | AN-193, AN-247, AN-258, AN-280 |
| ADC0817 | AN-247, AN-258, AN-280 |
| ADC0820 | AN-237 |
| ADC0831 | AN-280, AN-281 |
| ADC0832 | AN-280, AN-281 |
| ADC0833 | AN-280, AN-281 |
| ADC0834 | AN-280, AN-281 |
| ADC0838 | AN-280, AN-281 |
| ADC1001 | AN-276, AN-280, AN-281 |
| ADC1005 | AN-280 |
| ADC1210 | AN-245 |
| ADC3501 | AN-200, AN-202 |
| ADC3511 | AN-200 |
| ADC3701 | AN-200 |
| ADC3711 | AN-200 |
| AH0014 | AN-38 |
| AH0019 | AN-38 |
| CD4016 | AB-10 |
| DACXXXX | AN-156 |
| DAC0830 | AN-284 |
| DAC0831 | AN-271, AN-284 |
| DAC0832 | AN-271, AN-284 |
| DAC1000 | AN-271, AN-275, AN-277, AN-284 |
| DAC1001 | AN-271, AN-275, AN-277, AN-284 |
| DAC1002 | AN-271, AN-275, AN-277, AN-284 |
| DAC1006 | AN-271, AN-275, AN-277, AN-284 |
| DAC1007 | AN-271, AN-275, AN-277, AN-284 |

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| DAC1008 | AN-271, AN-275, AN-277, AN-284 |
| DAC1020 | AN-263, AN-269, AN-293, AN-294, AN-299 |
| DAC1021 | AN-269 |
| DAC1022 | AN-269 |
| DAC1208 | AN-271, AN-284 |
| DAC1209 | AN-271, AN-284 |
| DAC1210 | AN-271, AN-284 |
| DAC1218 | AN-293 |
| DAC1220 | AN-253, AN-269 |
| DAC1221 | AN-269 |
| DAC1222 | AN-269 |
| DAC1230 | AN-284 |
| DAC1231 | AN-271, AN-284 |
| DAC1232 | AN-271, AN-284 |
| DAC1280 | AN-261, AN-263 |
| DH0034 | AN-253 |
| DH0035 | AN-49 |
| DS8606 | AN-381, AN-382 |
| DS8608 | AN-382 |
| DT1058 | AN-287 |
| DT1060 | AN-287 |
| DTSW250E2 | AN-287 |
| DTSW250GI | AN-287 |
| INS8070 | AN-260 |
| LF111 | LB-39 |
| LF155 | AN-263, AN-447 |
| LF198 | AN-245, AN-294 |
| LF311 | AN-301 |
| LF347 | AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447 |
| LF351 | AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C |
| LF351A | AN-240 |
| LF351B | Appendix D |
| LF353 | AN-256, AN-258, AN-263, AN-264, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D |
| LF356 | AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447 |
| LF357 | AN-263, AN-447, LB-42 |
| LF398 | AN-247, AN-258, AN-266, AN-294, AN-298, LB-45 |
| LF400 | AN-428, AN-447 |
| LF411 | AN-294, AN-301, AN-344, AN-447 |
| LF412 | AN-272, AN-299, AN-301, AN-344, AN-447 |
| LF441 | AN-301, AN-447 |
| LF13006 | AN-344 |
| LF13007 | AN-344 |
| LF13331 | AN-294, AN-447 |
| LF13508 | AN-289, AN-360, AN-447 |
| LF13509 | AN-289, AN-295, AN-447 |
| LH0002 | AN-13, AN-63, AN-227, AN-244, AN-263, AN-272, AN-301 |
| LH0022 | AN-63, AN-75 |
| LH0023 | AN-245, AN-360 |
| LH0024 | AN-253 |
| LH0032 | AN-242, AN-244, AN-253 |
| LH0033 | AN-48, AN-115, AN-227, AN-253 |
| LH0042 | AN-63 |

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| LH0043 | AN-245 |
| LH0052 | AN-63 |
| LH0053 | AN-245 |
| LH0062 | AN-75 |
| LH0063 | AN-227 |
| LH0070 | AN-301 |
| LH0071 | AN-245 |
| LH0082 | AN-244, AN-266 |
| LH0086 | AN-245, AN-360 |
| LH0091 | AN-180 |
| LH0094 | AN-301 |
| LH0101 | AN-261 |
| LH1605 | AN-343 |
| LM10 | AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300 |
| LM11 | AN-241, AN-242, AN-260, AN-266, AN-271 |
| LM12 | AN-446 |
| LM101 | AN-4, AN-13, AN-20, AN-24, AN-75, LB-42, Appendix A |
| LM101A | AN-29, AN-30, AN-31, AN-79, AN-241, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28 |
| LM102 | AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11 |
| LM103 | AN-110, LB-41 |
| LM104 | AN-21, LB-3, LB-7, LB-10, LB-40 |
| LM105 | AN-21, AN-23, AN-110, LB-3, LB-7, LB-10 |
| LM106 | AN-41, LB-6, LB-12 |
| LM107 | AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A |
| LM108 | AN-29, AN-30, AN-31, AN-63, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21 |
| LM108A | AN-260, LB-15, LB-19 |
| LM109 | AN-42, LB-15 |
| LM109A | LB-15 |
| LM110 | LB-11, LB-42 |
| LM111 | AN-41, AN-103, LB-12, LB-16, LB-32, LB-39 |
| LM112 | AN-63, LB-19 |
| LM113 | AN-56, AN-110, LB-21, LB-24, LB-28, LB-37 |
| LM117 | AN-178, AN-181, AN-182, LB-46, LB-47 |
| LM117HV | LB-46, LB-47 |
| LM118 | LB-17, LB-19, LB-21, LB-23, Appendix A |
| LM119 | AN-115, LB-23 |
| LM120 | AN-182 |
| LM121 | AN-79, AN-104, AN-184, AN-260, LB-22 |
| LM121A | LB-32 |
| LM122 | AN-97, LB-38 |
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| LM126 | AN-82 |
| LM129 | AN-173,AN-178, AN-262, AN-266 |
| LM131 | AN-210, Appendix D |
| LM131A | AN-210 |
| LM134 | LB-41 |
| LM135 | AN-225, AN-262, AN-292, AN-298 |
| LM137 | LB-46 |
| LM137HV | LB-46 |
| LM138 | LB-46 |
| LM139 | AN-74 |
| LM143 | AN-127, AN-271 |
| LM148 | AN-260 |

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| LM150 | LB-46 |
| LM158 | AN-116 |
| LM160 | AN-87 |
| LM161 | AN-87, AN-266 |
| LM163 | AN-295 |
| LM194 | AN-222, LB-21 |
| LM195 | AN-110 |
| LM199 | AN-161, AN-260, AN-360 |
| LM199A | AN-161 |
| LM211 | LB-39 |
| LM216A | LB-37 |
| LM231 | AN-210 |
| LM231A | AN-225 |
| LM235 | AN-225 |
| LM239 | AN-74 |
| LM258 | AN-116 |
| LM260 | AN-87 |
| LM261 | AN-87 |
| LM301A | AN-178, AN-181, AN-222 |
| LM304 | LB-40 |
| LM308 | AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D |
| LM308A | AN-225, LB-24 |
| LM309 | AN-178, AN-182 |
| LM311 | AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39 |
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| LM316 | AN-258 |
| LM317 | AN-178, LB-35, LB-46 |
| LM317H | LB-47 |
| LM318 | AN-115, AN-299, LB-21 |
| LM319 | AN-115, AN-271, AN-293 |
| LM320 | AN-288 |
| LM321 | LB-24 |
| LM324 | AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C |
| LM329 | AN-256, AN-263, AN-284, AN-295, AN-301 |
| LM329B | AN-225 |
| LM330 | AN-301 |
| LM331 | AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix, C Appendix D |
| LM331A | AN-210, Appendix C |
| LM334 | AN-242, AN-256, AN-284 |
| LM335 | AN-225, AN-263, AN-295 |
| LM336 | AN-202, AN-247, AN-258 |
| LM337 | LB-46 |
| LM338 | LB-49, LB-51 |
| LM339 | AN-74, AN-245, AN-274 |
| LM340 | AN-103, AN-182 |
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| LM342 | AN-288 |
| LM346 | AN-202, LB-54 |
| LM347 | LB-44 |
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| LM349 | LB-42 |
| LM358 | AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C |
| LM358A | Appendix D |

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| LM359 | AN-278, AB-24 |
| LM360 | AN-87 |
| LM361 | AN-87, AN-294 |
| LM363 | AN-271 |
| LM380 | AN-69, AN-146 |
| LM381 | AN-64, AN-104 |
| LM382 | AN-147 |
| LM385 | AN-242, AN-256, AN-301, AN-344 |
| LM386 | LB-54 |
| LM389 | AN-256, AN-263, AN-264, AN-274 |
| LM391 | AN-272 |
| LM392 | AN-274, AN-286 |
| LM393 | AN-271, AN-274, AN-293 |
| LM394 | AN-262, AN-263, AN-264, AN-271, AN-293, AN-299, AN-311, LB-52 |
| LM395 | AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, LB-28 |
| LM399 | AN-184 |
| LM555 | AB-7 |
| LM556 | AB-7 |
| LM565 | AN-46, AN-146 |
| LM566 | AN-146 |
| LM567 | AN-46 |
| LM709 | AN-24, AN-30 |
| LM710 | AN-41, LB-12 |
| LM725 | LB-22 |
| LM741 | AN-75, AN-79, LB-19, LB-22 |
| LM832 | AN-386, AN-390 |
| LM833 | AN-346 |
| LM1036 | AN-390 |
| LM1310 | AN-81 |
| LM1524 | AN-272, AN-288, AN-292, AN-293 |
| LM1800 | AN-81, AN-147 |
| LM1812 | AB-20 |
| LM1818 | AN-407 |
| LM1820 | LB-29 |
| LM1823 | AN-391 |
| LM1828 | Appendix B |
| LM1830 | AB-10 |
| LM1837 | AN-407 |
| LM1845 | Appendix B |
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| LM1865 | AN-382, AN-390 |
| LM1870 | AN-382 |
| LM1886 | AN-402 |
| LM1889 | AN-402 |
| LM1894 | AN-384, AN-386, AN-390 |
| LM1897 | AN-407 |
| LM2878 | AN-147 |
| LM2889 | AN-391, AN-402 |
| LM2907 | AN-162 |
| LM2917 | AN-162 |
| LM2931 | AB-12 |
| LM2931CT | AB-11 |

| DEVICE NUMBER | APPLICATION NOTE |
|---|---|
| LM3045 | AN-286 |
| LM3046 | AN-146, AN-299 |
| LM3089 | AN-147 |
| LM3524 | AN-272, AN-288, AN-292, AN-293 |
| LM3820 | AN-147, LB-29 |
| LM3900 | AN-72, AN-263, AN-274, AN-278, LB-20, AB-24 |
| LM3909 | AN-154 |
| LM3911 | LB-27 |
| LM3914 | LB-48, AB-25 |
| LM3915 | AN-386 |
| LM3999 | AN161 |
| LM4250 | AN-88, LB-34 |
| LM7800 | AN-178 |
| LM78L12 | AN-146 |
| LMC835 | AN-435 |
| LP324 | AN-284 |
| MF10 | AN-307 |
| MM1458 | AN-116 |
| MM1558 | AN-116 |
| MM1558C | AN-116 |
| MM2716 | LB-54 |
| MM54104 | AN-252, AN-287, LB-54 |
| MM57110 | AN-382 |
| MM74C00 | AN-88 |
| MM74C02 | AN-88 |
| MM74C04 | AN-88 |
| MM74C948 | AN-193 |
| MM74LS138 | LB-54 |
| 2N4339 | AN-32 |
| LH4101 | AN-480 |
| LM34/35 | AN-460 |
| LM32900 | AN-478 |
| LM3578 | AB-30 |
| LPXXXX | AN-462 |
| LM34 | AN-462 |
| LM35 | AN-462 |
| LM385 | AN-462 |
| LMC13334 | AN-462 |
| LP2950 | AN-462 |
| LP2951 | AN-462 |
| LP311 | AN-462 |
| LP324 | AN-462 |
| LP339 | AN-462 |
| LP365 | AN-462 |

National
Semiconductor
Corporation

# Appendix C
# Summary of Commercial Reliability Programs

## General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

## A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

**Note:** Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

## P+ Product Enhancement

The P+ product enhancement program applies to regulator devices and offers an added advantage. P+ involves a dynamic self-heating burn-in that tests the thermal shutdown of the regulator. P+ is proven more effective than the standard 125°C burn-in as an early screen for infant mortality defects. It sharply reduces the cost of testing incoming components. Reliability Report L-140 further explains the P+ process. The following chart lists regulators which receive P+ prior to shipment and at no additional cost.

| Device | Package Types | | | | |
|---|---|---|---|---|---|
| | TO-3 K STEEL | TO-39 H | TO-220 T | TO-202 P | TO-92 Z |
| LM109/309 | X | X | | | |
| LM117/317 | X | X | X | X | |
| LM117HV/317HV | X | X | | | |
| LM120/320 | X | X | X | X | |
| LM123/323 | X | | | | |
| LM137/337 | X | X | X | X | |
| LM137HV/337HV | X | X | | | |
| LM138/338 | X | | | | |
| LM140/340 | X | X | X | X | |
| LM145/345 | X | | | | |
| LM150/250/350 | X | | | | |
| LM196/396 | X | | | | |
| LM2930/2935/2940/2984 | | | X | | |
| LM2931 | | | X | | X |
| LM78XX | | | X | | |

**National Semiconductor Corporation**

# Appendix D
# Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

## MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government-certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

## DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales offices, or DESC. DESC is located in Dayton, Ohio.

## MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

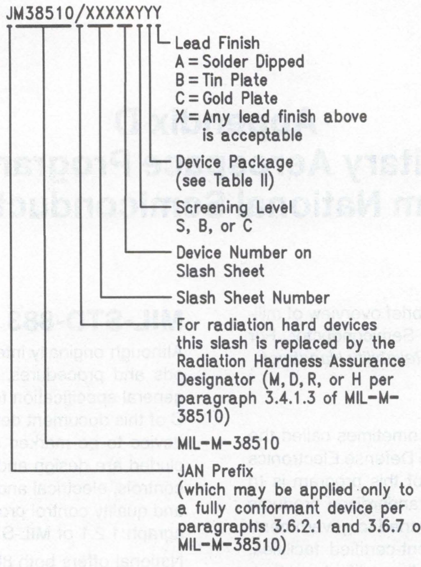
As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

## Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

## TABLE I. The MIL-M-38510 Part Marking


JM38510/XXXXXXYYY
Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable
Device Package (see Table II)
Screening Level S, B, or C
Device Number on Slash Sheet
Slash Sheet Number
For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H per paragraph 3.4.1.3 of MIL-M-38510)
MIL-M-38510
JAN Prefix (which may be applied only to a fully conformant device per paragraphs 3.6.2.1 and 3.6.7 of MIL-M-38510)

CI24-1

## TABLE II. JAN Package Codes

| 38510 Package Designation | Microcircuit Industry Description |
|---|---|
| A | 14-Pin 1/4″ X 1/4″ (metal) flat pack |
| B | 14-Pin 3/16″ X 1/4″ flat pack |
| C | 14-Pin 1/4″ X 3/4″ dual-in-line |
| D | 14-Pin 1/4″ X 3/8″ (ceramic) flat pack |
| E | 16-Pin 1/4″ X 3/8″ dual-in-line |
| F | 16-Pin 1/4″ X 3/8″ (metal or ceramic) flat pack |
| G | 8-pin TO-99 can or header |
| H | 10-pin 1/4″ x 1/4″ (metal) flat pack |
| I | 10-pin TO-100 can or header |
| J | 24-pin 1/2″ x 1-1/4″ dual-in-line |
| K | 24-pin 3/8″ x 5/8″ flat pack |
| L | 24-pin 1/4″ x 1-1/4″ dual-in-line |
| M | 12-pin TO-101 can or header |
| N | (Note 1) |
| P | 8-pin 1/4″ x 3/8″ dual-in-line |
| Q | 40-pin 3/16″ x 2-1/16″ dual-in-line |
| R | 20-pin 1/4″ x 1-1/16″ dual-in-line |
| S | 20-pin 1/4″ x 1/2″ flat pack |
| T | (Note 1) |
| U | (Note 1) |
| V | 18-pin 3/8″ x 15/16″ dual-in-line |
| W | 22-pin 3/8″ x 1-1/8″ dual-in-line |
| X | (Note 1) |
| Y | (Note 1) |
| Z | (Note 1) |
| 2 | 20-terminal 0.350″ x 0.350″ chip carrier |
| 3 | 28-terminal 0.450″ x 0.450″ chip carrier |

**Note 1:** These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

**TABLE III. 100% Screening Requirements**

| Screen | Class S |  | Class B |  |
|---|---|---|---|---|
|  | **Method** | **Reqmt** | **Method** | **Reqmt** |
| 1. Wafer Lot Acceptance | 5007 | All Lots |  | — |
| 2. Nondestructive Bond Pull | 2023 | 100% |  | — |
| 3. Internal Visual (Note 1) | 2010, Condition A | 100% | 2010, Condition B | 100% |
| 4. Stabilization Bake | 1008, Condition C, 24 hrs. Min. | 100% | 1008, Condition C, 24 hrs. Min. | 100% |
| 5. Temp. Cycling (Note 2) | 1010, Condition C | 100% | 1010, Condition C | 100% |
| 6. Constant Acceleration | 2001, Condition E (Min.) $Y_1$ Orientation Only | 100% | 2001, Condition E, (Min.), $Y_1$ Orientation Only | 100% |
| 7. Visual Inspection (Note 3) |  | 100% |  | 100% |
| 8. Particle Impact Noise Detection (PIND) | 2020, Condition A (Note 4) | 100% |  | — |
| 9. Serialization | (Note 5) | 100% |  | — |
| 10. Interim (Pre-Burn-In) Electrical Parameters | Per Applicable Device Specification (Note 13) | 100% | Per Applicable Device Specification (Note 6) | — |
| 11. Burn-In Test | 1015<br>240 Hrs. @ 125°C Min.<br>(Cond. F Not Allowed) | 100% | 1015<br>160 Hrs. @ 125°C Min. | 100% |
| 12. Interim (Post-Burn-In) Electrical Parameters | Per Applicable Device Specification (Note 13) | 100% |  |  |
| 13. Reverse Bias Burn-In (Note 7) | 1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed) | 100% |  | — |
| 15. PDA Calculation | 5% Parametric (Note 14), 3% Functional −25°C | All Lots | 5% Parametric (Note 14) | All Lots |
| 16. Final Electrical Test | Per Applicable Device Specification |  | Per Applicable Device Specification |  |
| a) Static Tests |  |  |  |  |
| 1) 25°C (Subgroup 1, Table I, 5005) |  | 100% |  | 100% |
| 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) |  | 100% |  | 100% |
| b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005) |  | 100% |  | 100% |
| c) Functional Test, 25°C (Subgroup 7, Table I, 5005) |  | 100% |  | 100% |

**TABLE III. 100% Screening Requirements** (Continued)

| Screen | Class S | | Class B | |
|---|---|---|---|---|
| | Method | Reqmt | Method | Reqmt |
| 17. Seal Fine, Gross | 1014 | 100%, (Note 8) | 1014 | 100%, (Note 9) |
| 18. Radiographic (Note 10) | 2012 Two Views | 100% | | — |
| 19. Qualification or Quality Conformance Inspection Test Sample Selection | (Note 11) | Samp. | (Note 11) | Samp. |
| 20. External Visual (Note 12) | 2009 | 100% | | 100% |

**Note 1:** Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

**Note 2:** For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

**Note 3:** At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

**Note 4:** The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

**Note 5:** Class S devices shall be serialized prior to interim electrical parameter measurements.

**Note 6:** When specified, all devices shall be tested for those parameters requiring delta calculations.

**Note 7:** Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

**Note 8:** For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

**Note 9:** For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

**Note 10:** The radiographic screen may be performed in any sequence after step 19.

**Note 11:** Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

**Note 12:** External Visual shall be performed on the lot any time after step 19 and prior to shipment.

**Note 13:** Read and Record when past burn-in delta measurements are specified.

**Note 14:** PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

# Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| AH0014D | x | | | |
| AH0015D | x | | | |
| AH0019D | x | | | |
| LF111H | x | | | |
| LF11201D | | x | | |
| LF11202D | | x | | |
| LF11331D | | x | | |
| LF11332D | | x | | |
| LF11333D | | x | | |
| LF11508D | x | | | |
| LF11509D | x | | | |
| LF147D | | x | | |
| LF155AH | | x | | |
| LF155H | | x | | x |
| LF155J-8 | | | | x |
| LF155W | | | | x |
| LF156AH | | x | | |
| LF156H | | x | | x |
| LF156J-8 | | | | x |
| LF156W | | | | x |
| LF157AH | | x | | |
| LF157H | | x | | |
| LF198H | | x | | |
| LF411MH | | x | | x |
| LF411W | | | | x |
| LF412MH | | x | | x |
| LF441MH | x | | | |
| LF442MH | | x | | |
| LF444MD | | x | | |
| LH0002H | | x | x | |
| LH0003H | x | | | |
| LH0004H | x | | | |
| LH0020G | x | | | |
| LH0021K | x | | | |
| LH0022D | x | | | |
| LH0022H | x | | | |
| LH0023G | x | | | |
| LH0024H | x | | | |

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| LH0032G | x | | x | |
| LH0033AG | x | | | |
| LH0033G | x | | x | |
| LH0036G | x | | | |
| LH0038D | x | | | |
| LH0041G | x | | | |
| LH0042D | x | | | |
| LH0042H | x | | | |
| LH0043G | x | | | |
| LH0044AH | x | | | |
| LH0044H | x | | | |
| LH0052H | x | | | |
| LH0053G | x | | | |
| LH0061K | x | | | |
| LH0062D | x | | | |
| LH0062H | x | | | |
| LH0063K | x | | | |
| LH0070-0H | x | | | |
| LH0070-1H | x | | | |
| LH0070-2H | x | | | |
| LH0071-0H | x | | | |
| LH0071-1H | x | | | |
| LH0071-2H | x | | | |
| LH0075G | x | | | |
| LH0076G | x | | | |
| LH0082D | x | | | |
| LH0084D | x | | | |
| LH0086D | x | | | |
| LH0091D | x | | | |
| LH0094D | x | | | |
| LH00101AK | x | | | |
| LH0101K | x | | | |
| LH2101AD | | x | | |
| LH2108AD | | x | | |
| LH2108D | | x | | |
| LH2110D | | x | | |
| LH2111D | | x | | |
| LH2111F | x | | | |

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

# Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| LH24250F | x | | | |
| LM10H | | x | | |
| LM101AH | | x | | x |
| LM101AJ-14 | | x | | x |
| LM101AJ | | x | | |
| LM101AW | | | | x |
| LM102H | | x | | |
| LM103H-3.0 | | x | x | |
| LM103H-3.3 | | x | x | |
| LM103H-3.6 | | x | x | |
| LM103H-3.9 | | x | x | |
| LM104H | | x | | |
| LM105H | | x | | |
| LM106H | | x | | |
| LM107H | | x | | |
| LM107J-14 | | x | | |
| LM107J | | x | | |
| LM108AH | | x | | x |
| LM108AJ-8 | | x | | x |
| LM108AJ | | x | | |
| LM108AW | | | | x |
| LM108H | | x | | |
| LM108J-8 | | x | | |
| LM108J | | x | | |
| LM109H | | x | | |
| LM109KSTEEL | | x | | |
| LM11H | | x | | |
| LM110H | | x | | |
| LM110J-8 | | x | | |
| LM110J | | x | | |
| LM111H | | x | | x |
| LM111J | | x | | x |
| LM111W | | | | x |
| LM112H | | x | | |
| LM113-1H | | x | x | |
| LM113-2H | | x | x | |
| LM113H | | x | x | |
| LM117H | | x | x | x |

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| LM117HVH | | x | x | |
| LM117HVKSTL | | x | x | |
| LM117KSTEEL | | x | x | x |
| LM118H | | x | | x |
| LM118J-8 | | x | | x |
| LM118J | | x | | |
| LM118W | | | | x |
| LM119H | | x | x | |
| LM119J | | x | x | |
| LM120H-12 | | x | | |
| LM120H-15 | | x | | |
| LM120H-5.0 | | x | | |
| LM120K-12 | | x | | |
| LM120K-15 | | x | | |
| LM120K-5.0 | | x | | |
| LM121AH | | x | | |
| LM121H | | x | | |
| LM122H | | x | | |
| LM123KSTEEL | | x | | |
| LM124AJ | | x | | |
| LM124J | | x | | x |
| LM125H | | x | | |
| LM126H | | x | | |
| LM129AH | | x | | |
| LM129BH | | x | | |
| LM131AH | | x | | |
| LM131H | | x | | |
| LM135H | | x | | |
| LM136AH-2.5 | | x | x | |
| LM136H-2.5 | | x | | |
| LM136H-5.0 | | x | | |
| LM137H | | x | x | |
| LM137HVH | | x | x | |
| LM137HVKSTEEL | | x | x | |
| LM137KSTEEL | | x | x | |
| LM138KSTEEL | | x | | |
| LM139AJ | | x | | |
| LM139J | | x | | x |

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

# Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| LM139W | | | | x |
| LM140AK-12 | | x | | |
| LM140AK-15 | | x | | |
| LM140AK-5.0 | | x | | |
| LM140K-12 | | x | | |
| LM140K-15 | | x | | |
| LM140K-5.0 | | x | | |
| LM140LAH-12 | | x | | |
| LM140LAH-15 | | x | | |
| LM140LAH-5.0 | | x | | |
| LM143H | | x | x | |
| LM144H | | x | x | |
| LM145K-5.0 | | x | | |
| LM145K-5.2 | | x | | |
| LM146J | | x | | |
| LM148J | | x | | x |
| LM149J | | x | | |
| LM150KSTEEL | x | | | |
| LM1536H | | x | x | |
| LM1558H | | x | | |
| LM1558J | | x | | |
| LM158AH | | x | | |
| LM158AJ | | x | | |
| LM158H | | x | | |
| LM158J | | x | | |
| LM1596H | x | | | |
| LM160H | | x | | |
| LM160J-14 | | x | | |
| LM160J | | x | | |
| LM161F | x | | | |
| LM161H | | x | | |
| LM161J | | x | | |
| LM185BXH-1.2 | | x | | |
| LM185BYH-1.2 | | x | | |

| Device Type | Mil * Class B | 883 Class B | Desc | JAN |
|---|---|---|---|---|
| LM185H-1.2 | | x | | |
| LM193AH | | x | | |
| LM193H | | x | | x |
| LM193J-8 | | | | x |
| LM193W | | | | x |
| LM194H | | x | | |
| LM195H | | x | | |
| LM195K | | x | | |
| LM199AH-20 | | x | | |
| LM199AH | | x | | |
| LM199H | | x | | |
| LM4250H | x | | | |
| LM4250J | x | | | |
| LM555H | | x | | |
| LM555J | | x | | |
| LM556J | x | | | |
| LM567H | | x | | |
| LM709AH | | x | | |
| LM709H | | x | | |
| LM710H | | x | | |
| LM723H | | x | | |
| LM723J | | x | | x |
| LM725H | | x | | |
| LM733H | x | | | |
| LM741AJ-14 | | x | | |
| LM741AJ | | x | | |
| LM741H | | x | | x |
| LM7415-14 | | x | | |
| LM741J | | x | | x |
| LM741W | | | | x |
| LM747H | | x | | x |
| LM747J | | x | | |
| LM748H | | x | | |
| LM748J | | x | | |

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

**National Semiconductor Corporation**

# Appendix E
# Understanding Integrated Circuit Package Power Capabilities

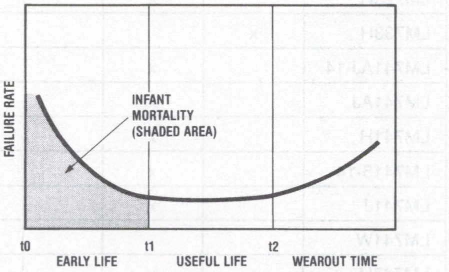
## INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

## FACTORS AFFECTING DEVICE RELIABILITY

*Figure 1* shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.



TL/H/9312–1

**FIGURE 1. Failure Rate vs Time**

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

## FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2.* This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

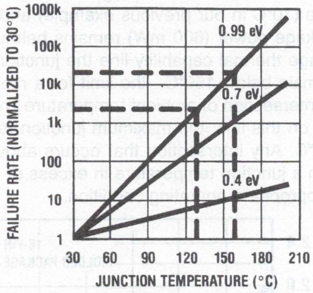


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**FIGURE 2. Failure Rate as a Function of Junction Temperature**

## DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

*Figure 3* shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

*Figure 4* is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D(\theta_{JA})$$

Where: $T_J$ = Die junction temperature

$T_A$ = Ambient temperature in the vicinity device

$P_D$ = Total power dissipation (in watts)

$\theta_{JA}$ = Thermal resistance junction-to-ambient

$\theta_{JA}$, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or $\theta_{JA}$.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

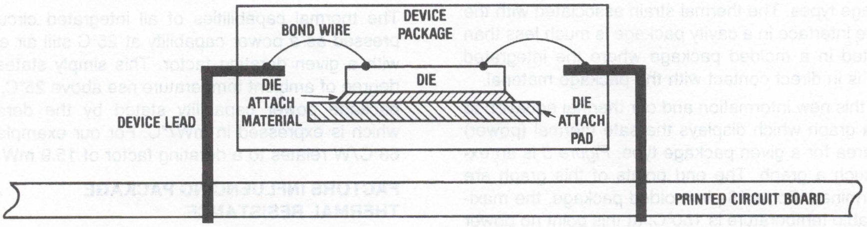

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**FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)**

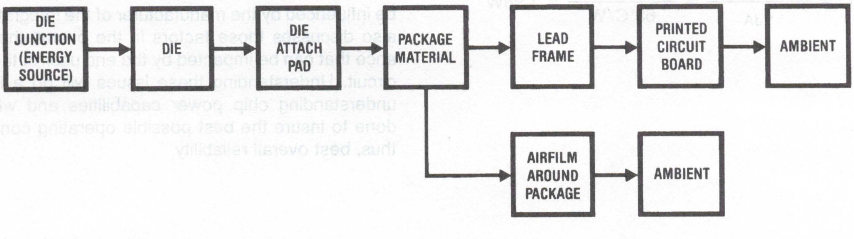

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**FIGURE 4. Thermal Flow (Predominant Paths)**

## DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, $\theta_{JA}$, worst-case ambient operating temperature, $T_A$(max), the only unknown parameter is device power dissipation, $P_D$. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

## MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D \text{ @ } 25°C = \frac{T_J(\text{max}) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

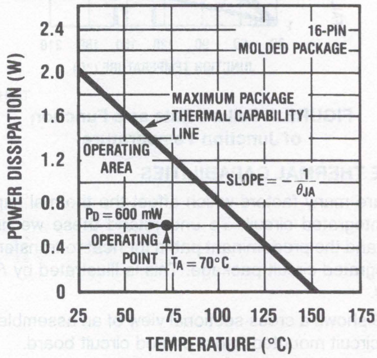

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a $\theta_{JA}$ of 63°C/W relates to a derating factor of 15.9 mW/°C.

## FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

### Die Size

*Figure 6* shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

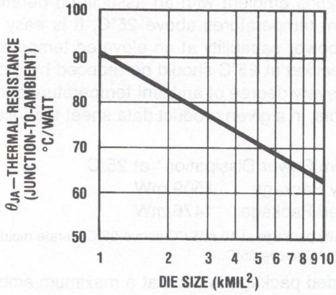

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**FIGURE 6. Thermal Resistance vs Die Size**

### Lead Frame Material

*Figure 7* shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

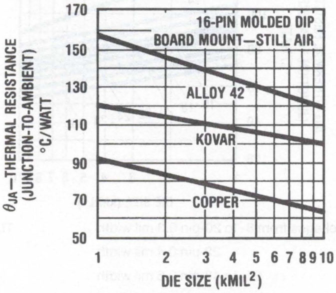

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**FIGURE 7. Thermal Resistance vs Lead Frame Material**

### Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

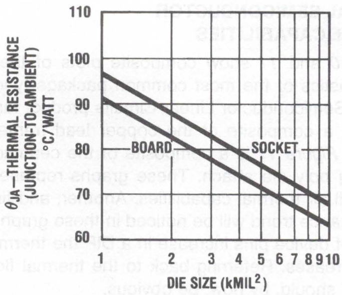

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**FIGURE 8. Thermal Resistance vs Board or Socket Mount**

### Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

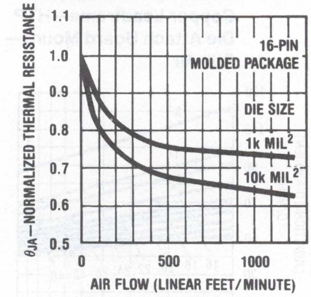

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**FIGURE 9. Thermal Resistance vs Air Flow**

### Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient ($\theta_{JA}$) and thermal resistance junction-to-case ($\theta_{JC}$). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

## NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

*Figures 10* and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

## RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

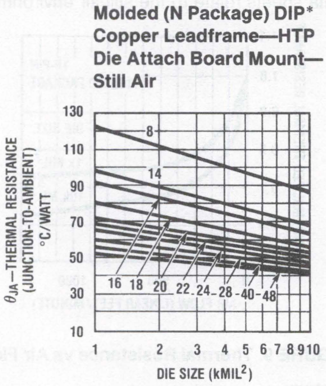
The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

| Maximum Power Dissipation* at 25°C | |
|---|---|
| Cavity Package | 1509 mW |
| Molded Package | 1476 mW |

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70^\circ\text{C} = 1476\text{ mW} - (11.8\text{ mW}/^\circ\text{C}) \times (70^\circ\text{C} - 25^\circ\text{C})$$
$$= 945\text{ mW}$$


Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air

*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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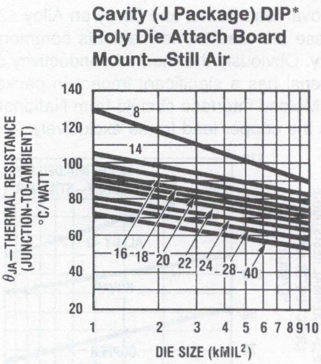
**FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)**


Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air

*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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**FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)**

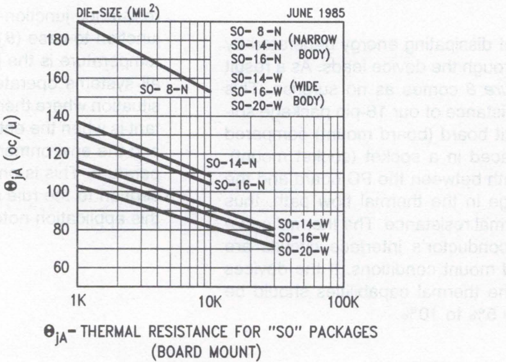

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**FIGURE 12**

National Semiconductor Corporation

# APPENDIX F
# How to Get the Right Information From a Data Sheet

*Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money*

**By Robert A. Pease**

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

## SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

## GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between $I_b$ and $Z_{in}$ permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the $Z_{in}$ *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours). The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

## TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current ($I_b$) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where $I_b$ is 40 nA on one batch (where the beta is high), and a month later, many parts where the $I_b$ is 140 nA when the beta is low.

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## Absolute Maximum Ratings (Note 11)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | +35V to −0.2V |
| Output Voltage | +6V to −1.0V |
| Output Current | 10 mA |
| Storage Temperature, | |
| TO-46 Package | −76°F to +356°F |
| TO-92 Package | −76°F to +300°F |
| Lead Temp. (Soldering, 4 seconds) * | |
| TO-46 Package | +300°C |
| TO-92 Package | +260°C |
| Specified Operating Temp. Range (Note 2) | **$T_{MIN}$ to $T_{MAX}$** |
| LM34, LM34A | −50°F to +300°F |
| LM34C, LM34CA | −40°F to +230°F |
| LM34D | +32°F to +212°F |

## DC Electrical Characteristics (Note 1, Note 6)

| Parameter | Conditions | LM34A Typical | LM34A Tested Limit (Note 4) | LM34A Design Limit (Note 5) | LM34CA Typical | LM34CA Tested Limit (Note 4) | LM34CA Design Limit (Note 5) | Units (Max) |
|---|---|---|---|---|---|---|---|---|
| Accuracy (Note 7) | $T_A = +77°F$ | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | °F |
| | $T_A = 0°F$ | ±0.6 | | | ±0.6 | | ±2.0 | °F |
| | $T_A = T_{MAX}$ | ±0.8 | ±2.0 | | ±0.8 | ±2.0 | | °F |
| | $T_A = T_{MIN}$ | ±0.8 | ±2.0 | | ±0.8 | | ±3.0 | °F |
| Nonlinearity (Note 8) | $T_{MIN} \le T_A \le T_{MAX}$ | **±0.35** | | **±0.7** | **±0.30** | | **±0.6** | °F |
| Sensor Gain (Average Slope) | $T_{MIN} \le T_A \le T_{MAX}$ | **+10.0** | **+9.9,**<br>**+10.1** | | **+10.0** | | **+9.9,**<br>**+10.1** | mV/°F, min<br>mV/°F, max |
| Load Regulation (Note 3) | $T_A = +77°F$ | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | mV/mA |
| | $T_{MIN} \le T_A \le T_{MAX}$<br>$0 \le I_L \le 1$ mA | **±0.5** | | **±3.0** | **±0.5** | | **±3.0** | mV/mA |
| Line Regulation (Note 3) | $T_A = +77°F$ | ±0.01 | ±0.05 | | ±0.01 | ±0.05 | | mV/V |
| | $5V \le V_S \le 30V$ | **±0.02** | | **±0.1** | **±0.02** | | **±0.1** | mV/V |
| Quiescent Current (Note 9) | $V_S = +5V, +77°F$ | 75 | 90 | | 75 | 90 | | μA |
| | $V_S = +5V$ | **131** | | **160** | **116** | | **139** | μA |
| | $V_S = +30V, +77°F$ | 76 | 92 | | 76 | 92 | | μA |
| | $V_S = +30V$ | **132** | | **163** | **117** | | **142** | μA |
| Change of Quiescent Current (Note 3) | $4V \le V_S \le 30V, +77°F$ | +0.5 | 2.0 | | 0.5 | 2.0 | | μA |
| | $5V \le V_S \le 30V$ | **+1.0** | | **3.0** | **1.0** | | **3.0** | μA |
| Temperature Coefficient of Quiescent Current | | **+0.30** | | **+0.5** | **+0.30** | | **+0.5** | μA/°F |
| Minimum Temperature for Rated Accuracy | In circuit of *Figure 1*, $I_L = 0$ | +3.0 | | +5.0 | +3.0 | | +5.0 | °F |
| Long-Term Stability | $T_j = T_{MAX}$ for 1000 hours | ±0.16 | | | ±0.16 | | | °F |

**Note 1:** Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. $V_S = +5$ Vdc and $I_{LOAD} = 50$ μA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to $T_{MAX}$ in the circuit of *Figure 1.*

**Note 2:** Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

**Note 3:** Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

**Note 4:** Tested limits are guaranteed and 100% tested in production.

**Note 5:** Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

**Note 6:** Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

**Note 7:** Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

**Note 8:** Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

**Note 9:** Quiescent current is defined in the circuit of *Figure 1.*

**Note 10:** Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

## A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

### APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family: "Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

### FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

### ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

## WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

*Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.*

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# Appendix G
# Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

| NSC Part Number | Replacement | Note |
|---|---|---|
| ADB1200 | ADC3711 | 2 |
| DAC1200/1201 | DAC1265 | 2 |
| LF352 | LM3631 | 2 |
| LF13300 | ADC3711 | 2 |
| LH0001 | LM4250 | 2 |
| LH0005/LH0005A | LH0003 | 2 |
| LH0037 | LH0036 | 3 |
| LH0132 | LH0032 | 2 |
| LH2011 | LM11 | 2 |
| LH2108 | LM108 | 2 |
| LH2201A | LM201A | 2 |
| LH2208 | LM208 | 2 |
| LH2208A | LM208A | 2 |
| LH2308 | LM308 | 2 |
| LH24250 | LM11 | 2 |
| LM170/270/370 | LM13600N | 2 |
| LM171/271/371 | no replacement | |
| LM172/272/372 | no replacement | |
| LM173/273/373 | no replacement | |
| LM174/274/374 | no replacement | |
| LM175/275/375 | no replacement | |
| LM216/316 | LM11 | 2 |
| LM388N-2/N-3 | LM388N-1 | 2 |
| LM377N | LM2877P | 3 |
| LM378N | LM2878P | 3 |
| LM379 | LM2879T | 3 |
| LM1014 | no replacement | |
| LM1017 | no replacement | |
| LM1019 | no replacement | |
| LM1821S | LM1823 | 2 |
| LM1822 | LM1823 | 3 |
| LM1828 | no replacement | |
| LM1848 | no replacement | |
| LM1877N-1/N-2/N-3 | LM1877N-9 | 2 |
| LM2003 | no replacement | |
| LM2808 | no replacement | |
| LM2831 | LM1851 | 2 |
| LM3011 | no replacement | |
| LM3064 | no replacement | |
| LM3075 | no replacement | |
| TBA120V | no replacement | |
| TBA440C | LM1823 | 2 |
| TBA510 | no replacement | |
| TBA530 | no replacement | |
| TBA540 | no replacement | |
| TBA560C | no replacement | |
| TBA920 | no replacement | |
| TBA950-2 | no replacement | |
| TBA970 | no replacement | |
| TBA990 | no replacement | |
| TDA440 | no replacement | |
| TDA2522/23 | no replacement | |
| TDA2530 | no replacement | |
| TDA2530/31 | no replacement | |
| TDA2540/41 | no replacement | |
| TDA2560 | no replacement | |
| TDA2590 | no replacement | |
| TDA3500 | no replacement | |

**Note 1:** IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

**Note 2:** FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

**Note 3:** SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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# Appendix H
# Products Not Recommended for New Designs

The popular National Semiconductor Corporation monolithic IC's may have been designed into your systems. We believe that there are more cost-effective circuits manufactured by National Semiconductor Corporation that should be considered in your new designs. These recommendations are listed in this section. To eliminate the necessity to redesign proven equipment, we are continuing to make these products for use in existing designs for which they were uniquely suitable.

| NSC Part Number | Recommended Replacement | Note |
|---|---|---|
| AF100 | LMF100 | 3 |
| AF150 | LMF100 | 3 |
| AF151 | LMF100 | 3 |
| AH0014 | LMC13421/LMC13422 | 3 |
| AH0015 | LMC13421/LMC13422 | 3 |
| AH0019 | LMC13421/LMC13422 | 3 |
| LH0023 | LF198/LF298 | 2 |
| LH2101A | LM101A | 2 |
| LH2108A | LM108A | 2 |
| LH2110 | LM110 | 2 |
| LH2111 | LM111 | 2 |
| LH2210 | LM210 | 2 |
| LH2211 | LM211 | 2 |
| LH2301A | LM301A | 2 |
| LH2308A | LM308A | 2 |
| LH2310 | LM310 | 2 |
| LH2311 | LM311 | 2 |
| LM103 | LM185 | 3 |
| LM113 | LM1851-2 | 1 |
| LM313 | LM3851-2 | 1 |
| LM377N | LM1877N-9 | 2 |
| LM377N | LM2877P | 3 |
| LM378N | LM2878P | 3 |
| LM391N-60 | LM391N-100 | 1 |
| LM391N-80 | LM391N-100 | 1 |
| LM709 | LF441 | 3 |
| LM710 | LM106 | 2 |
| LM725 | LM607 | 3 |
| LM748 | LF441 | 3 |

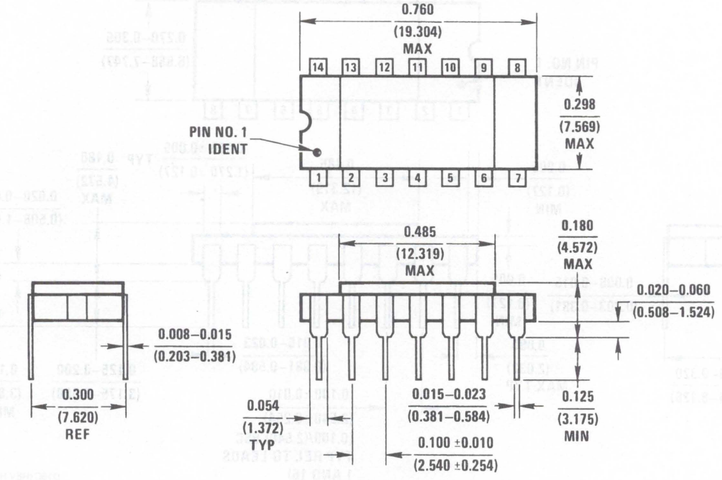
**Notes:**

**Note 1:** IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

**Note 2:** FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

**Note 3:** SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

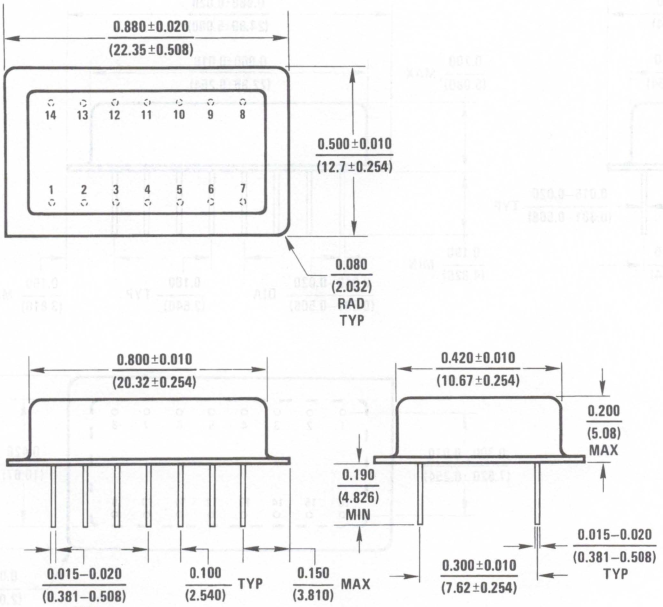
All dimensions are in inches (millimeters)


0.760
(19.304)
MAX
14
13
12
11
10
9
8
1
2
3
4
5
6
7
PIN NO. 1
IDENT
0.298
(7.569)
MAX
0.485
(12.319)
MAX
0.180
(4.572)
MAX
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.300
(7.620)
REF
0.054
(1.372)
TYP
0.015–0.023
(0.381–0.584)
0.100 ±0.010
(2.540 ±0.254)
0.125
(3.175)
MIN

D14E (REV E)

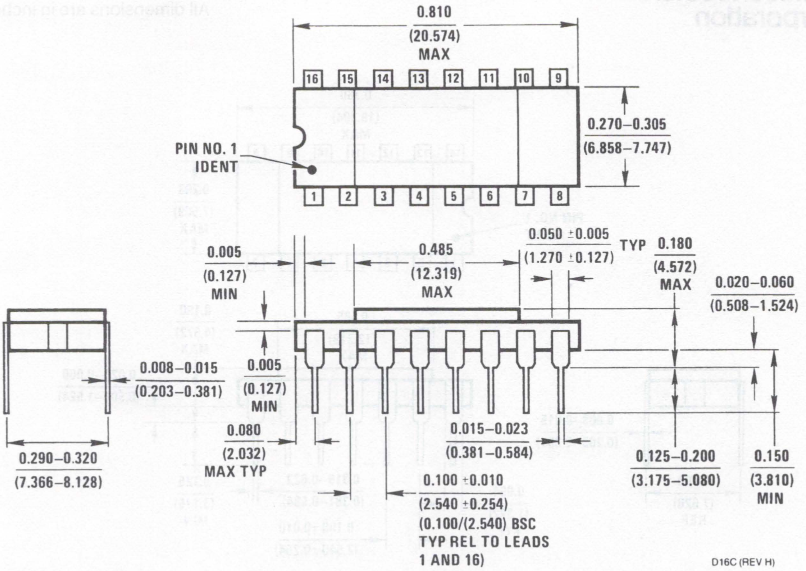
**NS Package D14E**

---

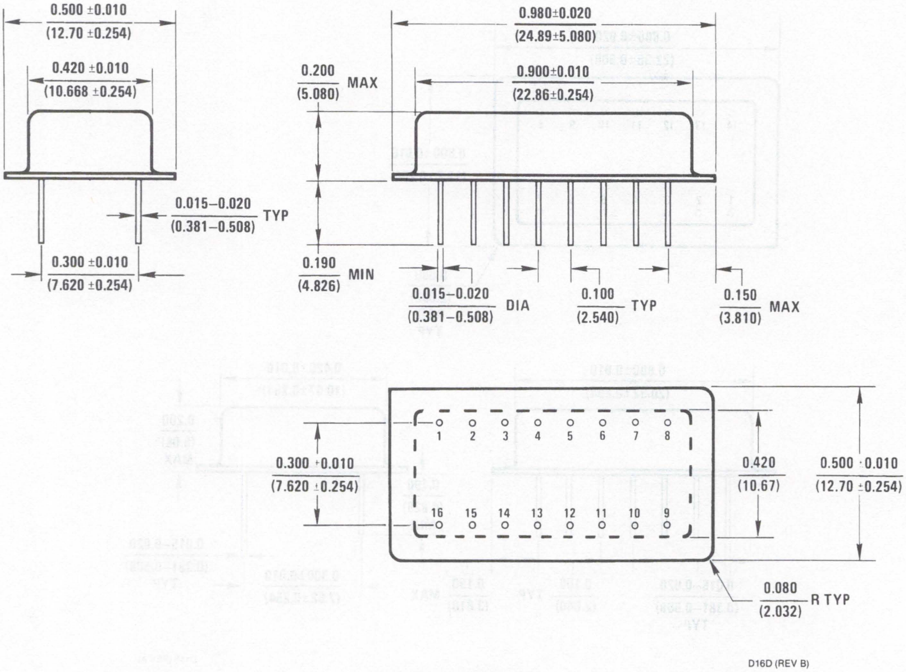

0.880±0.020
(22.35±0.508)
14
13
12
11
10
9
8
1
2
3
4
5
6
7
0.500±0.010
(12.7±0.254)
0.080
(2.032)
RAD
TYP
0.800±0.010
(20.32±0.254)
0.420±0.010
(10.67±0.254)
0.200
(5.08)
MAX
0.190
(4.826)
MIN
0.015–0.020
(0.381–0.508)
TYP
0.100
(2.540)
TYP
0.150
(3.810)
MAX
0.300±0.010
(7.62±0.254)
0.015–0.020
(0.381–0.508)
TYP

D14F (REV A)

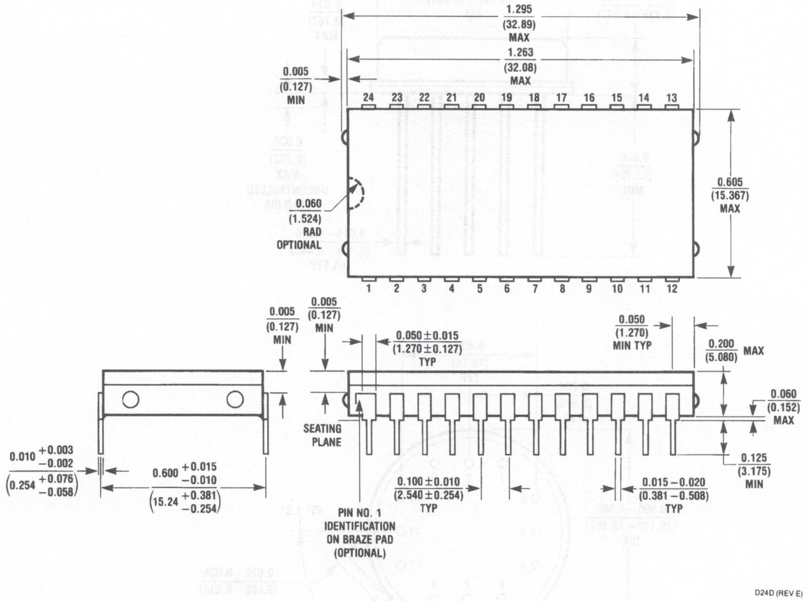
**NS Package D14F**


0.810
(20.574)
MAX
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
PIN NO. 1
IDENT
0.270–0.305
(6.858–7.747)
0.005
(0.127)
MIN
0.485
(12.319)
MAX
0.050 ±0.005
(1.270 ±0.127)
TYP
0.180
(4.572)
MAX
0.020–0.060
(0.508–1.524)
0.008–0.015
(0.203–0.381)
0.005
(0.127)
MIN
0.080
(2.032)
MAX TYP
0.015–0.023
(0.381–0.584)
0.125–0.200
(3.175–5.080)
0.150
(3.810)
MIN
0.290–0.320
(7.366–8.128)
0.100 ±0.010
(2.540 ±0.254)
(0.100/(2.540) BSC
TYP REL TO LEADS
1 AND 16)
D16C (REV H)

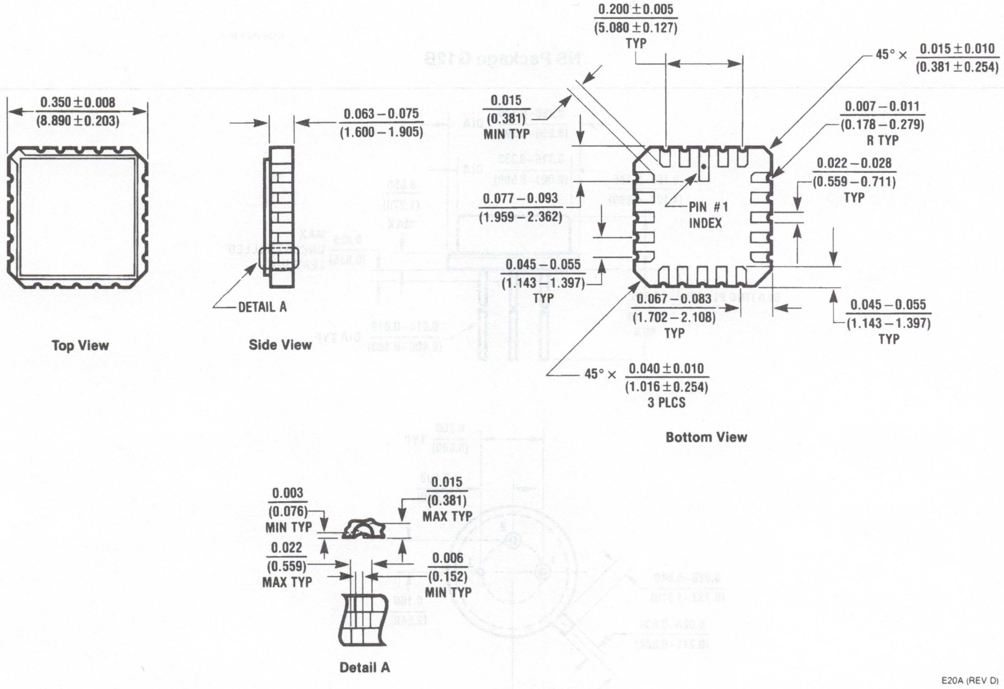
**NS Package D16C**


0.500 ±0.010
(12.70 ±0.254)
0.420 ±0.010
(10.668 ±0.254)
0.015–0.020
(0.381–0.508)
TYP
0.300 ±0.010
(7.620 ±0.254)
0.980±0.020
(24.89±5.080)
0.900±0.010
(22.86±0.254)
0.200
(5.080)
MAX
0.190
(4.826)
MIN
0.015–0.020
(0.381–0.508)
DIA
0.100
(2.540)
TYP
0.150
(3.810)
MAX
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9
0.300 ±0.010
(7.620 ±0.254)
0.420
(10.67)
0.500 ±0.010
(12.70 ±0.254)
0.080
(2.032)
R TYP
D16D (REV B)

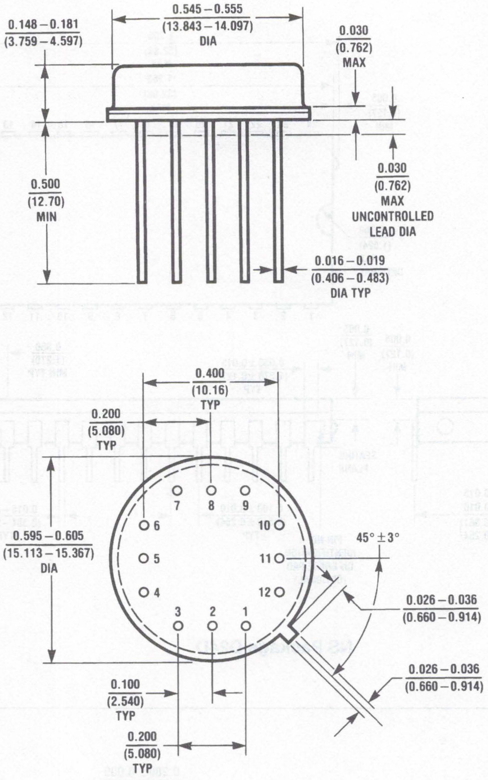
**NS Package D16D**


1.295
(32.89)
MAX
1.263
(32.08)
MAX
0.005
(0.127)
MIN
24 23 22 21 20 19 18 17 16 15 14 13
0.060
(1.524)
RAD
OPTIONAL
0.605
(15.367)
MAX
1 2 3 4 5 6 7 8 9 10 11 12
0.005
(0.127)
MIN
0.005
(0.127)
MIN
0.050 ± 0.015
(1.270 ± 0.127)
TYP
0.050
(1.270)
MIN TYP
0.200
(5.080)
MAX
0.060
(0.152)
MAX
SEATING
PLANE
0.010 +0.003 −0.002
(0.254 +0.076 −0.058)
0.600 +0.015 −0.010
(15.24 +0.381 −0.254)
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.015 − 0.020
(0.381 − 0.508)
TYP
0.125
(3.175)
MIN
PIN NO. 1
IDENTIFICATION
ON BRAZE PAD
(OPTIONAL)
D24D (REV E)

**NS Package D24D**


0.350 ± 0.008
(8.890 ± 0.203)
Top View
0.063 − 0.075
(1.600 − 1.905)
DETAIL A
Side View
0.200 ± 0.005
(5.080 ± 0.127)
TYP
45° × 0.015 ± 0.010
(0.381 ± 0.254)
0.015
(0.381)
MIN TYP
0.007 − 0.011
(0.178 − 0.279)
R TYP
0.022 − 0.028
(0.559 − 0.711)
TYP
0.077 − 0.093
(1.959 − 2.362)
PIN #1
INDEX
0.045 − 0.055
(1.143 − 1.397)
TYP
0.067 − 0.083
(1.702 − 2.108)
TYP
0.045 − 0.055
(1.143 − 1.397)
TYP
45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS
Bottom View
0.003
(0.076)
MIN TYP
0.015
(0.381)
MAX TYP
0.022
(0.559)
MAX TYP
0.006
(0.152)
MIN TYP
Detail A
E20A (REV D)

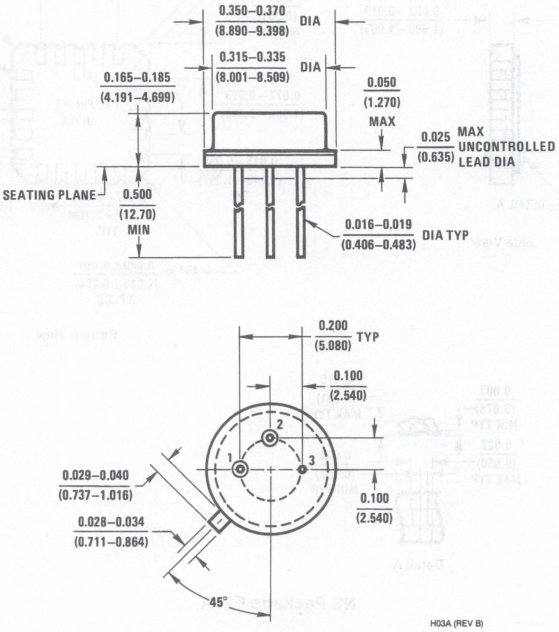
**NS Package E20A**



0.148 – 0.181
(3.759 – 4.597)
0.545 – 0.555
(13.843 – 14.097)
DIA
0.030
(0.762)
MAX
0.500
(12.70)
MIN
0.030
(0.762)
MAX
UNCONTROLLED
LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.400
(10.16)
TYP
0.200
(5.080)
TYP
7
8
9
6
10
5
11
4
12
3
2
1
0.595 – 0.605
(15.113 – 15.367)
DIA
45° ± 3°
0.026 – 0.036
(0.660 – 0.914)
0.026 – 0.036
(0.660 – 0.914)
0.100
(2.540)
TYP
0.200
(5.080)
TYP

G12B (REV B)

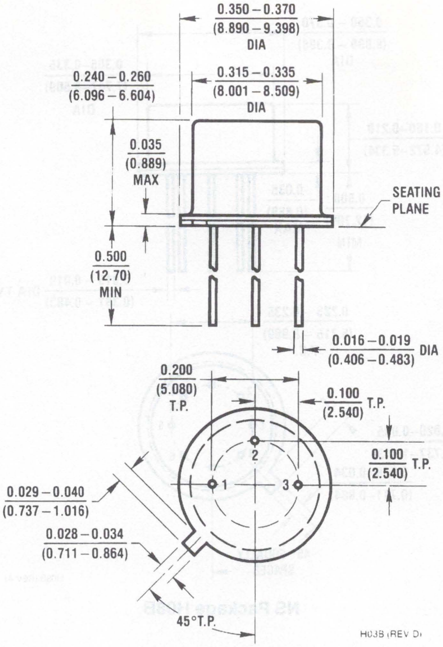
**NS Package G12B**



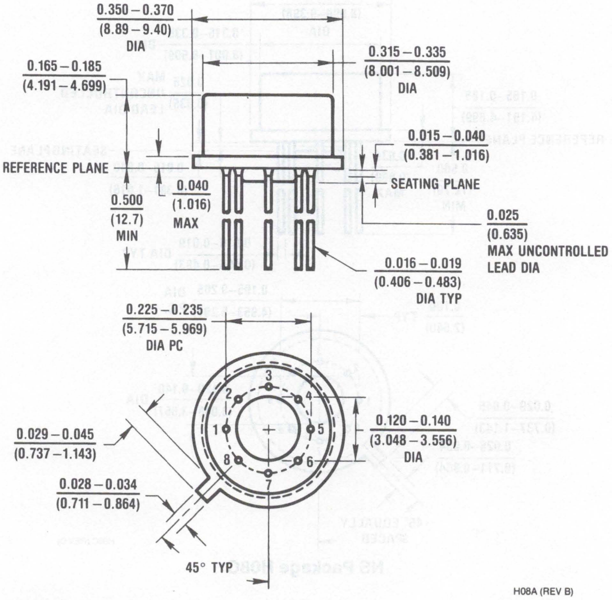
0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509)
DIA
0.165–0.185
(4.191–4.699)
0.050
(1.270)
MAX
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
SEATING PLANE
0.500
(12.70)
MIN
0.016–0.019
(0.406–0.483)
DIA TYP
0.200
(5.080)
TYP
0.100
(2.540)
2
1
3
0.029–0.040
(0.737–1.016)
0.028–0.034
(0.711–0.864)
0.100
(2.540)
45°

H03A (REV B)

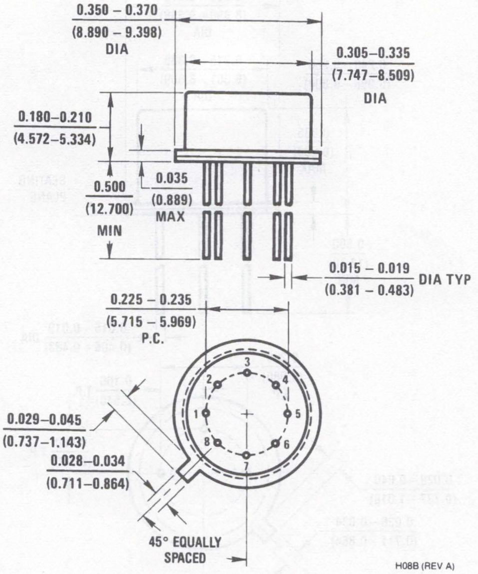
**NS Package H03A**


0.350 – 0.370
(8.890 – 9.398)
DIA
0.315 – 0.335
(8.001 – 8.509)
DIA
0.240 – 0.260
(6.096 – 6.604)
0.035
(0.889)
MAX
SEATING PLANE
0.500
(12.70)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA
0.200
(5.080)
T.P.
0.100
(2.540)
T.P.
0.100
(2.540)
T.P.
2
1
3
0.029 – 0.040
(0.737 – 1.016)
0.028 – 0.034
(0.711 – 0.864)
45°T.P.
H03B (REV D)

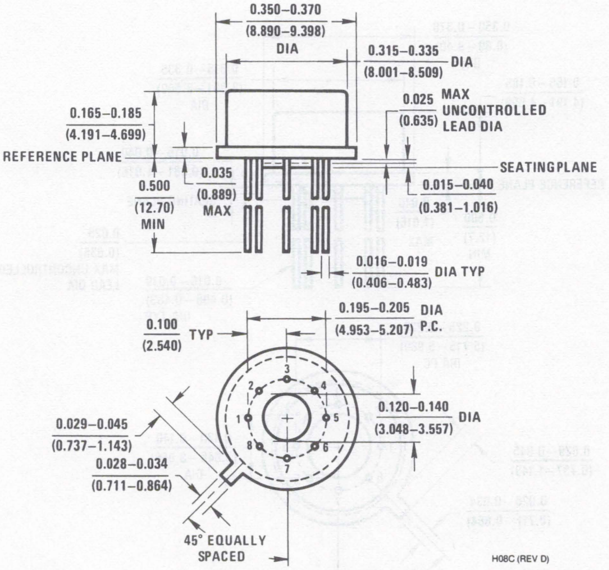
**NS Package H03B**


0.350 – 0.370
(8.89 – 9.40)
DIA
0.165 – 0.185
(4.191 – 4.699)
0.315 – 0.335
(8.001 – 8.509)
DIA
0.015 – 0.040
(0.381 – 1.016)
REFERENCE PLANE
SEATING PLANE
0.040
(1.016)
MAX
0.500
(12.7)
MIN
0.025
(0.635)
MAX UNCONTROLLED LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
DIA PC
3
2
4
1
5
8
6
7
0.120 – 0.140
(3.048 – 3.556)
DIA
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
45° TYP
H08A (REV B)

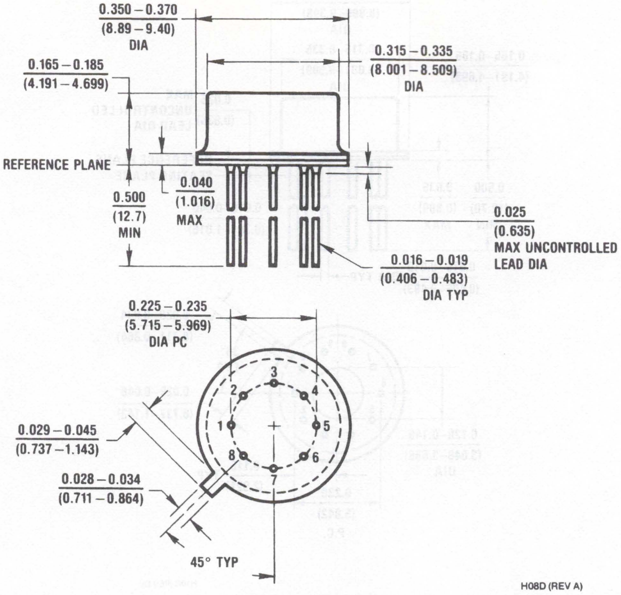
**NS Package H08A**


0.350 – 0.370
(8.890 – 9.398)
DIA
0.305–0.335
(7.747–8.509)
DIA
0.180–0.210
(4.572–5.334)
0.500
(12.700)
MIN
0.035
(0.889)
MAX
0.015 – 0.019
(0.381 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
P.C.
3
2
4
1
5
8
6
7
0.029–0.045
(0.737–1.143)
0.028–0.034
(0.711–0.864)
45° EQUALLY
SPACED
H08B (REV A)

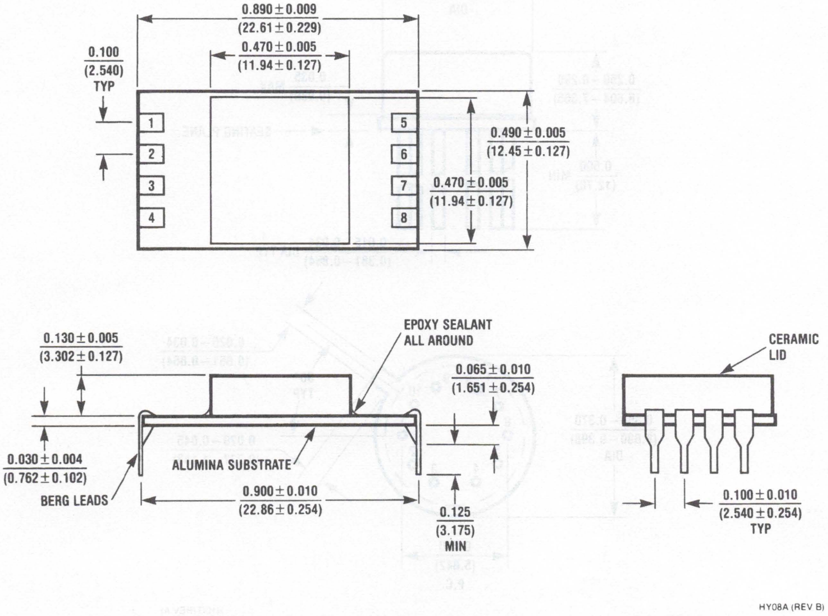
**NS Package H08B**


0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509)
DIA
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.165–0.185
(4.191–4.699)
REFERENCE PLANE
SEATINGPLANE
0.035
(0.889)
MAX
0.500
(12.70)
MIN
0.015–0.040
(0.381–1.016)
0.016–0.019
(0.406–0.483)
DIA TYP
0.195–0.205
(4.953–5.207)
DIA
P.C.
0.100
(2.540)
TYP
3
2
4
1
5
8
6
7
0.120–0.140
(3.048–3.557)
DIA
0.029–0.045
(0.737–1.143)
0.028–0.034
(0.711–0.864)
45° EQUALLY
SPACED
H08C (REV D)

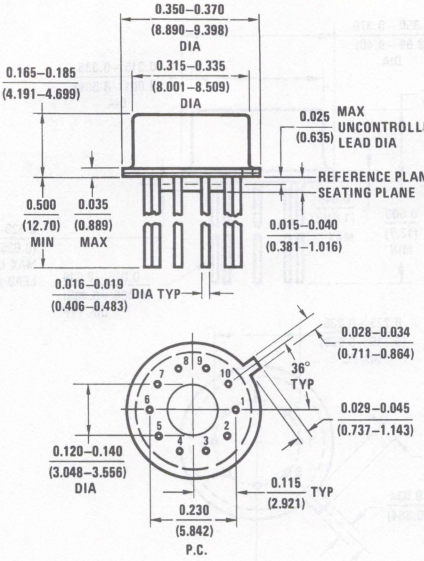
**NS Package H08C**


0.350 – 0.370
(8.89 – 9.40)
DIA
0.165 – 0.185
(4.191 – 4.699)
0.315 – 0.335
(8.001 – 8.509)
DIA
REFERENCE PLANE
0.040
(1.016)
MAX
0.500
(12.7)
MIN
0.025
(0.635)
MAX UNCONTROLLED
LEAD DIA
0.016 – 0.019
(0.406 – 0.483)
DIA TYP
0.225 – 0.235
(5.715 – 5.969)
DIA PC
1
2
3
4
5
6
7
8
0.029 – 0.045
(0.737 – 1.143)
0.028 – 0.034
(0.711 – 0.864)
45° TYP
H08D (REV A)

**NS Package H08D**

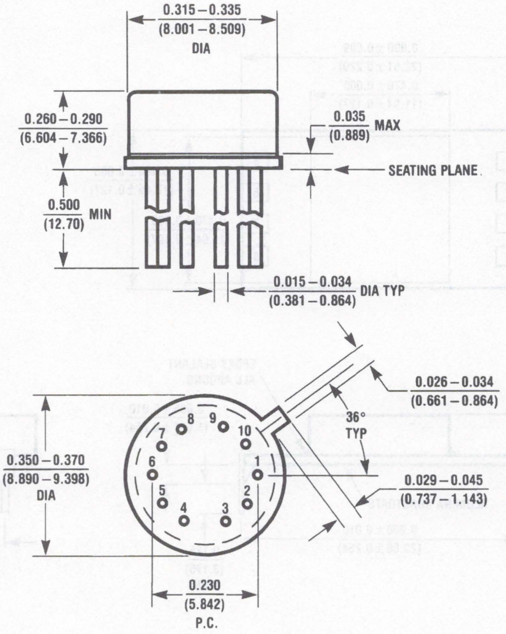

0.890 ± 0.009
(22.61 ± 0.229)
0.470 ± 0.005
(11.94 ± 0.127)
0.100
(2.540)
TYP
1
2
3
4
5
6
7
8
0.490 ± 0.005
(12.45 ± 0.127)
0.470 ± 0.005
(11.94 ± 0.127)
EPOXY SEALANT
ALL AROUND
CERAMIC
LID
0.130 ± 0.005
(3.302 ± 0.127)
0.065 ± 0.010
(1.651 ± 0.254)
0.030 ± 0.004
(0.762 ± 0.102)
ALUMINA SUBSTRATE
BERG LEADS
0.900 ± 0.010
(22.86 ± 0.254)
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
TYP
HY08A (REV B)

**NS Package HY8A**


0.350–0.370
(8.890–9.398)
DIA
0.315–0.335
(8.001–8.509)
DIA
0.165–0.185
(4.191–4.699)
0.025 MAX
(0.635) UNCONTROLLED LEAD DIA
REFERENCE PLANE
SEATING PLANE
0.500
(12.70)
MIN
0.035
(0.889)
MAX
0.015–0.040
(0.381–1.016)
0.016–0.019
(0.406–0.483)
DIA TYP
0.028–0.034
(0.711–0.864)
36°
TYP
0.029–0.045
(0.737–1.143)
0.120–0.140
(3.048–3.556)
DIA
0.115
(2.921)
TYP
0.230
(5.842)
P.C.
1
2
3
4
5
6
7
8
9
10

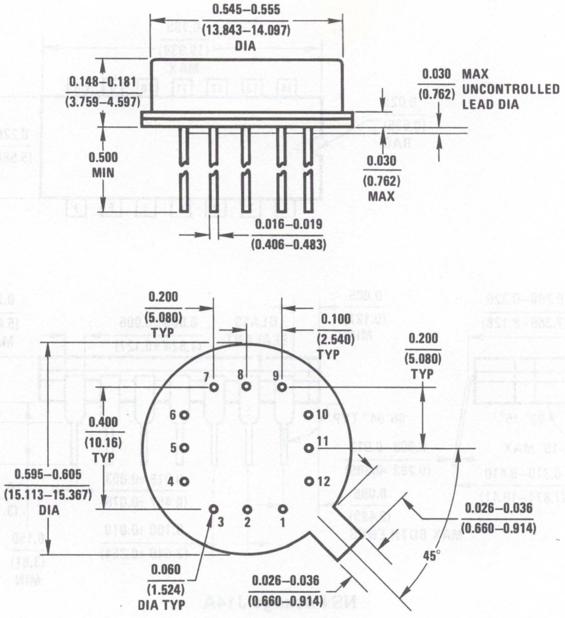
H10C (REV D)

**NS Package H10C**


0.315 – 0.335
(8.001 – 8.509)
DIA
0.260 – 0.290
(6.604 – 7.366)
0.035
(0.889) MAX
SEATING PLANE
0.500
(12.70) MIN
0.015 – 0.034
(0.381 – 0.864) DIA TYP
0.026 – 0.034
(0.661 – 0.864)
36°
TYP
0.029 – 0.045
(0.737 – 1.143)
0.350 – 0.370
(8.890 – 9.398)
DIA
0.230
(5.842)
P.C.
1
2
3
4
5
6
7
8
9
10

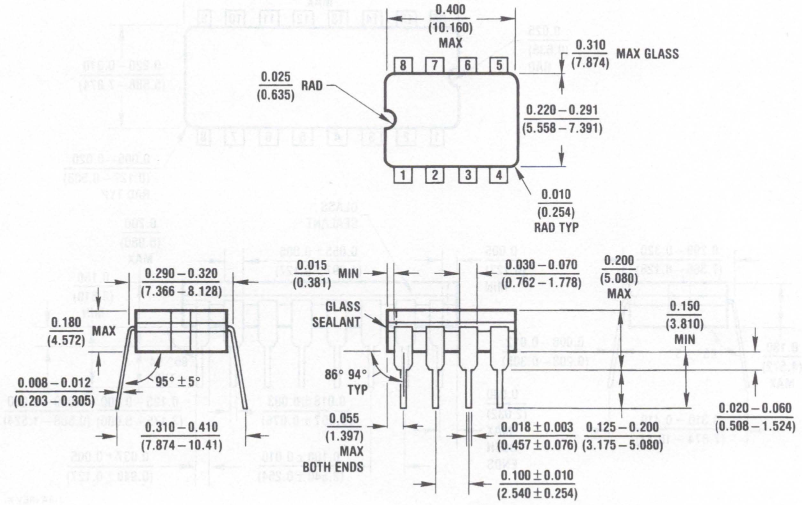
H10G (REV A)

**NS Package H10G**


0.545–0.555
(13.843–14.097)
DIA
0.148–0.181
(3.759–4.597)
0.030 MAX
(0.762) UNCONTROLLED LEAD DIA
0.500
MIN
0.030
(0.762)
MAX
0.016–0.019
(0.406–0.483)
0.200
(5.080)
TYP
0.100
(2.540)
TYP
0.200
(5.080)
TYP
7
8
9
6
10
5
11
4
12
3
2
1
0.400
(10.16)
TYP
0.595–0.605
(15.113–15.367)
DIA
0.026–0.036
(0.660–0.914)
45°
0.060
(1.524)
DIA TYP
0.026–0.036
(0.660–0.914)

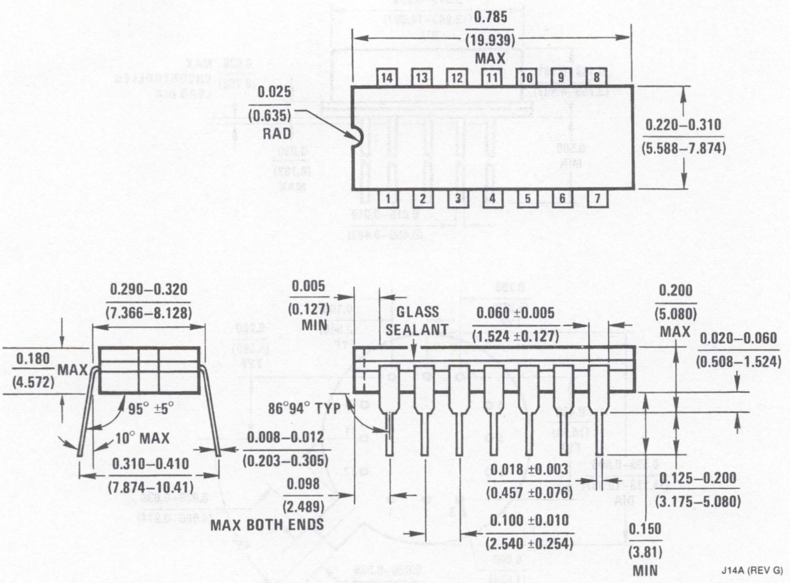
H12B (REV A)

**NS Package H12B**

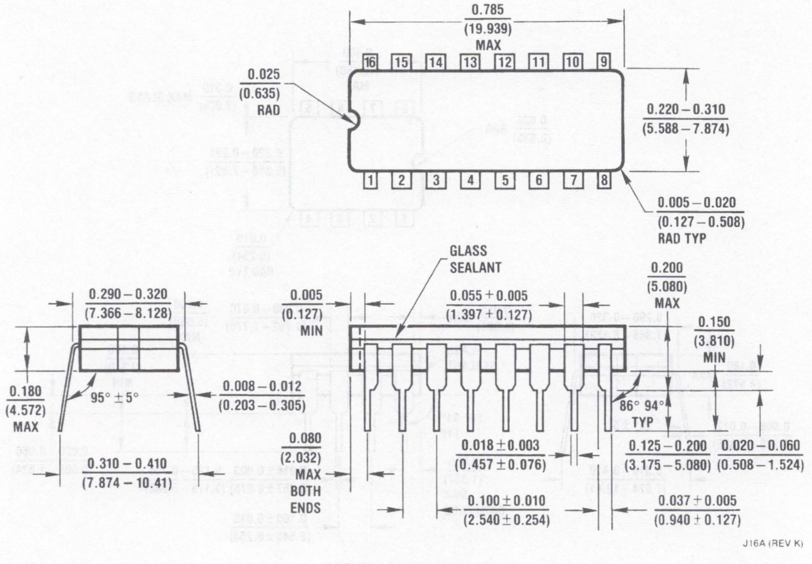

0.400
(10.160)
MAX
0.310
(7.874) MAX GLASS
8
7
6
5
0.025
(0.635) RAD
0.220 – 0.291
(5.558 – 7.391)
1
2
3
4
0.010
(0.254)
RAD TYP
0.290 – 0.320
(7.366 – 8.128)
0.015
(0.381) MIN
0.030 – 0.070
(0.762 – 1.778)
0.200
(5.080)
MAX
0.150
(3.810)
MIN
0.180
(4.572) MAX
GLASS
SEALANT
95° ± 5°
86° 94°
TYP
0.008 – 0.012
(0.203 – 0.305)
0.310 – 0.410
(7.874 – 10.41)
0.055
(1.397)
MAX
BOTH ENDS
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.100 ± 0.010
(2.540 ± 0.254)

J08A (REV H)

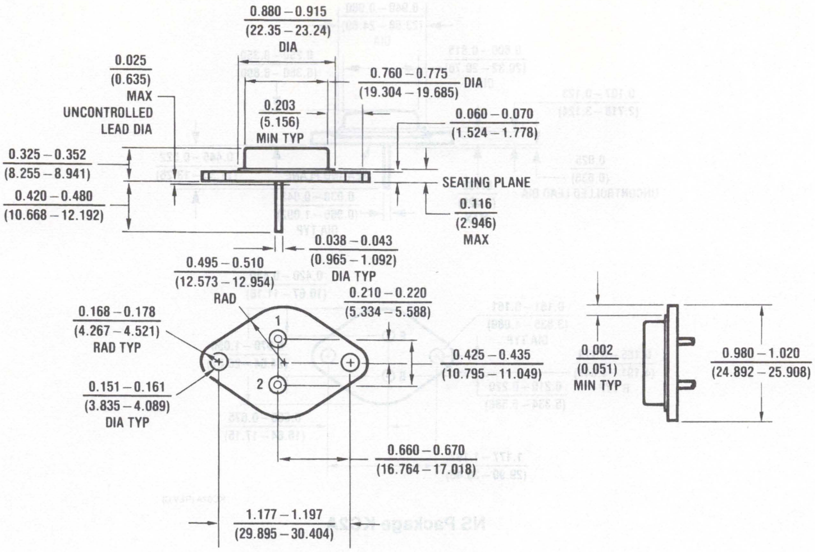
**NS Package J08A**


0.785
(19.939)
MAX
14
13
12
11
10
9
8
0.025
(0.635)
RAD
0.220–0.310
(5.588–7.874)
1
2
3
4
5
6
7
0.290–0.320
(7.366–8.128)
0.180
(4.572)
MAX
95° ±5°
10° MAX
0.310–0.410
(7.874–10.41)
0.005
(0.127)
MIN
GLASS
SEALANT
0.060 ±0.005
(1.524 ±0.127)
0.200
(5.080)
MAX
0.020–0.060
(0.508–1.524)
86°94° TYP
0.008–0.012
(0.203–0.305)
0.098
(2.489)
MAX BOTH ENDS
0.018 ±0.003
(0.457 ±0.076)
0.125–0.200
(3.175–5.080)
0.100 ±0.010
(2.540 ±0.254)
0.150
(3.81)
MIN
J14A (REV G)

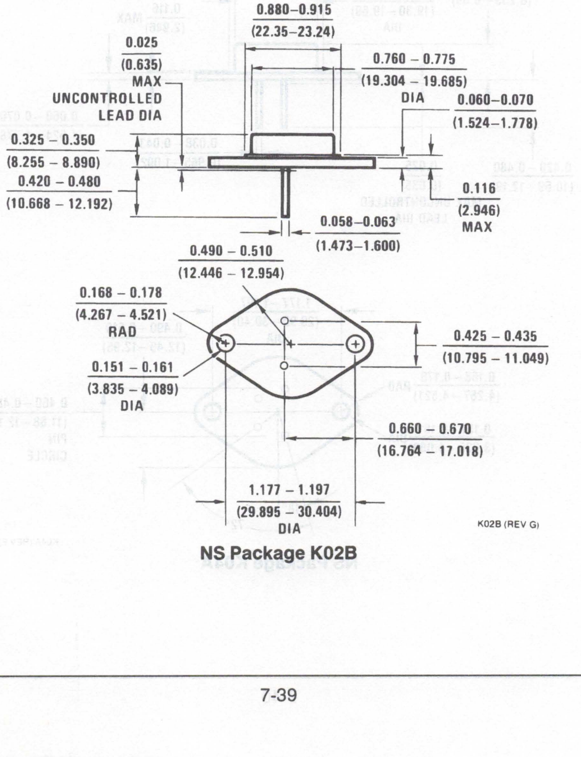
**NS Package J14A**


0.785
(19.939)
MAX
16
15
14
13
12
11
10
9
0.025
(0.635)
RAD
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
8
0.005 – 0.020
(0.127 – 0.508)
RAD TYP
GLASS
SEALANT
0.290 – 0.320
(7.366 – 8.128)
0.005
(0.127)
MIN
0.055 ± 0.005
(1.397 ± 0.127)
0.200
(5.080)
MAX
0.150
(3.810)
MIN
0.180
(4.572)
MAX
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
86° 94°
TYP
0.080
(2.032)
MAX
BOTH
ENDS
0.310 – 0.410
(7.874 – 10.41)
0.018 ± 0.003
(0.457 ± 0.076)
0.125 – 0.200
(3.175 – 5.080)
0.020 – 0.060
(0.508 – 1.524)
0.100 ± 0.010
(2.540 ± 0.254)
0.037 ± 0.005
(0.940 ± 0.127)
J16A (REV K)

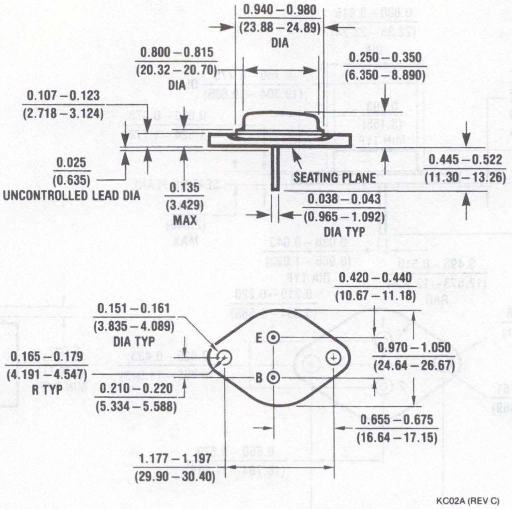
**NS Package J16A**


0.880 – 0.915
(22.35 – 23.24)
DIA
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.760 – 0.775
(19.304 – 19.685)
DIA
0.203
(5.156)
MIN TYP
0.060 – 0.070
(1.524 – 1.778)
0.325 – 0.352
(8.255 – 8.941)
SEATING PLANE
0.420 – 0.480
(10.668 – 12.192)
0.116
(2.946)
MAX
0.038 – 0.043
(0.965 – 1.092)
DIA TYP
0.495 – 0.510
(12.573 – 12.954)
RAD
0.210 – 0.220
(5.334 – 5.588)
0.168 – 0.178
(4.267 – 4.521)
RAD TYP
1
2
0.425 – 0.435
(10.795 – 11.049)
0.002
(0.051)
MIN TYP
0.980 – 1.020
(24.892 – 25.908)
0.151 – 0.161
(3.835 – 4.089)
DIA TYP
0.660 – 0.670
(16.764 – 17.018)
1.177 – 1.197
(29.895 – 30.404)

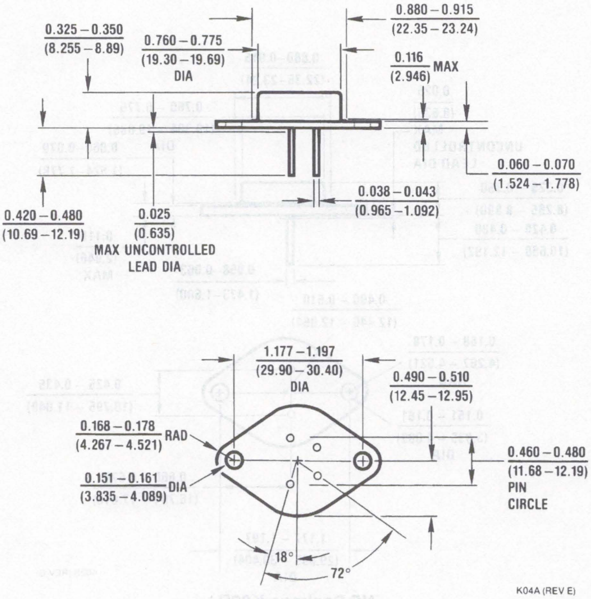
**NS Package K02A**


0.880–0.915
(22.35–23.24)
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.760 – 0.775
(19.304 – 19.685)
DIA
0.060–0.070
(1.524–1.778)
0.325 – 0.350
(8.255 – 8.890)
0.420 – 0.480
(10.668 – 12.192)
0.116
(2.946)
MAX
0.058–0.063
(1.473–1.600)
0.490 – 0.510
(12.446 – 12.954)
0.168 – 0.178
(4.267 – 4.521)
RAD
0.425 – 0.435
(10.795 – 11.049)
0.151 – 0.161
(3.835 – 4.089)
DIA
0.660 – 0.670
(16.764 – 17.018)
1.177 – 1.197
(29.895 – 30.404)
DIA
K02B (REV G)

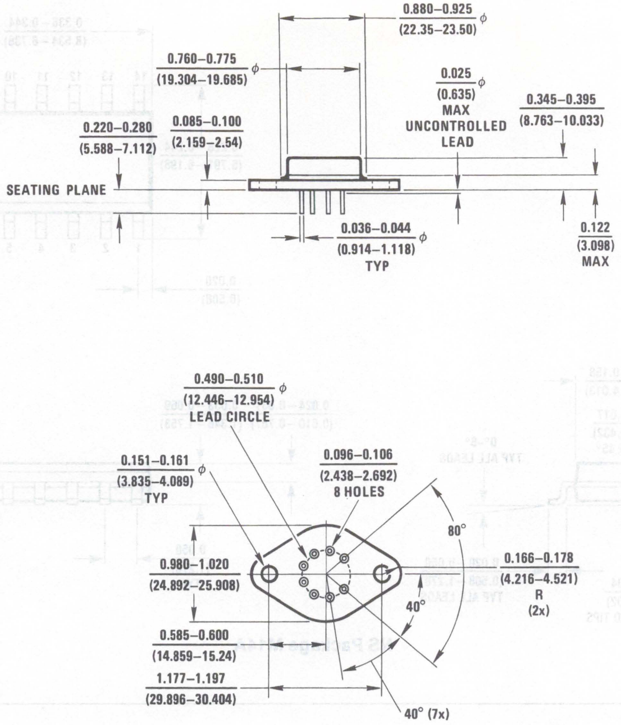
**NS Package K02B**


0.940 – 0.980
(23.88 – 24.89)
DIA
0.800 – 0.815
(20.32 – 20.70)
DIA
0.250 – 0.350
(6.350 – 8.890)
0.107 – 0.123
(2.718 – 3.124)
0.025
(0.635)
UNCONTROLLED LEAD DIA
0.135
(3.429)
MAX
SEATING PLANE
0.038 – 0.043
(0.965 – 1.092)
DIA TYP
0.445 – 0.522
(11.30 – 13.26)
0.420 – 0.440
(10.67 – 11.18)
0.151 – 0.161
(3.835 – 4.089)
DIA TYP
0.165 – 0.179
(4.191 – 4.547)
R TYP
0.210 – 0.220
(5.334 – 5.588)
E
B
0.970 – 1.050
(24.64 – 26.67)
0.655 – 0.675
(16.64 – 17.15)
1.177 – 1.197
(29.90 – 30.40)
KC02A (REV C)

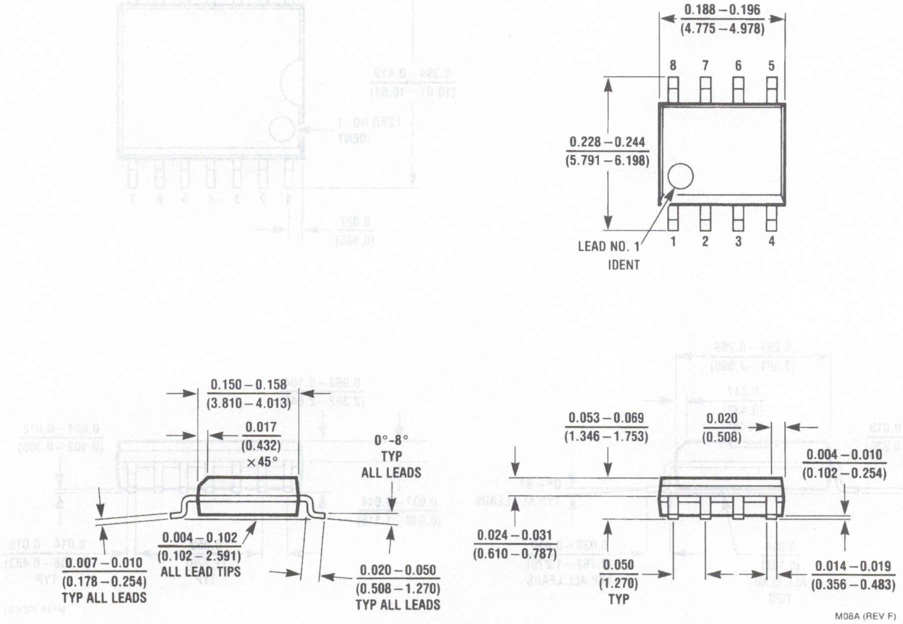
**NS Package KC2A**


0.880 – 0.915
(22.35 – 23.24)
0.325 – 0.350
(8.255 – 8.89)
0.760 – 0.775
(19.30 – 19.69)
DIA
0.116
(2.946)
MAX
0.060 – 0.070
(1.524 – 1.778)
0.038 – 0.043
(0.965 – 1.092)
0.420 – 0.480
(10.69 – 12.19)
0.025
(0.635)
MAX UNCONTROLLED
LEAD DIA
1.177 – 1.197
(29.90 – 30.40)
DIA
0.490 – 0.510
(12.45 – 12.95)
0.168 – 0.178
(4.267 – 4.521)
RAD
0.151 – 0.161
(3.835 – 4.089)
DIA
0.460 – 0.480
(11.68 – 12.19)
PIN
CIRCLE
18°
72°
K04A (REV E)

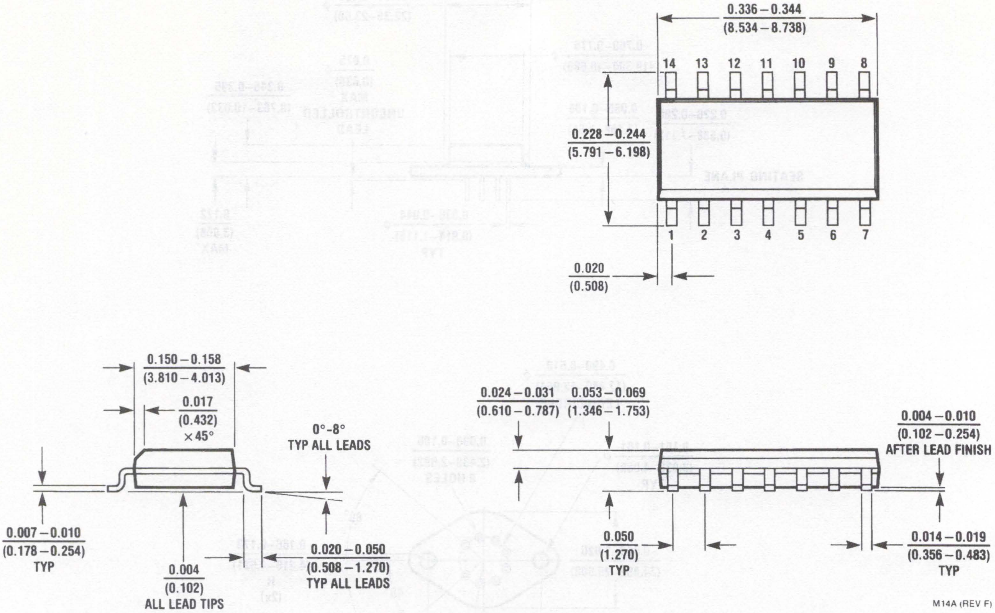
**NS Package K04A**


0.880–0.925 ϕ
(22.35–23.50)
0.760–0.775
(19.304–19.685) ϕ
0.025 ϕ
(0.635)
MAX
UNCONTROLLED
LEAD
0.345–0.395
(8.763–10.033)
0.220–0.280
(5.588–7.112)
0.085–0.100
(2.159–2.54)
SEATING PLANE
0.036–0.044 ϕ
(0.914–1.118)
TYP
0.122
(3.098)
MAX
0.490–0.510 ϕ
(12.446–12.954)
LEAD CIRCLE
0.151–0.161 ϕ
(3.835–4.089)
TYP
0.096–0.106
(2.438–2.692)
8 HOLES
80°
0.980–1.020
(24.892–25.908)
0.166–0.178
(4.216–4.521)
R
(2x)
40°
0.585–0.600
(14.859–15.24)
1.177–1.197
(29.896–30.404)
40° (7x)
K08A (REV C)

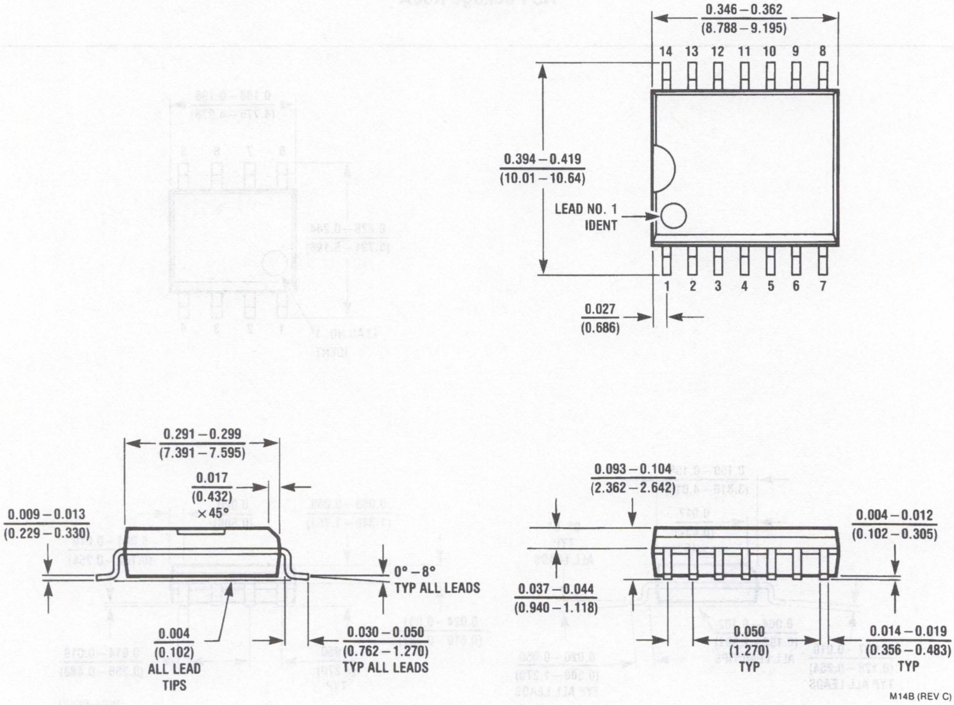
**NS Package K08A**


0.188 – 0.196
(4.775 – 4.978)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
LEAD NO. 1
IDENT
1 2 3 4
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
×45°
0°–8°
TYP
ALL LEADS
0.004 – 0.102
(0.102 – 2.591)
ALL LEAD TIPS
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.020
(0.508)
0.004 – 0.010
(0.102 – 0.254)
0.024 – 0.031
(0.610 – 0.787)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
M08A (REV F)

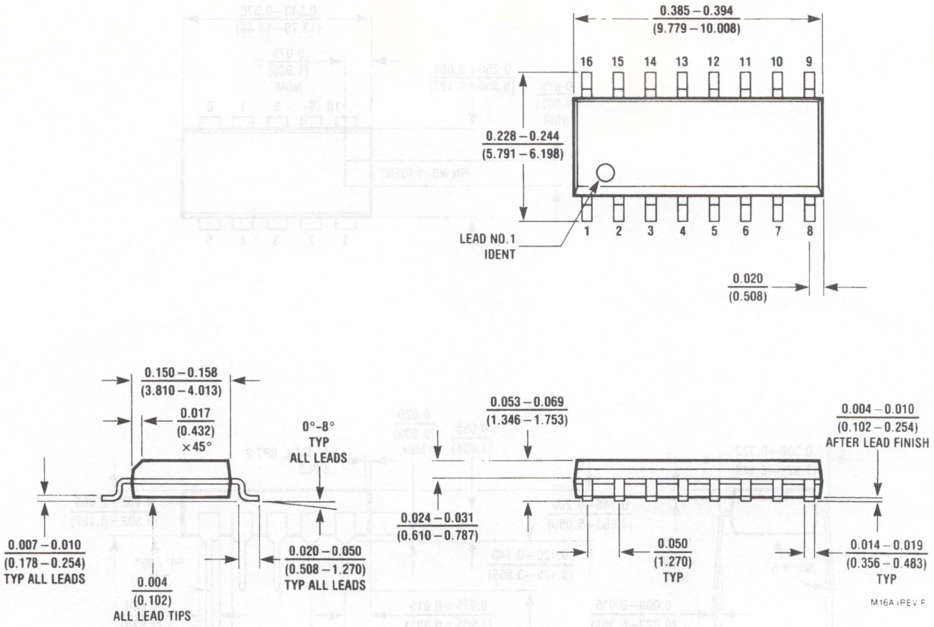
**NS Package M08A**


0.336 – 0.344
(8.534 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.198)
1 2 3 4 5 6 7
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
× 45°
0°–8°
TYP ALL LEADS
0.007 – 0.010
(0.178 – 0.254)
TYP
0.004
(0.102)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.024 – 0.031
(0.610 – 0.787)
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14A (REV F)

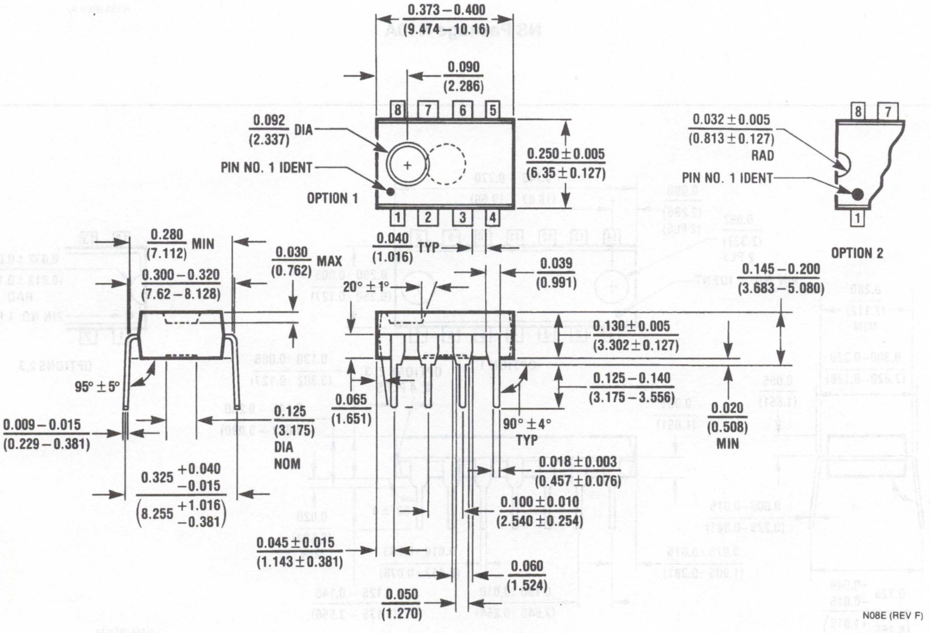
**NS Package M14A**


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
× 45°
0.009 – 0.013
(0.229 – 0.330)
0°–8°
TYP ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV C)

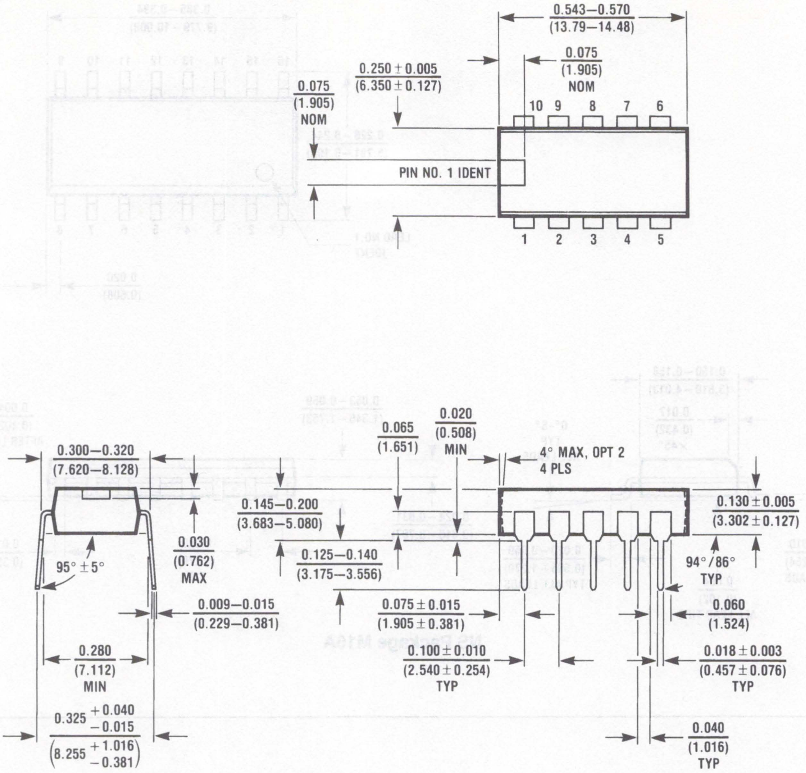
**NS Package M14B**


0.385 – 0.394
(9.779 – 10.008)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.198)
LEAD NO.1
IDENT
1 2 3 4 5 6 7 8
0.020
(0.508)
0.150 – 0.158
(3.810 – 4.013)
0.017
(0.432)
×45°
0°-8°
TYP
ALL LEADS
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
AFTER LEAD FINISH
0.024 – 0.031
(0.610 – 0.787)
0.007 – 0.010
(0.178 – 0.254)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.020 – 0.050
(0.508 – 1.270)
TYP ALL LEADS
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M16A (REV F

**NS Package M16A**

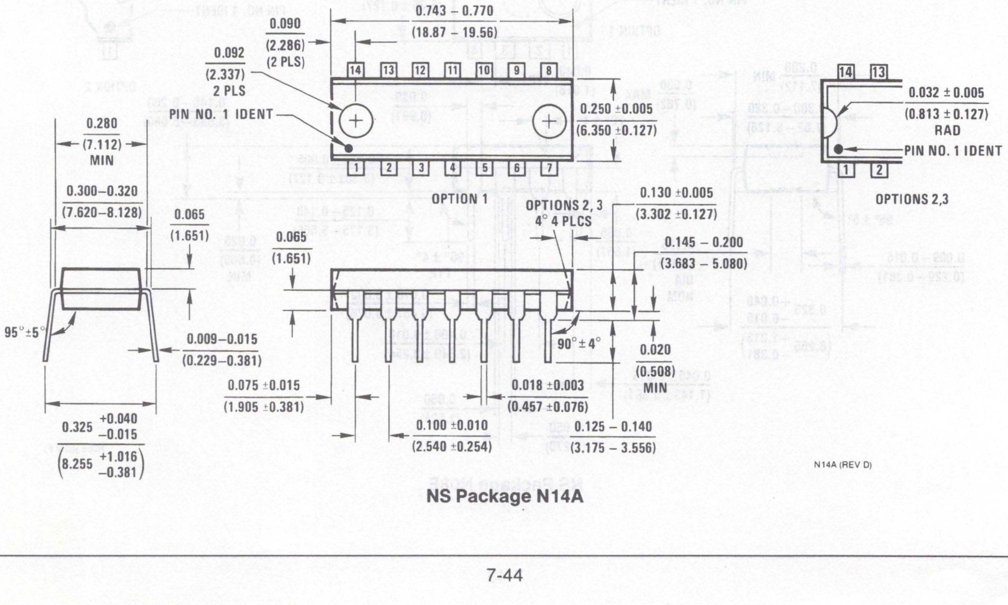

0.373 – 0.400
(9.474 – 10.16)
0.090
(2.286)
8 7 6 5
0.092
(2.337)
DIA
PIN NO. 1 IDENT
OPTION 1
0.250 ± 0.005
(6.35 ± 0.127)
1 2 3 4
0.032 ± 0.005
(0.813 ± 0.127)
RAD
PIN NO. 1 IDENT
8 7
1
OPTION 2
0.280
(7.112)
MIN
0.300 – 0.320
(7.62 – 8.128)
0.030
(0.762)
MAX
0.040
(1.016)
TYP
0.039
(0.991)
20° ± 1°
0.145 – 0.200
(3.683 – 5.080)
0.130 ± 0.005
(3.302 ± 0.127)
95° ± 5°
0.125 – 0.140
(3.175 – 3.556)
0.065
(1.651)
0.125
(3.175)
DIA
NOM
90° ± 4°
TYP
0.020
(0.508)
MIN
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
0.045 ± 0.015
(1.143 ± 0.381)
0.060
(1.524)
0.050
(1.270)
N08E (REV F)

**NS Package N08E**


0.543–0.570
(13.79–14.48)
0.075
(1.905)
NOM
0.250 ± 0.005
(6.350 ± 0.127)
0.075
(1.905)
NOM
10 9 8 7 6
PIN NO. 1 IDENT
1 2 3 4 5
0.300–0.320
(7.620–8.128)
0.145–0.200
(3.683–5.080)
0.065
(1.651)
0.020
(0.508)
MIN
4° MAX, OPT 2
4 PLS
0.130 ± 0.005
(3.302 ± 0.127)
95° ± 5°
0.030
(0.762)
MAX
0.125–0.140
(3.175–3.556)
94°/86°
TYP
0.009–0.015
(0.229–0.381)
0.075 ± 0.015
(1.905 ± 0.381)
0.060
(1.524)
0.280
(7.112)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
TYP
0.018 ± 0.003
(0.457 ± 0.076)
TYP
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.040
(1.016)
TYP

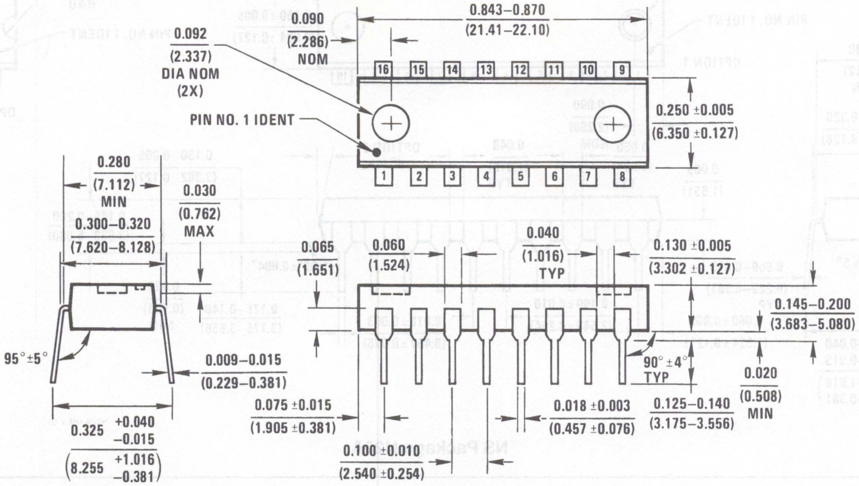
N10A (REV A)

**NS Package N10A**


0.743 – 0.770
(18.87 – 19.56)
0.090
(2.286)
(2 PLS)
0.092
(2.337)
2 PLS
PIN NO. 1 IDENT
14 13 12 11 10 9 8
1 2 3 4 5 6 7
0.250 ±0.005
(6.350 ±0.127)
OPTION 1
14 13
1 2
0.032 ±0.005
(0.813 ±0.127)
RAD
PIN NO. 1 IDENT
OPTIONS 2,3
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.065
(1.651)
0.065
(1.651)
OPTIONS 2, 3
4° 4 PLCS
0.130 ±0.005
(3.302 ±0.127)
0.145 – 0.200
(3.683 – 5.080)
95°±5°
0.009–0.015
(0.229–0.381)
90° ±4°
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.100 ±0.010
(2.540 ±0.254)
0.125 – 0.140
(3.175 – 3.556)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

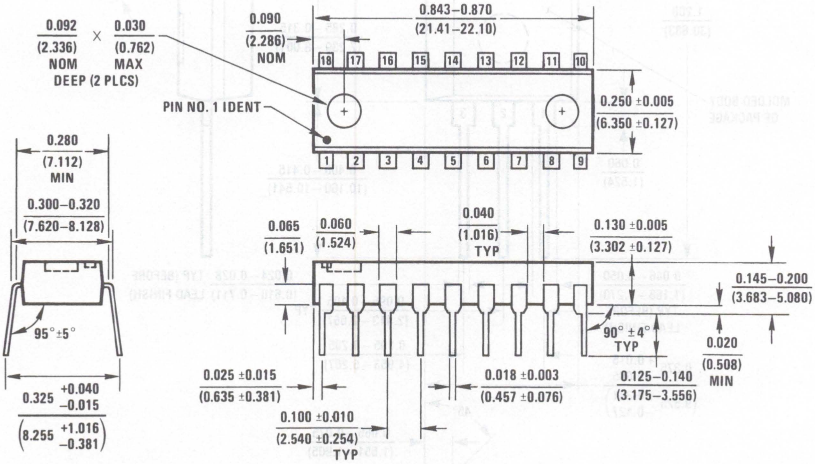
N14A (REV D)

**NS Package N14A**


0.092
(2.337)
DIA NOM
(2X)
PIN NO. 1 IDENT
0.090
(2.286)
NOM
0.843–0.870
(21.41–22.10)
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.030
(0.762)
MAX
0.300–0.320
(7.620–8.128)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
95° ±5°
0.009–0.015
(0.229–0.381)
90° ±4°
TYP
0.020
(0.508)
MIN
0.075 ±0.015
(1.905 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ±0.010
(2.540 ±0.254)

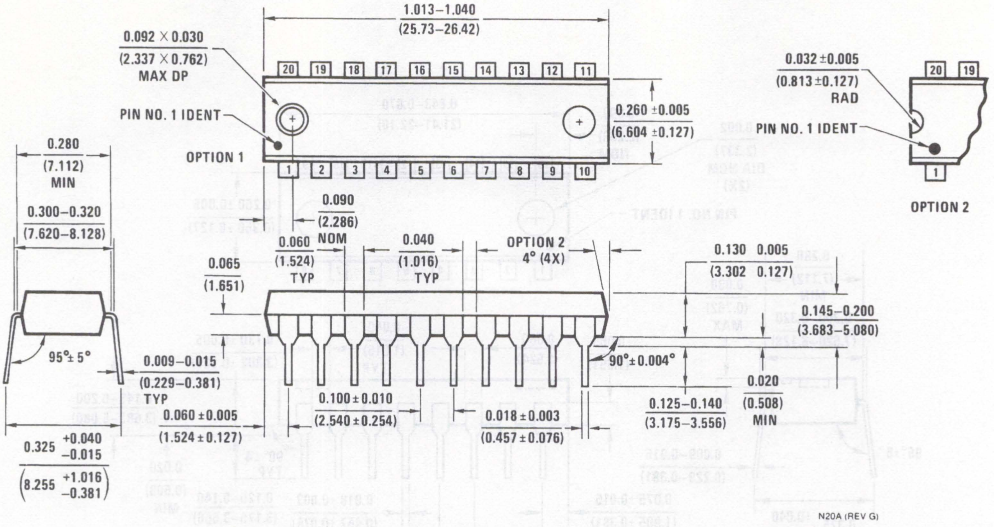
N16A (REV E)

**NS Package N16A**


0.092
(2.336)
NOM
×
0.030
(0.762)
MAX
DEEP (2 PLCS)
0.090
(2.286)
NOM
0.843–0.870
(21.41–22.10)
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
PIN NO. 1 IDENT
0.250 ±0.005
(6.350 ±0.127)
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.065
(1.651)
0.060
(1.524)
0.040
(1.016)
TYP
0.130 ±0.005
(3.302 ±0.127)
0.145–0.200
(3.683–5.080)
95° ±5°
90° ±4°
TYP
0.020
(0.508)
MIN
0.025 ±0.015
(0.635 ±0.381)
0.018 ±0.003
(0.457 ±0.076)
0.125–0.140
(3.175–3.556)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)
0.100 ±0.010
(2.540 ±0.254)
TYP

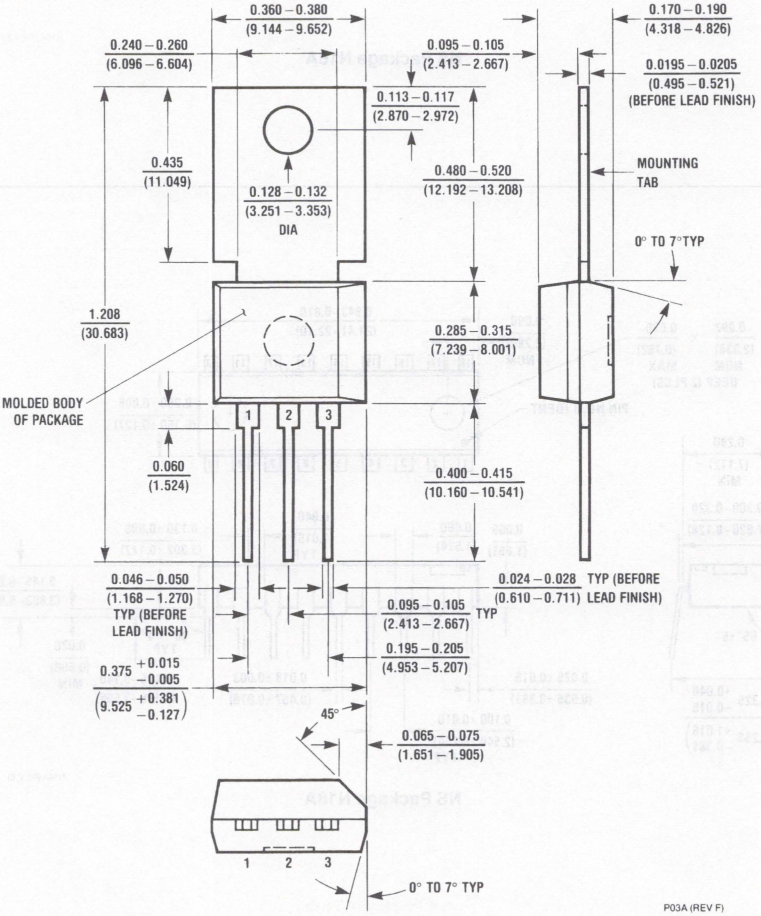
N18A (REV E)

**NS Package N18A**


1.013–1.040
(25.73–26.42)
0.092 × 0.030
(2.337 × 0.762)
MAX DP
PIN NO. 1 IDENT
OPTION 1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
0.260 ±0.005
(6.604 ±0.127)
0.032 ±0.005
(0.813 ±0.127)
RAD
PIN NO. 1 IDENT
OPTION 2
0.280
(7.112)
MIN
0.300–0.320
(7.620–8.128)
0.090
(2.286)
NOM
0.060
(1.524)
TYP
0.040
(1.016)
TYP
OPTION 2
4° (4X)
0.065
(1.651)
0.130 0.005
(3.302 0.127)
0.145–0.200
(3.683–5.080)
95° ± 5°
0.009–0.015
(0.229–0.381)
TYP
90° ± 0.004°
0.020
(0.508)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
0.125–0.140
(3.175–3.556)
0.060 ± 0.005
(1.524 ± 0.127)
0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

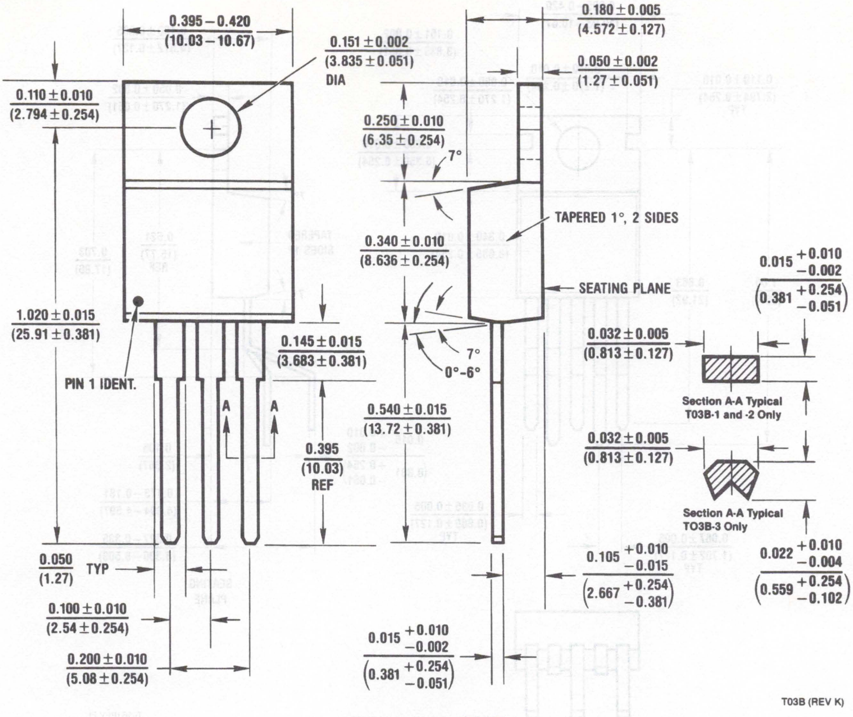
N20A (REV G)

NS Package N20A

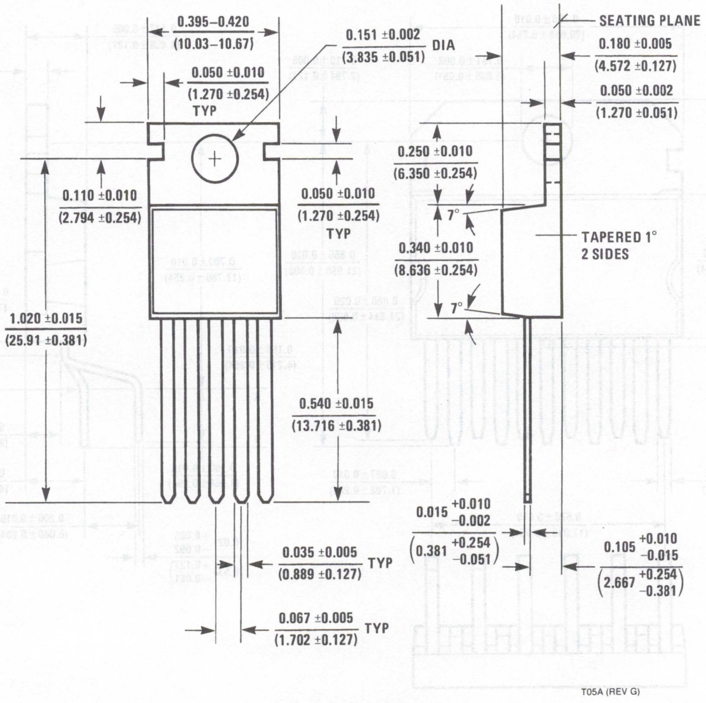

0.360 – 0.380
(9.144 – 9.652)
0.170 – 0.190
(4.318 – 4.826)
0.240 – 0.260
(6.096 – 6.604)
0.095 – 0.105
(2.413 – 2.667)
0.0195 – 0.0205
(0.495 – 0.521)
(BEFORE LEAD FINISH)
0.113 – 0.117
(2.870 – 2.972)
MOUNTING
TAB
0.435
(11.049)
0.480 – 0.520
(12.192 – 13.208)
0.128 – 0.132
(3.251 – 3.353)
DIA
0° TO 7°TYP
1.208
(30.683)
0.285 – 0.315
(7.239 – 8.001)
MOLDED BODY
OF PACKAGE
1
2
3
0.060
(1.524)
0.400 – 0.415
(10.160 – 10.541)
0.046 – 0.050
(1.168 – 1.270)
TYP (BEFORE
LEAD FINISH)
0.024 – 0.028 TYP (BEFORE
(0.610 – 0.711) LEAD FINISH)
0.095 – 0.105
(2.413 – 2.667)
TYP
0.195 – 0.205
(4.953 – 5.207)
0.375 +0.015 −0.005
(9.525 +0.381 −0.127)
45°
0.065 – 0.075
(1.651 – 1.905)
1
2
3
0° TO 7° TYP

P03A (REV F)

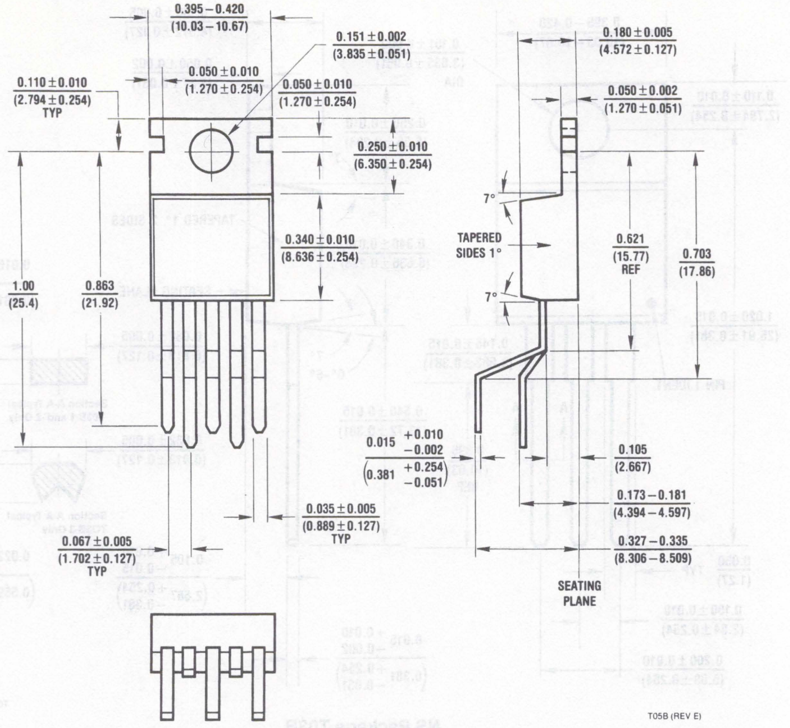
NS Package P03A


0.395 – 0.420
(10.03 – 10.67)
0.151 ± 0.002
(3.835 ± 0.051)
DIA
0.110 ± 0.010
(2.794 ± 0.254)
1.020 ± 0.015
(25.91 ± 0.381)
PIN 1 IDENT.
0.050
(1.27)
TYP
0.100 ± 0.010
(2.54 ± 0.254)
0.200 ± 0.010
(5.08 ± 0.254)
0.145 ± 0.015
(3.683 ± 0.381)
A
A
0.395
(10.03)
REF
0.250 ± 0.010
(6.35 ± 0.254)
7°
0.340 ± 0.010
(8.636 ± 0.254)
7°
0°–6°
0.540 ± 0.015
(13.72 ± 0.381)
0.015 +0.010 −0.002
(0.381 +0.254 −0.051)
0.180 ± 0.005
(4.572 ± 0.127)
0.050 ± 0.002
(1.27 ± 0.051)
TAPERED 1°, 2 SIDES
SEATING PLANE
0.015 +0.010 −0.002
(0.381 +0.254 −0.051)
0.032 ± 0.005
(0.813 ± 0.127)
Section A-A Typical
T03B-1 and -2 Only
0.032 ± 0.005
(0.813 ± 0.127)
Section A-A Typical
T03B-3 Only
0.105 +0.010 −0.015
(2.667 +0.254 −0.381)
0.022 +0.010 −0.004
(0.559 +0.254 −0.102)
T03B (REV K)

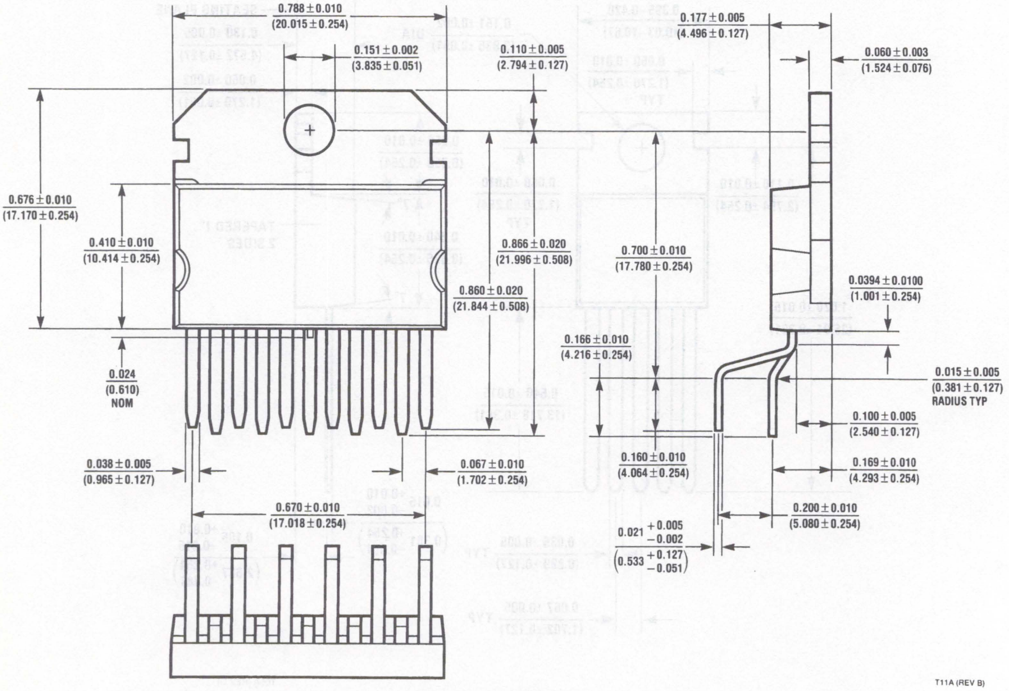
NS Package T03B


0.395–0.420
(10.03–10.67)
0.050 ±0.010
(1.270 ±0.254)
TYP
0.151 ±0.002
(3.835 ±0.051)
DIA
0.110 ±0.010
(2.794 ±0.254)
0.050 ±0.010
(1.270 ±0.254)
TYP
1.020 ±0.015
(25.91 ±0.381)
0.540 ±0.015
(13.716 ±0.381)
0.035 ±0.005
(0.889 ±0.127)
TYP
0.067 ±0.005
(1.702 ±0.127)
TYP
SEATING PLANE
0.180 ±0.005
(4.572 ±0.127)
0.050 ±0.002
(1.270 ±0.051)
0.250 ±0.010
(6.350 ±0.254)
7°
0.340 ±0.010
(8.636 ±0.254)
7°
TAPERED 1°
2 SIDES
0.015 +0.010 −0.002
(0.381 +0.254 −0.051)
0.105 +0.010 −0.015
(2.667 +0.254 −0.381)
T05A (REV G)

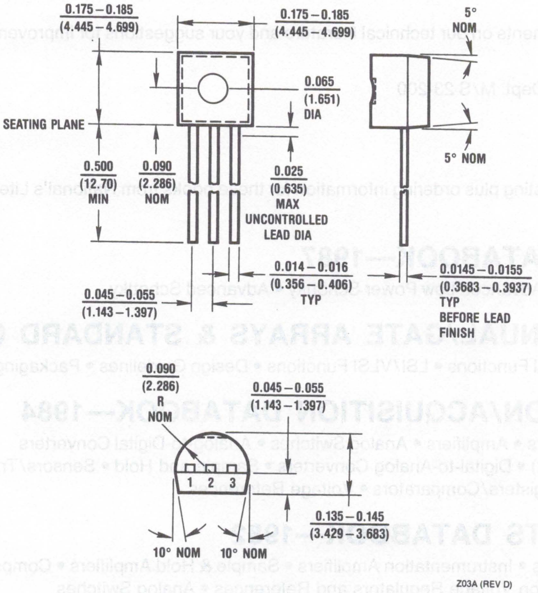
NS Package T05A


0.395 – 0.420
(10.03 – 10.67)
0.151 ± 0.002
(3.835 ± 0.051)
0.180 ± 0.005
(4.572 ± 0.127)
0.110 ± 0.010
(2.794 ± 0.254)
TYP
0.050 ± 0.010
(1.270 ± 0.254)
0.050 ± 0.010
(1.270 ± 0.254)
0.050 ± 0.002
(1.270 ± 0.051)
0.250 ± 0.010
(6.350 ± 0.254)
7°
TAPERED
SIDES 1°
0.340 ± 0.010
(8.636 ± 0.254)
0.621
(15.77)
REF
0.703
(17.86)
1.00
(25.4)
0.863
(21.92)
7°
0.015 +0.010 −0.002
(0.381 +0.254 −0.051)
0.105
(2.667)
0.173 – 0.181
(4.394 – 4.597)
0.035 ± 0.005
(0.889 ± 0.127)
TYP
0.327 – 0.335
(8.306 – 8.509)
0.067 ± 0.005
(1.702 ± 0.127)
TYP
SEATING
PLANE
T05B (REV E)

NS Package T05B


0.788 ± 0.010
(20.015 ± 0.254)
0.177 ± 0.005
(4.496 ± 0.127)
0.151 ± 0.002
(3.835 ± 0.051)
0.110 ± 0.005
(2.794 ± 0.127)
0.060 ± 0.003
(1.524 ± 0.076)
0.676 ± 0.010
(17.170 ± 0.254)
0.410 ± 0.010
(10.414 ± 0.254)
0.866 ± 0.020
(21.996 ± 0.508)
0.700 ± 0.010
(17.780 ± 0.254)
0.860 ± 0.020
(21.844 ± 0.508)
0.0394 ± 0.0100
(1.001 ± 0.254)
0.166 ± 0.010
(4.216 ± 0.254)
0.024
(0.610)
NOM
0.015 ± 0.005
(0.381 ± 0.127)
RADIUS TYP
0.100 ± 0.005
(2.540 ± 0.127)
0.038 ± 0.005
(0.965 ± 0.127)
0.067 ± 0.010
(1.702 ± 0.254)
0.160 ± 0.010
(4.064 ± 0.254)
0.169 ± 0.010
(4.293 ± 0.254)
0.670 ± 0.010
(17.018 ± 0.254)
0.200 ± 0.010
(5.080 ± 0.254)
0.021 +0.005 −0.002
(0.533 +0.127 −0.051)
T11A (REV B)

NS Package T11A


0.175 – 0.185
(4.445 – 4.699)
0.175 – 0.185
(4.445 – 4.699)
5°
NOM
0.065
(1.651)
DIA
SEATING PLANE
5° NOM
0.500
(12.70)
MIN
0.090
(2.286)
NOM
0.025
(0.635)
MAX
UNCONTROLLED
LEAD DIA
0.014 – 0.016
(0.356 – 0.406)
TYP
0.0145 – 0.0155
(0.3683 – 0.3937)
TYP
BEFORE LEAD
FINISH
0.045 – 0.055
(1.143 – 1.397)
0.090
(2.286)
R
NOM
0.045 – 0.055
(1.143 – 1.397)
1
2
3
0.135 – 0.145
(3.429 – 3.683)
10° NOM
10° NOM
Z03A (REV D)

**NS Package Z03A**

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## INTUITIVE IC OP AMPS—1984

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